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Energy-Efficient Programmable Gain Amplifier to a Biomedical Engineering and Healthcare Tunable Front-End Sensor

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Declaration

I declare that this document is an original work of my own authorship and that it fulfills all the requirements of the Code of Conduct and Good Practices of the Universidade de Lisboa.

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I would like to extend my gratitude to my family for the support, patience and motivation given during my journey to achieve my engineering degree.

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Abstract

This work comprises the research and development and implementation of a energy-efficient Programmable Gain Amplifier to be implemented in a tunable front-end sensor for different human-body signals. Human-body signals that will be considered for the development of this project are electromyography and electrooculography. These bio-potential signals operate in a separate broadband yet both follow an impulse-shape type of transmission hence suitable to be applied to the same receiver. The field of biomedical engineering and Healthcare as seen a consistent tendency to integrate complex circuitry inside battery-powered small form-factor systems, which allow for the continuously sensing of bio-potential signals unobtrusively and uncumbersomly for extended period of times. Hence requiring this systems to be energy efficient and have low power consumption. In this work, state-of-the-art projects are studied and presented and a Programmable Gain Amplifier topology is proposed in order to be developed and implemented. The energy-efficient Programmable Gain Amplifier will be developed using the electronic design software Cadence, in the United Microelectronics Corporation (UMC) 130nm Complementary Metal Oxide Semiconductor (CMOS) technology.

The Programmable Gain Amplifier (PGA) is implemented at sizing and layout level, from post-layout results a variable gain of 50 dB and 60 dB is achieved with high linearity and low area, while consuming under 1 µA.

Keywords

Programmable Gain Amplifier, Low-Power, Low-Noise, Biomedical, Healthcare, Bio-potential signals, Energy-Efficient, CMOS.

Resumo

Este trabalho compreende o estudo, o desenvolvimento e a implementação de um amplificador de ganho programável, com o objetivo de que o mesmo seja implementado num sensor capaz de detetar diferentes sinais do corpo humano.

Os sinais do corpo humano que serão considerados para o desenvolvimento deste projeto são a eletromiografia e a eletrooculografia. Estes sinais bio-potenciais, operam numa largura de banda separada, embora ambos apresentem uma transmissão em forma de impulso, portanto, sendo assim apropriado aplicar ao mesmo recetor.

No campo da engenharia biomédica e da saúde existe a tendência para integrar circuitos complexos dentro de sistemas, alimentados por bateria, que permitem a deteção contínua de sinais bio-potenciais, de forma discreta e incomoda por um período prolongado. Portanto é imprescindível que esses sistemas tenham um baixo consumo de energia.

Neste relatório, é analisado e apresentado o estado da arte, topologias de Amplificadores de Ganho Programável são analisadas e é proposto um circuito para ser desenvolvido e implementados. O Amplificador de Ganho Programável deve ser energeticamente eficiente e será desenvolvido no software de design eletrônico Cadence, com a tecnologia CMOS UMC 130nm. O Amplificadores de Ganho Programável é dimensionado e o seu layout é realizado, através de simulações é possível verificar a obtenção de uma ganho variável de 50 dB e de 60 dB com elevada linearidade e uma área reduzida, enquanto o consumo de corrente é menor que 1 µA para ambos os ganhos.

Palavras-Chave

Amplificador de Ganho Programável , Baixo Consumo, Baixo Ruído, Biomédicas, Saúde, Sinais Bio Potenciais, Energéticamente Eficiente, CMOS, AIDA.

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Acronyms

AC	Alternate Current
ADC	Analog-to-Digital Converters
AIDA	Analog IC Design Automation
BW	Bandwidth
CMFB	Common Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common-Mode Rejection Ratio
DAC	Digital to Analog Converter
DC	Direct Current
DFT	Discrete Fourier Transform
DRC	Design rule checking
ECG	Electrocardiography
EEG	Electroencephalography
EMG	Electromyography
EOG	Electrooculography
FOM	Fiure-of-Merit
FS	Sampling Frequency
GBW	Gain-BandWidth Product
HPF	High-Pass Filter
HRP	high resistivity polysilicon
IA	Instrumentation Amplifier
LFP	Local field potential
LFT	Local-Feedback Transconductors

LNA	Low Noise Amplifier
LPF	Low-Pass Filter
LVS	Layout Versus Schematic
MSI	Medium-scale integration
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type Metal Oxide Semiconductor
OPAMP	Operational Amplifier
OTA	Operational Transconductance Amplifier
P1dB	1-dB Gain Compression Point
P3dB	3-dB Gain Compression Point
PMOS	P-type Metal Oxide Semiconductor
PGA	Programmable Gain Amplifier
PG-IA	Programmable Gain Instrumentation Amplifier
PGB-INA	Programmable Gain and Bandwidth Instrumentation Amplifier
PSRR	Power Supply Rejection Ratio
PVT	Process, Voltage, Temperature
RF	Radio-Frequency
RMS	Root Mean Square
RR-CMI	Rail-to-rail Current Mirror Input
SC	Switched-capacitor
SC-CMFB	switched-capacitor common-mode feedback circuit
SD	Spectral Density
THD	Total Harmonic Distortion
UMC	United Microelectronics Corporation
VBIAS	Voltage-Bias
VGA	Variable Gain Amplifier
VC	Voltage-combiners
VOS	Offset Voltage
AIDA	Analog IC Design Automation

Symbols

a	Open-Loop Voltage Gain
A_d	Differential-Mode Gain
A_v	Voltage Gain
f_c	Cutoff Frequency
g_m	Transconductance
I_d	drain current
U_T	Thermal Voltage
V_{cm}	Common-Mode Voltage
V_d	Differential-Mode Voltage
V_{DC}	DC voltage
V_{DD}	Power Supply
V_{in}	Input Voltage
V_{OUT}	Output Voltage
V_{TH}	Threshold Voltage

1

Introduction

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Introduction

1.1 Motivation

In this day and age biomedical devices used to sense bio-potential signals are on the rise, since the information collected from those signals can help in diagnosis of diseases, treatment and rehabilitation. Signals such as Electroencephalography (EEG), EMG, Electrocardiography (ECG), and EOG can be recorded in a non-invasive way, by placing electrodes on the skin. These biomedical signals have bandwidth between a few hundred mHz to a few kHz and a amplitude variation from a few μV to a few mV as detailed in Table 1.1. For continuous monitoring, low power-consumption is paramount to maximize battery life and therefore prolong operation hours.

Generally health monitoring systems consists of five blocks, sensors, Low Noise Amplifier (LNA), dedicated filtering, in the case a Low-Pass Filter (LPF), programmable gain amplifiers, PGA and multiplexed Analog-to-Digital Converters (ADC) with Radio-Frequency (RF) circuitry to send and receive raw data, Figure 1.1.

Usually any bio-potential signals is quantized by an ADC so that complex signal processing can be performed in the digital domain and a PGA is usually placed before the ADC, Figure 1.1, being an important building block in modern day sensing applications. The PGA controls the amplitude signal applied at the inputs of the ADC, providing the much needed flexibility to be able to maximize the ADC dynamic range. Moreover the PGA needs to maintain its high linearity and low noise over the entire signal bandwidth. The gain can be controlled by trimmers, digital controls methods or multiplexing techniques.

Large dynamic range and small harmonic distortion are also important for bio-signal recordings, so that the ADC can reconstruct the signal as true as possible to the original signal. If the system is not on battery, but connected to the grid the system would be subjected to powerline interference. Since this interference is one of the principal noise source in bio-sensing devices, the PSRR should be maximized, to solve this problem.

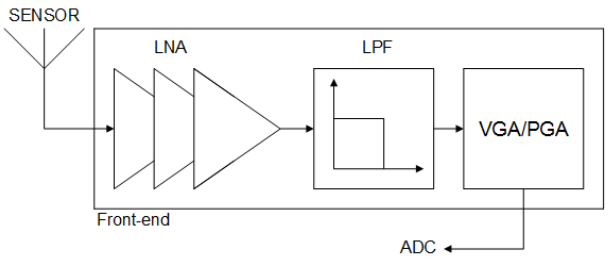

Figure 1.1: Front-end block diagram.

1.2 Goals and challenges

The main goal of this work consists on the research and development of an energy-efficient PGA for biomedical applications, in order to allow the measuring of bio-potential signals, mainly EMG and EOG, which are recorded from different parts of the human-body, and have different characteristic, thus an adaptive gain range is necessary. The signals operate in different broadbands, but both follow a similar impulse-shape type of transmission, thus are suitable to be applied to the same receiver. The PGA will be implmented in UMC 130 nm, parasitic extraction will be done post-layout, the PGA will operate with 3.3 V and consume under 1 μA. Since the bio-potential signals of the human body are low voltage, a high gain is necessary, plus since the signals are different depending on the body location, a variable gain is also necessary, therefore the PGA should have a gain of 40 dB and a Bandwidth (BW) of 2000 Hz for the EMG signal, a 60 db gain for the EOG with a BW higher than 10 Hz. Plus the linearity should be maintained over this range. As shown in Table 1.1, the powerline interference is important, thus a PSRR, of 60 dB, is required. The objectives are summarized in Table 1.2.

Table 1.1: Characteristics of Biomedical Signal Processing.

	ECG	EEG	EMG	EOG
Amplitude (mV)	1 - 5	0.001 - 0.01	1 - 10	0.01 - 0.1
Frequency Range (Hz)	0.05 - 100	0.5 - 40	20 - 2000	DC - 10
Primary Noise Source	Powerline interference;	Thermal, powerline; Induced interference; RF interference;	Powerline interference; RF interference;	Powerline interference;
Primary Interference Source	Nearby muscle activity (EMG signal);	Motion artifact; Muscle noise; Eye motion; Blink effect; Heartbeat signal;	Motion artifact;	Skin potential; Motion Artifact; DC drift;

Table 1.2: Target Goals.

	Unit	Target Values
Technology	nm	130
VDD	V	3.3
IDD	μA	1
Gain	dB	40-60 dB
BW	Hz	2000
Current Consumption	μA	≤ 1
CMRR	dB	≥ 60
PSRR	dB	≥ 80
Dynamic Range	dB	≥ 60
THD	%	<1
Load	pF	1

1.3 Document Organization

This document presents various sections, in chapter 2 where theoreticall concepts related to PGA, and important performance metrics, are explained, furthermore state-of-the-art topologies and techniques are considered and presented. In chapter 3, is where the architecture of the proposed circuit is shown, as well the theoretical understanding of the circuit. Furthermore in chapter 4, the sizing, the simulations and results for circuit schematic are presented. At last in chapter 5 the layout is presented with some considerations, simulations and results comparison between schematic and layout are done. This document is concluded in chapter 6 with a comparison between the state-of-the-art and the obtained results, finally some future work considerations are presented.

2

State of the Art

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State-of-the-Art

2.1 Overview

This section intends to study theoretical concepts important for the development of this work, including important metrics, and different amplifiers circuits and configurations.

2.1.1 Operational Amplifier

Operational amplifiers are designed to sense the voltage difference between the signals applied at its input terminals, thus having an differential input. The ideal OPAMP would not draw any input current, that is the input signals currents into the input terminals are zero, which is equivalent to say that, the input impedance is infinite in an ideal OPAMP. The output terminal in a ideal OPAMP, behaves as the output terminal of an ideal voltage source, which is equivalent to say that, the output impedance of an ideal OPAMP is zero. The OPAMP is a versatile building block capable of performing different tasks such as mathematical operation, signal conditioning or filtering. A conceptual schematic diagram of an ideal OPAMP, is shown in Figure 2.1a generically, the gain considered in Figure 2.1a, refers to the differential gain, A_d, however since the common-mode voltage, V_{cm} defined as the constant value applied to both inputs at the same time, Equation 2.3, is also amplified. the gain applied to the common-mode voltage is defined as the common-mode gain, which, ideally, is zero. the OPAMP output voltage, V_{OUT}, can be computed as Equation 2.1, where the differential-mode voltage, V_d, between the two inputs is determined by Equation 2.2, and multiplied by the Open-Loop Voltage Gain (a). Figure 2.1b represents the contributions from the differential-mode gain ,A_d, and the common-mode gain. Hence, the output voltage can be computed by Equation 2.4 [1].

$$V_{out} = V_d \cdot a \tag{2.1}$$

$$V_d = v_+ - v_- \tag{2.2}$$

$$V_{cm} = (v_+ - v_-)/2 \tag{2.3}$$

$$V_{out} = A_d \cdot V_d + A_c \cdot V_{cm} \tag{2.4}$$

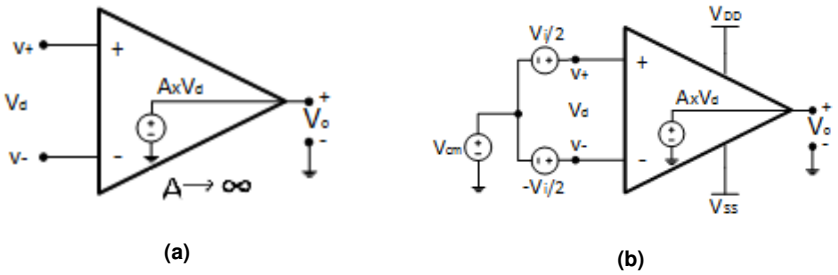


Figure 2.1: (a) Ideal OpAmp internal circuit, (b) Definition of OpAmp applied inputs and output.

2.1.2 Operational Transconductance Amplifier

Operational Transconductance amplifiers OTA, are versatile building blocks, useful for many filtering and signal processing applications, offering intrinsically wide bandwidth for many types of amplifiers. OTA can be generically defined as voltage-controlled current source with active gain. Therefore, an OTA is basically a voltage-to-current transducer. The gain of OPAMP can be programmable, in some topologies, through the DC current. In an ideal OTA the output current is linear function of the differential input voltage, V_{in}, and can be computed by Equation 2.5.

$$I_o = g_m \cdot V_{in} \tag{2.5}$$

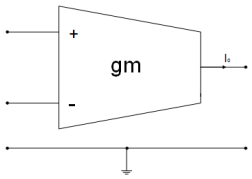


Figure 2.2: CMOS Operational Transconductance Amplifier.

2.1.3 Low Noise Amplifiers

Generally, the main objective for using an LNA in a first stage of a receiver is to provide enough gain to overcome the noise from the additional stages. The noise figure of the LNA directly adds to that of the system, since is the first gain stage, [2]. therefore, the LNA must add few noise as possible, further-

more it has to accommodate large signals without distortion, also the input source, generally presents a specific impedance, specially if after the LNA, a passive filter is implemented, since the transfer characteristics of the filter can be sensitive to the quality of the termination [3]. Power consumption in many applications is an important aspect to consider when designing a LNA. In order to attenuate the noise from the LNA current consumption, as to increase, thus a trade-off is often necessary. When the noise requirements are relaxed, the main limitation to decrease the power consumption comes from the LNA transconductance, g_m. One of the most effective approaches to minimize the dissipated power and thereby have lower power consumption is bias the transistors in the weak inversion region where the maximum g_m/I_d can be achieved [4].

2.1.4 Switched-CapacitorAmplifiers

A switched-capacitor, SC, is a circuit that functions by moving charges in and out of capacitors with switches determining the order. Normally, non-overlapping signals are used to controls the switches, guarantying that all switches are not closed at the same time. Capacitors instead of resistors are often used as passive elements in feedback amplifiers, In DC terms, an equivalent resistor equals $1/f_sC$ where f_S is the switching frequency. An OPAMP can appear in the feedback configuration in many applications, such as a switched-capacitor gain stage and a switched-capacitor integrator [2]. Figure 2.3, shows an switched-capacitor amplifier, the relation between the output and a input is based on the charge conservation. First when C_2 is grounded, the charge stored on the plates of the capacitors that connect to the the op-amp input node during the first phase, $\emptyset_1$, is Equation 2.6. In the second phase, $\emptyset_2$, the charge stored in C_2 is Equation 2.7, If the op amp is ideal, the voltage V_i from the inverting OPAMP input to ground is driven to zero by negative feedback during $\emptyset_2$. By charge conservation, $Q_2 = Q_1$ [1]; therefore, V_o/V_s is given by Equation 2.8. Equation 2.8 is onllly valid as long as the OPAMP is ideal, because the output voltage waveform depends on the rates at which the capacitors are charged and discharged also these rates depend on the bandwidth of the OPAMP and the resistances of the closed switches.

$$Q_1 = (0 - V_s)C_1 + (0)C_2 = (0 - V_s)C_1 \tag{2.6}$$

$$Q_2 = (0 - V_s)C_1 + (0 - V_0)C_2 = (0 - V_o)C_2 \tag{2.7}$$

$$\frac{\Delta V_0}{\Delta V_S} = \frac{C_1}{C_2} \tag{2.8}$$

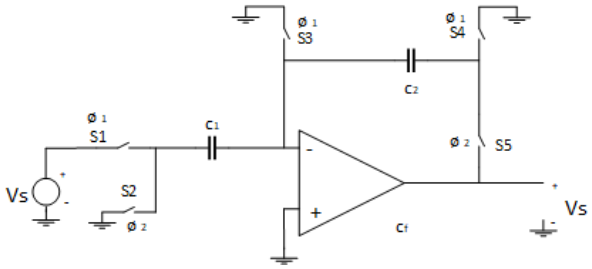


Figure 2.3: Schematic of a switched-capacitor amplifier with ideal switches.

2.1.5 Instrumentation Amplifier

An IAs, amplifies the difference between its input signals, an IA employs an internal feedback resistor network that is isolated from its signal input terminals, and defines the gain of the amplifier. the gain is either preset internally by an internal resistor or external gain resistor. A relevant characteristic of an IA is the rejection of any signals that are common to both inputs, providing the capability of extracting small signals from transducers and other signal sources. Common-mode rejection, CMRR, i.e canceling out any signals that are common, while amplifying any signals that are differential, is an important characteristic of an instrumentation amplifier. One of the most common IA topology is shown in Figure 2.4, is the three-OpAmp topology. This topology features, three OPAMP, that form the IA, through feedback by a resistor bridge network [5]. The voltage gain (A_v) is given by Equation 2.9 and controlled by an often variable resistor, R_{gain}. Finally, this topology operates properly with bridge-type sensors, which are common in biomedical measurement equipment [5].

$$A_v = \frac{V_{out}}{V_2 - V_1} = \left(1 + \frac{2R_1}{R_{gain}}\left(\frac{R_3}{R_2}\right)\right) \tag{2.9}$$

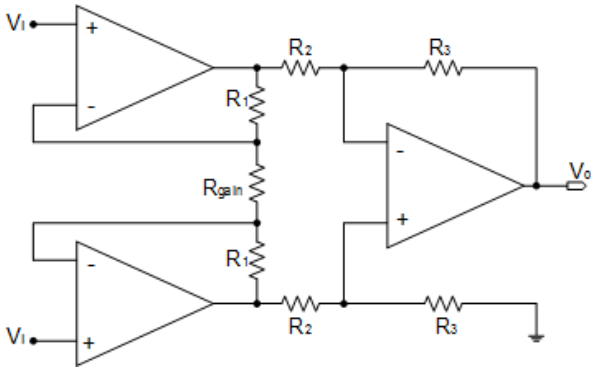


Figure 2.4: IA with Three OPAMP.

2.1.6 Programmable Gain Amplifiers

A programmable-gain amplifier, PGA, is usually placed before an analog-to-digital converter, ADC, in order to ease the dynamic range requirement for the ADC. The PGA, generally has three main topologies shown in Figure 2.5 [6].

Figure 2.5a, is a current divider, the control voltage V_c determines the dividing ratio although a linear-in-dB gain setting is difficult to realize due to the quadratic characteristic of the current divider. The overall linearity is limited by the input transconductor which generates I_i.

Changing the bias current of the transistors shown in Figure 2.5b implies a variance of the transconductance g_m of the source-coupled pair. The gain of the circuit is proportional to g_m of the input transistors. if the input signal is weak, a large bias current is needed to obtain high-gain and low-noise performance. Although when the input signal is large, the low bias current can degrade the linearity.

In Figure 2.5c the transconductance g_m of the source-coupled pair is varied by changing the resistance of the degeneration resistor R_s. When the input signal is weak, a small bias R_s is used to obtain high gain and low noise. When the input signal is large, a large Rs is used to obtain low gain and high linearity. Thus, this topology can achieve constant signal-to-noise-and-distortion ratio for the fixed output level regardless of the gain settings.

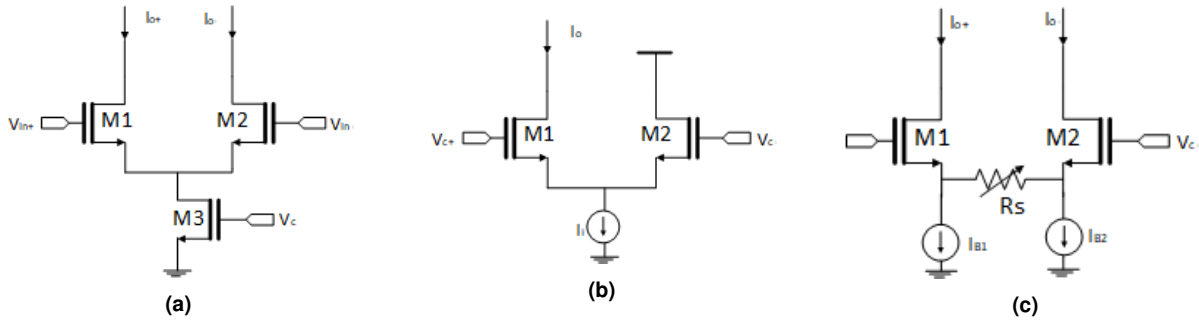


Figure 2.5: (a) Current Divider topology, (b) Source-coupled differential topology, (c) Source-coupled with degeneration.

2.2 Relevant Performance Metrics

To enable a suitable analysis of the PGA, in this section is described the most relevant metrics of the PGA performance.

2.2.1 Gain and Bandwidth

Signal amplification is from a conceptual point of view the simplest signal-processing task , an amplifier that preserves the details of the signal waveform is characterized by the relation (Equation 2.10),

that describes the ratio between the output voltage and the input voltage, (A_v), therefore represents the magnitude of amplification. The gain of active circuits has changes depending on the frequency, due the influence of the poles and zeros in the circuit, as seen in Figure 2.6a, where f_c is defined by the frequency where the gain decreases 3 dB regarding the maximum value. the spectrum of frequencies where the gain does not decrease 3 dB from the maximum value, describes the concept of BW [7].

The Gain-BandWidth Product (GBW) is the frequency where the gain equal 0dB.

$$A_v = \frac{V_{out}}{V_{in}} \tag{2.10}$$

2.2.2 Noise

Noise can be defined as a random unwanted disturbance in the signal of interest, and the problem created with the existence of noise, is dealt by trading it with power dissipation, speed, and linearity. By dividing the Root Mean Square (RMS) of the noise at the output, by the squared voltage gain of an amplifier, the input-referred noise is obtained. The input-referred is used to determine the noise contribution of a circuit when it is used in a system. There are different types of noise represented in Figure 2.6b, flicker noise, or $1/f$ noise, is a type of noise found in all active devices, this noise increases with the decreasing of the frequency of the system, limiting the bandwidth. The main cause for the existence of flicker noise is the random trapping of charge at the oxide-silicon interface of Metal Oxide Semiconductor Field Effect Transistor (MOSFET), designing larger transistors reduces the impact of this effect. The power density of the flicker noise decreases as the frequency increase and is characterized in Figure 2.6b by the corner frequency f_c, which is between the low-frequency region and the higher-frequency "flat-band", as it is indicated [3].

Shot noise is associated with a direct-current flow and a potential barrier for the charge carriers to overcome, it is the randomness of the arrival that generates shot noise.

The thermal noise comes from the thermally agitated charge carriers in a conductor that constitutes a randomly varying current that gives rise to a random voltage. Thermal noise is directly proportional to absolute temperature (unlike shot noise, which is independent of U_T), if U_T approaches zero, thermal noise also approaches zero [2].

Generally noise is not considered by its Spectral Density (SD), but converted to RMS noise, especially when its used to determine the total noise of a system. This conversion is done by integrating the noise SD in the desired BW, as expressed in Equation 2.11, where f_L and f_H are the inferior and superior limits of the BW, SD_f is the noise SD in the referred BW.

$$V_{RMS} = \sqrt{\int_{f_L}^{f_H} (SD_f)^2 df} \tag{2.11}$$

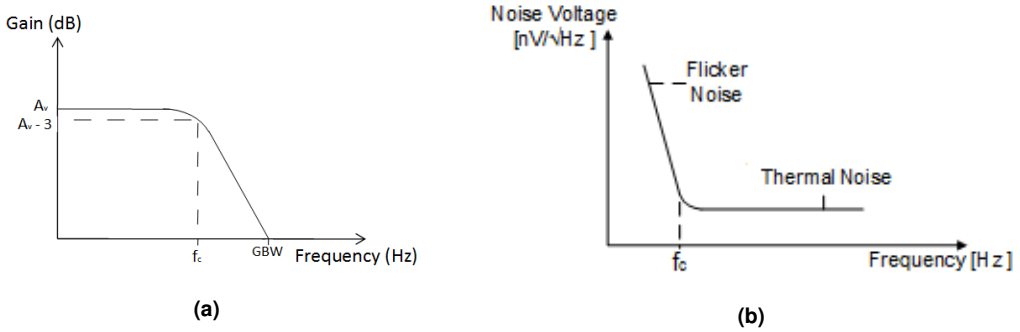


Figure 2.6: (a) Amplifier's gain in the frequency domain, (b) Flicker noise and thermal noise.

2.2.3 Common-Mode Rejection Ratio and Power Supply Rejection Ratio

The Common-Mode Rejection Ratio and Power Supply Rejection Ratio, CMRR, is defined as the magnitude of the ratio between the desired differential-mode gain and the undesired common-mode gain and is calculated by Equation 2.12. A low CMRR in a OPAMP would result in undesired signals, like noise that is common on both inputs, to also be amplified. Ultimately this can result in the saturation of the circuit or system.

The CMRR metric is essential and should be as high as possible, to reject coupled noise in each input. Moreover, an amplifier with multiple stages, its CMRR is the same as the CMRR of the input stage.

The PSRR determines how capable is an amplifier of suppressing any small variations on the power supplies or ground power buses. As with other analog circuits, op amps are often supplied from noisy lines and must therefore "reject" the noise adequately.

The PSRR can be defined as the ratio between the differential gain, and the gain from the power supply (V_{DD}) ripple at the output with the differential input set to zero, and it is given by Equation 2.13.

$$CMRR = \left| \frac{A_d}{A_c} \right| \tag{2.12}$$

$$PSRR = 20 \log \left(\frac{A_d}{A_{dd}(V_{in} = 0)} \right) \tag{2.13}$$

2.2.4 Total Harmonic Distortion

If a sinusoidal waveform is applied to a nonlinear system, the output signal will have harmonics in multiples of the fundamental frequency, including the fundamental harmonic.

Total Harmonic Distortion (THD) of a signal is characterized as the ratio of the total power of all second and higher harmonic components to the power of the fundamental harmonic for that signal, as

defined in Equation 2.14,

If a sinusoidal waveform is applied to a nonlinear system, the output signal will have harmonics in multiples of the fundamental frequency.

THD of a signal is the ratio of the sum of the magnitudes of all second or higher harmonic components to the power of that signal fundamental harmonic, as defined in Equation 2.14, where V_n is the RMS voltage of the n harmonics and V_1 is the RMS voltage of the fundamental harmonic.

For practical reasons, the power of only the first few harmonics, are considered since the distortion components falls off quickly for higher harmonics.

$$THD(\%) = 100 \cdot \frac{\sqrt{\sum V_n^2}}{V_1} \tag{2.14}$$

2.2.5 Linearity

Linearity, is an important metric to consider when characterizing an amplifier as amplifying signals without adding noise is not enough, it must also remain linear as strong signal are received, the amplifier must maintain a linear operation when receiving a weak signal in the presence of a strong interfering one, meaning that a gain compression can occur, by the reduction of gain for large power signals, caused by non-linearity of the transfer function of the amplifying circuit.

The gain compression can be represented as in Figure 2.7, where the output power is described as a function of the input power. While an ideal amplifier shown a linear behavior throughout (green), a real amplifier does not (red). The input power point where the real characteristic drops 1 dB, when referring to the ideal characteristic, is denominated 1-dB Gain Compression Point (P1dB). The point where this relation is 3 dB is also considered, and is denominated 3-dB Gain Compression Point (P3dB). A higher input power value where the gain compression phenomenon occurs is desirable, in the sense that the linearity is preserved for a larger spectrum of input power [3].

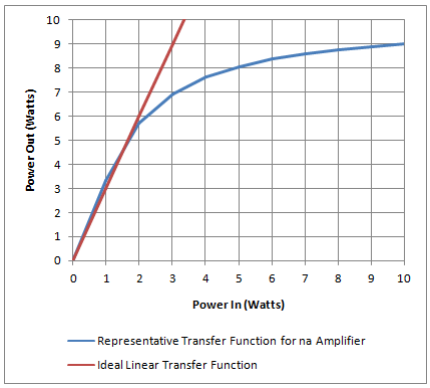


Figure 2.7: Gain compression phenomenon.

2.2.6 Figure-of-Merit

The energy-efficiency of the amplifier is evaluated according to the figure-of-merit Fiure-of-Merit (FOM) defined in Equation 2.15, i.e., the energy-efficiency is evaluated through the ratio of the GBW and the current consumption, i.e. I_{DD}, for a given output load i.e, C_L. the energy-efficiency FOM is used as a metric of comparison within the sate-of-the-art.

$$FOM = \frac{GBW \times C_[L]}{I_{DD}} \tag{2.15}$$

2.3 Circuit Topologies and Configurations

In this section amplifier topologies, from state-of-the-art work, are presented and discussed for the design of PGAs.

2.3.1 Negative Feedback gm Boosted Degenerated Differential Pair

A low-voltage low-power differential programmable gain amplifier is presented in paper [8], based on a gm-boosted source-degenerated differential pair. The programmability of the gain is given by a MOS-polysilicon resistor network and programmable output current mirrors. The proposed PGA is shown in Figure 2.8a, current flowing through transistor M_1 is held constant [9], [10], transistors M_1,M_2 form a two-pole negative-feedback loop that reduces the equivalent source resistance of the input voltage buffer M_1 down to 50 Ω, value approximately given by $1/(g_{m1}r_{o1}g_{m2})$.

The differential transconductance can be expressed as α/R, where α is the M_1 gate-to-source DC voltage gain. The modified differential pair makes it very useful for high-frequency and low-voltage operation. The linearized differential signal current, copied out by loading each M_2 gate terminal with a matched N-type Metal Oxide Semiconductor (NMOS) device and using cascode transistors M_3 to provide a high output resistance, is converted to voltage through load resistors R_L. Thereby, the differential gain of this stage is given by Equation 2.16.

The amplifier gain can be selected by using a variable degeneration resistor while maintaining a constant load resistor. which results in a fixed dominant pole at the PGA output nodes, and thus a constant bandwidth is maintained throughout all the gain stages [11]. This paper combines a linear polysilicon resistor and MOS transistors biased in the triode region, which act simultaneously as resistors and switches, to preserve good linearity and moderate area consumption, as shown Figure 2.8b.

The minimum gain setting is imposed by a fixed high resistivity polysilicon, high resistivity polysilicon (HRP) resistor R_0. The gain is then digitally controlled by adding in parallel a new linear resistor in series with two Medium-scale integration (MSI) NMOS switches biased in the triode region. An additional gain programmability degree is provided at the output current mirrors implemented through M_2-M_3 by adding

identical output stages in parallel, as shown also in Figure 2.8c. The M_3 cascode transistors act as the switching elements, controlled through a_j bits that fix the cascade gate voltage to $Vcas$ or to ground, thus allowing to set the output current mirror gain K to the desired value.

The PGA implementation is shown in Figure 2.8c. The supplied voltage is 1.8 V and the bias current value has been fixed to 40 pA, biasing currents have been implemented through cascode configurations. The total gain range is 0 to 21 dB, the gain programmability range is 3 dB steps, by a 4-bit discrete coarse tuning.

$$GAIN = \alpha \times \frac{R_L}{R} \tag{2.16}$$

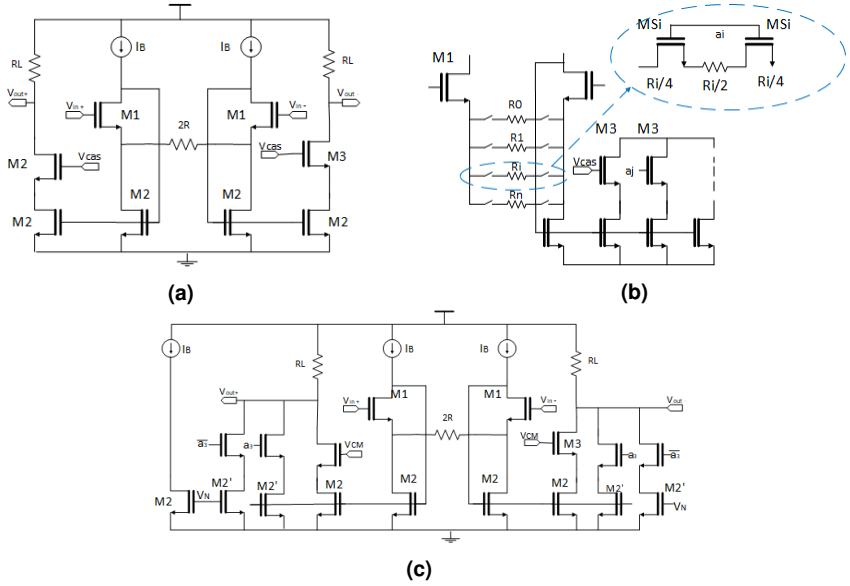


Figure 2.8: (a) Proposed PGA, (b) Digital gain programmability implementation, (c) PGA detailed schematic.

2.3.2 Fully Differential Voltage-Current Degeneration Amplifier

The paper [12] presents a low-voltage and low-power programmable gain amplifier, consisting of three fixed-gain stages and a variable-gain stage. It works at 2 MHz with a voltage gain range of 0 dB to 70 dB in steps of 2 dB. The fixed gain stage with an open-loop amplifier with source degeneration, achieving a gain range of 0 to 54 dB with 18 dB steps. AC coupling is applied to combine three of them together to eliminate DC offset due to its low power and ease of use. The variable gain stage is a closed-loop amplifier with switchable resistive feedback, it exhibits better linearity.

The variable-gain stage is a fully differential voltage-current degeneration amplifier, presented in Figure 2.9a. If the amplifier is assumed to be ideal, gain of the close-loop amplifier is given by Equation 2.17.

The gain varies through the variation of either R_f or R_{in}. It features high-linearity and high-precision

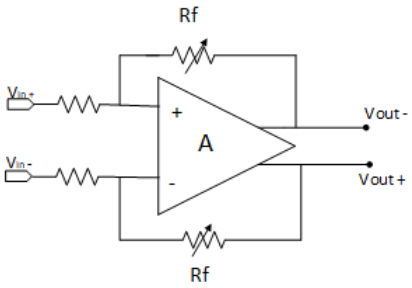
if the loop gain is large enough. If R_f is variable, the bandwidth of the amplifier is unstable. If R_{in} is variable, the input impedance of the amplifier is variable which makes it a variable load to the preceding stage.

Schematic of low-voltage amplifier, for the variable stage gain can be seen in Figure 2.9b. Taking into consideration the voltage requirement for the input, the lowest possible VDD can be obtained Equation 2.18 [13].

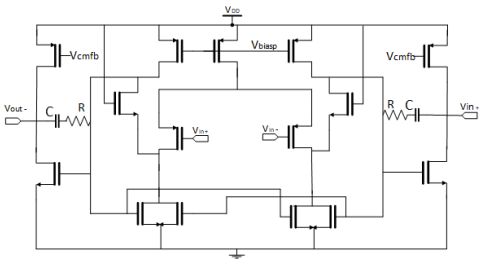
A cross-coupled active load is employed to realize a folded-cascode stage, acting like a built in CMFB circuit which senses the output of the first stage and regulates its common mode voltage [14]. The second stage of the op-amp is a common-gate amplifier with a shunt-shunt feedback. The output stage is a typical class-A amplifier which can deliver a high output swing by fixing the out-put common voltage to near $VDD/2$, requiring a CMFB circuit. A regular miller compensation capacitor is added between the second stage and the output stage to ensure the stability.

$$GAIN = \frac{R_F}{R_{in}} \tag{2.17}$$

$$VDD = |V_{t,p}| + 2V_{SDsat} + V_{DSsat} \tag{2.18}$$



(a) Voltage-current degeneration amplifier.



(b) Schematic of low-voltage amplifier.

2.3.3 PVT Insensitive Variable Gain Amplifier

Neural signals are low voltage and low frequency, between 1KHz and 8KHz and are contaminated by flicker and thermal noise, therefore a LNA should be able to detect any µV signal with low power consumption [15].

The authors of the paper [16], start with a basic differential pair without having any degeneration resistor, to implement a basic Variable Gain Amplifier (VGA), because there is no tail current noise problems and the circuit becomes insensitive to parasitic tail cap due to the virtual ground. The programmable gain is achieved by varying the current because tail current variation will create a variation on g_m in the input devices, the gain is given by $g_m(R_L||R_0)$.

This approach to achieve gain variation has two problems [17], one is variation in gain across Process, Voltage, Temperature (PVT) because g_m and R_L are sensitive to PVT. To solve the problem of variation of g_m due to PVT, a self-bias circuit to bias the amplifier is needed, this circuit uses a resistor as a reference and adjusts the bias current to make $g_m = 1/R_{ref}$. Thus the amplifier gain is given by Equation 2.19, making the gain insensitive to process.

The second problem is variation of the output common mode, due to variation in the current, which may push M_1 and M_2 out of saturation region. To solve this problem an output common mode feedback loop has been implemented, as shown in Figure 2.10a, as R_{cm}, M_3 and M_4 form the CMFB loop. M_3 and M_4 behave like variable current sources and inject control amount of current to keep out common mode close to the reference voltage. The constant g_m bias circuit show in Figure 2.10b, is based on the transistor overdrive voltage, as the based reference current has to be generated by subtracting V_{gs} of two scaled transistors and using a reference voltage. Transistor M_1 is 4x times larger than M_2. M_1 current can be expressed Equation 2.20

In Equation 2.20 R_s represents the effective resistance of M_1. To vary the bias current to change the amplifier gain a 4 bit resistor Digital to Analog Converter (DAC) has been used as shown in Figure 2.10b and by programming the gain control word, programmable amplifier can be achieved.

$$gain = g_m R_L = \frac{R_L}{R_S} \tag{2.19}$$

$$I_{N1} = \frac{2}{U_n C_{ox} \frac{W}{L}} \frac{1}{4R_S^2} \tag{2.20}$$

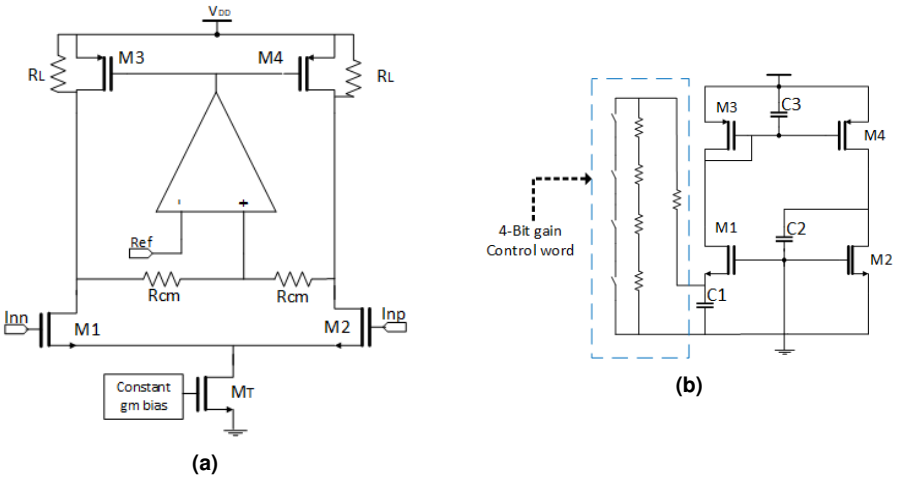


Figure 2.10: (a) Proposed PGA, (b) Constant g_m bias.

2.3.4 Local-Feedback Transconductors

The linear PGA using reconfiguration Local-Feedback Transconductors (LFT) schematic from [18], is presented in Figure 2.11 and intents to be used in an allergy biosensor. It is composed by a source follower stage, a reconfiguration encoder, a reconfiguration LFT gain stage, a voltage divider, a CMFB circuit and a bias circuit. The source follower stage is composed of two source followers which are used as the PGA's input devices, outputting one level shifted output signal each. The reconfiguration encoder, Figure 2.12a, is composed of three OR gates, and generates the digital control signals for the reconfiguration LFT stages. The reconfiguration LFT gain stage presented in Figure 2.13a main function is to obtain a process and temperature immunity variable gain without the loading effect [19].

It is composed of 8 LFT stages, controlled by digital signals. The configuration of the LFT stages changes according to the digital signal Dvga3 between gain stages (Gm-stage), which presents a pseudo-exponential approximation function and load stage. So, when Dvga3=1, stage1-4 are the gain stages and stage5-6 are the load stages as shown in Figure 2.13b, being otherwise when Dvga3=0. With this implementation a better linearity is achieved against the input voltage, for the variation of the system transconductance. In Figure 2.12b, the voltage divider is illustrated which bias the reconfiguration LFT stages along with the bias circuit that is shown in Figure 2.12c. The CMFB circuit in Figure 2.12d, senses the output signals and set the common-mode voltage of the LFT stages.

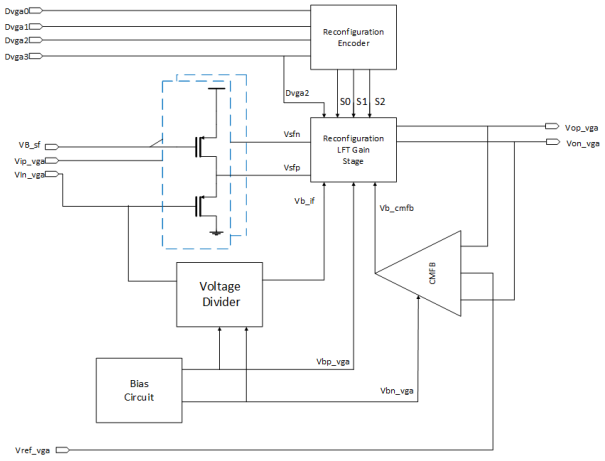


Figure 2.11: Linear PGA.

2.3.5 Programmable Gain Instrumentation Amplifier

In [20] a PGB-INA is proposed, Figure 2.14, featuring programmable gains and bandwidth, as well as low noise and high CMRR. The gain of the PGB-INA is given by Equation 2.21, where $(\frac{1}{r_{o_{p_1}}} + \frac{1}{r_{o_{N_1}}}) = \frac{1}{r_{o_{p_n}}}$, considering that $g_m << \frac{1}{R_1}$ and $g_m r_{o_{p_n}} >> 1$, the gain can be defined as Equation 2.22. Since it is intended for biomedical applications, High-Pass Filter (HPF) is implemented, reducing the flicker noise

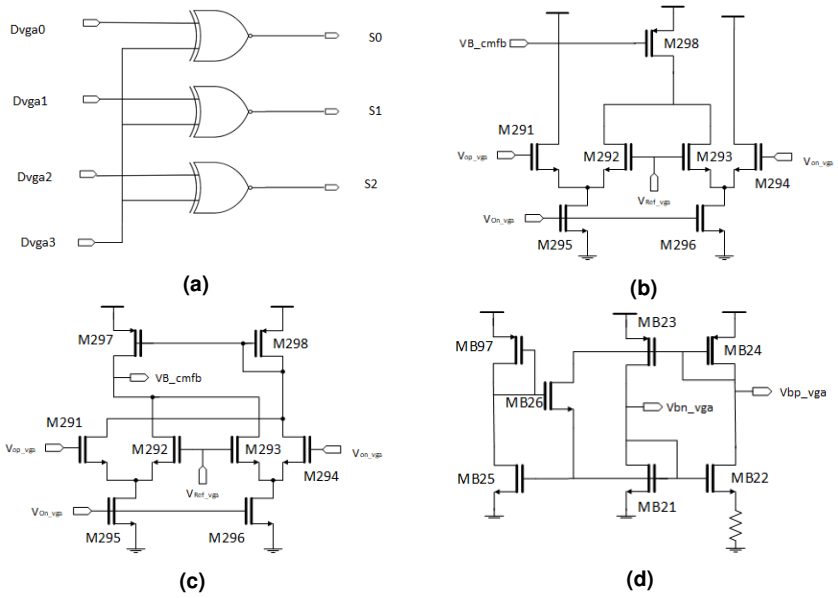


Figure 2.12: (a) Reconfiguration encoder, (b) voltage divider, (c) CMFB circuit, (d) bias circuit.

and DC offset voltage from the electrodes [21], while setting the input common-mode voltage and low-pass cutoff frequency. At the input stage the transistors $M_{P_{1,2}}$ and $M_{N_{1,2}}$ form a pair of input devices in an inverter configuration to enhance their transconductance, but are the main contributors for the noise performance. $M_{cas_{1,2}}$, improve the impedance level of the $M_{P_{1,2}}$'s drain, thus helping to achieve a higher loop gain. M_3 and M_4 are the output transistors, they pass the small-signal AC current from R_1 to R_2. M_5-M_8 are current sources, establish the current flowing through their respective stages. M_7 and M_8 along with M_9 and M_10, which are pseud-resistors, also set the output common-mode voltage. M_{11} and M_{12} are independent current sources that bias both the input and output stages. Transistors M_{13} and M_{14} and the capacitor C implement the embedded programmable LPF. The BW is set by controlling the current I_T, through the external control voltage $VBWC$ that bias the transistors M_{15} and M_{16}.

$$\frac{V_{od}}{V_{id}} = -\frac{\left(\frac{R_2}{2}\right)\cdot\left(g_m+\frac{4}{R_1}\right)}{1+\frac{\left(g_m+\frac{2}{R_1}\right)\cdot\left(\frac{R_2}{2}\right)}{g_{mr_{opn}}\cdot\left(\frac{g_{m_3}R_2}{g_{m_3}R_2+2}\right)}}\times\frac{1}{1+\frac{2C.s}{g_{m_{1,3}}}} \tag{2.21}$$

$$\frac{V_{od}}{V_{id}} = \frac{-2\times R_2}{R_1} \tag{2.22}$$

2.3.6 Fully Differential Rail-to-rail Current Mirror Input Amplifier

The PG-IA proposed in [22] was developed for biomedical signal processing. Its top-level architecture, shown in Figure 2.15, has a fully differential input and the gain is given by $\Delta V_{OUT} = (C_{IN}/C_F)\Delta V_{IN}$, where C_{IN} is a programmable capacitor to present different gains. To be applied in biomedical applica-

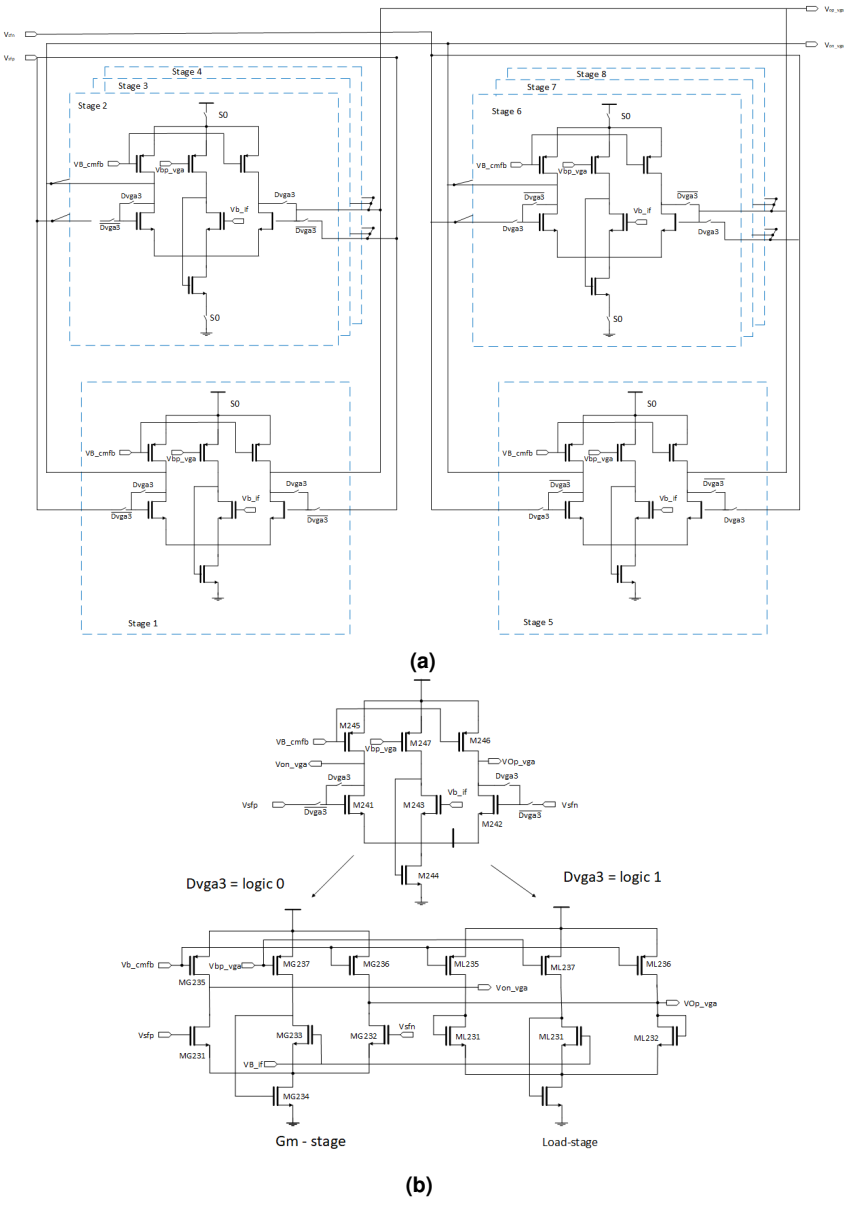


Figure 2.13: (a) Reconfiguration LFT gain stage , (b) Operation reconfiguration LFT stage.

tions a programmable HPF is used at the PG-IA input, thus reducing the flicker noise and the DC offset voltage from the electrodes.

On a low-level, the PG-IA implements a RR-CMI amplifier topology, intending to improve the dynamic performance, while reducing the power consumption and input referred noise, when compared to its counterparts. The RR-CMI, presented in Figure 2.16 has an input section (M_1 M_8), a current summing section (M_9 M_{17}, M_{19}, M_{22} and M_{24}) and a class AB output stage section (M_{18}, M_{20}, M_{21}, M_{23}). The input section is divided into two parts: the first, the transistors M_1 M_4 are calibrated one time to reduce the DC offset voltage; and the second part, the transistors M_5 M_8 that improve the device

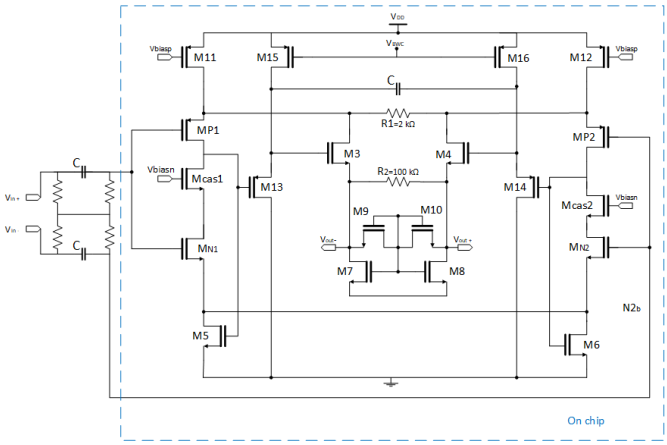


Figure 2.14: PGB-INA circuit diagram.

transconductance, input referred noise and DC offset voltage by combining their small signal current. The current summing section mirrors the input small signal current, providing the voltage to bias the output stage along with R_1 and R_2 resistors, which reduces the crossover distortion.

The class AB output section to improve the DC PSRR consists of a push-pull P-type Metal Oxide Semiconductor (PMOS) and NMOS cascode. The transistors operate mostly in the sub-threshold region to reduce the power consumption without compromising the performance. The RR-CMI 's gain is given by Equation 2.23, where A_{v1}, A_{v2} and A_{v3} are the gain of the input section, current summing section and class AB outputstage section, respectively.

However, the RR-CMI requires a CMFB circuit, a biasing circuit, and a calibration circuit, illustrated in Figure 2.17a, Figure 2.17b, Figure 2.17c, respectively. The CMFB circuit sets the common-mode DC voltage at the current summing section, presenting a static voltage reference of 0.5 V. Regarding the bias circuit, it generates the bias voltage $V_{BP1,2}$ and $V_{BN1,2}$. The topology is chosen due to its high PSRR and low flicker noise. Finally, the calibration circuit calibrates the input devices M_1 M_4 and R_{bias} from the biasing circuit, to reduce the mismatch ratio and therefore lowering the DC offset. The calibration is done by using an internal voltage reference to reduce DC offset and dynamic power consumption.

$$A_V = (A_{V1} \times K \times A_{V2} \times A_{V3}) \tag{2.23}$$

2.3.7 Switched-Capacitor PGA

The SC-PGA was developed by [23] to improve the accuracy, sampling rate and enhance the performance of a system. This PGA topology is presented in Figure 2.18 and is composed of a sampling

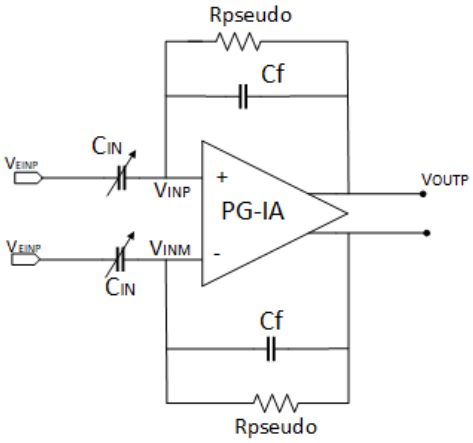


Figure 2.15: PG-IA top level architecture.

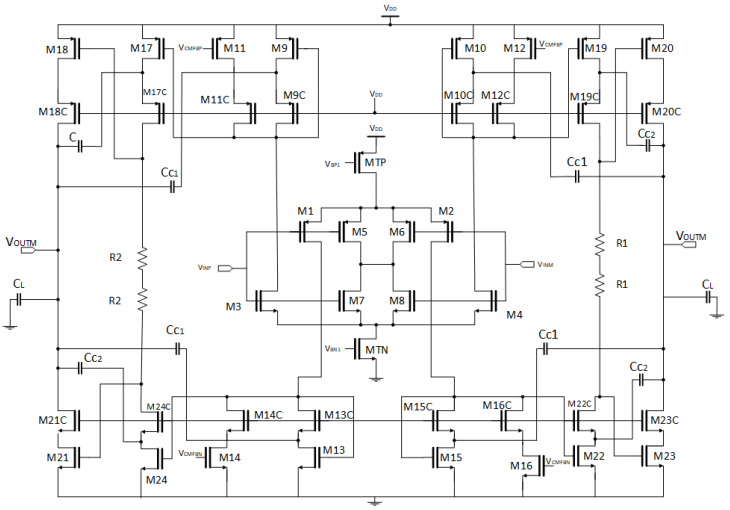


Figure 2.16: RR-CMI topology.

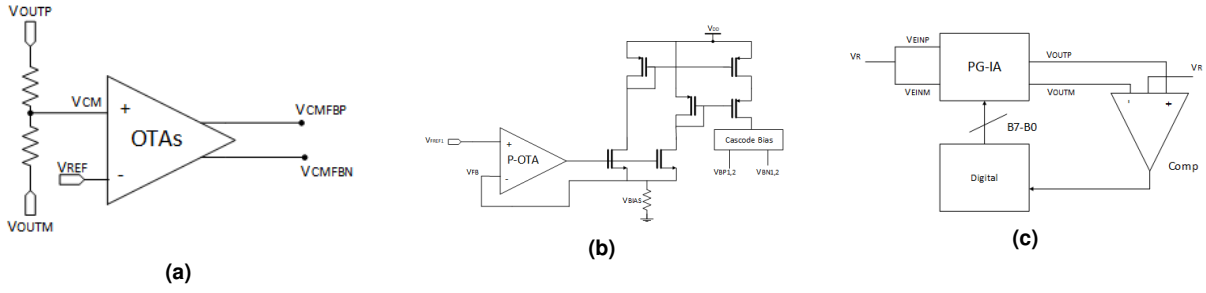


Figure 2.17: (a) CMFB circuit , (b) Biasing circuit, (c) Calibration circuit.

circuit, a two-stage amplifier, the feedback capacitor array, and the offset correction DAC capacitor array. The circuit is based on charge redistribution SC, presenting two non-overlapping clock signals, where the first sets $s5$, $s6$ to the common mode voltage, and the reference voltages respectively while closing

$s1$, $s3$, $s4$ and $s7$; the second sets $s6$ and $s5$ to the signal inputs and connects the DAC capacitor arrays, respectively. Thereby amplifying and correcting the offset simultaneously. Moreover, by increasing the PGA gain the output referred correction steps and ranges also increase. The output voltage is given by Equation 2.24. The DAC is required to provide the correction of the offset.

On a low-level, the two-stage OTA, Figure 2.19, used is based on folded-cascode, where the first stage presents a telescopic OTA architecture to enhance the gain and achieve high accuracy [24]. Since the common-mode voltage of an OTA with high gain has high sensitivity to the devices characteristic and mismatch a switched-capacitor common-mode feedback circuit, switched-capacitor common-mode feedback circuit (SC-CMFB), is used [25]. To stabilize the circuit a Miller capacitor array is implemented, since the variation of the PGA gain changes the GBW and phase margin.

$$V_{op} - V_{on} = \frac{C_s}{C_f}(V_{ip} - V_{in}) + \frac{C_{dac1}}{C_f}(V_{ref1} - V_{ref2}) \tag{2.24}$$

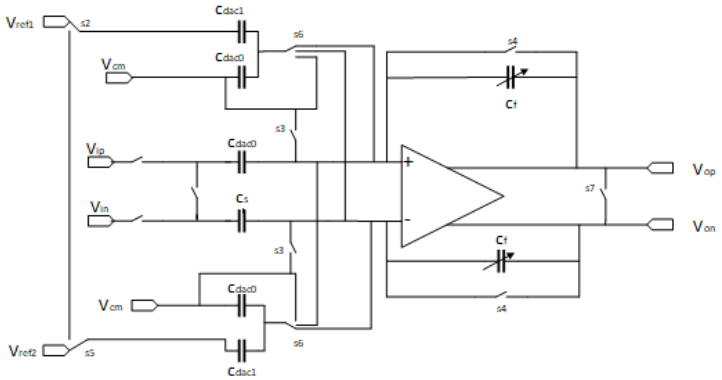


Figure 2.18: SC-PGA topology.

2.3.8 Operational Trans-Conductance PGA

In this paper [26], a neural amplifier for Local field potential (LFP), signals and spikes is implemented, the amplifier is tuned using digitally programmable array of capacitors to achieve different gains varying from 40 dB to 70 dB, and a tunable pseudoresistor to get a programmable lower cutoff frequency.

The amplifier consists of an operational trans-conductance amplifier, OTA, with a feedback MOS-bipolar pseudo-resistor in parallel with a capacitor in order to achieve a low cutoff frequency [27], as shown in Figure 2.20 [28] [29]. The amplifier has two inputs, where the reference voltage represents the voltage of the electrode in order to make the amplifier measurement with respect to it [21].

The gain of the amplifier is adjusted through the ratio between C_1/C_2, while the amplifier bandwidth is approximately equal to $g_m/A_M C_L$, where A_M is the amplifier gain, g_m is the trans-conductance of the OTA, and C_L is the load capacitance. In order to have a programmable gain two banks of capacitors, as

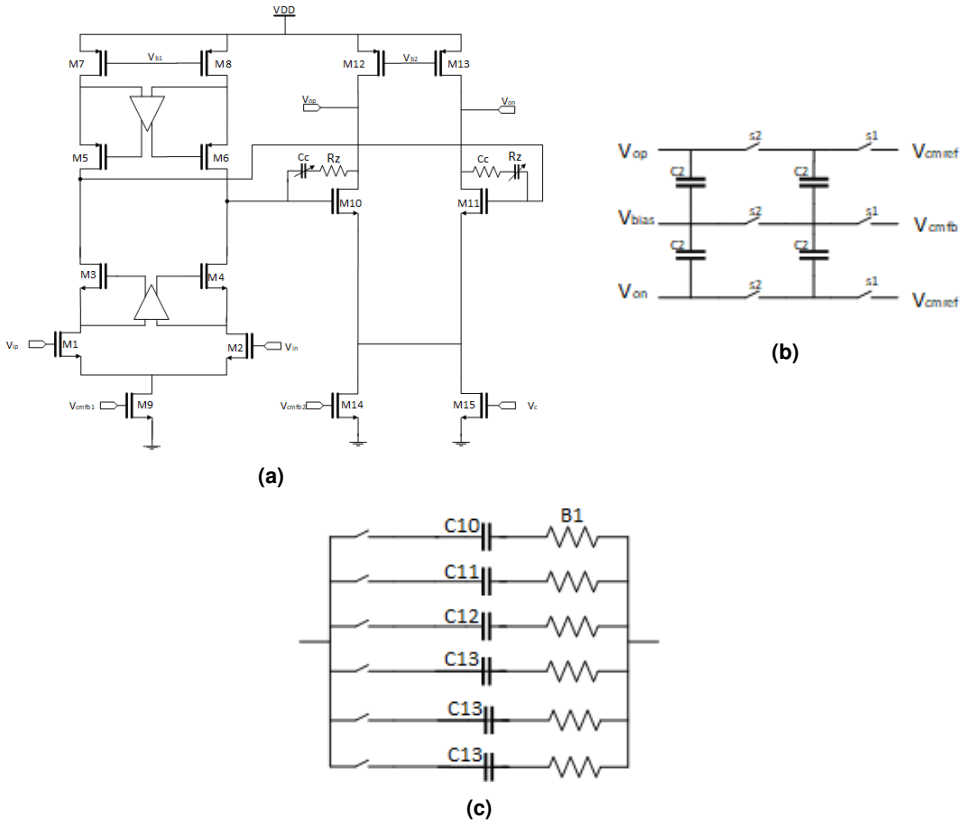


Figure 2.19: a) OTA topology; b) switched-capacitor common-mode feedback circuit; c) Miller capacitor array

show in Figure 2.21a were placed instead of C_1 and C_2. To achieve different gains, a series of control words are inserted to select between different values of capacitors, B_1-B_4, program C_1 and B_1-B_4 program C_2.

The OTA presented in [26] is shown in Figure 2.22, where M_{10} and M_{11} are the differential input pair transistors which control the transconductance g_m. Cascode transistors M_5, M_7, M_8, M_9 are used to increase the open loop gain. While, M_6 and M_{12} represent the cascode biasing transistors for the differential pair. Cascode transistors from M_{13} to M_{16} were added to increase the output resistance and hence the overall gain of the corresponding amplifier.

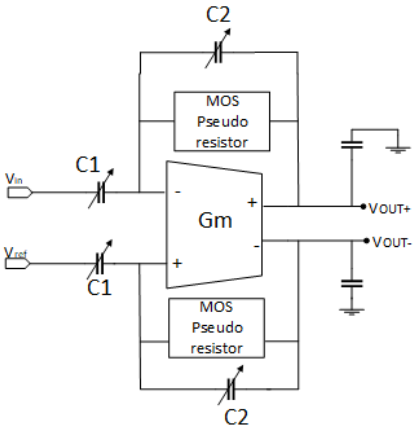


Figure 2.20: Digitally programmable neural amplifier.

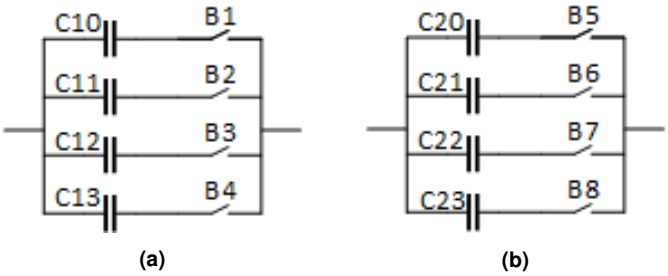


Figure 2.21: Bank of capacitors (a) C1 (b) C2

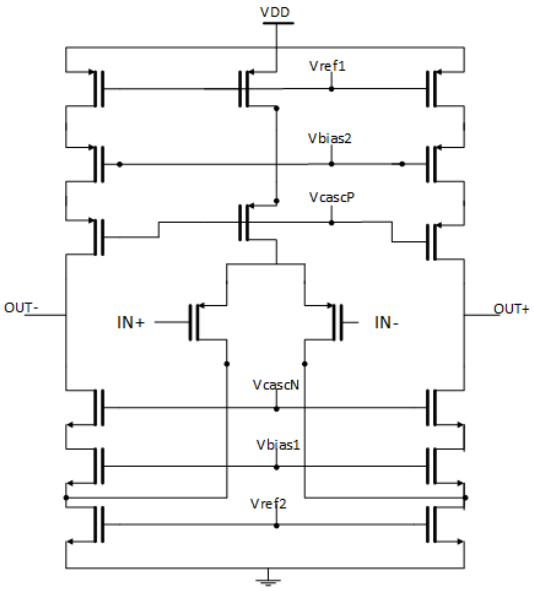


Figure 2.22: Fully differential OTA.

2.3.9 Summary

A summary of the state-of-the-art analyzed is compiled and summarized in Table 2.1, mainly performance metrics of the different circuit topologies and configurations. In [8], a source degenerated amplifier is used with a variable degeneration resistor to achieve a variable gain, achieving compact a area, but its linearity performance is depended on modern supply voltages. Paper [12] presents a fixed stage gain, based on an open-loop source generated amplifier, presenting a better trade-off between linearity and power consumption, however the variable stage is composed by a closed-loop voltage-current amplifier with switchable resistive feedback to help the linearity of the whole system, this has a higher area and a bigger current consumption than other approaches. In [16] a basic differential pair without any degeneration resistor, having variable gain by varying the current, a constant g_m self bias circuit is used to allow for the gain to be insensitive to the process variation, this approach requires a start-up circuit to kick start the bias current. Paper [18] uses reconfiguration local-feedback transconductance, allowing for the transconductance to be linear against the input voltage, yet this circuit has a large power consumption and a large area due to the utilization of buffers. In [20] a programmable gain and bandwidth instrumentation amplifier, with a variable gain given by changing the effective value of the resistance connected across the output terminals, salient features include high CMRR, and low area although it requires off chip resistors. Paper [22], uses a a low power programmable gain instrumentation amplifier, with improved DC PSRR and improved DC offset. Paper [26], presents low voltage fully differential gain and bandwidth amplifier through pseudo-resistor and capacitor in parallel, yet it has a power consumption of 12.48 µW higher than others.

Table 2.1: Summary of state-of-the-art PGA.

Work	[8]	[12]	[16]	[18]	[20]	[22]	[23]	[26]
Year	2006	2013	2017	2012	2017	2017	2017	2012
Tech (nm)	350	180	65	180	180	180	180	90
Gain (dB)	0-21	0-70	2-25	-24 - 21	30-40	35-70	-3 - 19	40-70
BW (MHz)	100	6.6-15	2	66.28	0.05-11 kHz	800-1400 Hz	40	175-316 mHz 23-69 Hz
Supply Current (mA)	0.28	1.26	0.5	5.3	0.0182	0.6μA	19.6	0.01
Supply voltage (V)	1.8	1	1.5V	1.8	1.8	1	3.3	1.2
Area (mm^2)	0.004	0.94	0.0045	0.7	0.03	0.0625	-	-

3

Circuit Topology

Contents

3.1 Theoretical Analysis 33
3.2 Biasing Strategy 34
3.3 Small-Signal Analysis 35
3.4 Ideal CMFB Circuit 37
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Circuit Topology

For a better understanding of the proposed circuit, an analytical study is done. Such study, begins with a review of the different aspects of the circuit, then a biasing strategy is defined, and finishing with a small signal analysis. The PGA topology chosen to be implemented, is presented in Figure 3.1, based on fully-differential OTA amplifier. Since it allows to obtain a different gain for each signal, presenting the possibility to have a low current consumption, enhanced GBW and linearity and also a low area.

3.1 Theoretical Analysis

For a better understanding of the proposed circuit, in Figure 3.1, an analytical study of all aspects of the circuit is done. The selection of the different gains of the circuit is done by transistors, $Pselb1$, $Pselc1$, $Pselb2$, $Pselc2$, this transistors are controlled by a selection signal, S, and act as switches, setting the current mirror factoring for the output stage. The value of the output current is defined by the size ratio of the transistors that form the PMOS basic current mirrors. Either is the currents mirrors $Pb1$-$Pc1$, $Pb2$-$Pc2$ outputting current with a ratio of K:1, or is $Pa1$-$Pc1$, $Pa2$-$Pc2$, with a ratio of h:1. Furthermore, a common mode feedback loop circuit must be employed, since this is a fully differential implementation.

The innovation proposed in this circuit, when compared to the known symmetrical CMOS OTA, relies on the fact that the traditional NMOS current-source that biases the differential-pair has been removed. Instead, two VC, in a cross coupled configuration ($Nvcup1$, $Nvcdn1$ and $Nvcup2$, $Nvcdn2$) are used to bias the differential-pair. The VC form a structure comprising of a common drain and a common-source device, in a cross-coupled configuration as Figure 3.2 shows. This has a twofold effect, the two voltage-combiners provide additional DC gain while biasing the differential pair and each one of the differential-pair devices act as common-source and common-gate, simultaneously. This way, GBW is enhanced and so is the energy-efficiency. The transfer function of this circuit was extracted using SapWin, for better comprehensibility, some aspects were simplified namely the body-effect of the transistors is neglected, and is presented in Equation 3.1, where $gds_{Nvcup+Nvcdn} = gds_{Nvcup} + gds_{Nvcdn}$ and $cdb_{Nvcup+Nvcdn} = cdb_{Nvcup} + cdb_{Nvcdn}$. From this transfer function is possible to obtain the open-circuit gain expression of the VC. Considering a gm_{Nvcup} and $gm_{Nvcdn} >> gds_{Nvcup+Nvcdn}$, Equation 3.2, can be simplified.

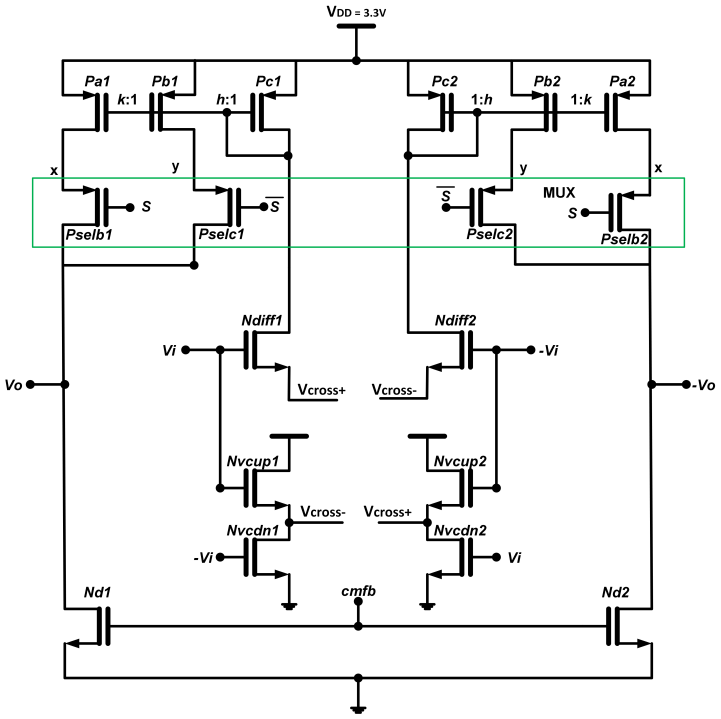


Figure 3.1: Implemented circuit.

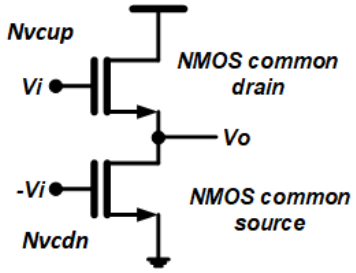


Figure 3.2: Voltage-combiner circuit.

$$H(s) = \frac{gm_{Nvcdn} + gm_{Nvcup} + (cgs_{Nvcup} - cgd_{Nvcdn}) \times s}{gm_{Nvcup} + gds_{Nvcup+Nvcdn} + (cdb_{Nvcup+Nvcdn} + cgs_{Nvcup} + cgd_{Nvcdn}) \times s} \tag{3.1}$$

$$A_{VC} = \frac{gm_{Nvcdn} + gm_{Nvcup}}{gm_{Nvcup} + gds_{Nvcup+Nvcdn}} \approx 1 + \frac{gm_{Nvcdn}}{gm_{Nvcup}}, |A_{VC}| > 1 \tag{3.2}$$

3.2 Biasing Strategy

Some definitions should be taken into account for the biasing strategy. Thereby, it is defined that, at an initial stage, V_{DD}=3.3 V, Threshold Voltage (V_{TH})= 1 V, V_{OUT}=1.65 V and the current consumption should be below 1 µA. The proposed PGA biasing strategy is started considering an ideal source

current instead of the VC, Figure 3.3a, for this circuit a first approach was design to achieve the gain requirements, considering the current limitation. Then the VC are considered and the biasing is strategy defined, Figure 3.3b. Some considerations taken into account while developing the biasing strategy are that transistors should be in the saturation region. Since the transistors,$Nvcdn1$, $Nvcdn2$, impose the current consumption of the differential pair and the VC's transistors, in order to maximize the gain without increase the current consumption, the transistors, $Nvcup$, $Ndiff$, should be in the sub-threshold region to achieve high gm/id. Considering the technology sizing limitations, and the current budget the least amount of current in order to obtain the gain was a design strategy for the proposed PGA is depicted in Figure 3.3b

3.3 Small-Signal Analysis

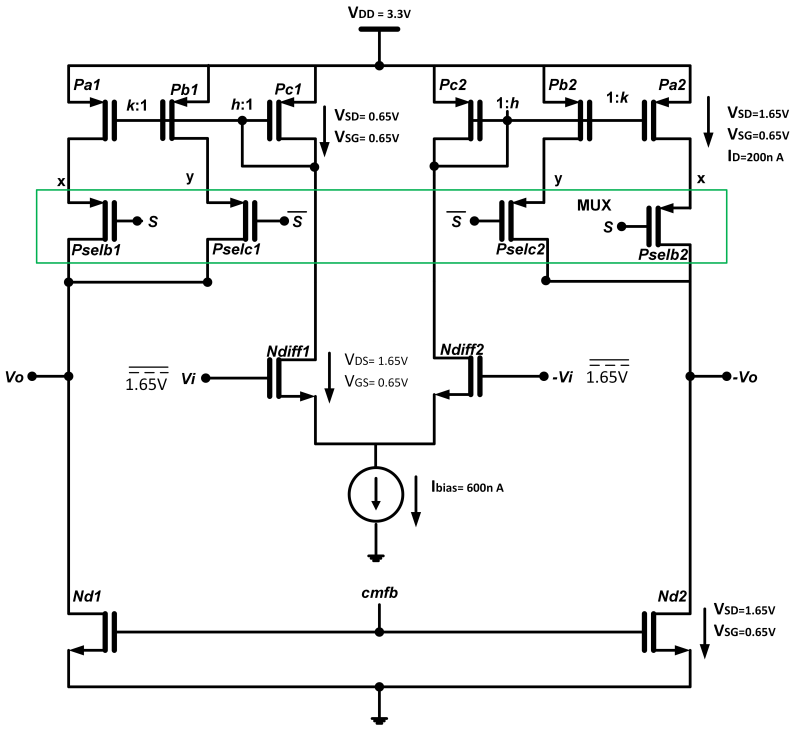
In this section the small-signal equivalent circuits of the components of the PGA are presented along with the gain equations. The Bartlett's bisection theorem is used to obtain the circuit. When a differential voltage signal is applied to both inputs an exchange of current between both networks will occur. This occurs due to the counterpart nodes movement from both networks, since they have the same amplitude but with phase opposition, just like the differential voltage. However, to support the condition where there are symmetric voltages between the two symmetric networks, the voltages connecting the nodes that are shared along the axis of symmetry have to be equal to zero, a virtual ground.

3.3.1 Current Biased PGA

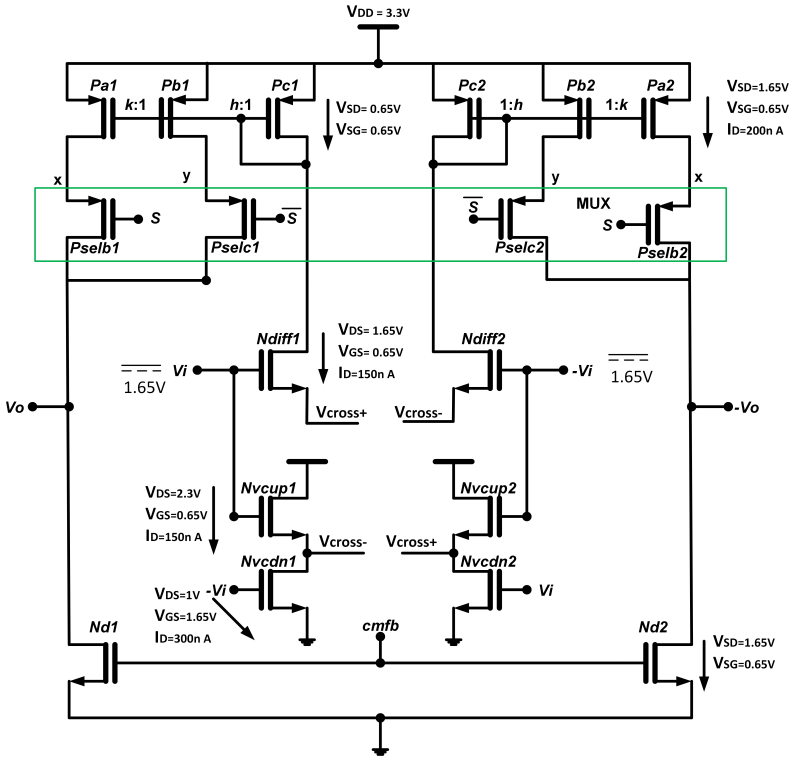
The circuit without the voltage combiners and instead an ideal current source is analysed, Figure 3.3a. The small signal analysis is considered and utilizing the bisection theorem, the small signal equivalent circuit is obtained Figure 3.4. Through the analyzed of the circuit it is possible to determine the gain, Equation 3.3. The contributions to the gain are the current-mirror factor, B, given by Equation 3.4, the parallel of the transistors Pb's or Pa's resistance, $r_{o_{Pa/b}}$, with the transistors Nd's resistance, $r_{o_{Nd}}$, finally the transconductance of transistors $Ndiff$.

$$A_v = B \times gm_{ndiff} \times (r_{o_{Pa/b}} || r_{o_{PNd}}) \tag{3.3}$$

$$B = \frac{I_{out}}{I_{ref}} = \frac{\frac{1}{2}\mu_p C_{ox}\frac{W_{Pa/b}}{L_{Pa/b}}(V_{SG_{Pa/b}} - V_{TH})^2}{\frac{1}{2}\mu_p C_{ox}\frac{W_{Pc}}{L_{Pc}}(V_{SG_{Pc}} - V_{TH})^2} = \frac{\frac{W_{Pa/b}}{L_{Pa/b}}}{\frac{W_{Pc}}{L_{Pc}}} \tag{3.4}$$



(a) Current Biased PGA.



(b) VC Biased PGA.

Figure 3.3: Biasing strategy.

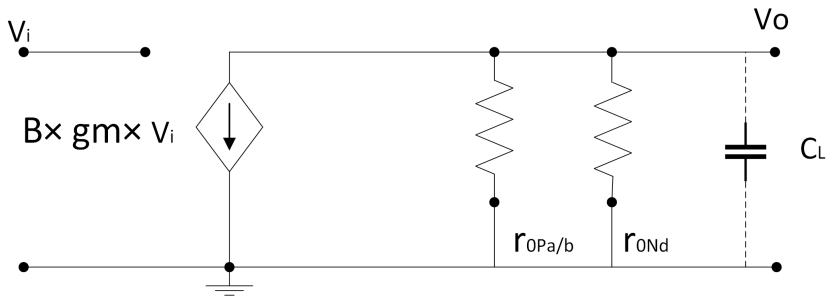


Figure 3.4: Small-signal equivalent circuit of current biased PGA.

3.3.2 VC Biased PGA

The gain expression for the VC biased circuit, can be obtained through the combination of the calculations done for the VC's gain, Equation 3.2, and for the current biased PGA. As such, the gain of PGA with the added gain provided by the VC, is as demonstrated in Equation 3.5, thus demonstrating that the VC, will increase the global gain of the PGA.

$$A_v = B \times \frac{gm_{ndiff}(1 + A_{V_{VC}})}{gds_{Pa/b} + gds_{Nd}} \tag{3.5}$$

3.4 Ideal CMFB Circuit

A CMFB circuit senses the common-mode voltage, comparing it with a proper reference, and feeding back the corrected common-mode signal on both nodes of the fully-differential circuit, with the purpose to cancel the output common-mode current component, and to fix the DC outputs to the desired level. The ideal and continuous-time common mode feedback, CMFB, circuit shown in Figure 3.5, must be employed, since this is a fully-differential implementation. The CMFB circuit implements directly the Equation 3.6, where the differential Offset Voltage (VOS) is compensated in the CMFB mode, taking into consideration the Voltage-Bias (VBIAS) voltage that directs the output.

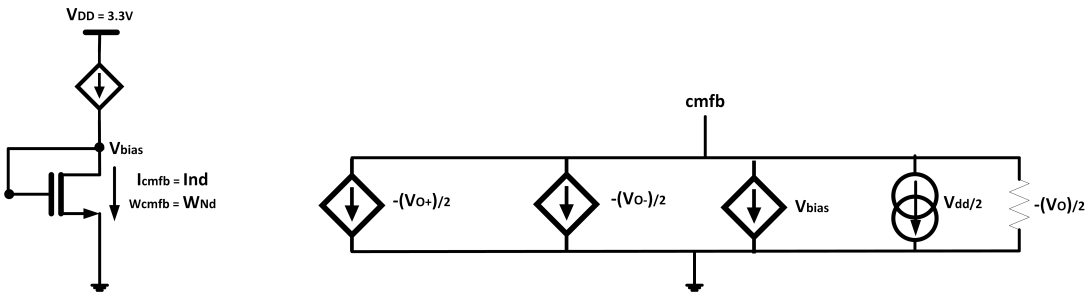


Figure 3.5: CMFB circuit.

$$cmfb = -\left(\frac{V_{DD}}{2} - \left(\frac{V_{out+}}{2}\right) - \left(\frac{V_{out-}}{2}\right) - V_{bias}\right) \tag{3.6}$$

3.5 Summary

In this chapter a theoretical analysis of the circuit was done, through the use of the bisection theorem the small signal circuit was obtained and the gain equation determined. An initial biasing strategy was established by defining the current consumption in each branch of the circuit and the voltage value in each node of the circuit. In the next chapter a continuation of the biasing and the sizing of the transistors is performed and explained.

4

Implementation and Simulations Results

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Implementation and Simulations Results

This section presents the various phases for the implementation of the PGA. An initial circuit implementation is done in UMC 130 nm CMOS technology using the software Cadence IC. The proposed PGA is implemented at sizing level, design strategies and simulation results are presented. During the circuit sizing a special attention is given to the current consumption.

4.1 PGA DC Biasing Strategy

As in chapter 3, some specification have to be defined as such V_{DD}=3.3 V, V_{TH}= 0.7 V, V_{DC}=1.65 V. This section presents the final biasing of the PGA. The biasing developed for the VC biased PGA is presented in Table 4.1. These results show the DC operating points and current present in all transistors. To extract the values a DC simulation is done with both inputs having a DC bias voltage of $V_{DD}/2$. Since the bio-potential signal EOG has as a lower amplitude than the EMG signal, the gain applied should be respectively 60 dB and 40 dB.

Most of the transistors operate in the saturation region, except transistors $Nvcup$, $Ndiff$, which operate in the sub threshold region to achieve the pretended gain values. Transistors $Pselb1$, $Pselc1$, $Pselb2$, $Pselc2$, which function as switches and operate in the triode region when selected or in the cut-off otherwise.

4.2 Programmable Gain

The gain value, 60 dB, is given when the output stage composed by the transistors Pa and Nd is activated through the transistors $Pselb$, the gain value, 40 dB, is given when the output stage composed but the transistors Pb and Nd is activated through the transistors $Pselc$.

The gain value of the PGA, given by Equation 4.1, depends on the gm of the differential pair, transistors $Ndiff$, on the gain given by the VC, $A_{v_{VC}}$, given by Equation 4.2, the transconductance of the

Table 4.1: DC analysis.

	V_{DS} [V]	V_{GS} [V]	V_{TH} [V]	V_{DSAT} [mV]	I_D [nA]
Ndiff	1.64	1	0.630	43.2	155
Nvcup	2.28	0.630	0.741	43.1	146
Nvcdn	1	1.65	1	377	898
Pc	0.640	0.640	0.604	68.9	155
	V_{DS} [V]	V_{GS} [V]	V_{TH} [V]	V_{DSAT} [mV]	I_D [nA]
Pa	1.38	0.640	0.603	69.6	191.6
Nd	1.9	0.696	0.398	219	191.6
Pselb	0.0083	1.9	1.15	594	191.6
	V_{DS} [V]	V_{GS} [V]	V_{TH} [V]	V_{DSAT} [mV]	I_D [nA]
Pb	1.38	0.640	0.553	88.1	191
Nd	1.9	0.696	0.398	219	191
Pselc	0.0083	1.9	1.15	594	191

transistors are given by Equation 4.3.

Taking into consideration that the transistors drain current, in the saturation region, is given by Equation 4.4, the strategy to increase the gain to the desired value is to adjust the width and length of the transistors to increase or decrease the drain current as necessary. Therefore as a starting point the ratio W/L of the transistor $Nvcdn$ is considered in order to have the least drain current possible while maintaining transistors in saturation region. Next the racio W/L of the $Nvcup$ and $Ndiff$ are projected with the intention to have a similar drain current in both transistors as this gives a better balance between obtaining the gain value and have a higher bandwidth. Transistors $Nvcup$ and $Ndiff$ are designed to operate in the sub-threshold region in order to maximize the gm/ID relation. The racio, of the transistors Pc and Pb, ($\frac{W_{Pb}}{L_{Pb}}/\frac{W_{Pc}}{L_{Pc}}$), or Pc and Pa, ($\frac{W_{Pa}}{L_{Pa}}/\frac{W_{Pc}}{L_{Pc}}$), represented by B in Equation 4.1, also influences the gain. The value of B is chosen in order to have the gain value pretended for the respective signals, while keeping the current consumption under 1 µA. Finally the gain of the PGA is depended on the gds of transistor Nd and gds of transistors Pa or Pb depending on the gain value selected, as gds is given by Equation 4.5.

$$A_v = B \times \frac{gm_{ndiff}(1 + A_{V_{VC}})}{gds_{Pa/b} + gds_{Nd}} \tag{4.1}$$

$$A_{VC} = \frac{gm_{Nvcdn} + gm_{Nvccup}}{gm_{Nvccup} + gds_{Nvccup+Nvcdn}} \tag{4.2}$$

$$gm = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GS} - V_T} \tag{4.3}$$

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 \tag{4.4}$$

$$gds = \frac{1}{r_o} = \lambda I_D \tag{4.5}$$

4.3 Cadence Schematic Implementation

In this section, it is shown the PGA's components sizing and schematics. All the components are designed with 130 nm technology and are built with PMOS transistors PHG33L130E and NMOS transistors NHG33L130E. The components biasing region is also presented and the description of the numbers used is shown on Table 4.2, which are obtained via DC simulation on the Cadence program. The electric schematic is presented in Figure 4.1 and the size of the transistors and their operating region, that compose the PGA are presented in Table 4.3.

Table 4.2: Transistors regions code.

Region	Code
Cut-off	0
Triode	1
Saturation	2
Sub-Threshold	3

4.4 Test-benches and Simulations

In this section, the PGA's simulations necessary to verify if the sizing reaches the intended requirements are done also the test-benches used are presented. A brief introduction is done to coherent sampling necessary for the DFT simulation. The analysis is focus on the EMG and EOG signals, considering an amplitude of 1 mV, 100 µV respectively.

4.4.1 Gain and Phase Margin Simulations

To verify if the sizing reaches the intended requirements, some simulations are needed. Therefore, the test bench presented in Figure 4.2 is used to simulate the gain and BW, phase margin and noise.

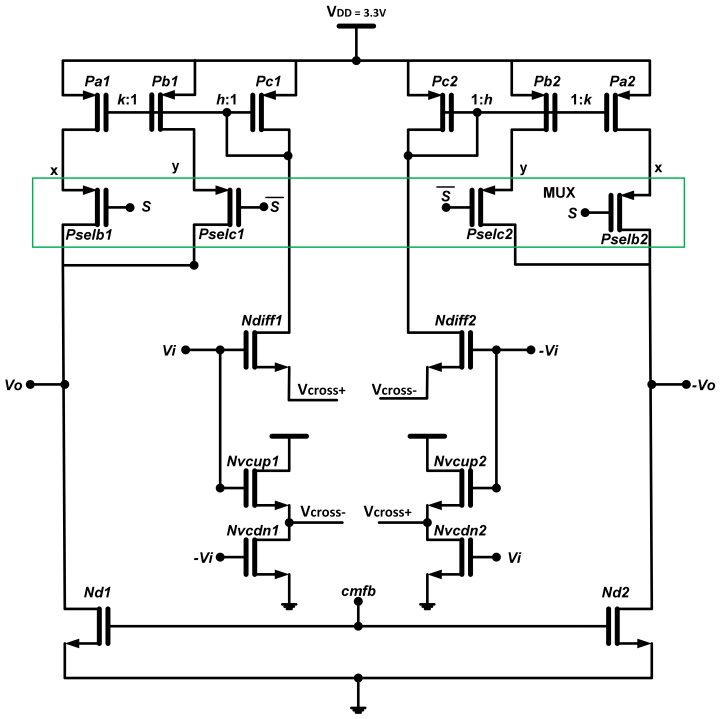

Figure 4.1: Implemented circuit.

Table 4.3: Transistors sizing.

	W [µm]	L [µ m]	Region
Ndiff	27	3	3
Nvcup	25	3	3
Nvcdn	0.2	47	2
Pc	4	2	2
Pa	4.8	2	2
Pb	0.3	0.3	2
Nd	1u	25	2
Pselb	1	1	1
Pselc	1	1	1

The gain simulation is given by the the slope calculation of the PGA output 0 to 1 V of the differential input voltage. Thus, V_{in+} and V_{in-} have both a DC voltage of 1.65 V and an AC voltage of 1 V and 0 V, respectively. The analysis done to obtain the gain is an AC with a logarithmic frequency variation from 1 Hz to 1 MHz. The resulting voltage gain is 61.83 dB, with a BW of 617.86 Hz, as showed in Figure 4.3, for the EOG signal. As for the phase margin for this signal, it is portrayed in Figure 4.4 presenting a value of 82.32°. The voltage gain is 40.77 dB, with a BW of 5.87 kHz, as showed in Figure 4.5, for the

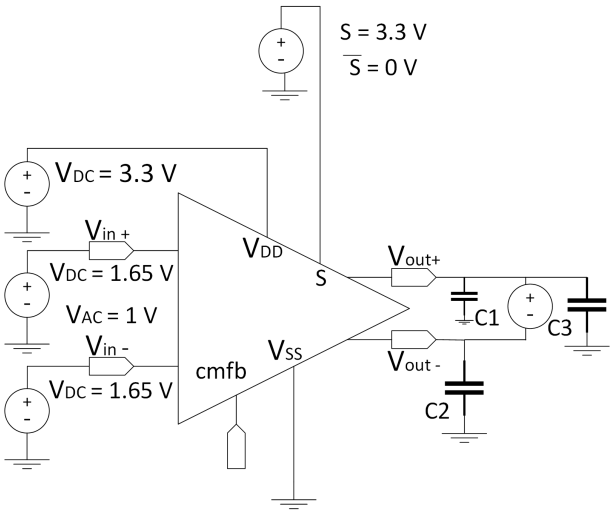

Figure 4.2: Test-bench for PGA's noise and AC simulations

EMG signal. As for the phase margin, it is portrayed in Figure 4.6 presenting a value of 84.01°.

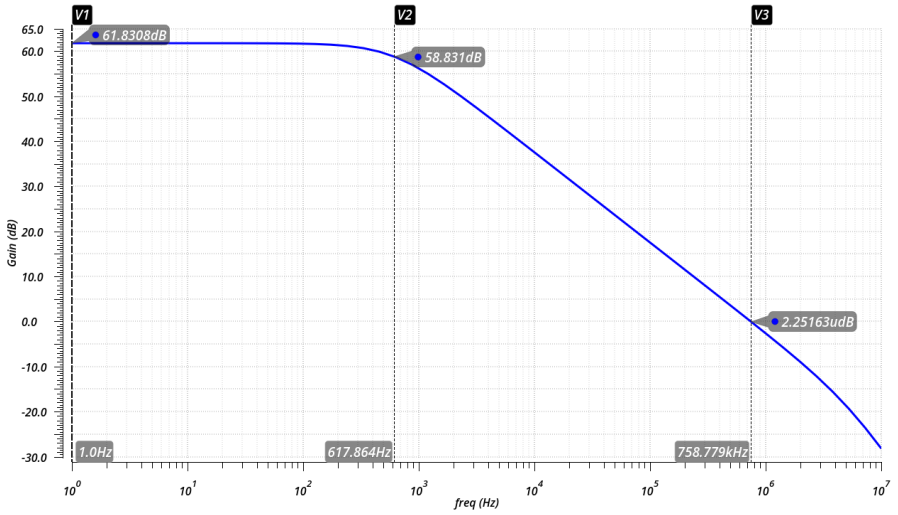

Figure 4.3: PGA gain simulation EOG signal.

The noise simulations are executed in the same test-bench and is done by having logarithmic frequency variation from 0.1 Hz to 1 MHz, the plots are presented in Figure 4.7, for EOG and Figure 4.8, for EMG. The circuit presents a flicker noise of 15.14 μVrms and a thermal noise of 8.1 μVrms for the signal EOG, and a flicker noise of 96.4 μVrms and a thermal noise of 22.8 μVrms, for the signal EMG. The input referred-noise is 23.2 μVrms and 117 μVrms, for the signal EOG and for the signal EMG, respectively.

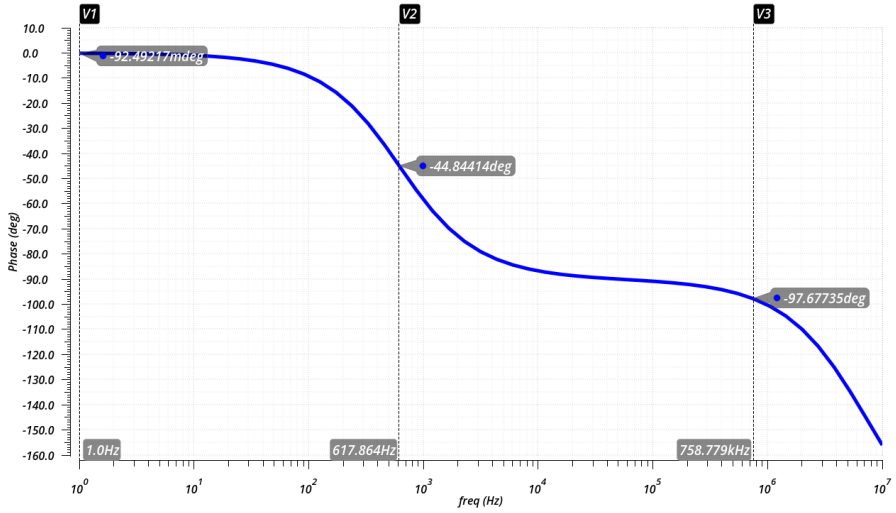

Figure 4.4: PGA phase simulation EOG signal

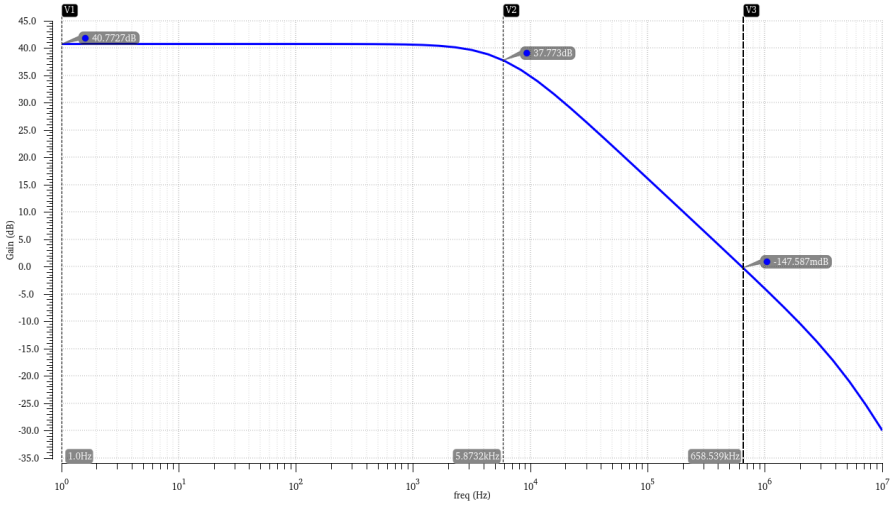

Figure 4.5: PGA gain simulation EMG signal.

4.4.2 Coherent Sampling Transient Analysis

To verify the PGA linearity when EOG and EMG signals are applied, one must calculate the THD and dynamic range values. In order to do so, the PGA transient response and respective DFT for each signal is required, as such, a proper test bench that enables it, is demonstrated in Figure 4.9. In this test bench, a sine voltage supply is applied to the positive input, with DC voltage of 1.65 V, and an amplitude and frequency depending on each signal that is being simulated, while at the negative input is applied only the DC voltage of 1.65 V.

As mentioned before, to obtain the THD and dynamic range values, the DFT from a transient output has to be calculated. In order to obtain the DFT output, coherent sampling is considered, since it reduces

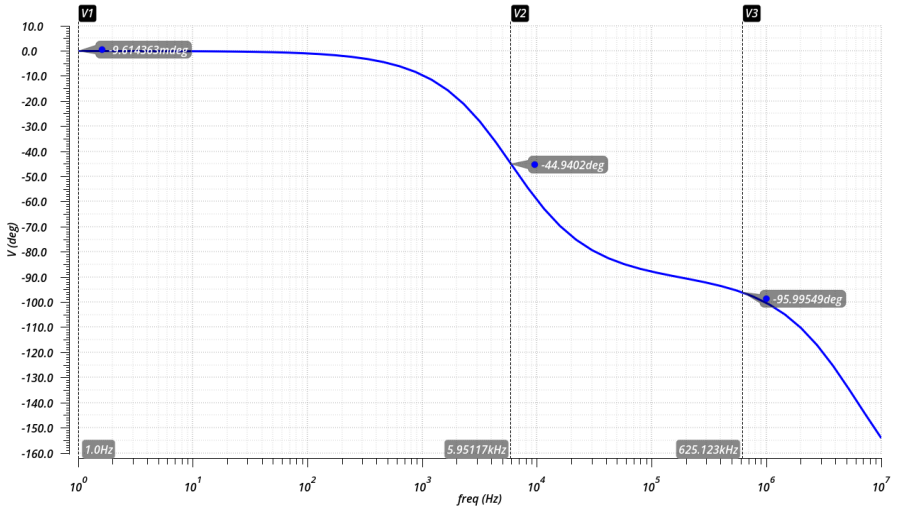

Figure 4.6: PGA phase simulation EMG signal

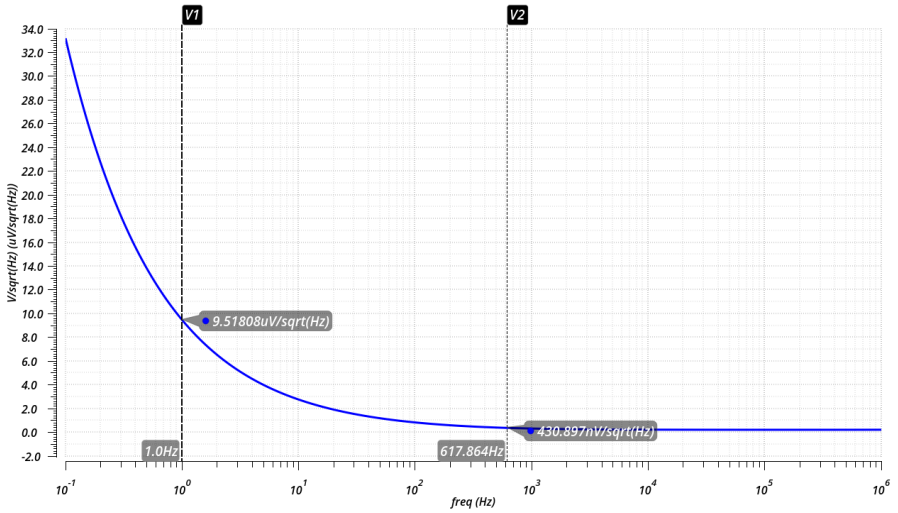

Figure 4.7: PGA input referred noise for EOG signal

the spectral leakage. Coherent sampling is the sampling of a periodic signal, where an integer number of its cycles is adjusted into a predefined sampling window, as depict in Equation 4.6, in which f_{in} is the input frequency, f_S is the Sampling Frequency, M_{cycles} is the number of cycles and $N_{samples}$ is the number of samples. To assure coherent sampling, first Sampling Frequency (FS) and the number of samples are chosen, taking into account that FS should be at least two times more than the input frequency according to the Nyquist's theorem, and the number of samples have to be a power of two, corresponding to the bit accuracy. Then, using a intended input frequency, the number of cycles is calculated. Since the number of cycles has to be integer and should be prime so that samples do not be repeated, the calculated number of cycles is rounded to the nearest prime number, from which maintaining FS and the number of samples, the input frequency that will be used is obtained. As the

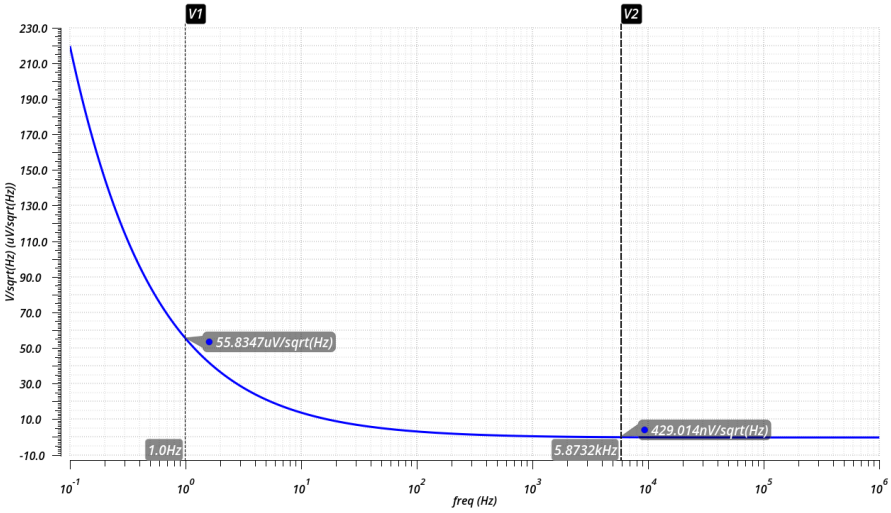

Figure 4.8: PGA input referred noise for EMG signal

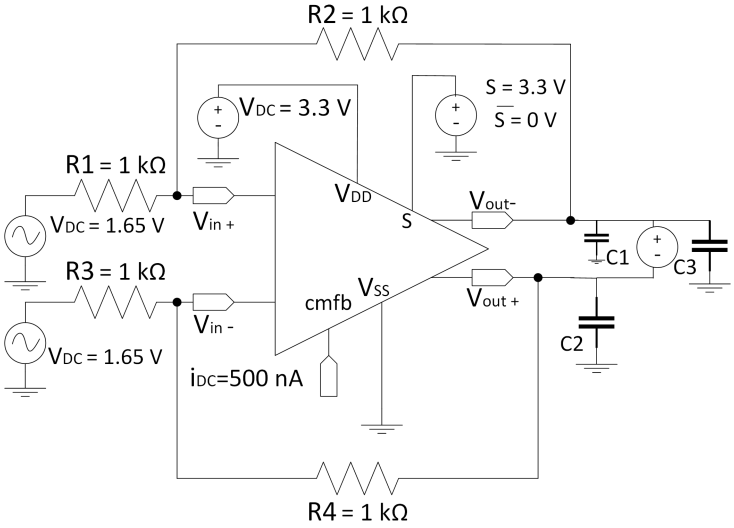

Figure 4.9: Test bench for the closed loop transient analysis.

DFT does not consider continuous samples, spectral leakage is inevitable, therefore to minimize it, a window function is normally used. In this case the hamming window is applied because it is normally used in experimental measurements, plus Hamming window does a better job of cancelling the nearest side lobe but a poorer job of canceling any others. Thus, this window functions is useful for noise measurements where presenting better frequency resolution [30]. Thus, beginning with the EOG signal, the applied amplitude is 0.1 mV and the frequency, according to Equation 4.6, is 8.544 921 875 Hz, for FS of 5 kHz, 7 cycles and 4096 samples, i.e., an accuracy of 12 bit. Figure 4.10 presents the transient response and its DFT plot obtained from 0.1 s to 0.9192 s in a hamming truncation window. Hence, the obtained THD is 0.277 % and the dynamic range is 143.82 dB. As for the EMG signal, the PGA transient

and DFT response to a 101.318 359 375 Hz sinusoidal input, corresponding to a FS of 5 kHz, 83 cycles and 4096 samples, with an amplitude of 1 mV is illustrated in Figure 4.11, where the DFT is obtained in the same time period as the one before. This figure shows a THD of 0.0399 %, while the dynamic range is 68.93 dB.

$$\frac{f_{in}}{f_S} = \frac{M_{cycles}}{N_{samples}} \tag{4.6}$$

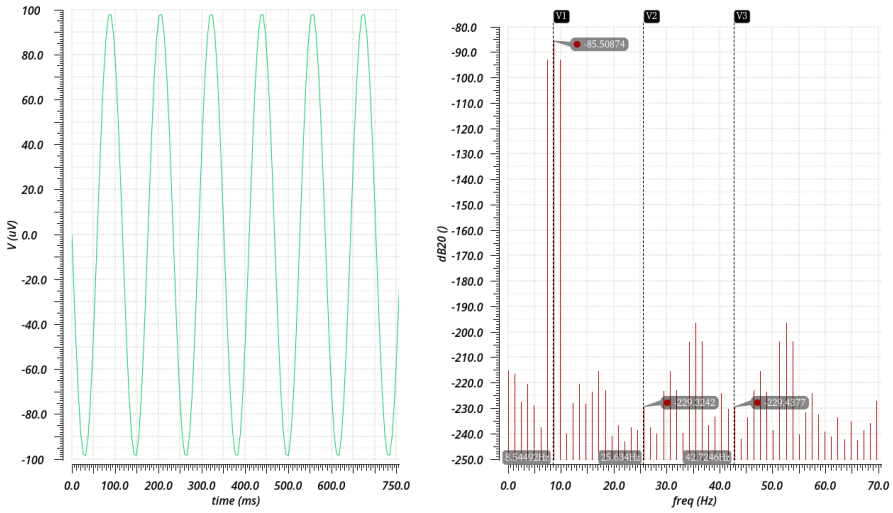

Figure 4.10: Simulated PGA transient and DFT response to a 0.1 mV of amplitude and 8.544 921 875 Hz sinusoidal input signal.

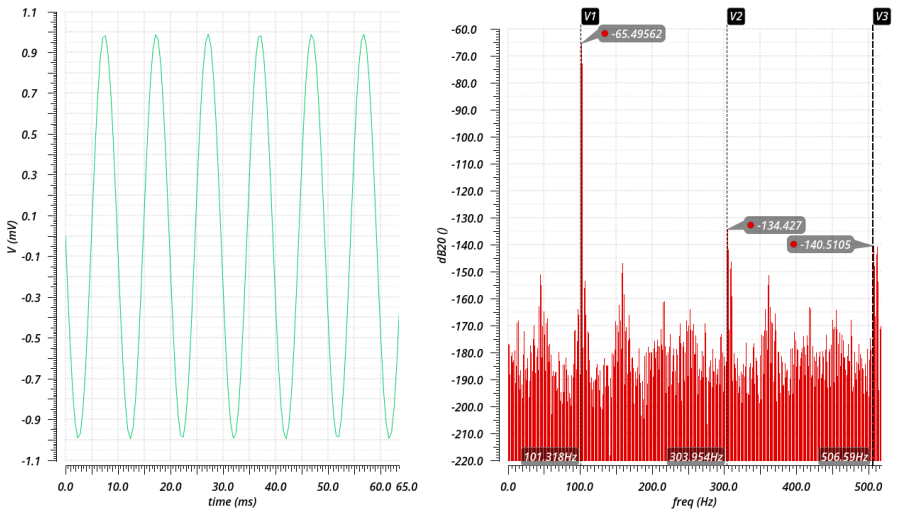

Figure 4.11: Simulated PGA transient and DFT response to a 1 mV of amplitude and 101.318 359 375 Hz sinusoidal input signal.

4.4.3 CMRR and PSRR Test-benches and Simulations

To obtain the CMRR analysis, the test bench presented in, Figure 4.12, is used. For this simulation the same voltage should be applied to both inputs. The common mode gain is subtracted to the differential gain to obtain the CMRR, presenting a value of 213.38 dB for the EOG signal and of 235.49 dB, for the EMG signal, the values are represented in Figure 4.13 and Figure 4.14.

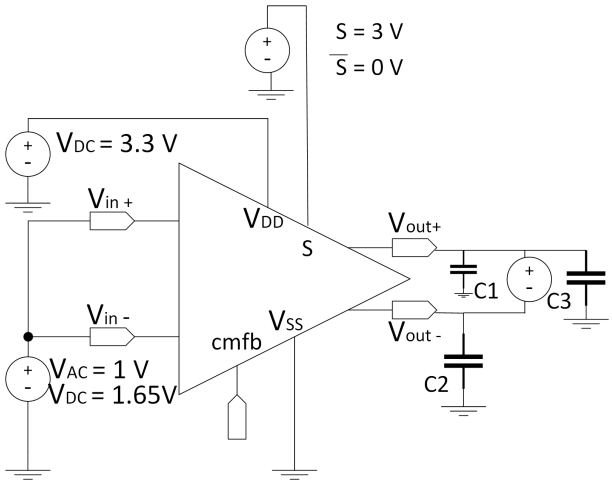

Figure 4.12: Test bench for the CMRR analysis

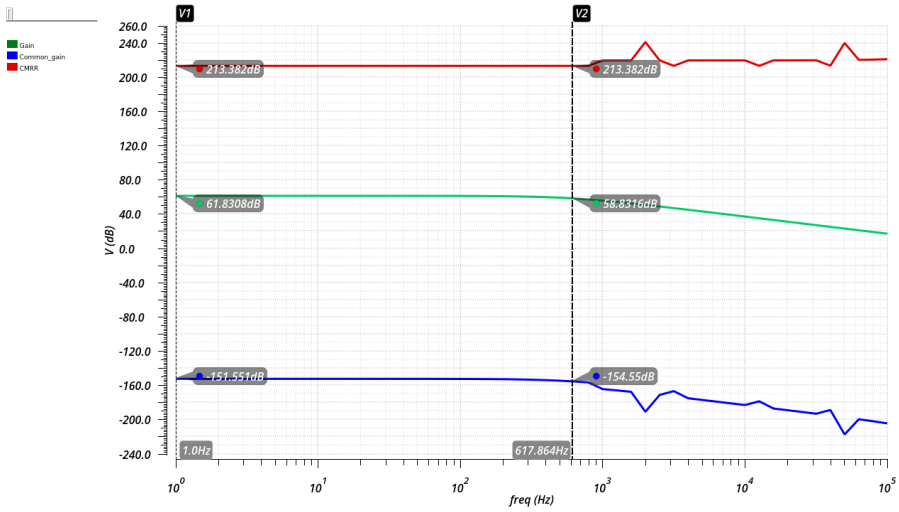

Figure 4.13: Simulated PGA CMRR for EOG.

As for the PSRR analysis, the test bench Figure 4.15 is used. For this simulation, an AC voltage of 1 V along with a DC voltage of 3.3 V is applied to V_{DD}, resulting in a power supply gain. The PSRR is obtained by subtracting the power supply gain to the differential gain and is presented in Figure 4.16 with a value of 261.51 dB for the EOG signal and in Figure 4.17 with a value of 243.41 dB for the EMG signal.

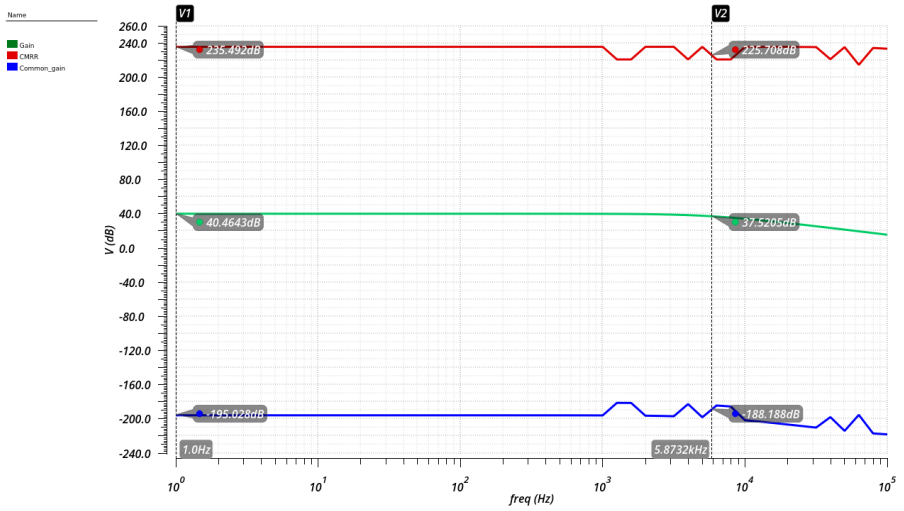

Figure 4.14: Simulated PGA CMRR for EMG.

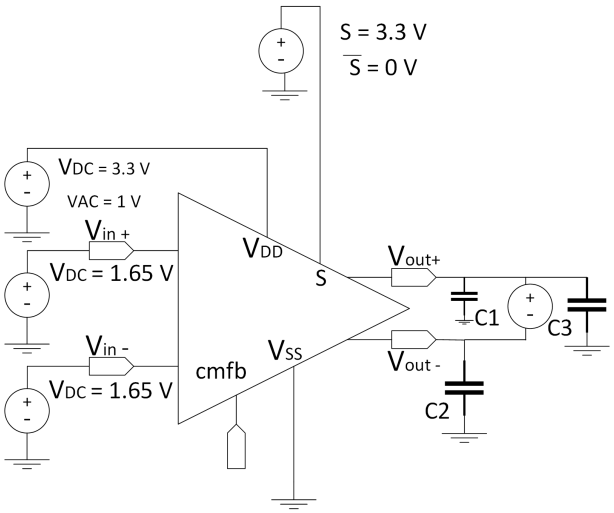

Figure 4.15: Test bench for the PSRR analysis.

4.4.4 Transistors Resizing

In order to obtain the pretended of 40 dB, as seen before, the width and length of transistors, Pb are 0.3 µm, using this length and width is not a good layout practice as only allow for the utilization of one contact as such due to the fabrication process, the connections of the transistor could be blocked. So a new resizing of transistor Pb is done with a length and width of 0.7 µm, the biasing developed and size is presented in Table 4.4. The resizing will change the gain value and BW, as such new simulations, for the EMG signal, are done, to verify the results of the new sizing and allow a comparison with the post-layout simulation done in the next section, as for the EOG signal the results are not influenced by the resizing.

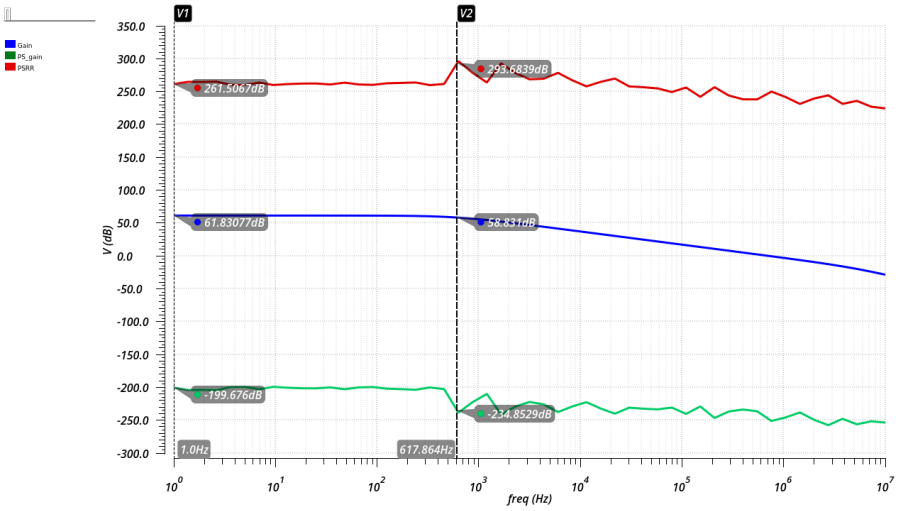

Figure 4.16: Simulated PGA PSRR for EOG.

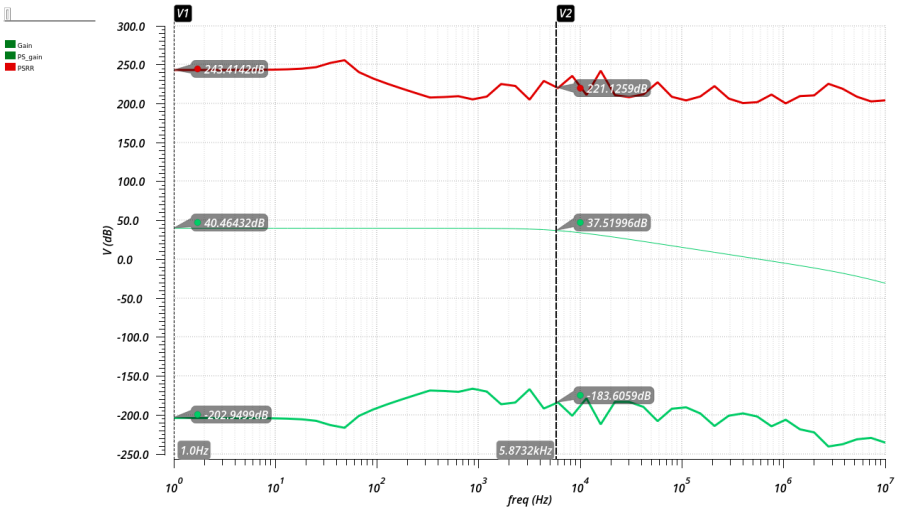

Figure 4.17: Simulated PGA PSRR for EMG.

Table 4.4: Transistor Pb parameters for new resizing.

	V_{DS} [V]	V_{GS} [V]	V_{TH} [V]	V_{DSAT} [mV]	I_D [nA]	L [µm]	W[µm]
Pb	1.52	0.639	0.608	64.9	69	0.7	0.7
Nd	1.78	0.569	0.398	138	69	25	1
Pselc	0.0038	1.78	1.18	0.472	69	1	1

A new gain is simulated for the EMG signal, shown in Figure 4.18, with a value of 49.658 dB, with a BW of 925.68 Hz, as for the phase margin, it is portrayed in Figure 4.19 presenting a value of 87.22°. The new resizing presents a flicker noise of 36 μVrms, a thermal noise of 21.79 μVrms and a input referred-noise of 45.3 μVrms, the noise simulation is presented in Figure 4.20.

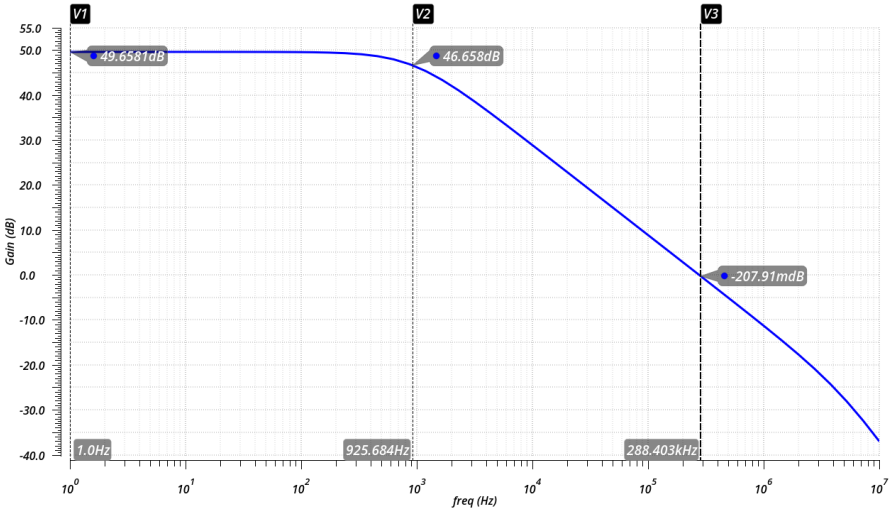

Figure 4.18: PGA gain simulation EMG signal, for new resizing.

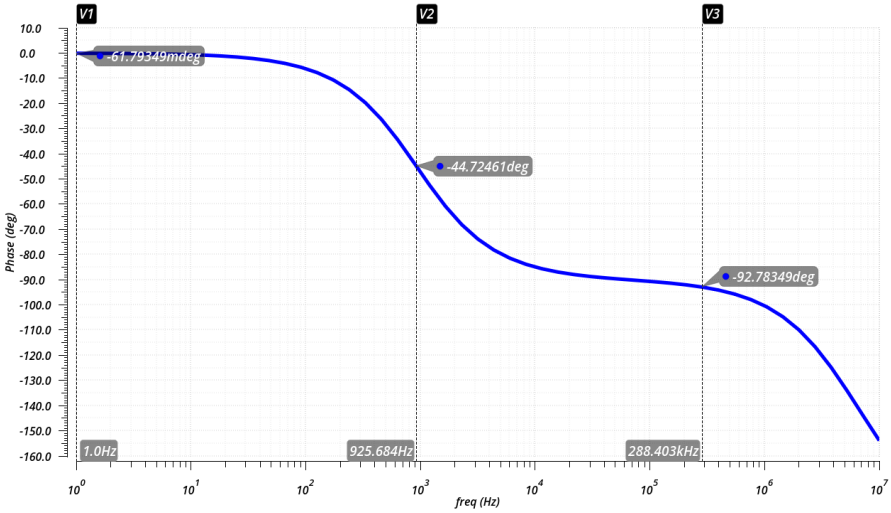

Figure 4.19: PGA phase simulation EMG signal, for new resizing.

The PGA transient response and respective DFT is illustrated in Figure 4.21 for the EOG test signal, where the DFT is obtained in the same time period as the one before. This figure shows a THD of 0.038 %, while the dynamic range is 69.22 dB.

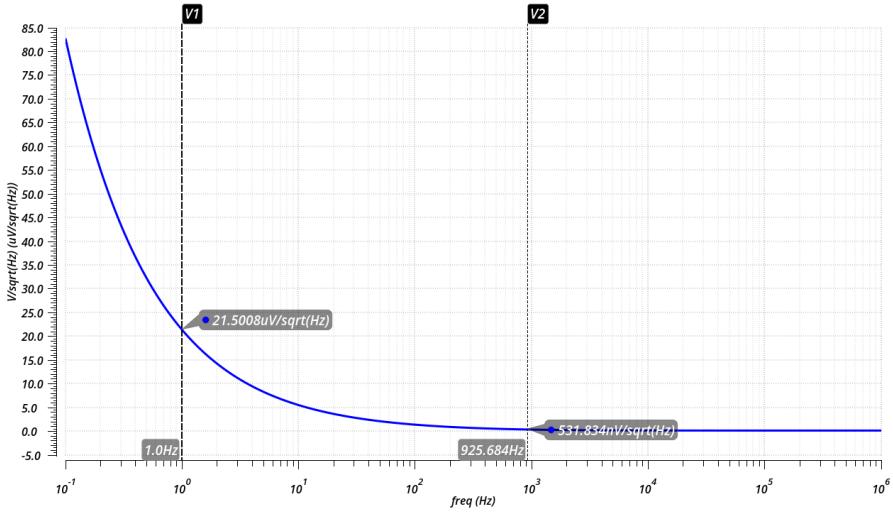

Figure 4.20: PGA input referred noise for EMG signal, for new resizing.

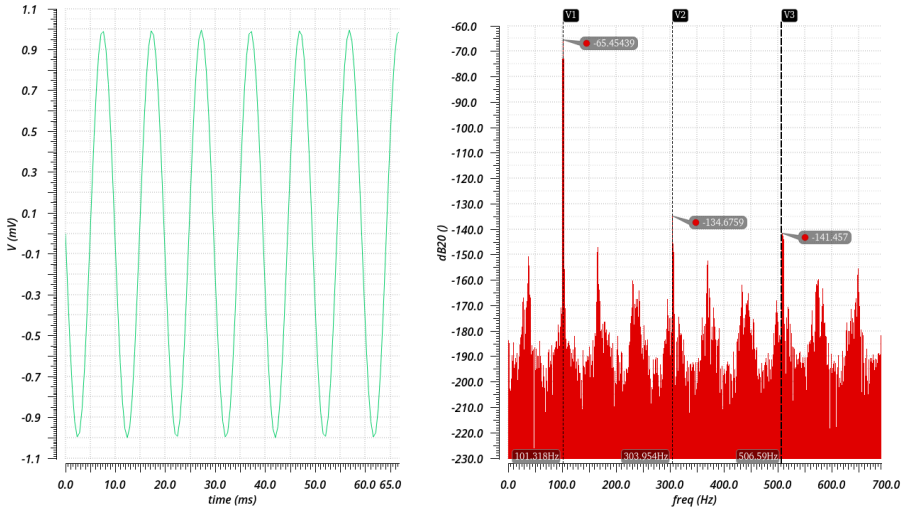

Figure 4.21: Simulated PGA transient and DFT response to a 1 mV of amplitude and 101.318 359 375 Hz sinusoidal input signal, for new resizing.

To obtain the CMRR value, the common mode gain is subtracted to the differential gain, the CMRR is represented in Figure 4.22, presenting a value of 220.464 dB. As for the PSRR is obtained by subtracting the power supply gain to the differential gain and is presented in Figure 4.23 with a value of 208.723 dB.

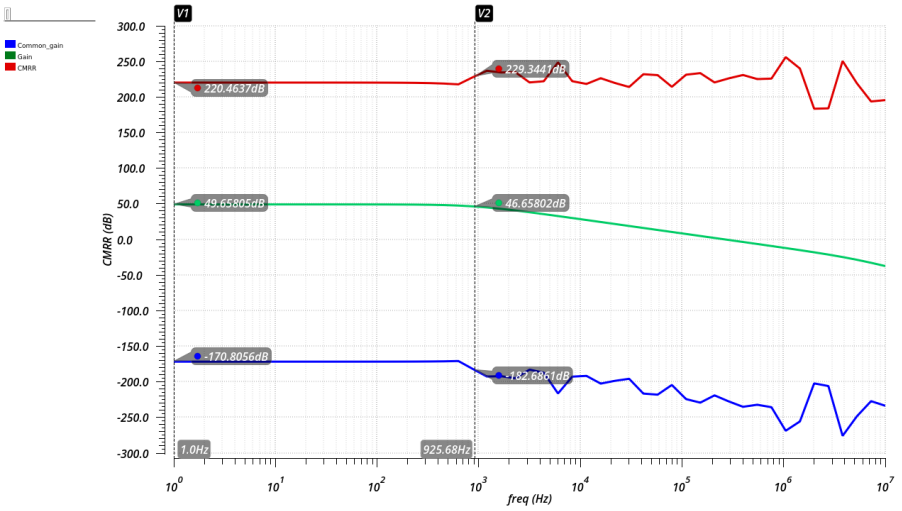

Figure 4.22: Simulated PGA CMRR for EMG, for new resizing.

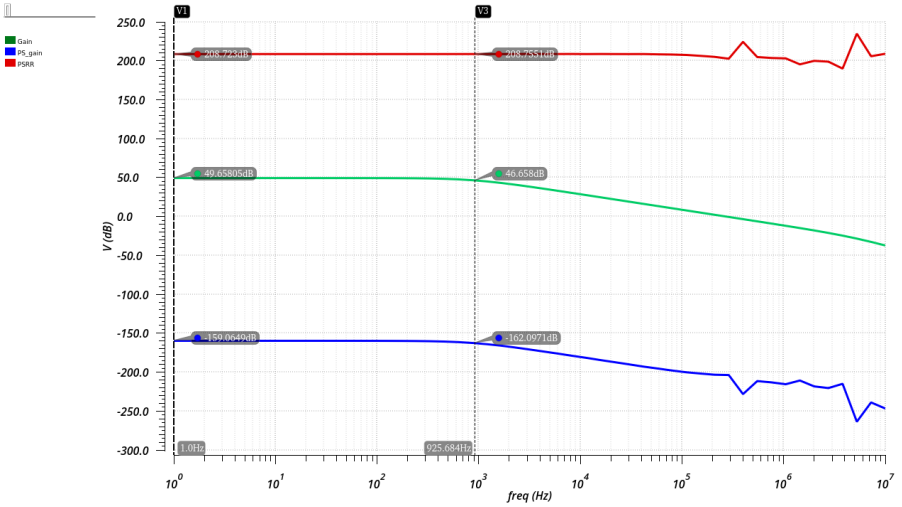

Figure 4.23: Simulated PGA PSRR for EMG, for new resizing.

4.5 Summary

This section presents the final results of the simulations done for the EOG and EMG signals, for the schematic implementation of the PGA. For EMG signal and a DC voltage of 1.65 V the gain that the PGA introduces to this signal is 49.7 dB. Whereas the EOG signal the PGA presents a 61.8 dB gain, the current consumption for both gains is under 1 µA. The specifications for CMRR and PSRR are accomplished as well for the dynamic range. Finally, having achieved the THD specification it is guarantied that minimum disruption to the signal will occur from the harmonics. A resume of the achieved results is presented in Table 4.5.

Table 4.5: Schematic simulation results.

	Target Values	Results		
		EMG	EMG(re-sized)	EOG
Supply [V]	3.3	3.3		
Gain [dB]	40 - 60	40.77	49.66	61.83
BW [Hz]	0.05 - 2000	5.87k	925.68	617.864
Current Consumption [μA]	$<$1	0.7585	0.741	0.986
CMRR [dB]	$>$100	235.49	220.46	213.38
PSRR [dB]	$>$100	243.4	208.74	261.51
Dynamic Range [dB]	$>$60	68.93	69.22	143.8
THD [%]	$<$1	0.039	0.038	0.277

5

Layout

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Layout

This section presents the layout design of the PGA and the post-layout simulations and comparison to the original schematic results.

5.1 Layout Design Considerations

For the development of the circuit's layout, some initial considerations were taken to optimize the design and minimize the parasitic capacitance's. First, the position of the transistors were kept symmetric, while placing the PMOS separately from the NMOS. The placement of the transistors is done to minimize area and the paths length and number. The rooting is implemented in order to minimize overlaps between paths and not overlap with transistors. For the rooting, the width and area of the paths are sized with the rule 1 μm per 1 mA, the width of the paths are kept at value orders of magnitude above the minimum. To minimize parasitic capacitances the connections to Power Supply (V_{DD}) are done with M2 metal, connections to GND with metal M1 and connections between transistors with metal M3 and above. To minimize the resistance and prevent complications from manufacturing several contacts are used. In order to improve short-circuit protection two rings are implemented around the transistors. To prevent current leakage, the NMOS have a dedicated guard ring (P Plus) which polarizes the substrate to ground. There is also a guard ring (N Plus) which contains the whole circuit, but only polarizes the PMOS. The layout can be seen in Figure 5.1, has an area of 0.0043 mm^2 (77.805 µmX54.75 µm).

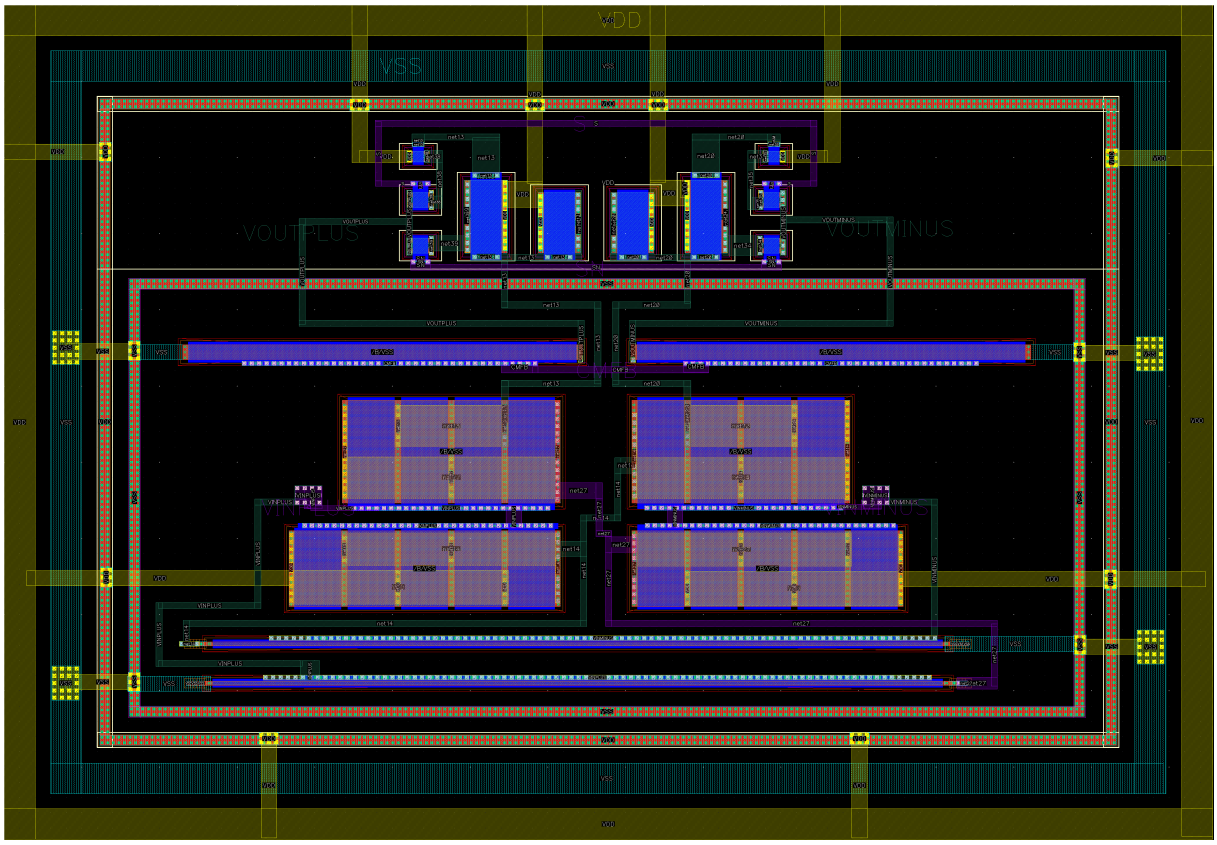

Figure 5.1: PGA Layout.

5.2 Post-Layout Simulations

After the layout is completed, Design rule checking (DRC) and Layout Versus Schematic (LVS) verification's are done to ensure the layout is correctly designed, then the parasitic extraction is executed, finally some post-layout simulations are done. There are some variations in the results when compared to the ones obtained before layout. The test-bench for each simulation is the same as explained in chapter 4. In Figure 5.2 and Figure 5.3 is demonstrated the PGA AC response for EOG and EMG signals, respectively. For the first signal, a gain of 61.863 dB and a BW of 610.577 Hz are achieved, as for the second signal a gain of 49.657 dB and a BW of 921 Hz are obtained. For the phase margin a value of 81.2° is obtained, as shown in Figure 5.4. For the EOG signal a phase margin of 86.85°, as shown in Figure 5.5, is accomplished.

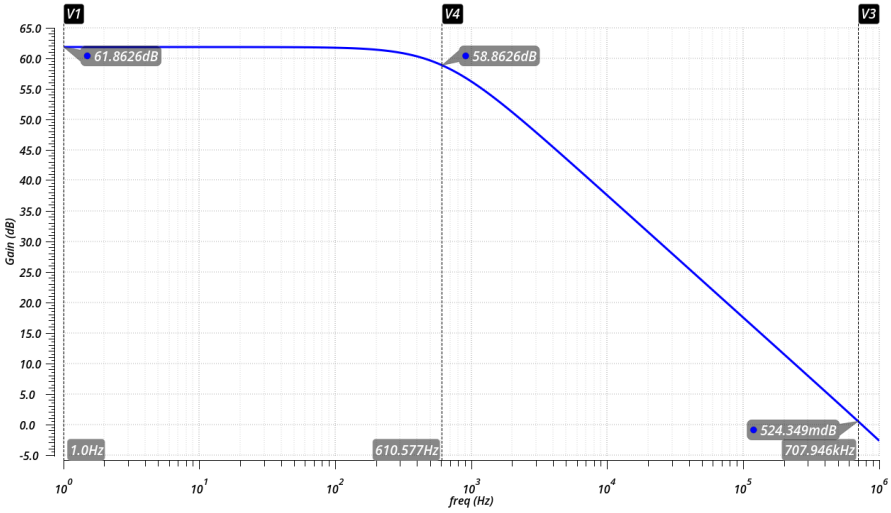

Figure 5.2: Simulated PGA post-layout AC response, for EOG signal.

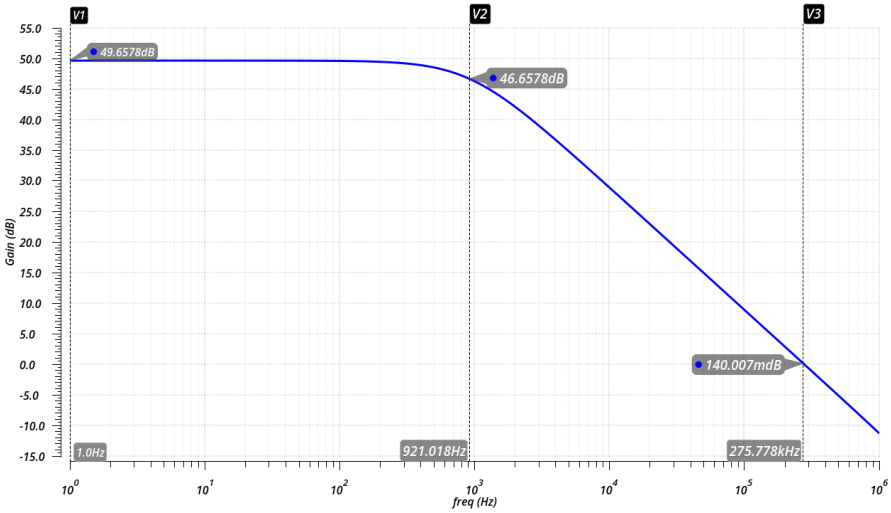

Figure 5.3: Simulated PGA post-layout AC response, for EMG signal.

The noise response, post-layout, for the EOG signal is shown in Figure 5.6 and in Figure 5.7 the EMG's noise response, resulting in an integrated equivalent input-referred noise of 23.27 µV and 45.23 µV in their respective BW. The circuit layout presents a flicker noise of 15 μVrms and a thermal noise of 8.12 μVrms for the signal EOG, and a flicker noise of 36.08 μVrms and a thermal noise of 9.15 μVrms, for the signal EMG.

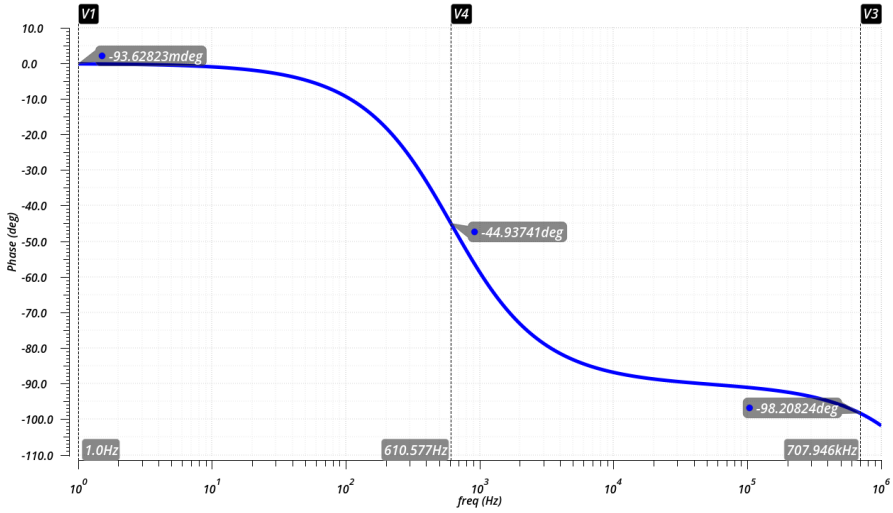

Figure 5.4: Simulated PGA post-layout Phase, for EOG signal.

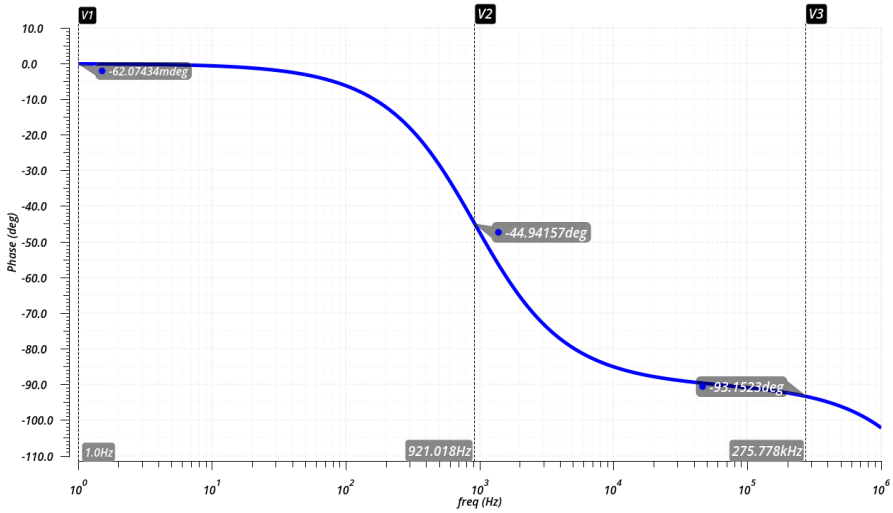

Figure 5.5: Simulated PGA post-layout Phase, for EMG signal.

As for the CMRR and PSRR, they are simulated in post-layout conditions. For the EOG case, the CMRR, Figure 5.8, achieves a value of 144.55 dB and the PSRR a value of 165.17 dB, as shown in Figure 5.9. Concerning the EMG case, the CMRR and PSRR are shown in Figure 5.10 and Figure 5.11, respectively, with the values of 167.23 dB and 140.1 dB. When compared to the values obtained in the schematic simulations, there is a relevant difference with the layout values being lower than the schematic ones.

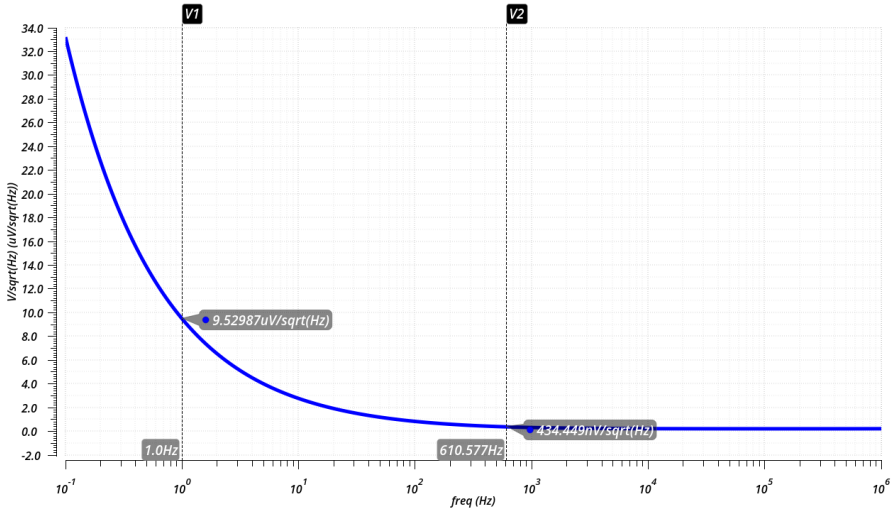

Figure 5.6: Simulated PGA post-layout equivalent input-referred noise, for EOG signal.

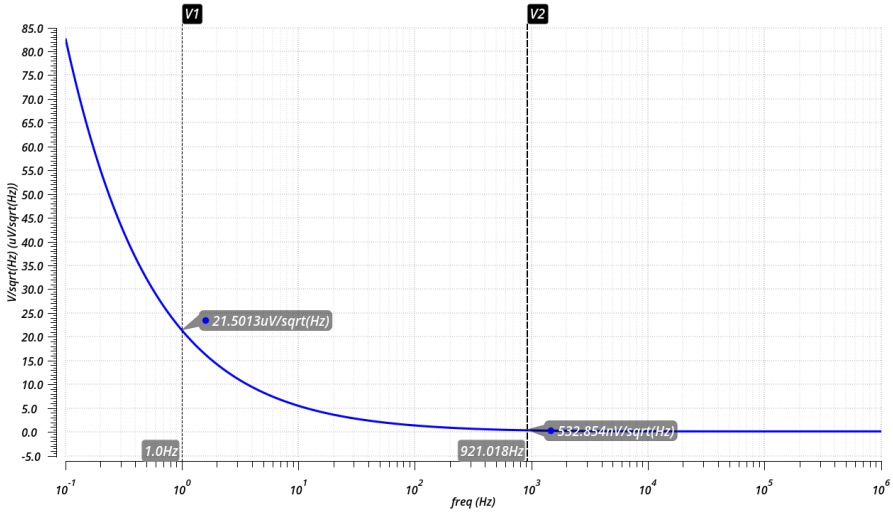

Figure 5.7: Simulated PGA post-layout equivalent input-referred noise, for EMG signal.

The transient analysis of the PGA response and respective DFT is shown in Figure 5.12 for the EOG case and in Figure 5.13 for the EMG case. The first one presents a THD value of 0.283 % and a dynamic range value of 143.49 dB. As for the second case, a THD value of 0.0415 % and a dynamic range value of 68.7 dB.

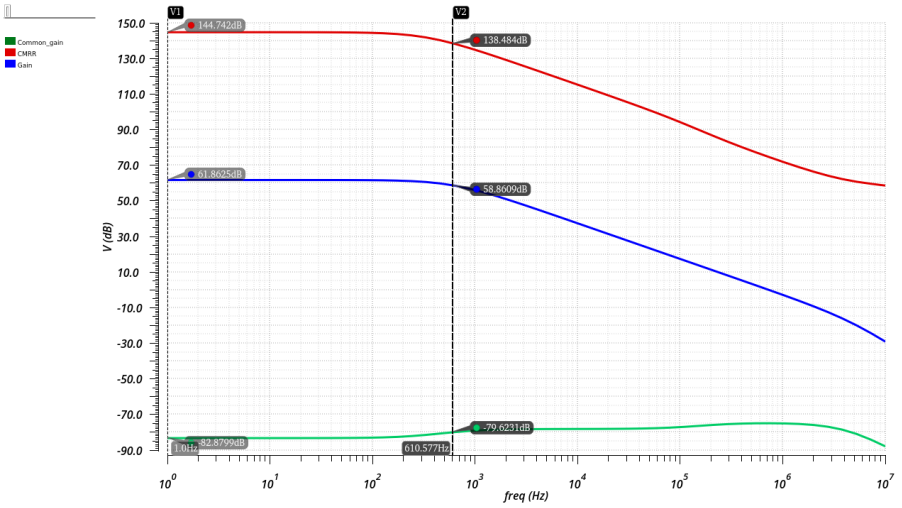

Figure 5.8: Simulated PGA post-layout CMRR, for EOG signal.

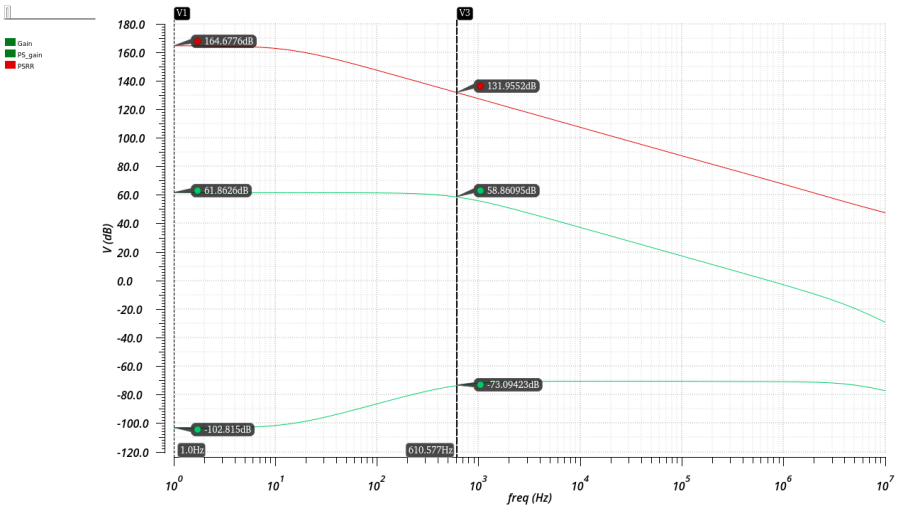

Figure 5.9: Simulated PGA post-layout PSRR, for EOG signal.

5.3 Summary

This section presents the simulation results comparing schematic simulation and the layout simulations. The results obtained are summarized in Table 5.1. The results are similar in almost all parameters, except for the values of CMRR and PSRR which decreases for both gains, in the post-layout results and the values of THD which increases slightly.

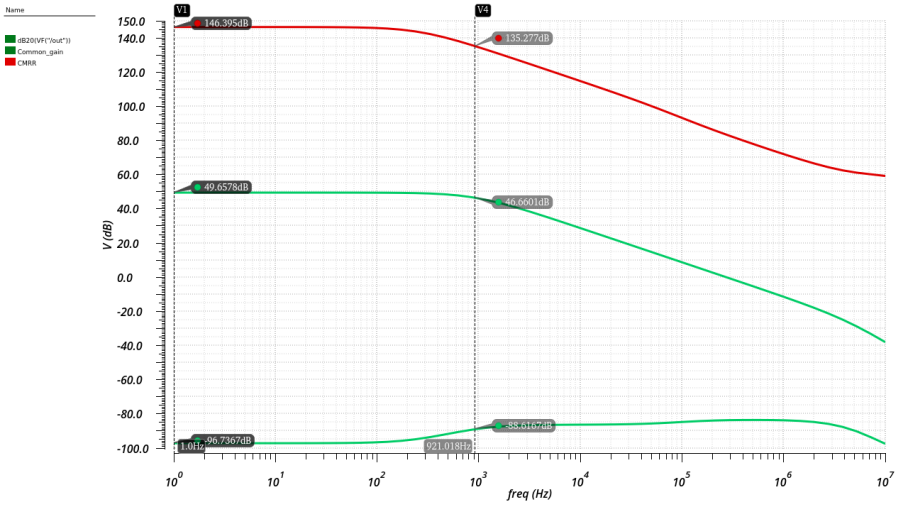

Figure 5.10: Simulated PGA post-layout CMRR, for EMG signal.

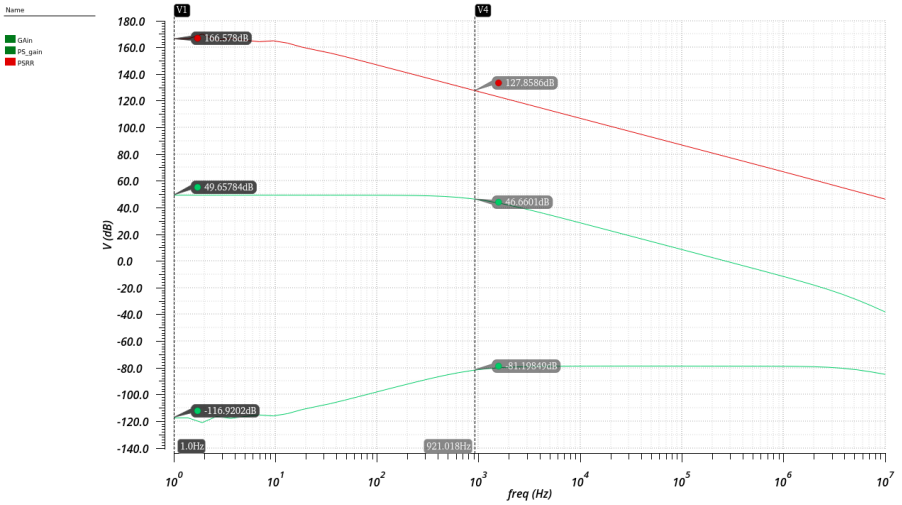

Figure 5.11: Simulated PGA post-layout PSRR, for EMG signal.

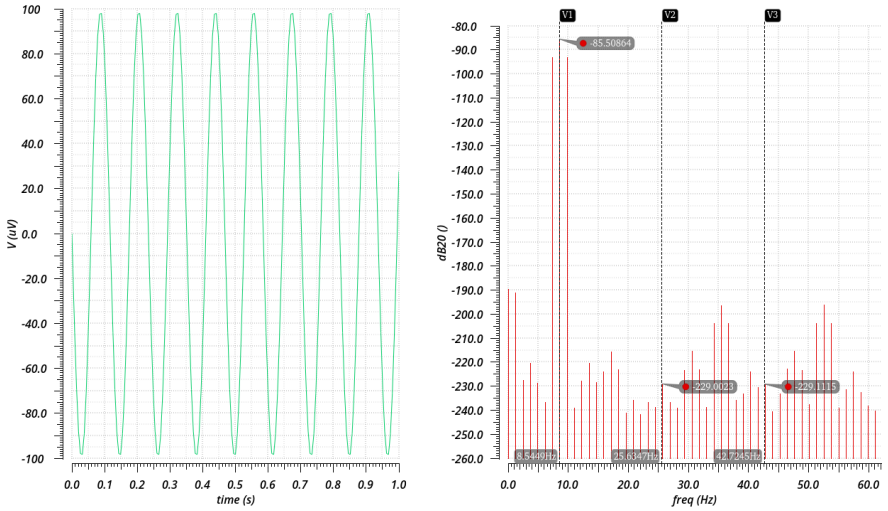

Figure 5.12: Simulated post-layout PGA transient and DFT response to a response to a 0.1 mV of amplitude and 8.544 921 875 Hz sinusoidal input signal.

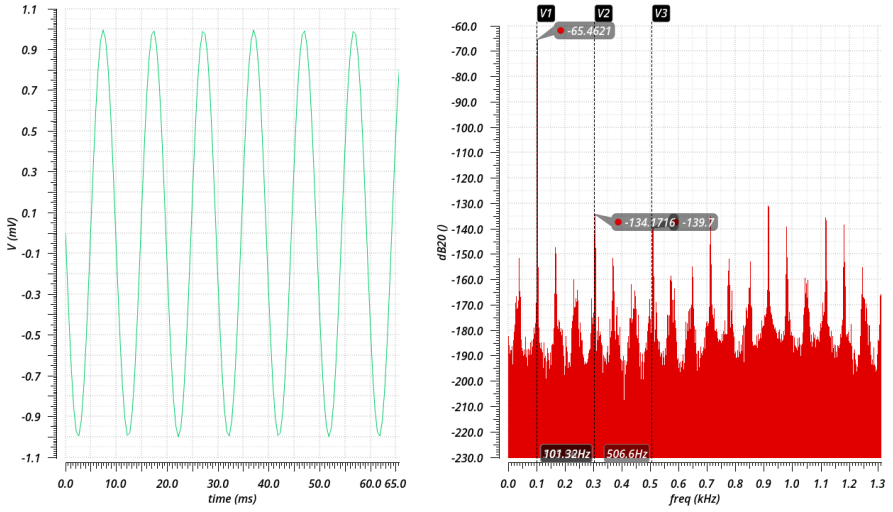

Figure 5.13: Simulated post-layout PGA transient and DFT response to a 1 mV of amplitude and 101.318 359 375 Hz sinusoidal input signal.

Table 5.1: PGA simulation results.

	Target Values	Results		Post-Layout Results	
		EMG	EOG	EMG	EOG
Supply [V]	3.3				
Gain [dB]	40 - 60	49.7	61.8	49.7	61.9
Frequency Range [Hz]	0.05 - 2000	925.6	617.86	921	610.5
Current Consumption [μA]	$<$1	0.741	0.986	0.742	0.984
CMRR [dB]	$>$100	220.5	213.38	146.4	144.7
PSRR [dB]	$>$100	160	283.9	131.8	159.2
Dynamic Range [dB]	$>$60	69.22	143.82	69.7	143.49
THD [%]	$<$1	0.038	0.277	0.0415	0.283

6

Conclusion

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Conclusion and Future Work

This chapter presents the conclusions of this dissertation work, emphasising on the most important metrics in this work. Future work on this dissertation is also proposed.

6.1 Conclusion

As described before, this work proposes to develop a PGA for use in a system to acquire bio-potential signal, mainly EMG and EOG. Since both signals, recordings present low voltage, the amplification must be as noiseless as possible, while being power efficient. Therefore the PGA with VC biasing structures implementation is chosen as this will provide additional gain and better energy-efficiency. The current consumption must be less than 1 µA, also the PGA should have programmable gain range between 50 dB and 60 dB and a CMRR and PSRR of 60 dB and 80 dB respectively.

A study of the basic concepts and most relevant metrics required for the understanding of the PGA, is presented. Afterwards, a study and analysis of the state-of-art in the field of PGAs used for biomedical applications is done.

In chapter 3, the proposed PGA design is presented and a theoretical analysis is done. Next in chapter 4 the sizing of the PGA is accomplished, which guarantees most of the proposed specifications, as the simulations done in the same chapter demonstrate. Therefore, while consuming under 1 µA the PGA presents a gain of 49.7 dB for the signal EMG and a gain of 61.8 dB for the signal EOG, while consuming less than 1 µA for both gains. As for the linearity metrics, the targeted values are achieved, for the THD with 0.0415 % and a dynamic range of 69.7 dB, for the EMG siganl. As for the EOG signal the linearity metrics are also achieve with a value for the THD of 0.283 % and a dynamic range of 143.8 dB. In both cases the proposed targets for CMRR and PSRR are achieved well above the requirements.

Finally, in the previous chapter the layout design of the PGA core is designed, presenting an area of 0.0043 mm^2, after parasitic extraction post-layout simulations are carried out. The grand majority of the post-layout results do not have a significant deviation from the ones obtained in the schematic simulations. A comparison with state-of-the-art is presented in Table 6.1. This work compared to the ones studied in the stat-of-the-art is competitive in terms of power consumption, as for the CMRR and

PSRR metrics they are higher for this work. As for the THD metric and area, this circuit is on par with the ones studied in the state-of-the-art.

6.2 Future Work

The following tasks are proposed as future work for this dissertation:

• Improve sizing in order to reduce the input-referred noise.

• The optimization of the PGA using the Analog IC Design Automation (AIDA) tool to maximize all metrics.

• The development at physical level and experimentation evaluation of a fabricated prototype of the PGA, for complete validation.

• Finally, the other blocks of the monitoring system should also be developed and physically assemble them for prototype testing and experimentation evaluation.

Table 6.1: Comparison of the state-of-the-art with this work.

Work	[8]	[12]	[16]	[18]	[20]	[22]	[26]	This Work
Year	2006	2013	2017	2012	2017	2017	2012	2021
Tech (nm)	350	180	65	180	180	180	90	130
Gain (dB)	0-21	0-70	2-25	-24 - 21	30-40	35-70	40-70	50-60
BW (MHz)	100	6.6-15	2	66.28	0.05-11 kHz	800-1400 Hz	175-316 mHz 23-69 Hz	921Hz 610.5 Hz
Supply Current (mA)	0.28	1.26	0.5	5.3	0.0182	0.32μA	1.2μA	0.742 μA 0.984 μA
Supply voltage (V)	1.8	1	1.5V	1.8	1.8	1	3.3	3.3
CMRR (dB)	-	-	-	-	84	102	-	146 145
PSRR (dB)	-	-	-	-	86.9	104	-	132 159
THD (%)	0.1 @0.2Vpp	-	-	-	-	-	0.96 @10mVpp 1.1 @5mVpp	0.0415 @2mVpp 0.283 @200 μVpp
Area (mm^2)	0.004	0.94	0.0045	0.7	0.03	0.0625	-	0.0043

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