Charge Pump for Ultrasonic Implant Stimulation

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***Abstract*—This thesis main objective is the design optimization of a fully integrated Multiple Output Switched Capacitor Converter (MOSCC) to be used in a neural stimulator implant developed in the context of the M4M European project. Initially, the state of the art modeling and analysis of a Switched Capacitor Converter (SCC) is presented. The output resistance is analysed based on the topology charge multipliers and component sizes by considering the converter in two ideal regimes: Slow Switching Limit (SSL) and Fast Switching Limit (FSL). As this analysis, as it is found in the literature, is only adequate for single output converters it was extended to the case of multiple outputs by using a transimpedance model. The most significant work on this thesis is the proposal of a method for optimally sizing a given MOSCC topology for a specific application based on the previously presented analysis. The method takes as inputs the topology's charge multipliers, the characteristics of the components used to implement it and the application specification, and calculates the optimal size of each component to minimize area and losses. The proposed method was automated using a Python script and used to size a MOSCC for the M4M application. The obtained circuit and the optimization process were validated using simulation.**

***Index Terms*—Switched Capacitor Converter, Multiple Output, Optimization, Integrated Circuit, Power Electronics, M4M.**

I. Introduction

Moore4Medical (M4M) is a project funded by the European Union and headed by a consortium composed of multiple companies and universities throughout Europe. The project addresses emerging medical applications and technologies that offer significant new opportunities for patients as well as for industry including: bioelectronic medicines, organ-on-chip, drug adherence monitoring, smart ultrasound, radiation free interventions and continuous monitoring. The new technologies will help fighting the increasing cost of healthcare by reducing the need for hospitalisation, helping to develop personalized therapies, and realising intelligent point-of-care diagnostic tools [1].

Introduced in the project is a demonstrator for a implantable Ultra High Frequency (UHF) neural stimulator powered by an ultrasonic link whose architecture is illustrated in Figure 1. In the scope of M4M, this work focuses on the design of the Single Input Multiple Output (SIMO) DC to DC power converter (DCDC) converter which supplies the output stage with the multiple voltage rails required for efficient stimulation. This thesis' work was developed in cooperation with Silicongate Lda, one partner of the M4M consortium responsible for the development of the SIMO DCDC converter.

The SIMO DCDC in Figure 1 is required to generate voltages both above and below the input voltage of $4.5\,\mathrm{V}$ with maximum total power in the order of $100\,\mathrm{mW}$ for outputs between $1.5\,\mathrm{V}$ and $9\,\mathrm{V}$. Since up-conversion is required, Low Dropout Output regulator (LDO) regulators cannot be used. Inductive converters also face some challenges in this application. Being the application implantable, it must be designed to handle being inside Magnetic Resonance Imaging (MRI) machines which use radio frequency and magnetic fields that would interfere with any magnetic core inductor used, such that much bigger air core inductors would be needed. Switched Capacitor Converters (SCCs) turn out to be ideal for this type of applications due to the possibility of full integration in the silicon chip, that results in a small total area, absence of magnetic components and high efficiency. This Multiple Output Switched Capacitor Converter (MOSCC) topology must be chosen correctly and its components correctly sized to obtain a small occupied area and high efficiency while meeting the specifications. There is a lack of literature available about the subject of sizing MOSCCs and, to the best knowledge of the author, no method as been proposed that can be directly applied to solving this problem.

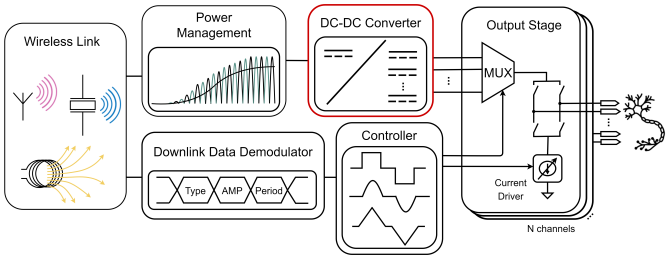

Fig. 1: Block diagram of the UHF neural stimulator[1].

A. Objectives

In the scope of this master thesis, a method for optimally sizing the components of a MOSCC is to be developed. The method is then used to aid in the development of a MOSCC solution for the specific application of a UHF neural stimulator implant. The specifications for the MOSCC were provided by the partners of Silicongate in the M4M project and are listed in Table I.

TABLE I: Converter specifications for ultrasonic implant stimulation application.

Spec	Value
V_{in}	min: $4.5\,\mathrm{V}$, typ: $4.6\,\mathrm{V}$, max: $4.7\,\mathrm{V}$
Ideal V_{out} ratios	1/3, 2/3, 4/3, 5/3, 6/3
Ideal V_{out} @ $V_{in} = 4.5\,\mathrm{V}$	$1.5\,\mathrm{V}$, $3.0\,\mathrm{V}$, $6.0\,\mathrm{V}$, $7.5\,\mathrm{V}$, $9.0\,\mathrm{V}$
$I_{out,max}$	$4\,\mathrm{mA}$ per output
$\Delta V_{out,max}$	5% of V_{out} @ $4.5\,\mathrm{V}$
$V_{out,PP.max}$	2% of V_{out} @ $4.5\,\mathrm{V}$
Fabrication Technology	TSMC 0.18um BCD GenII
Integration	Fully integrated (no external capacitors)

[1]Figure drawn by Konstantina Kolovou Kouri (who is also part of the M4M project), reproduced with the author's permission

II. SCC MODELING AND ANALYSIS

A. MOSCC model

The SCC output impedance analysis performed by [2] using considering the Slow Switching Limit (SSL) and Fast Switching Limit (FSL) converter regimes is extended to the case of MOSCC using a transimpedance model proposed by [3]. The model for one of the outputs is shown in Figure 2 where A_k is the output ideal voltage ratio and z_{xy} is the corresponding element in the transimpedance matrix $\boldsymbol{Z}$ (1).

$$\boldsymbol{Z} = \begin{bmatrix} z_{11} & z_{21} & \cdots & z_{1m} \\ z_{21} & z_{22} & \cdots & z_{2m} \\ \vdots & \vdots & \ddots & \vdots \\ z_{m1} & z_{m2} & \cdots & z_{mm} \end{bmatrix} [\Omega] \tag{1}$$

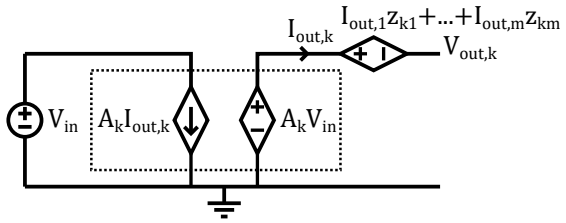

Fig. 2: Model of an output of a MOSCC.

The transimpedance matrix elements on SSL regime $z_{SSL,xy}$ are given by

$$z_{SSL,kl} = \sum_{i \in caps} \frac{b_{c,ik} b_{c,il}}{f_{sw} C_i} \tag{2}$$

while the transimpedance matrix elements on FSL regime $z_{FSL,xy}$ are given by

$$z_{FSL,kl} = \sum_{i \in sws} \frac{b_{r,ik} b_{r,il}}{D G_i} \tag{3}$$

The total transimpedance matrix elements z_{xy} are given by

$$z_{kl} = \sqrt{z_{SSL,kl}^2 + z_{FSL,kl}^2} \tag{4}$$

and the total power loss due to output loading is

$$P_{rout} = \sum_{j \in outs} \sum_{i \in outs} z_{ij} i_{out,i} i_{out,j} \tag{5}$$

B. SCC components analysis

The practical performance of any SCC is largely dependent on the performance of the components used to implement the circuit, so it is crucial to model and access the performance of these devices and their influence in the overall converter performance.

Real capacitors used in SCC, and their interconnects, present parasitic capacitances to other nodes. This capacitances are usually referred to a ground node and can be lumped in each capacitor bottom and top plate [4], as pictured in Figure 3. αC and βC are, respectively, the bottom plate parasitic capacitance and the top plate parasitic capacitance. Real switches present a non-zero resistance when turned-on and require a given energy to be turned-on.

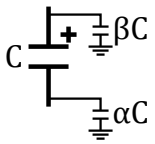

Fig. 3: Capacitor parasitics.

The performance of capacitors and switches can be evaluated using a range of metrics relating their value with their cost of implementation [2]. Two costs are considered, area and losses, resulting in two metrics for each kind of device. m_{Ca} and m_{Cl} for capacitor and m_{Sa} and m_{Sl} for switches. m_{Ca} is the capacitor areal capacitance density given by

$$m_{Ca,i} = \frac{C_i}{A_i} \tag{6}$$

where C_i is the main capacitance and A_i is the occupied layout area. m_{Cl} is the ratio of main capacitance with total parasitic capacitance defined by

$$m_{Cl,i} = \frac{C_i}{\alpha_i C_i + \beta_i C_i} = \frac{1}{\alpha_i + \beta_i} \tag{7}$$

where α_i and β_i are, respectively, the ratio between bottom and top plate parasitic capacitances to the main capacitance (see Figure 3). m_{Sa} is the switch conductance per area defined by

$$m_{Sa,i} = \frac{G_i}{A_i} \tag{8}$$

where G_i is the switch conductance or the inverse of the switch resistance R_i and A_i is the switch area. m_{Sl} is the ratio of switch conductance to energy required to drive the switch

$$m_{Sl,i} = \frac{G_i}{E_{drv,i}} \tag{9}$$

where $E_{drv,i}$ is the energy required to drive the switch a single switching cycle. These metrics are more adequate to describe the performance of specific technology devices, for specific voltage levels, but cannot be extrapolated for for other voltage ratings. In fact, for a specific technology, the performance and cost of each device has be evaluated individually.

C. Losses model

Apart from the losses due to output loading, SCCs present additional losses due to parasitics in capacitors, switches and interconnects which represent a significant part of the total losses, specially, in fully integrated implementations.

1) Capacitor parasitc losses: Since the flying capacitors terminals are switched between two different potentials during the switching cycle the parasitic capacitances get charged and discharged in a lossy way. The total power wasted in the parasitic capacitors P_{cpar} can be calculated by

$$P_{cpar} = f_{sw} \sum_{i \in caps} \frac{C_i \left(v_{cb,i}\right)^2}{m_{Cl,i}} \tag{10}$$

where *caps* is the set of capacitors use to implement the SCC, f_{sw} is the switching frequency and C_i, $v_{cb,i}$ and $m_{Cl,i}$ are the i^{th} capacitor capacitor capacitance, terminal voltage swing and loss metric, respectively.

2) Switch driving losses: The only losses considered in the switches are a consequence of the power necessary to drive them P_{sdrv}. In the case of a switch implemented with a Metal Oxide Semiconductor Field Effect Transistor (MOSFET), which accounts for most practical applications, these losses are the power dissipated in charging and discharging the gate capacitance. The losses caused by the switches on-state resistance are already accounted for in the output resistance losses P_{rout}. The total power dissipated driving the switches P_{sdrv} is given by

$$P_{sdrv} = f_{sw} \sum_{i \in sws} \frac{G_i}{m_{Sl,i}} \tag{11}$$

where sws is the set of switches used to implement the SCC, and G_i and $m_{Sl,i}$ are the i^{th} capacitor conductance and loss metric, respectively.

D. Total losses and efficiency

The total SCC losses is given by

$$P_{loss} = P_{rout} + P_{cpar} + P_{sdrv} \tag{12}$$

where P_{rout}, P_{cpar} and P_{srdv} are given by (5). (10) and (11), respectively.

The total converter efficiency is then given by

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{\sum_{k \in outs} V_{out,k} I_{out,k}}{\sum_{k \in outs} V_{out,k} I_{out,k} + P_{loss}} \tag{13}$$

III. MOSCC SIZING METHOD

A. Proposed methodology

The proposed method consists on the following steps:

1) Generate a set of stage conductance distributions.
2) For each conductance distribution:
   a) Find the total conductance required to keep all outputs above the maximum voltage drop at maximum load.
   b) Optimize the distribution of $Z_{st,SSL}$ and $Z_{st,FSL}$ within each stage to minimize the cost each stage.
   c) Calculate the total solution cost taking into account total area and losses.
3) Choose the conductance distribution with the lowest cost as the optimal solution.

The optimal stage conductance is found by evaluating a set of solutions in a search space and choosing the best solution. This is necessary due to the extra constraints caused by the maximum voltage drop specifications for each output which do not allow a general expression to be found for the optimal stage conductance.

This algorithm was implemented in a Python program that takes as inputs the topology characteristics (charge multipliers), the technology device characteristics (device performance metrics) and, the application specifications and outputs the optimized topology sizing and its performance.

B. Stage conductance distributions generation

The search space is created by generating all permutations (with repetition) of integers from 1 to res (the resolution of the sizing), normalizing each number by dividing by the total such that they sum to 1 and assigning the normalized values h_i to each of the topology stages. The conductance of each stage is given as

$$G_{st,i} = h_i G_{st,tot} \tag{14}$$

where $G_{st,tot}$ is the sum of all stages conductance and needs to be calculated to meet the voltage drop specification on each of the outputs.

C. Total conductance sizing

Assuming a given stage conductance distribution, the required $G_{st,tot}$ needs to be found. Given the load distribution, maximum drop specification, and the coupling between outputs, there may be outputs that require a small stage conductance to achieve a voltage drop below the spec while other outputs may require higher conductance to meet spec. The circuit must be sized such that all outputs are within spec and, therefore, the output that requires higher total conductance must be found.

Multiplying the transimpedance matrix elements by $G_{st,tot}$ yields a matrix $\boldsymbol{\zeta}$ with elements given by

$$\zeta_{kl} = z_{kl} G_{st,tot} = \sum_{i \in stages} \frac{b_{st,ik} b_{st,il}}{h_i} \tag{15}$$

$\boldsymbol{\zeta_{st}}$ describes how $\boldsymbol{Z}$ scales with $G_{st,tot}$ for a given stage conductance distribution $\boldsymbol{h}$.

The total conductance required for each output to meet the maximum voltage drop specification with full load on every output can be obtained from

$$G_{st,req,k} = \sum_{l \in outs} \frac{\zeta_{kl} i_{out,max,l}}{\Delta V_{out,max,l}} \tag{16}$$

Since all outputs must meet the specification at the same time the higher $G_{st,req,k}$ is taken as $G_{st,tot}$:

$$G_{st,tot} = \max_{k \in outs} \{G_{st,req,k}\} \tag{17}$$

To ensure that the maximum drop in a given output is obtained for the maximum loading on every output all elements of the matrix $\boldsymbol{Z}$ (or $\boldsymbol{\zeta}$) must be positive. This way, an increase in current in a given output always causes a voltage drop on other outputs, never a rise. Any conductance distributions that generate negative transimpedance elements are discarded.

D. Intra stage optimization

With the total conductance already calculated, the conductance of each stage can be calculated using (14) and each stage can be optimized by itself to achieve the required stage conductance, while optimizing area and power losses. The SSL, FSL and total output resistance of each stage (considering the charge multipliers are unitary) are given by eqs. (18) to (20).

$$Z_{st,SSL} = \frac{1}{f_{sw} C_1} \tag{18}$$

$$Z_{st,FSL} = \sum_{i=1}^{4} \frac{1}{DG_i} \tag{19}$$

$$Z_{st,tot} = \sqrt{Z_{st,SSL}^2 + Z_{st,FSL}^2} \tag{20}$$

1) Capacitor sizing to meet $Z_{st,SSL}$: Since each stage has only one capacitor, the capacitance required to achieve a given SSL output resistance is directly given by (21).

$$C_1 = \frac{1}{f_{sw} Z_{st,SSL}} \tag{21}$$

2) Switch sizing to meet $Z_{st,FSL}$: This stages are often implemented with different MOSFETs for each switch, commonly 2 NMOS and 2 PMOS of the smallest voltage rating above the V_Δ of the stage, but possibly even devices of different voltage ratings are used due to startup considerations, for example. The relative sizing of this switches within each stage can then be optimized based on their differing performance metrics using the method on [5]. The optimization is performed to minimize a cost, either switch area or driving losses depending on which parameter is more important in the design power density or efficiency. The cost considered is the switch driving losses as it is the most relevant for fully integrated designs or semi-integrated designs aiming for maximum efficiency, yet the same method can easily be applied to other metrics. The total switch driving energy is obtained by dividing each switch conductance G_i by its loss metric $m_{Sl,i}$ and summing:

$$E_{tot} = \sum_{i=1}^{4} \frac{G_i}{m_{Sl,i}} \tag{22}$$

The result of the optimization yields the optimized switch conductance (23) dependent on the required FSL output impedance.

$$G_i = \frac{\sqrt{m_{Sl,i}}}{D Z_{st,FSL}} \left(\sum_{k=1}^{4} \frac{1}{\sqrt{m_{Sl,k}}} \right) \tag{23}$$

3) Optimization of $Z_{st,SSL}$ and $Z_{st,FSL}$ distribution: Both $Z_{st,SSL}$ and $Z_{st,FSL}$ contribute to the total output impedance $Z_{st,tot}$ according to the relationship (20). The same $Z_{st,tot}$ can then be obtained using different distributions of $Z_{st,SSL}$ and $Z_{st,FSL}$ which results in different capacitor and switch sizes according to equations (21) and (23), respectively. Combining (6) and (21) yields the stage's capacitor area and its relationship to $Z_{st,SSL}$ given by (24), where K_{Acap} is given by (25).

$$A_{cap} = \frac{C_1}{m_{Ca,1}} = \frac{1}{Z_{st,SSL}} \frac{1}{f_{sw} m_{Ca,1}} = \frac{K_{Acap}}{Z_{st,SSL}} \tag{24}$$

$$K_{Acap} = \frac{1}{f_{sw} m_{Ca,1}} \tag{25}$$

Combining (10) and (21) and noting the stage's V_Δ is equal to the the capacitor's terminal voltage swing $v_{cb,i}$ yields the stage's capacitor losses and its relationship to $Z_{st,SSL}$ given by (26), where K_{Pcpar} is given by (27).

$$P_{cpar} = \frac{C_1 V_\Delta^2 f_{sw}}{m_{Cl,1}} = \frac{1}{Z_{st,SSL}} \frac{V_\Delta^2}{m_{Cl,1}} = \frac{K_{Pcpar}}{Z_{st,SSL}} \tag{26}$$

$$K_{Pcpar} = \frac{V_\Delta^2}{m_{Cl,1}} \tag{27}$$

Combining (8) and (23) and summing over the 4 switches yields the stage's total switch area area and its relationship to $Z_{st,FSL}$ given by (28), where K_{Asw} is given by (29).

$$\begin{aligned} A_{sw} &= \sum_{i=1}^{4} \frac{G_i}{m_{Sa,i}} \\ &= \frac{1}{Z_{st,FSL}} \sum_{i=1}^{4} \left[\frac{\sqrt{m_{Sl,i}}}{D m_{Sa,i}} \left(\sum_{k=1}^{4} \frac{1}{\sqrt{m_{Sl,k}}} \right) \right] \\ &= \frac{K_{Asw}}{Z_{st,FSL}} \end{aligned} \tag{28}$$

$$K_{Asw} = \sum_{i=1}^{4} \left[\frac{\sqrt{m_{Sl,i}}}{D m_{Sa,i}} \left(\sum_{k=1}^{4} \frac{1}{\sqrt{m_{Sl,k}}} \right) \right] \tag{29}$$

Combining (11) and (23) and summing over the 4 switches yields the stage's total stage's switch driving losses and its relationship to $Z_{st,FSL}$ given by (30), where K_{Psdrv} is given by (31).

$$\begin{aligned} P_{sdrv} &= \sum_{i=1}^{4} \frac{G_i f_{sw}}{m_{Sl,i}} \\ &= \frac{1}{Z_{st,FSL}} \sum_{i=1}^{4} \left[\frac{f_{sw}}{D\sqrt{m_{Sl,i}}} \left(\sum_{k=1}^{4} \frac{1}{\sqrt{m_{Sl,k}}} \right) \right] \\ &= \frac{K_{Psdrv}}{Z_{st,FSL}} \end{aligned} \tag{30}$$

$$K_{Psdrv} = \sum_{i=1}^{4} \left[\frac{f_{sw}}{D\sqrt{m_{Sl,i}}} \left(\sum_{k=1}^{4} \frac{1}{\sqrt{m_{Sl,k}}} \right) \right] \tag{31}$$

Defining $Z_{st,FSL}$ as $Z_{st,SSL}$ multiplied by a constant r (32) allows obtaining $Z_{st,tot}$ as (33). Using the definition of r, the relationship between $Z_{st,SSL}$ and $Z_{st,tot}$ is given by (34) while the relationship between $Z_{st,FSL}$ and $Z_{st,tot}$ is (35).

$$Z_{st,FSL} = r Z_{st,SSL} \tag{32}$$

$$Z_{st,tot} = \sqrt{1 + r^2} Z_{st,SSL} \tag{33}$$

$$Z_{st,SSL} = \frac{1}{\sqrt{1 + r^2}} Z_{st,tot} \tag{34}$$

$$Z_{st,FSL} = \frac{r}{\sqrt{1 + r^2}} Z_{st,tot} \tag{35}$$

The total stage area A_{st} can now be obtained by summing the capacitor and switch areas while the total stage power losses Pst is obtained by summing the capacitor parasitics and switch driving losses. By using the relationships (34) and

(35) the dependencies of A_{st} and P_{st} on $Z_{st,tot}$ and r are obtained as (36) and (37), respectively.

$$\begin{aligned} A_{st} &= \frac{K_{Acap}}{Z_{st,SSL}} + \frac{K_{Asw}}{Z_{st,FSL}} \\ &= \frac{1}{Z_{st,tot}} \left(\sqrt{1+r^2} K_{Acap} + \frac{\sqrt{1+r^2}}{r} K_{Asw} \right) \end{aligned} \tag{36}$$

$$\begin{aligned} P_{st} &= \frac{K_{Pcpar}}{Z_{st,SSL}} + \frac{K_{Psdrv}}{Z_{st,FSL}} \\ &= \frac{1}{Z_{st,tot}} \left(\sqrt{1+r^2} K_{Pcpar} + \frac{\sqrt{1+r^2}}{r} K_{Psdrv} \right) \end{aligned} \tag{37}$$

Since there may be a trade-off between the stage's occupied area and losses it cannot be simultaneously optimized for both quantities. A cost function f (38) and a design parameter λ are introduced to account for the trade-off. f includes both the area and losses cost with the losses portion affected of parameter λ which denotes the relative importance of the losses in relation to the occupied area. λ choice is in charge of the designer which should tune it to match the application characteristics.

$$f = A_{st} + \lambda P_{st} \tag{38}$$

The optimal ratio between $Z_{st,SSL}$ and $Z_{st,FSL}$ is found by minimizing f. The derivative of f is set to zero (39) and solved for r yielding the optimized r (40).

$$\begin{aligned} \frac{\partial f}{\partial r} = \frac{1}{Z_{st,tot}} \Bigg[& \frac{r}{\sqrt{1+r^2}} (K_{Acap} + \lambda K_{Pcpar}) - \\ & - \frac{1}{r^2 \sqrt{1+r^2}} (K_{Asw} + \lambda K_{Psdrv}) \Bigg] = 0 \end{aligned} \tag{39}$$

$$r_{opt} = \sqrt[3]{\frac{K_{Asw} + \lambda K_{Psdrv}}{K_{Acap} + \lambda K_{Pcpar}}} \tag{40}$$

r_{opt} will be smaller than 1 if the design is mostly capacitor constrained as is usually the case of fully integrated designs and it will be higher than 1 for designs switch constrained as is usually the case for designs using external capacitors.

Figure 4 shows how the stage area A_{st} and losses P_{st} vary with the ratio r for an example stage. If the stage was optimized only for minimum area the optimal r would be 0.21 while if it was optimized for minimum losses the optimal r would 0.93. Figure 5 shows the plot of the cost function (38) with respect to r for three different λ. The optimal r is always between the r for minimum area and the r for minimum losses with the parameter λ governing the tradeoff between the two. When λ is small r_{opt} is close to the optimal r for minimum area, while for higher λ, meaning a bigger importance on losses, r_{opt} gets closer to the optimal r for minimum losses.

With r calculated the stage component values can be calculated. To calculate the stage capacitance $Z_{st,SSL}$ needs to be found using (34) and then C_1 is obtained with (21). To calculate the conductance of each of the stage's switches $Z_{st,FSL}$ is found using (35) and then G_i is obtained for each switch with (23).

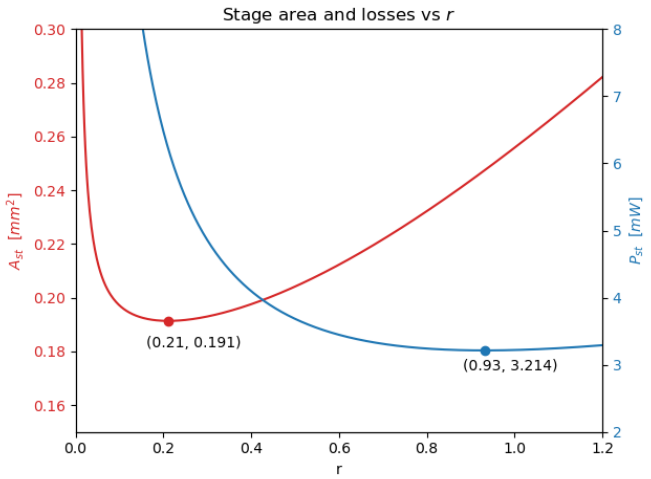

Fig. 4: Variation of the stage area and losses with the ratio r. Minimum points are marked.

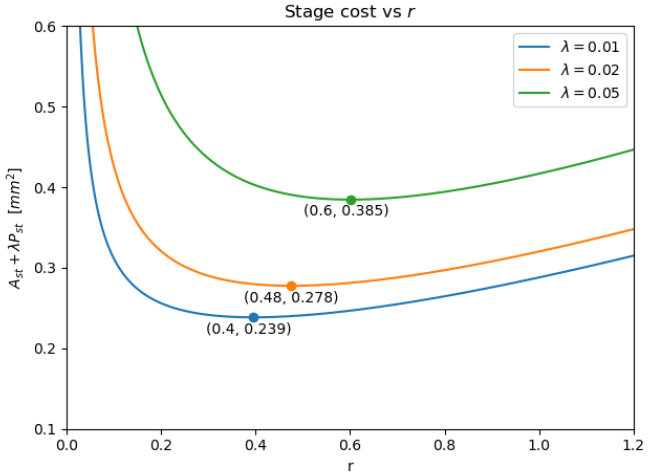

Fig. 5: Variation of the stage total cost with the ratio r for different λ. Minimum points are marked.

E. Choosing the final sizing solution

Each stage conductance distribution will generate a solution with optimized stages. Figure 6 shows the total area and power loss of an example topology with 5 stages with optimally sized stages for each stage conductance distribution generated. λ is set to 0.02 and a sizing resolution res of 10 was used (total of $10^5 = 100000$ solutions calculated).

To find the overall optimal solution, a cost function based on the same parameter λ as the stage optimization cost function (38) is used. This cost function is given by (41) where A_{tot} is the sum of each stage area and P_{tot} is the sum of each stage power losses. If A_{tot} is expressed in [m^2] and P_{tot} in [W] then λ has units of [m^2/W] such that it expresses how much extra area is occupied to reduce a given amount of losses.

$$F = A_{tot} + \lambda P_{tot} \tag{41}$$

The solution with the minimum cost is the optimal sizing for the topology (and correspondent device technology as-

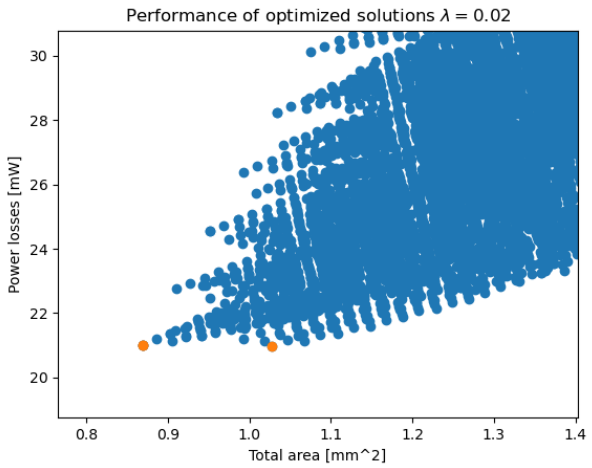

Fig. 6: Performance of optimally sized topology for a set of stage conductance distributions. $\lambda = 0.02\,\mathrm{mm}^2/\mathrm{mW}$.

signment), switching frequency f_{sw}, λ and application specs considered. The topology, switching frequency and λ can be varied by the designer to find the most advantageous solution for the application.

IV. M4M Application

A. Specifications

To support the multiple simultaneous stimulation channels with both high and low voltage rails, voltages both bellow and above the input voltage need to be generated with high efficiency. From a regulated input voltage of $4.5\,\mathrm{V}$ a total of 6 supply rails, including the input voltage, are to be generated in steps of $(1/3)V_{in}$. Each output V_{ox} provides a nominal conversion ratio of $(x/3), x \in \{1, .., 6\}$ and should be sized to supply $4\,\mathrm{mA}$ at a maximum drop of 5% from the nominal conversion ratio. The specifications are presented in Table I.

B. Switches and capacitor implementation

The converter is to be designed in TSMC 180nm BCD GenII process. Three types of capacitors are possible of being implemented in this technology: Metal Oxide Semiconductor (MOS), Metal Oxide Metal (MOM) and Metal Insulator Metal (MIM). Their performance metrics for each of the considered capacitance structures are presented in table II.

TABLE II: Performance metrics of the capacitance structures considered.

Structure	m_{SA} [nF/mm^2]	α	β	m_{SL}
NMOS 1V8	8.9	2%	0	50
NMOS 5V	4.1	4%	0	25
PMOS 1V8	8.9	0	1%	100
PMOS 5V	4.1	0	2%	50
MOM M2-M5 70V	0.8	2.3%	2.3%	22
MIM 5V	1.55	0.7%	0	143

This technology provides MOSFETs up to $70\,\mathrm{V}$ voltage rating yet considering the input voltage is $4.5\,\mathrm{V}$ and the maximum output voltage is $9\,\mathrm{V}$ only devices with ratings of $1.8\,\mathrm{V}$ (core), $5\,\mathrm{V}$ (IO) and $12\,\mathrm{V}$ (LDMOS) are considered. Core devices use thin gate oxide with a gate-source voltage rating of $1.8\,\mathrm{V}$ while IO and LDMOS devices use thick gate oxide with a gate-source voltage rating of $5\,\mathrm{V}$. Both NMOS and PMOS are available for each voltage rating and means of insulating transistor bulks from the substrate with enough withstand voltage are provided by the usage of a N+ buried layer. With this insulation layer, all MOSFETs can be implemented in any topology without suffering body effect even if their souce is connected to a potencial higher than their voltage rating. The switch performance metrics are presented in table III.

TABLE III: Performance metrics of MOSFET available to be used as switches.

Switch	m_{SA} [mS/um^2]	m_{SL} [mS/pJ]
NMOS 1V8	0.97	440
PMOS 1V8	0.36	120
NMOS 5V	0.29	17
PMOS 5V	0.11	5.5
NMOS 12V	0.11	7.4
PMOS 12V	0.023	1.8

C. Topology choice

There are several approaches to generate the five required voltage rails. The traditional method would be to design five independent SCC and optimize each one using the methods proposed by [2]. This approach requires a minimum of 11 capacitors [6] and more than 30 switches. This creates a complex circuit, requiring more auxiliary circuits and creating layout area overheads.

Since the application requires linearly spaced voltage ratios a simple approach would be a linear topology with each stage generating a step of $1/3V_{in}$ similar to [7] and [8]. This topology's (TOP1) stage arrangement is shown in Figure 9(a). The minimum capacitor and switch voltage rating and device technology used for each stage are presented in Table IV. Each stage is assumed to be implemented with two NMOS and two PMOS for switches. TOP1 stages ST4 and ST5 require capacitors with a voltage rating of at least $6.3\,\mathrm{V}$ and $7.9\,$, respectively. For this voltage ratings only MOM capacitors can be used which present very low capacitance density and very high parasitic capacitance.

TABLE IV: Voltage step and minimum capacitor and switch voltage rating for each stage of topology TOP1.

TOP1	V_Δ	V_{cap}	cap tech	V_{sw}	sw tech
ST1	$1/3V_{in}$	1.6 V	MOS 1V8	1.6 V	2x NMOS 1V8 + 2x PMOS 1V8
ST2	$1/3V_{in}$	3.2 V	MOS 5V	1.6 V	2x NMOS 1V8 + 2x PMOS 1V8
ST3	$1/3V_{in}$	4.7 V	MOS 5V	1.6 V	2x NMOS 1V8 + 2x PMOS 1V8
ST4	$1/3V_{in}$	6.3 V	MOM 70V	1.6 V	2x NMOS 1V8 + 2x PMOS 1V8
ST5	$1/3V_{in}$	7.9 V	MOM 70V	1.6 V	2x NMOS 1V8 + 2x PMOS 1V8

Inputting this topology's characteristics and the application specifications in the proposed sizing algorithm and considering a switching frequency of $32\,\mathrm{MHz}$ and $\lambda = 0.02$ yielded

the optimal stage conductance, r and area for each of the topology's stages. This values appear in Table V. Although the two upper stages are attributed the lowest conductances they occupy the biggest area derived from the usage of MOM capacitors that present low capacitance density. The r values are also smaller for those two stages since the optimization process tried to minimize the capacitor size by increasing the switch size to achieve the required conductance.

TABLE V: Optimal stage conductance distribution, r and area for each of the stages of TOP1 for $f_{sw} = 32\,\mathrm{MHz}$ and $\lambda = 0.02$.

Stage	h_i	$G_{st,i}$ [mS]	r_i	$A_{st,i}$ [mm^2]
ST1	0.29	164	0.34	0.64
ST2	0.29	164	0.26	1.32
ST3	0.25	143	0.26	1.16
ST4	0.11	61	0.16	2.46
ST5	0.07	41	0.16	1.66

With optimal sizing this topology achieves a power density of $14.4\,\mathrm{mW/mm^2}$ and an efficiency of 70.2% which is a very poor performance compared to the other topologies proposed bellow.

The two biggest factors hindering the performance of this topology are: the, already identified, use of MOM capacitors and the inefficiency in the generation of V_{o6} that can be observed in the topology's charge multipliers in (42). All elements on the last column of the matrix (42) are non-zero, meaning all capacitors are involved in the charge transfer from the input to the fifth output V_{o6} resulting in high required conductances, and consequently high area and losses, to meet the specification.

$$\boldsymbol{B_{st,TOP1}} = \begin{bmatrix} -\frac{1}{3} & \frac{1}{3} & -\frac{1}{3} & -1 & 1 \\ \frac{1}{3} & \frac{2}{3} & \frac{1}{3} & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{42}$$

To address the problems of TOP1 a number of other topologies are proposed. TOP2 stage arrangement is shown in Figure 9(b) and the required stage voltage ratings and technology attribution is shown in Table VI. In this topology ST1, ST2 and ST3 are connected exactly the same way as TOP1 to generate V_{o1}, V_{o2} and V_{o4}. V_{o5} is generated with a step of $2/3V_{in}$ above V_{in} and V_{o6} is generated with a step of $2/3V_{in}$ above V_{in}. In this configuration no stage requires MOM capacitors with ST4 using a 5V MOS capacitor and ST5 using aMIM capacitor. A MIM capacitor is used in ST5 because this stage as a bigger step equal to V_{in}, causing significantly higher losses in the parasitic capacitances as studied in section II-C1. V_{o6} is now much more efficiently generated as it is generated independently using ST5. The resulting charge multipliers, presented in (43), are in general lower and show how both V_{o5} and V_{o6} are generated with charge transfer through a lower number of stages (more zeros in the fourth and fifth columns).

TABLE VI: Voltage step and minimum capacitor and switch voltage rating for each stage of topology TOP2.

TOP2	V_Δ	V_{cap}	cap tech	V_{sw}	sw tech
ST1	$1/3V_{in}$	1.6 V	MOS 1V8	1.6 V	2x NMOS 1V8 + 2x PMOS 1V8
ST2	$1/3V_{in}$	3.2 V	MOS 5V	1.6 V	2x NMOS 1V8 + 2x PMOS 1V8
ST3	$1/3V_{in}$	4.7 V	MOS 5V	1.6 V	2x NMOS 1V8 + 2x PMOS 1V8
ST4	$2/3V_{in}$	4.7 V	MOS 5V	3.2 V	2x NMOS 5V + 2x PMOS 5V
ST5	$3/3V_{in}$	4.7 V	MIM 5V	4.7 V	2x NMOS 5V + 2x PMOS 5V

$$\boldsymbol{B_{st,TOP2}} = \begin{bmatrix} -\frac{1}{3} & \frac{1}{3} & -\frac{1}{3} & \frac{1}{3} & 0 \\ \frac{1}{3} & \frac{2}{3} & \frac{1}{3} & \frac{2}{3} & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{43}$$

Passing this topology through the sizing algorithm yields much smaller stages as can be observed in Table VII. All stages are significantly smaller due both to smaller required conductances (better charge multipliers), and the usage of capacitors with better capacity density. This results in a power density of $118\,\mathrm{mW/mm^2}$ and an efficiency of 83%, a performance much superior to TOP1.

TABLE VII: Optimal stage conductance distribution, r and area for each of the stages of TOP2 for $f_{sw} = 32\,\mathrm{MHz}$ and $\lambda = 0.02$.

Stage	h_i	$G_{st,i}$ [mS]	r_i	$A_{st,i}$ [mm^2]
ST1	0.18	18	0.34	0.07
ST2	0.36	36	0.26	0.28
ST3	0.18	18	0.26	0.15
ST4	0.18	18	0.6	0.16
ST5	0.09	9	0.48	0.21

TOP3 is another alternative topology whose stage arrangement is shown in Figure 9(c) and the required stage voltage ratings and technology attribution is shown in Table VIII. V_{o1}, V_{o2} and V_{o6} are generated exactly the same as TOP2, the difference between TOP2 and TOP3 is stages ST3 and ST4 both using a step of V_{in} to generate V_{o4} and V_{o5} respectively. TOP3 has the same charge multipliers as TOP2 so the only differences in terms in performance is that stages ST4 and ST5 require lower capacitor voltage ratings but require higher switch voltage ratings and present higher voltage swings on the capacitors, that may increase total loss.

Two more topologies are presented, TOP4 and TOP5, that consist of mixing stages ST3 and ST4 from TOP2 and TOP3. The stage arrangements are shown in Figure 9(d) and Figure 9(e). The charge multipliers are equal in all four topologies TOP2, TOP3, TOP4 and TOP5, so their performance differences are only due to different combinations of component ratings and voltage swings in stages ST3 and ST4.

A different approach from the other topologies is taken in TOP6. Instead of using step-up stages to generate V_{o4} and V_{o5} from a combination of V_{in} and the lower voltages, V_{o4} and V_{o5} are generated by stepping-down V_{o6} and using V_{in} as the reference voltage for ST3 and ST4. V_{o6} is generated using stage

TABLE VIII: Voltage step and minimum capacitor and switch voltage rating for each stage of topology TOP3.

TOP3	V_Δ	V_{cap}	cap tech	V_{sw}	sw tech
ST1	$1/3V_{in}$	1.6 V	MOS 1V8	1.6 V	2x NMOS 1V8 + 2x PMOS 1V8
ST2	$1/3V_{in}$	3.2 V	MOS 5V	1.6 V	2x NMOS 1V8 + 2x PMOS 1V8
ST3	$3/3V_{in}$	1.6 V	MOS 1V8	4.7 V	2x NMOS 5V + 2x PMOS 5V
ST4	$3/3V_{in}$	3.2 V	MIM 5V	4.7 V	2x NMOS 5V + 2x PMOS 5V
ST5	$3/3V_{in}$	4.7 V	MIM 5V	4.7 V	2x NMOS 5V + 2x PMOS 5V

ST5 with the same connections as the previous topologies. The stage arrangement for TOP6 is shown in Figure 9(f) while the required stage voltage ratings and technology attribution is shown in Table IX. In this topology, since V_{o4} and V_{o5} are not generated using V_{o1} and V_{o2}, the step-up outputs are independent from the step-down outputs as can be seen from the charge multipliers in (44). The result is that passing this topology through the sizing algorithm yields smaller stages ST1 and ST2 but a bigger ST5 as can be observed in Table X. This topology has the advantage that all stages except ST5 use a step of $1/3V_{in}$ reducing the capacitor parasitics loss while requiring the same device voltage ratings.

TABLE IX: Voltage step and minimum capacitor and switch voltage rating for each stage of topology TOP6.

TOP6	V_Δ	V_{cap}	cap tech	V_{sw}	sw tech
ST1	$1/3V_{in}$	1.6 V	MOS 1V8	1.6 V	2x NMOS 1V8 + 2x PMOS 1V8
ST2	$1/3V_{in}$	3.2 V	MOS 5V	1.6 V	2x NMOS 1V8 + 2x PMOS 1V8
ST3	$1/3V_{in}$	1.6 V	MOS 1V8	1.6 V	2x NMOS 1V8 + 2x PMOS 1V8
ST4	$1/3V_{in}$	3.2 V	MOM 5V	1.6 V	2x NMOS 1V8 + 2x PMOS 1V8
ST5	$3/3V_{in}$	4.7 V	MIM 5V	4.7 V	2x NMOS 5V + 2x PMOS 5V

$$\boldsymbol{B_{st,TOP6}} = \begin{bmatrix} -\frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 \\ \frac{1}{3} & \frac{2}{3} & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{3} & \frac{1}{3} & 0 \\ 0 & 0 & \frac{1}{3} & \frac{2}{3} & 0 \\ 0 & 0 & \frac{1}{3} & \frac{2}{3} & 1 \end{bmatrix} \tag{44}$$

TABLE X: Optimal stage conductance distribution, r and area for each of the stages of TOP6 for $f_{sw} = 32\,\text{MHz}$ and $\lambda = 0.02$.

Stage	h_i	$G_{st,i}$ [mS]	r_i	$A_{st,i}$ [mm^2]
ST1	0.12	9	0.34	0.03
ST2	0.23	17	0.26	0.14
ST3	0.08	6	0.34	0.02
ST4	0.31	23	0.26	0.19
ST5	0.27	21	0.48	0.21

The sizing of all six topologies was optimized for a switching frequency of 32 MHz and $\lambda = 0.02$. A plot of efficiency versus power density of the 6 topologies is shown in Figure 7.

Topology TOP1 is inferior to the other solutions by a big margin. Topology TOP5 is the most power dense topology but

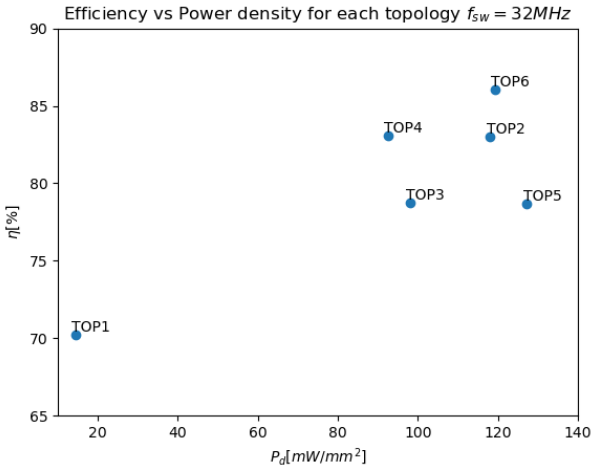

Fig. 7: Efficiency vs Power density for topologies 1 to 6. $f_{sw} = 32\,\text{MHz}$, $\lambda = 0.02$

presents significantly lower efficiency than TOP2, TOP4 and TOP6. Only considering power density and efficiency TOP6 seems to be the most advantageous topology. Nevertheless TOP6 presents extra implementation challenges related to startup and switch driving due to the reference of stages ST3 and ST4 being V_{in} instead of ground. This challenges considerably increase the design effort of topology TOP6. Another aspect that can be considered is the possibility of independent regulation of outputs. In TOP2 the outputs V_{o4}, V_{o5} and V_{o6} can be independently regulated and/or shut down, because stages ST3, ST4 and ST5 transfer charge to a single output, such that clock gating those stages allows independent regulation of each of the step-up outputs. This is advantageous in this application because it allows some stages and all of its auxiliary circuits to be turned off when the upper outputs are not required, reducing the static consumption of those circuits. In TOP6 the three upper outputs are coupled such that loading outputs V_{o4} or V_{o5} implies that all three stages ST3, ST4 and ST5 must be clocked to maintain the output voltage in the loaded output even though only one of the top outputs is being used. Considering the extra design complexity of topology TOP6 and the small performance gains it provides in relation to TOP2, the latter was chosen to be implemented for the M4M project.

V. Results

The chosen topology (TOP2) was designed in Cadence® Virtuoso® shematic and simulated using the HSPICE® simulator with MOSFETs and capacitor models from TSMC 0.18 µm BCD GenII technology. Ideal gate drivers were used to drive the MOSFETs as switches, generating the required voltages correctly referenced to the source of each MOSFET while drawing the energy required to drive the gate capacitance from the input source. Using multiple small switch and capacitor units, each component was implemented with a size as close as possible to the sizing algorithm result. The input voltage and switching frequency are the same passed to the sizing algorithm, 4.5 V and 32 MHz, respectively. Since the sizing

algorithm does not take into account ripple and output capacitors, those were sized such that the simulated ripple was below the specification. The output capacitors occupy a total area of $2.06\,\mathrm{mm}^2$. The output voltages of the simulated topology are shown in Figure 8.

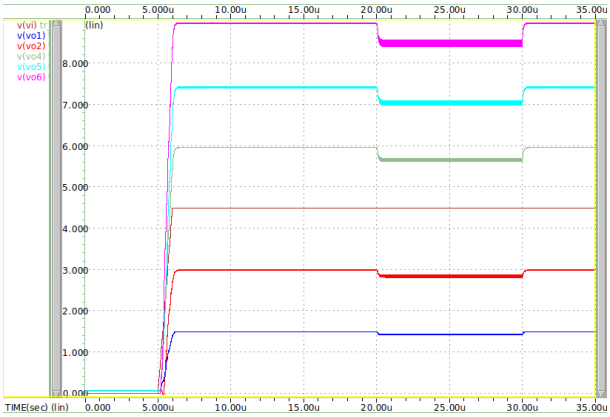

Fig. 8: Output voltages of the simulated SCC. The outputs are loaded with $4\,\mathrm{mA}$ each at $20\,\mu\mathrm{s}$ and unloaded at $30\,\mu\mathrm{s}$.

The specification, theoretical (obtained through the sizing algorithm) and simulated values for each output, as well as the error between the theoretical and simulated values, are presented in Table XI. The average output voltages $V_{out,k}$ are measured with all outputs fully loaded with $4\,\mathrm{mA}$. The gain of each output A_k is calculated by dividing the unloaded output voltage by the input voltage. The simulated output voltage values have less than 1% error to the theoretical values. Similar deviations are observed in the gain of each output. This deviations can be explained by the effects of capacitor parasitics in the converter voltage gain and output impedance (or transimpedance) [4] that were not considered in the proposed sizing method. The power loss, and therefore the efficiency, present much larger errors, with the simulated loss being 16.1% higher than expected, with resulting 2.8% lower efficiency. One possible cause for the extra losses include MOSFET capacitances that where not taken into account and create extra loss when the capacitor terminals are switched. Another cause is the fact that the MOS capacitors' parasitics to the substrate are formed by diodes which present a voltage dependent junction capacitance. The parasitics where measured with a constant bias voltage in relation to the capacitor bulk while in the circuit this bias is different for different stages and at each phase causing some deviation in the effective α and β of the capacitor.

The final characteristics of the designed solution, including the output capacitors, are presented in Table XII.

VI. Conclusions

During the development of this master's thesis a MOSCC was successfully sized for the M4M application with the aid of an original method for sizing the components of the MOSCC. The method is generic enough that it was applied to six different candidate topologies. The method was implemented in Python and was validated through simulation that it is able to generate a correct sizing of the MOSCC components.

TABLE XI: Specified, theoretical and simulated values for TOP2.

Quantity	Spec Value	Theo Value	Sim Value	Unit	Error
V_{out1}	1.425	1.425	1.422	V	-0.2%
A_1	0.333	0.333	0.332	1	-0.3%
V_{pp1}	30	-	27	mV	-
V_{out2}	2.850	2.850	2.835	V	-0.5%
A_2	0.667	0.667	0.664	1	-0.4%
V_{pp2}	60	-	53	mV	-
V_{out4}	5.700	5.700	5.667	V	-0.6%
A_4	1.333	1.333	1.327	1	-0.5%
V_{pp4}	120	-	93	mV	-
V_{out5}	7.125	7.129	7.056	V	-1.0%
A_5	1.666	1.666	1.653	1	-0.8%
V_{pp5}	150	-	118	mV	-
V_{out6}	8.550	8.550	8.523	V	-0.3%
A_6	2.000	2.000	1.997	1	-0.1%
V_{pp6}	180	-	163	mV	-
P_{out}	-	102.6	102.0	mW	-0.6%
P_{loss}	-	21.0	24.4	mW	16.1%
η	-	83.0	80.7	%	-2.8%

TABLE XII: M4M solution characteristics.

	Value
Number of outputs	5
Voltage ratios	1/3, 2/3, 4/3, 5/3, 2
Integration	Fully integrated
Clock frequency	$32\,\mathrm{MHz}$
Silicon area	$2.93\,\mathrm{mm}^2$
Technology	TSMC $0.18\,\mu\mathrm{m}$ BCD GenII
Total output power	$102\,\mathrm{mW}$
Power density	$34.8\,\mathrm{mW/mm}^2$
Efficiency	$80.7\,\%$

The simulated output characteristics of the sized MOSCC were very close to the specifications passed to the algorithm, with errors up to 1%. However the simulation results show considerable error on the losses calculated from the presented losses model.

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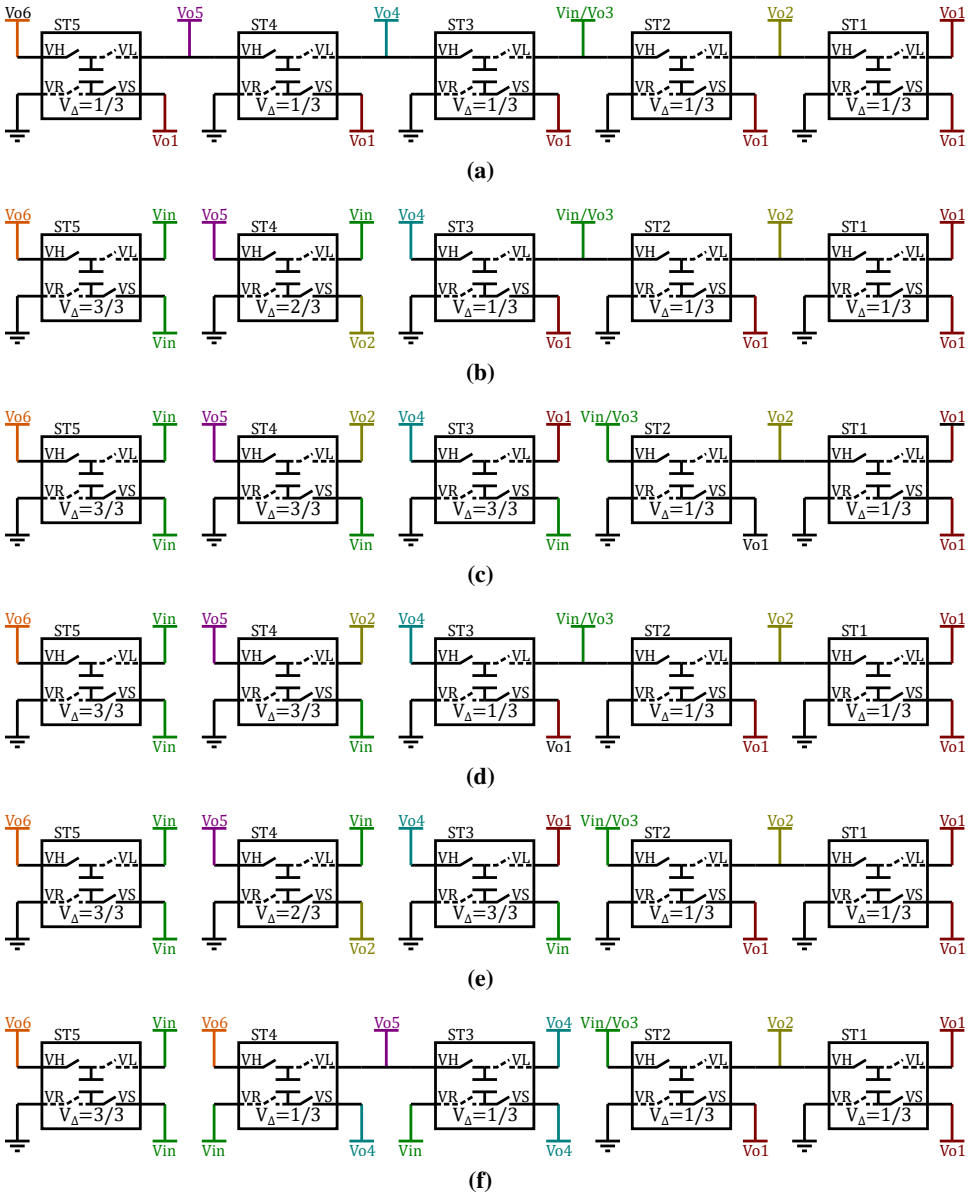

Fig. 9: Stage connections for topologies (a) TOP1, (b) TOP2, (c) TOP3, (d) TOP4, (e) TOP5, (f) TOP6.