Energy-Efficient Programmable Gain Amplifier to a Biomedical Engineering and Healthcare Tunable Front-End Sensor

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***Abstract*—This work comprises the research and development and implementation of a energy-efficient Programmable Gain Amplifier to be implemented in a tunable front-end sensor for different human-body signals.**

Human-body signals that will be considered for the development of this project are electromyography and electrooculography. These bio-potential signals operate in a separate broadband yet both follow an impulse-shape type of transmission hence suitable to be applied to the same receiver.

The field of biomedical engineering and Healthcare as seen a consistent tendency to integrate complex circuitry inside battery-powered small form-factor systems, which allow for the continuously sensing of bio-potential signals unobtrusively and uncumbersomly for extended period of times. Hence requiring this systems to be energy efficient and have low power consumption.

In this resport, state-of-the art projects are studied and presented and a Programmable Gain Amplifier topology is proposed in order to be developed and implemented. The energy-efficient Programmable Gain Amplifier will be developed in the electronic design software Cadence, with the UMC 130nm CMOS technology.

***Keywords*—Low-Power, Low-Noise, Biomedical, Healthcare, Bio-potential signals, Energy-Efficient, Tunable, CMOS.**

I. Introduction

In this day and age biomedical devices used to sense bio-potential signals are on the rise, since the information collected from those signals can help in diagnosis of diseases treatment and rehabilitation. These signals can be recorded in a non-invasive way, by placing electrodes on the skin, such as Electroencephalography (EEG), Electromyography (EMG), Electrocardiography (ECG), and Electrooculography (EOG). These biomedical signals have bandwidth range between a few hundred mHz to a few kHz and a amplitude variation from a few μV to a few mV as detailed in Table I. For continuous monitoring, low power-consumption is paramount to maximize battery life and therefore operation hours.

Generally health monitoring systems consists of five blocks, sensors, Low Noise Amplifier (LNA), dedicated filtering, in the case a Low-Pass Filter (LPF), programmable gain amplifiers, Programmable Gain Amplifier (PGA) and multiplexed Analog-to-Digital Converters (ADC) with Radio-Frequency (RF) circuitry to send and receive raw data, Figure 1.

Usually any bio-potential signals is quantized by an ADC so that complex signal processing can be performed in the digital domain and a PGA is usually placed before the ADC, Figure 1, and it is an important building block in modern day sensing applications. The PGA controls the amplitude signal applied at the inputs of the ADC, providing the much needed flexibility to be able to maximize the ADC dynamic range, also the PGA needs to maintain its high linearity and low noise over the entire signal bandwidth. The gain can be controlled by trimmers, digital controls methods or multiplexing techniques.

Large dynamic range and small harmonic distortion are also important for bio-signal recordings, so that the ADC can reconstruct the signal as true as possible to the original signal. If the system is not on battery, but connected to the grid the system would be subjected to powerline interference. Since this interference is one of the principal noise source in bio-sensing devices, the Power Supply Rejection Ratio (PSRR) be maximized, to solve this problem.

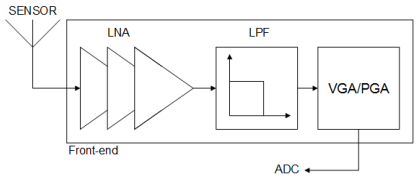


Fig. 1: Front-end block diagram.

Generally, the main objective for using Operational Transconductance amplifiers Operational Transconductance Amplifier (OTA), are versatile building blocks, useful for many filtering and signal processing applications, offering intrinsically wide bandwidth for many types of amplifiers. OTA can be generically defined as voltage-controlled current source with active gain. Therefore, an OTA is basically a voltage-to-current transducer. The gain of Operational Amplifier (OPAMP) can be programmable, in some topologies, through the DC current. In an ideal OTA the output current is linear function of the differential input voltage, V_{in}, and can be computed by (1).

$$I_o = g_m \cdot V_{in} \tag{1}$$

TABLE I: Characteristics of Biomedical Signal Processing.

	EMG	EOG
Amplitude (mV)	1 - 10	0.01 - 0.1
Frequency Range (Hz)	20 - 2000	Direct Current (DC) - 10
Primary Noise Source	Powerline interference; RF interference;	Powerline interference
Primary Interference Source	Motion artifact;	Skin potential; Motion Artifact; DC drift
	ECG	EEG
Amplitude (mV)	1 - 5	0.001 - 0.01
Frequency Range (Hz)	0.05 - 100	0.5 - 40
Primary Noise Source	Powerline interference;	Thermal, powerline; Induced interference; RF interference
Primary Interference Source	Nearby muscle activity (EMG signal);	Motion artifact; Muscle noise; Eye motion; Blink effect; Heartbeat signal

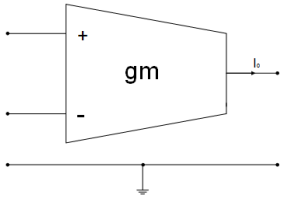


Fig. 2: CMOS Operational Transconductance Amplifier.

A programmable-gain amplifier, PGA, is usually placed before an analog-to-digital converter, ADC, in order to ease the dynamic range requirement for the ADC. The PGA, generally has three main topologies shown in Figure 3 [1].

Figure 3a, is a current divider, the control voltage V_c determines the dividing ratio although a linear-in-dB gain setting is difficult to realize due to the quadratic characteristic of the current divider. The overall linearity is limited by the input transconductor which generates I_i.

Changing the bias current of the transistors shown in Figure 3b implies a variance of the transconductance g_m of the source-coupled pair. The gain of the circuit is proportional to g_m of the input transistors. if the input signal is weak, a large bias current is needed to obtain high-gain and low-noise performance. Although when the input signal is large, the low bias current can degrade the linearity.

In Figure 3c the transconductance g_m of the source-coupled pair is varied by changing the resistance of the degeneration resistor R_s. When the input signal is weak, a small bias R_s is used to obtain high gain and low noise. When the input signal is large, a large Rs is used to obtain low gain and high linearity. Thus, this topology can achieve constant signal-to-noise-and-distortion ratio for the fixed output level regardless of the gain settings.

In this paper, is proposed a low power, PGA for signals from EMG and EOG. The signals operate in different broadbands,

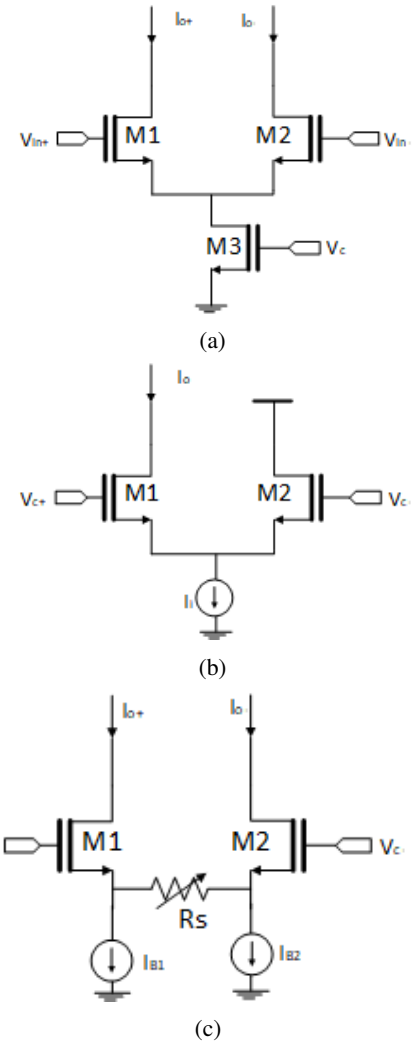


Fig. 3: (a) Current Divider topology, (b) Source-coupled differential topology, (c) Source-coupled with degeneration.

but both follow a similar impulse-shape type of transmission, thus are suitable to be applied to the same receiver. In order to have programmable gain the transistors acting as switches are incorporated, this transistors are controlled by a selection signal, S, thus allowing different gains. Moreover, simulated results show that the whole amplifier consumes under 1 µV.

The paper is organized as follows. In Section II the proposed low power, PGA is reviewed. The design implementation is discussed and simulations are presented in Section III. In Section IV, the low power, PGA layout is described and are shown results from post-layout simulations. Finally conclusions are drawn in Section V.

II. Proposed Low-Power, PGA

The proposed PGA topology chosen to implement is presented in 4, is a fully-differential OTA amplifier. In order to have programmable gain the transistors, $Pselb1$, $Pselc1$, $Pselb2$, $Pselc2$ are incorporated. this transistors are controlled by a selection signal, S, and act as switches, setting the

current mirror factoring for the output stage. Since x and y have different current value the gain will be different. The value of the output current is defined by the size ratio of the transistors that form the P-type Metal Oxide Semiconductor (PMOS) basic current mirrors. Either is the currents mirrors $Pa1$-$Pb1$, $Pa2$-$Pb2$ outputting current with a ratio of K:1, or is the $Pa1$-$Pc1$, $Pa2$-$Pc2$, with a ratio of h:1. Furthermore, a common mode feedback Common Mode Feedback (CMFB) loop circuit must be employed, since this is a fully differential implementation.

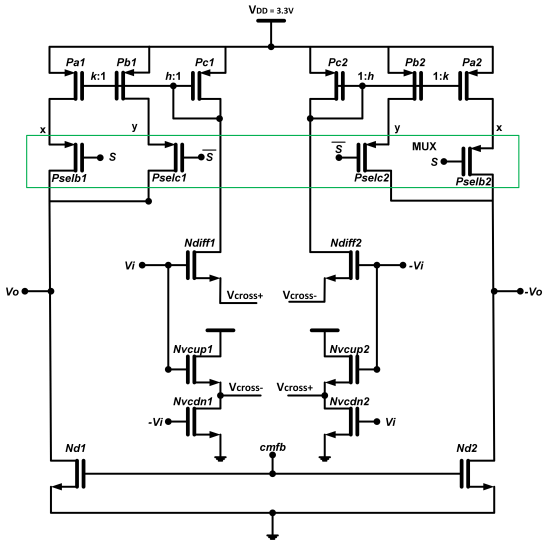


Fig. 4: Implemented circuit.

The innovation proposed in this circuit, when compared to the known symmetrical Complementary Metal Oxide Semiconductor (CMOS) OTA, relies on the fact that the traditional N-type Metal Oxide Semiconductor (NMOS) current-source that biases the differential-pair has been removed. Instead, two Voltage-combiners (VC), in a cross coupled configuration ($Nvcup1$, $Nvcdn1$ and $Nvcup2$, $Nvcdn2$) are used to bias the differential-pair. The VC form a structure comprising of a common drain and a common-source device, in a cross-coupled configuration as Figure 5 shows. This has a twofold effect, the two voltage-combiners provide additional DC gain while biasing the differential pair and each one of the differential-pair devices act as common-source and common-gate, simultaneously. This way, Gain-BandWidth Product (GBW) is enhanced and so is the energy-efficiency. The transfer function of this circuit was extracted using SapWin, for better comprehensibility, some aspects were simplified namely the body-effect of the transistors is neglected, and is presented in (2), where $gds_{Nvcup+Nvcdn} = gds_{Nvcup} + gds_{Nvcdn}$ and $cdb_{Nvcup+Nvcdn} = cdb_{Nvcup} + cdb_{Nvcdn}$. From this transfer function is possible to obtain the open-circuit gain expression of the VC. Considering a gm_{Nvcup} and $gm_{Nvcdn} >> gds_{Nvcup+Nvcdn}$, (3), can be simplified.

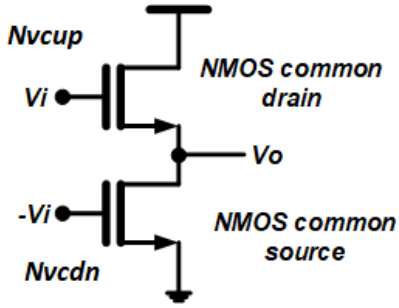


Fig. 5: Voltage-combiner circuit.

$$H(s) = \frac{gm_{Nvcdn} + gm_{Nvcup} + (cgs_{Nvcup} - cgd_{Nvcdn}) \times s}{gm_{Nvcup} + gds_{Nvcup+Nvcdn} + (cdb_{Nvcup+Nvcdn} + cgs_{Nvcup} + cgd_{N}} \quad (2)$$

$$A_{VC} = \frac{gm_{Nvcdn} + gm_{Nvcup}}{gm_{Nvcup} + gds_{Nvcup+Nvcdn}} \approx 1 + \frac{gm_{Nvcdn}}{gm_{Nvcup}}, |A_{VC}| > 1 \quad (3)$$

In this section the small-signal equivalent circuits of the components of the PGA are presented along with the gain equations. The Bartlett's bisection theorem is used to obtain the circuit. When a differential voltage signal is applied to both inputs an exchange of current between both networks will occur. This occurs due to the counterpart nodes movement from both networks, since they have the same amplitude but with phase op-position, just like the differential voltage. However, to support the condition where there are symmetric voltages between the two symmetric networks, the voltages connecting the nodes that are shared along the axis of symmetry have to be equal to zero, a virtual ground.

The circuit without the the voltage combiners and instead an ideal current source is analysed. The small signal analysis is considered and utilizing the bisection theorem, the small signal equivalent circuit is obtained Figure 6. Through the simplification of the circuit it is possible to determine the gain, (4), and understand the contributions to obtain the gain which are the current-mirror factors, given by (5), the parallel of the transistors Pb's or Pa's resistance, $r_{o_{Pa/b}}$, with the transistors PNd's resistance, $r_{o_{PNd}}$, finally the transconductance of transistors $Ndiff1$, $Ndiff2$.

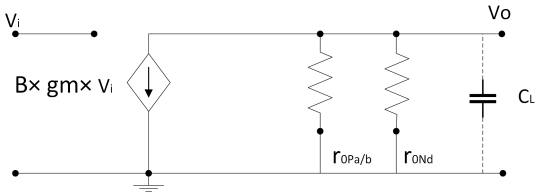


Fig. 6: Small-signal equivalent circuit of current biased PGA.

$$A_v = B \times gm_{ndiff} \times (r_{o_{Pa/b}} || r_{o_{PNd}}) \quad (4)$$

$$B = \frac{I_{out}}{I_{ref}} = \frac{\frac{1}{2}\mu_p C_{ox}\frac{W_{Pa/b}}{L_{Pa/b}}(V_{SG_{Pa/b}} - V_{TH})^2}{\frac{1}{2}\mu_p C_{ox}\frac{W_{Pc}}{L_{Pc}}(V_{SG_{Pc}} - V_{TH})^2} = \frac{\frac{W_{Pa/b}}{L_{Pa/b}}}{\frac{W_{Pc}}{L_{Pc}}} \quad (5)$$

The gain expression for the VC biased circuit, can be obtained through the combination of the calculations done for the VC's gain, (6), and for the current biased PGA. As such, the gain of PGA with the added gain provided by the VC, is as demonstrated in (7), thus demonstrating that the VC, will increase the global gain of the PGA.

$$A_{VC} = \frac{gm_{Nvcdn} + gm_{Nvccup}}{gm_{Nvccup} + gds_{Nvccup+Nvcdn}} \quad (6)$$

$$A_v = B \times \frac{gm_{ndiff}(1 + A_{V_{VC}})}{gds_{Pa/b} + gds_{Nd}} \quad (7)$$

A common mode feedback circuit is a circuit which senses the common-mode voltage, comparing it with a proper reference, and feeding back the correcting common-mode signal on both nodes of the fully-differential circuit, with the purpose to cancel the output common-mode current component, and to fix the DC outputs to the desired level. The ideal and continuous-time common mode feedback, CMFB, must be employed, since this is a fully-differential implementation. The CMFB circuit implements directly the (8), where the differential is compensated in the CMFB mode, taking into consideration the Voltage-Bias (VBIAS) voltage that directs the output.

$$cmfb = -\left(\frac{V_{DD}}{2} - \left(\frac{V_{out+}}{2}\right) - \left(\frac{V_{DD}}{2}\right) - V_{bias}\right) \quad (8)$$

The gain value, 60 dB, is given when the output stage composed by the transistors Pa and Nd is activated through the transistors $Pselc$, acting as a switch, the gain value,40 dB, is given when the output stage composed but the transistors $Pb2$ and Pd is activated through the transistors $Pselb$.

The gain value of the PGA, given by (7), depends on the gm of the differential pair, transistors $Ndiff$, on the gain given by the VC, $A_{v_{VC}}$, given by (6), the transconductance of the transistors are given by (10).

Taking into consideration that the transistors drain current, in the saturation region, is given by (11), the strategy to increase the gain to the desired value is to adjust the width and length of the transistors to increase or decrease the drain current as necessary. Therefore as a starting point the ratio W/L of the transistor $Nvcdn$ is considered in order the least drain current possible while maintaining transistors in saturation region, next the racio W/L of the $Nvcup$, is projected with the intention to increase $A_{v_{vc}}$, given by (6), therefore gm of transistors $Nvcup$, should be greater than $Nvcdn$, as such the transistors $Nvcup$ are designed to operate in the sub-threshold region in order to maximize the gm/ID relation. The racio, of the transistors Pc and Pb, ($\frac{W_{Pb}}{L_{Pb}}/\frac{W_{Pc}}{L_{Pc}}$), or Pc and Pa, ($\frac{W_{Pa}}{L_{Pa}}/\frac{W_{Pc}}{L_{Pc}}$), represented by B in (7), also influences the gain, the value of B is chosen in order to have the maximum value of current in the output branch while keep the current consumption under the 1 µA and the pretended gain for each branch. Finally the gain of the PGA is depended on the gds of transistor Nd and gds of transistors Pa or Pb depending on the gain value selected, as gds is given by (9).

$$gds = \frac{1}{r_o} = \lambda I_D \quad (9)$$

$$gm = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GS} - V_T} \quad (10)$$

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 \quad (11)$$

III. Design Implementation

This section presents the design stages of the PGA from the biasing and sizing to design the layout. An initial circuit implementation is done in United Microelectronics Corporation (UMC) 130 nm CMOS technology using the software Cadence IC. The proposed PGA is implemented at sizing level, design strategies and simulation results. During the circuit sizing a special attention is given to the current consumption.

A. Implementation

Some specification have to be defined as such V_{DD}=3.3 V, Threshold Voltage (V_T)= 0.7 V, V_{DC}=1.65 V. This section presents the final biasing of the PGA. The biasing developed for the VC biased PGA are presented in Table II. These results show the DC voltage parameters and current present in all transistors. To extract the values a DC simulation is done with both inputs having a DC bias voltage of $V_{DD}/2$. Since the bio-potential signal EOG has as a lower amplitude than the EMG signal, the gain applied should be respectively 60 dB and 40 dB.

Most of the transistors operate in the saturation region, except transistors $Nvcup$, $Ndiff$, which operate in the sub threshold region to achieve the pretended gain values. Transistors $Pselb1$, $Pselc1$, $Pselb2$, $Pselc2$, which function as switch and operate in the triode region when selected or in the cut-off otherwise.

The gain value, 60 dB, is given when the output stage composed by the transistors Pa and Nd is activated through the transistors $Pselc$, the gain value, 40 dB, is given when the output stage composed but the transistors $Pb2$ and Pd is activated through the transistors $Pselb$.

The gain value of the PGA, given by (7), depends on the gm of the differential pair, transistors $Ndiff$, on the gain given by the VC, $A_{v_{VC}}$, given by (6), the transconductance of the transistors are given by (10).

Taking into consideration that the transistors drain current, in the saturation region, is given by (11), the strategy to increase the gain to the desired value is to adjust the width and length of the transistors to increase or decrease the drain current as necessary. Therefore as a starting point the ratio W/L of the transistor $Nvcdn$ is considered in order to have the least drain current possible while maintaining transistors

TABLE II: DC analysis.

	V_{DS} [V]	V_{GS} [V]	V_{TH} [V]	V_{DSAT} [mV]	I_D [nA]
Ndiff	1.64	1	0.630	43.2	155
Nvcup	2.28	0.630	0.741	43.1	146
Nvcdn	1	1.65	1	377	898
Pc	0.640	0.640	0.604	68.9	155
	V_{DS} [V]	V_{GS} [V]	V_{TH} [V]	V_{DSAT} [V]	I_D [nA]
Pa	1.38	0.640	0.603	69.6	191.6
Nd	1.9	0.696	0.398	219	191.6
Pselb	0.008	1.9	1.15	594	191.6
	V_{DS} [V]	V_{GS} [V]	V_{TH} [V]	V_{DSAT} [V]	I_D [nA]
Pb	1.52	0.639	0.608	64.9	69
Nd	1.9	0.696	0.398	219	191
Pselc	0.008	1.9	1.15	594	191

in saturation region, next the racio W/L of the $Nvcup$ and $Ndiff$ are projected with the intention have a similar drain current in both transistors as this shown to achieve a better balance between obtaining the gain values and have a higher bandwidth. Transistors $Nvcup$ and $Ndiff$ are designed to operate in the sub-threshold region in order to maximize the gm/ID relation. The racio, of the transistors Pc and Pb, $(\frac{W_{Pb}}{L_{Pb}}/\frac{W_{Pc}}{L_{Pc}})$, or Pc and Pa, $(\frac{W_{Pa}}{L_{Pa}}/\frac{W_{Pc}}{L_{Pc}})$, represented by B in (7), also influences the gain, the value of B is chosen in order to have the maximum value of current in the output branch while keep the current consumption under1 µA and have the pretended gain for each branch. Finally the gain of the PGA is depended on the gds of transistor Nd and gds of transistors Pa or Pb depending on the gain value selected, as gds is given by (9).

B. Simulations

In this section, the PGA's final schematics and test-benches used are presented, along with the test-benches designed to simulate. A brief introduction is done to coherent sampling necessary for it, Alternate Current (AC) simulation and noise analysis of the input referred noise. The analyzes is focus on the EMG and EOG signals, considering an amplitude of 1 mV, 100 µV respectively. To verify if the sizing reaches the intended requirements, some simulations are needed The gain simulation is given by the the slope calculation of the PGA output 0 to 1 V of the differential input voltage. Thus, V_{in+} and V_{in-} have both a DC voltage of 1.65 V and an AC voltage of 1 V and 0 V, respectively and VDD is 3.3 V. The analysis done to obtain the gain is an AC with a logarithmic frequency variation from 1 Hz to 1 MHz. The resulting voltage gain is 61.83 dB, with a Bandwidth (BW) of 617.86 Hz, as showed in Figure 7, for the EOG signal. As for the PGA phase margin, presenting a value of 82.32°. The voltage gain is 49.658 dB, with a BW of 925.68 kHz, as showed in Figure 8, for the EMG signal. As for the PGA phase margin, presenting a value of 87.22°.

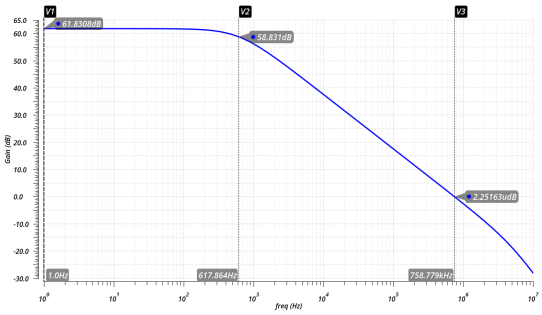


Fig. 7: PGA gain simulation EOG signal.

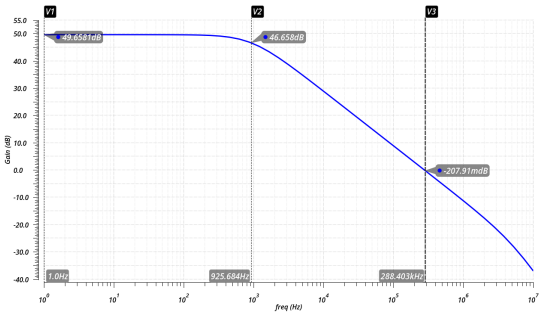


Fig. 8: PGA gain simulation EMG signal.

The noise simulations are executed in the same test-bench and is done by having logarithmic frequency variation from 0.1 Hz to 1 MHz, the plots are presented in Figure 9, for EOG and Figure 10, for EMG. The circuit presents a flicker noise of 15.14 µVrms and a thermal noise of 8.1 µVrms for the signal EOG, and a flicker noise of 36 µVrms and a thermal noise of 21.79 µVrms, for the signal EMG. The input referred-noise is 23.2 µVrms and 45.3 µVrms, for the signal EOG and for the signal EMG, respectively.

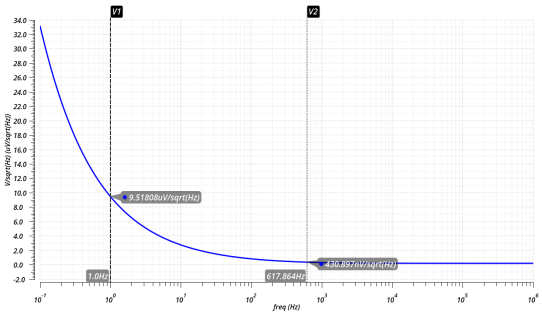


Fig. 9: PGA input referred noise for EOG signal

As mentioned before, to obtain the Total Harmonic Distortion (THD) and dynamic range values, the Discrete Fourier Transform (DFT) from a transient output has to be calculated.

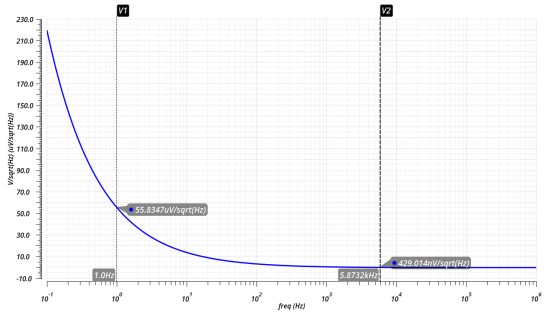


Fig. 10: PGA input referred noise for EMG signal

Thus, beginning with the EOG signal, Figure 11, presents the transient response and its DFT plot obtained from 0.1 s to 0.9192 s in a hamming truncation window. Hence, the obtained THD is 0.277 %, corresponding to a dynamic range of 143.82 dB. As for the EMG signal, illustrated in Figure 12, where the DFT is obtained in the same time period as the one before. This figure shows a THD of 0.0399 %, while the dynamic range is 68.93 dB.

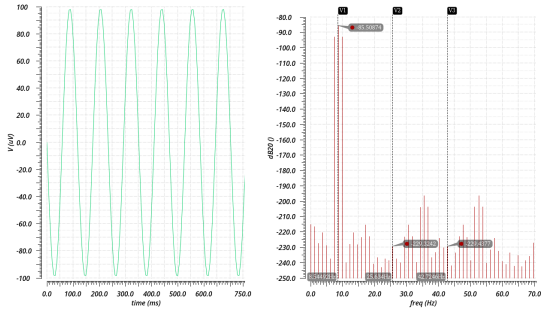


Fig. 11: Simulated PGA transient and DFT response to a 0.1 mV of amplitude and 8.544 921 875 Hz sinusoidal input signal.

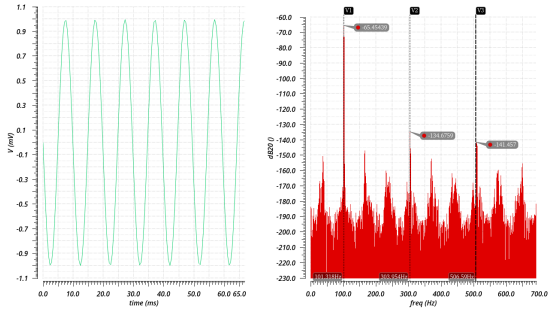
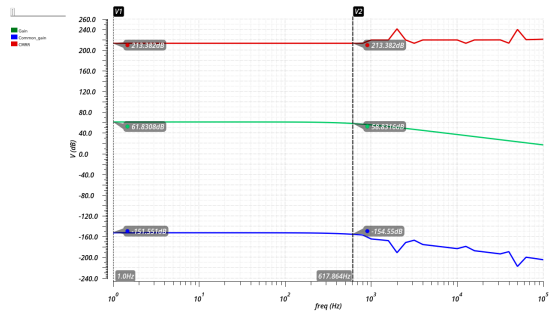
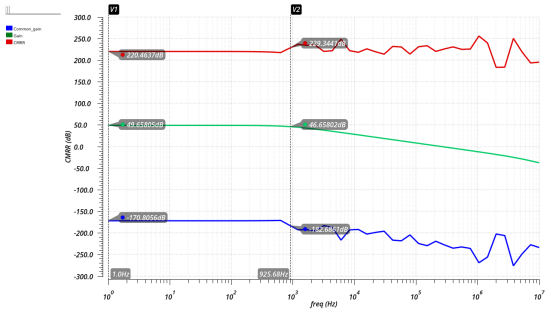


Fig. 12: Simulated PGA transient and DFT response to a 1 mV of amplitude and 101.318 359 375 Hz sinusoidal input signal.

The Common-Mode Rejection Ratio (CMRR), presenting a value of 213.38 dB for the signal EOG, and 220.46 dB, for the signal EMG, the values are represented in Figure 13a and Figure 13b.



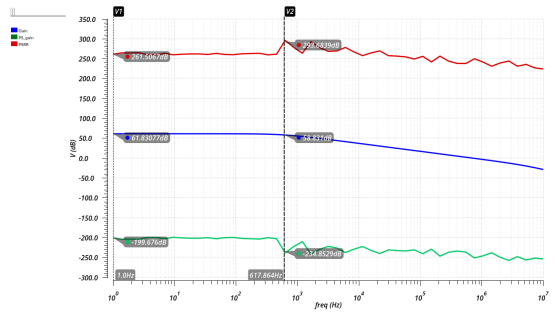
(a)



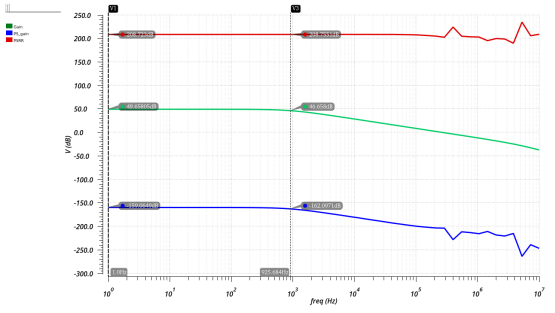
(b)

Fig. 13: (a) Simulated PGA CMRR for EOG; (b) Simulated PGA CMRR for EMG.

As for the PSRR analysis, in Figure 14a with a value of 261.51 dB for the signal EOG and in Figure 14b with a value of 208.74 dB for the signal EMG.



(a)



(b)

Fig. 14: (a) Simulated PGA PSRR for EOG; (b) Simulated PGA PSRR for EMG.

IV. Layout

This section presents the layout design of the PGA and the post-layout simulations and comparison to the original schematic results.

For the development of the circuit's layout, some initial considerations were taken to optimize the design and minimize the parasitic capacitance's. Firstly, the transistor's positions were kept symmetric, while grouping the PMOS separately from the NMOS. The disposition is done to minimize area and the length and number of paths. The rooting is designed to minimize overlaps between paths and not overlap with transistors. For the rooting, the width and area of the paths are sized with the rule 1 µm per 1 mA, the width and area of the paths are kept almost all at value orders of magnitude above the minimum. To minimize parasitic capacitances the connections to Power Supply (V_{DD}) are done with M2 metal, connections to GND with metal M1 and connections between transistors metal M3 and above. To minimize the resistance and prevent complications from manufacturing several contacts are used. Finally, to improve short-circuit protection two rings are implemented around the transistors. To prevent current leakage, the NMOS have a dedicated guard ring (P Plus) which polarizes the substrate to ground. There is also a guard ring (N Plus) which contains the whole circuit, but only polarizes most of the PMOS. The layout can be seen in Figure 15, as an area of 0.0043 mm^2 (77.805 µmX54.75 µm).

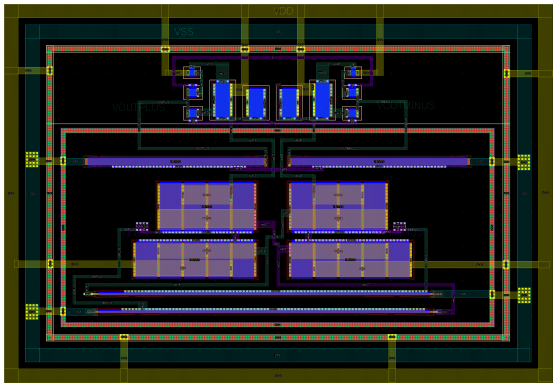


Fig. 15: PGA Layout.

After the layout is completed the parasitic extraction is executed, some post-layout simulations are done. There are some variations in the results when compared to the ones obtained before layout, however the variations are not relevant. The test-bench for each simulation is the same as explained in the previous chapter. In Figure 16 and Figure 17 is demonstrated the PGA AC response for EOG and EMG signals, respectively. For the first signal, a gain of 61.863 dB, a 610.577 Hz BW and phase margin of 81.8°.The second signal presents a gain of 49.657 dB, a BW of 921 Hz and phase margin of 86.85°.

The noise response, post-layout is done, resulting in an integrated equivalent input-referred noise of 23.27 µV and 45.23 µV in their respective BW. The circuit layout presents a flicker noise of 15 µVrms and a thermal noise of 8.12 µVrms

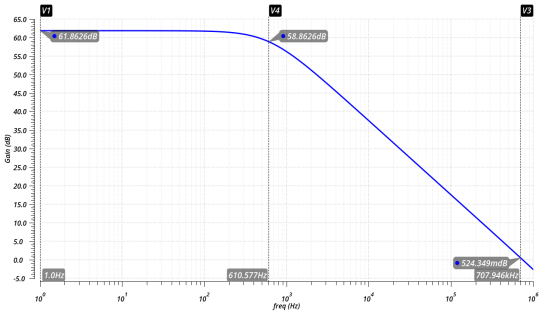


Fig. 16: Simulated PGA post-layout AC response, for EOG signal.

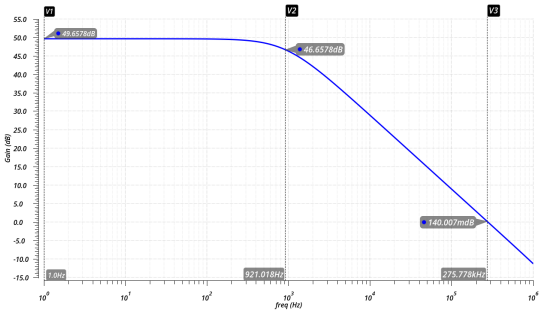


Fig. 17: Simulated PGA post-layout AC response, for EMG signal.

for the signal EOG, and a flicker noise of 36.08 µVrms and a thermal noise of 9.15 µVrms, for the signal EMG.

As for the CMRR and PSRR, they are simulated in post-layout conditions, as shown in Figure 18. For the EOG case, the CMRR achieves a value of 144.55 dB and the PSRR a value of 165.17 dB, as shown in Figure 19. Concerning the EMG case, the CMRR and PSRR are shown in Figure 20, Figure 21, respectively, with the values of 167.23 dB and 140.1 dB. When compared to values obtained in the schematic simulations, there is a relevant difference with the layout values being lower than the schematic ones.

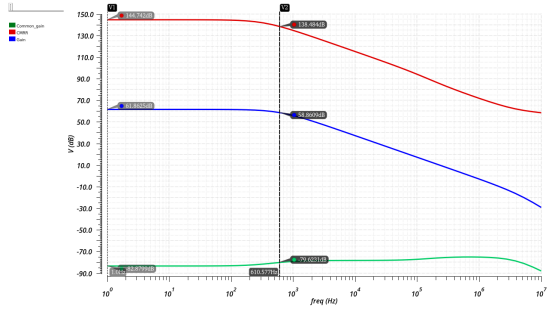


Fig. 18: Simulated PGA post-layout CMRR, for EOG signal.

The transient analysis of the PGA response and respective DFT is shown in Figure 22 for the EOG case and in Figure 23 for the EMG case. The first one presents a THD value of 0.283 % and a dynamic range value of 143.49 dB. As for the

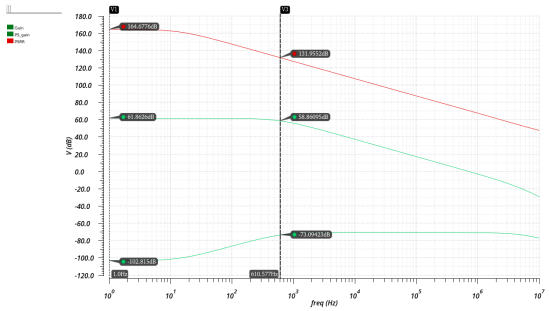


Fig. 19: Simulated PGA post-layout PSRR, for EOG signal.

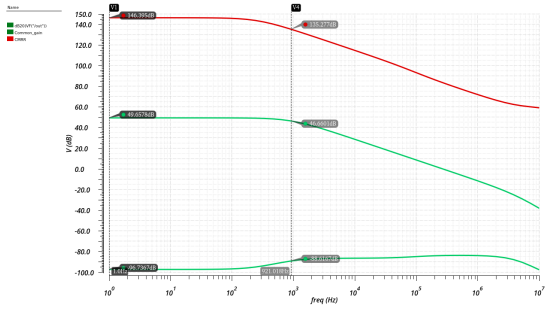


Fig. 20: Simulated PGA post-layout CMRR, for EMG signal.

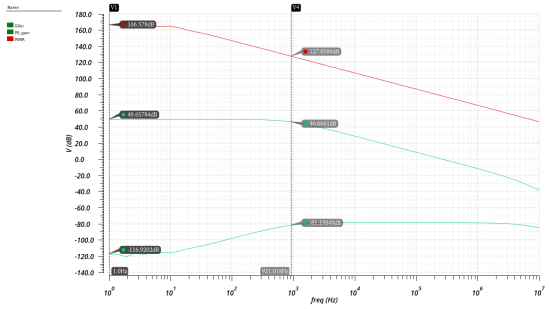


Fig. 21: Simulated PGA post-layout PSRR, for EMG signal.

second case, a THD value 0.0415 % and a dynamic range value of 68.7 dB.

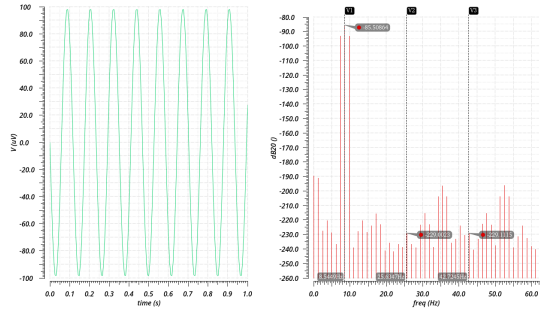


Fig. 22: Simulated post-layout PGA transient and DFT response to a response to a 0.1 mV of amplitude and 8.544 921 875 Hz sinusoidal input signal.

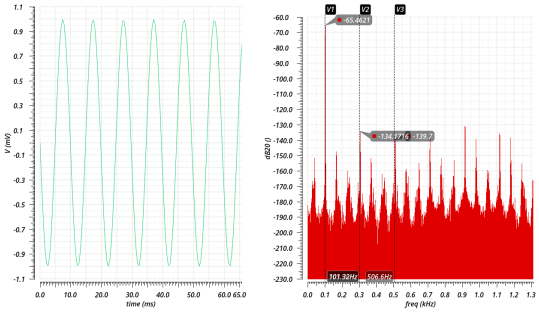


Fig. 23: Simulated post-layout PGA transient and DFT response to a 1 mV of amplitude and 101.318 359 375 Hz sinusoidal input signal.

V. Conclusion

As described before, this work proposes to develop an PGA for use in a system to acquire bio-potential signal, The power consumption be less than 3.3 µW, also the PGA should have programmable gain range between 50 dB and 60 dB and a CMRR and PSRR of 60 dB and 80 dB respectively. In Section II, the proposed PGA design is presented, starting with a theoretical analysis followed by the sizing, which guarantees most of the proposed specifications, as the simulations done demonstrate. Therefore, while consuming under 1 µA the PGA presents a gain of 49.7 dB for the signal EMG and a gain of 61.8 dB for the signals EOG, while consuming less than 1 µA for both gains. As for the linearity metrics, the targeted values are achieved for the THD with 0.038 % and a dynamic range of 69.22 dB, for the EMG, and a value for the THD of 0.277 % and a dynamic range of 143.8 dB, for the EOG thus accomplishing the specification. In both cases the proposed targets for CMRR and PSRR are achieved. The grand majority of the post-layout results do not have a significant deviation from the ones obtained in the schematic simulations, for example, both the gains and the linearity metrics. A comparison with state-of-the-art is presented in Table III. This work is competitive in the current consumption, in the CMRR and PSRR metrics and on the THD compared to the with state-of-the-art studied.

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TABLE III: Comparison of the state-of-the-art with this work.

Work	[2]	[3]	[4]	[5]	[6]	[7]	[8]	This Work
Year	2006	2013	2017	2012	2017	2017	2012	2021
Tech (nm)	350	180	65	180	180	180	90	130
Gain (dB)	0-21	0-70	2-25	-24 - 21	30-40	35-70	40-70	50-60
BW (MHz)	100	6.6-15	2	66.28	0.05-11 kHz	800-1400 Hz	175-316 mHz 23-69 Hz	921Hz 610.5 Hz
Supply Current (mA)	0.28	1.26	0.5	5.3	0.0182	0.6μA	1.2μA	0.742 μA 0.984 μA
Supply voltage (V)	1.8	1	1.5V	1.8	1.8	1	3.3	3.3
CMRR (dB)	-	-	-	-	84	102	-	146 145
PSRR (dB)	-	-	-	-	86.9	104	-	132 159
THD (%)	0.1 @0.2Vpp	-	-	-	-	-	0.96 1.1 @10mVpp @5mVpp	0.0415 0.283
Area (mm^2)	0.004	0.94	0.0045	0.7	0.03	0.0625	-	0.0043

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