BIOCAS: A Tunable Transconductance-Based Active Filter for Biomedical and Healthcare Applications

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Thesis to obtain the Master of Science Degree in Electrical and Computer Engineering

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Declaration

I declare that this document is an original work of my own authorship and that it fulfills all the requirements of the Code of Conduct and Good Practices of the Universidade de Lisboa.
Acknowledgments

I would like to give a very special thanks to my family and friends who supported me and accompanied me through all these years away from home, allowing me to follow my dreams of achieving a higher education.

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Abstract

This work consists in the development of a tunable transconductance-based active low-pass filter. The filter will have the final goal of being embedded in a system for biomedical and healthcare monitoring. For this purpose, the filter must be energy-efficient and low-power since this circuit will be a part of a long-lasting battery powered and portable system. The signals which priority is given to are: Electromyography, which has a frequency range of 20 - 2000 Hz; and Electrooculography, which has a range of DC - 10 Hz, for the corresponding operating frequencies. Therefore, it is necessary to design a tunable low-pass filter to capture the desired signal and minimize interference. Common sensing systems are usually composed of a low-noise amplifier, a low-pass filter and a variable or programmable gain amplification stage.

In this report, low-pass filters are presented and studied, alongside a section of important concepts and another with metrics considered in low-pass filter design, and the circuit proposal is presented in generic terms. The circuit will be designed in a Complementary Metal-Oxide Semiconductor (CMOS) 130 nm technology, the 130 nm United Microelectronics Corporation (UMC), using Cadence software and further optimization sizing will be carried out using the Analog IC Design Automation (AIDA) framework, developed at Instituto de Telecomunicações. The expected results consist of a frequency range between 0.01 - 2000 Hz, a total harmonic distortion lower than -60 dB with a dynamic range of more than 60 dB, an integrated noise below 50 $\mu$V rms and a gain greater than 0 dB relieving the specifications for the prior low-noise amplifier, all under a voltage supply below 1 V and a power consumption inferior to 1 $\mu$W.

Keywords

Active-filter, Tunable, CMOS, Low-power, Transconductance, Gm-C, Biquad, Tow-Thomas, Biomedical, Healthcare
Resumo

Este trabalho consiste no desenvolvimento de um filtro passa-baixo ajustável baseado em transcondutância. Este filtro tem como finalidade ser implementado num sistema de monitorização para aplicações biomédicas e de cuidados de saúde. Para este propósito, o filtro terá de ser eficiente com a energia fornecida e funcionar a baixas potências, pois este filtro será uma componente de um sistema portátil duradouro e carregado por uma bateria. Os sinais aos quais é dada prioridade são: Electromiografia, que tem um alcance de frequências de 20 - 2000 Hz; e Electroocolografia que tem um alcance de DC - 20 Hz, para as correspondentes frequências de operação. Deste modo, é necessário um filtro passa-baixo ajustável para capturar o sinal desejado e minimizar interferência. Sistemas de monitorização normalmente são compostos por um amplificador de baixo ruído, um filtro passa-baixo e um amplificador de ganho programável.

Neste relatório, o estado-de-arte de filtros passa-baixo são apresentados e estudados, do mesmo modo conceitos importantes e métricas consideradas no dimensionamento de um filtro passa-baixo, e o circuito proposto é apresentado em termos genéricos. Os circuitos serão dimensionados em tecnologia CMOS de 130 nm, a UMC de 130 nm, utilizando o software Cadence, futura otimização será feita utilizando a ferramenta AIDA, desenvolvida no Instituto de Telecomunicações. Os resultados esperados consistem num alcance de frequência entre 0.01 - 2000 Hz, uma distorção harmónica total menor que -60 dB com um alcance dinâmico superior a 60 dB, um ruído integrado inferior a 50 $\mu V_{rms}$ e um ganho superior a 60 dB aliviando as especificações do amplificador de baixo ruído antecedente, tudo com uma tensão fornecida inferior a 1.2 V e uma potência consumida inferior a 1 $\mu W$.

Palavras-Chave

Filto-ativo, Ajustável, CMOS, Baixa-potência, Transcondutância, Gm-C, Tow-Thomas, Biomédico, Cuidado de Saúde.
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<th>Description</th>
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<tbody>
<tr>
<td>AC</td>
<td>Alternate Current</td>
</tr>
<tr>
<td>AIDA</td>
<td>Analog IC Design Automation</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide Semiconductor</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DFT</td>
<td>Discrete Fourier Transform</td>
</tr>
<tr>
<td>ECG</td>
<td>Electrocardiography</td>
</tr>
<tr>
<td>EMG</td>
<td>Electromyography</td>
</tr>
<tr>
<td>EOG</td>
<td>Electrooculography</td>
</tr>
<tr>
<td>EDA</td>
<td>Electronic Design Automation</td>
</tr>
<tr>
<td>FFT</td>
<td>Fast Fourier Transform</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain–bandwidth Product</td>
</tr>
<tr>
<td>GC</td>
<td>Gain-compensation</td>
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<tr>
<td>IC</td>
<td>Integrated Circuit</td>
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<tr>
<td>IOT</td>
<td>Internet of Things</td>
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<tr>
<td>LNA</td>
<td>Low-Noise Amplifier</td>
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<tr>
<td>LPF</td>
<td>Low-pass Filters</td>
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<tr>
<td>MOSFET</td>
<td>Metal–Oxide–Semiconductor Field-effect Transistor</td>
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<tr>
<td>NMOS</td>
<td>N-type Metal-Oxide Semiconductor</td>
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<tr>
<td>Abbreviation</td>
<td>Description</td>
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<td>--------------</td>
<td>--------------------------------------------</td>
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<tr>
<td>OTA</td>
<td>Operational Transconductance Amplifier</td>
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<tr>
<td>OPAMP</td>
<td>Operational Amplifier</td>
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<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
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<tr>
<td>PF</td>
<td>Power Factor</td>
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<tr>
<td>PMOS</td>
<td>P-type Metal-Oxide Semiconductor</td>
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<tr>
<td>POF</td>
<td>Pareto Optimal Front</td>
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<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
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<tr>
<td>SC</td>
<td>Switched-capacitor</td>
</tr>
<tr>
<td>SD</td>
<td>Spectral Density</td>
</tr>
<tr>
<td>SSF</td>
<td>Subthreshold-Source-Follower</td>
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<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
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<td>UMC</td>
<td>United Microelectronics Corporation</td>
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<td>VCs</td>
<td>Voltage-combiners</td>
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## Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
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<tr>
<td>$A_{cm}$</td>
<td>common-mode gain</td>
</tr>
<tr>
<td>$A_{dm}$</td>
<td>differential-mode gain</td>
</tr>
<tr>
<td>$A_v$</td>
<td>voltage gain</td>
</tr>
<tr>
<td>$B$</td>
<td>current-mirroring factor</td>
</tr>
<tr>
<td>$f$</td>
<td>frequency</td>
</tr>
<tr>
<td>$f_c$</td>
<td>cut-off frequency</td>
</tr>
<tr>
<td>$f_s$</td>
<td>sampling frequency</td>
</tr>
<tr>
<td>$g_m$</td>
<td>small-signal transconductance</td>
</tr>
<tr>
<td>$G_m$</td>
<td>OTA transconductance</td>
</tr>
<tr>
<td>$i$</td>
<td>electric current</td>
</tr>
<tr>
<td>$I_{BIAS}$</td>
<td>bias current</td>
</tr>
<tr>
<td>$I_D$</td>
<td>drain current</td>
</tr>
<tr>
<td>$i_{out}$</td>
<td>output current</td>
</tr>
<tr>
<td>$L$</td>
<td>transistor length</td>
</tr>
<tr>
<td>$k$</td>
<td>Boltzmann constant</td>
</tr>
<tr>
<td>$U_t$</td>
<td>thermal voltage</td>
</tr>
<tr>
<td>$v$</td>
<td>voltage</td>
</tr>
<tr>
<td>$v_{cm}$</td>
<td>common-mode voltage</td>
</tr>
<tr>
<td>$v_d$</td>
<td>differential-mode voltage</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>positive supply voltage</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>gate-source voltage</td>
</tr>
<tr>
<td>$v_{in}$</td>
<td>input voltage</td>
</tr>
<tr>
<td>$v_{out}$</td>
<td>output voltage</td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>negative supply voltage</td>
</tr>
<tr>
<td>$W$</td>
<td>transistor width</td>
</tr>
<tr>
<td>$w_0$</td>
<td>angular cut-off frequency</td>
</tr>
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Introduction

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Introduction

1.1 Purpose and Motivation

Nowadays, after the popularity of Internet of Things (IOT), it is obvious the necessity of low-powered and long-lasting circuits for biomedical and healthcare applications. The wearable devices are an end in which these are being developed, and modern electronics are capable of detecting and monitoring physical and psychological signals. These new circuits need to be more and more energy efficient while improving the characteristics and performance for such systems. Wearable technology is the name given to the devices developed with the goal of being incorporated in clothes or worn on the body as implants or accessories. The devices have some challenges to their continuous improvement, such as portability, ergonomics, and battery longevity and lasting appeal [1].

The devices must be small enough to allow for comfortable monitoring of signals and the system need to drain a low current, in order to avoid excessive heat and even skin or tissue damage to the wearer. The involved signals are often low voltage and low frequency, with a few mV below tens of kHz, so, energy-efficient low-frequency noise filtering is essential in these devices. Electromyography signal that encode normal flexion of muscles has an amplitude range of 1 - 10 V and frequency range of 20 - 2000 Hz; while Electrooculography signal that encode movement of the eyes has an amplitude range of 0.01 - 0.1 mV for and vary from DC to 10 Hz in frequency, yet both types follow similar signal patterns. Therefore, the design of a selective Low-pass Filters (LPF) to allow the selection of the desired signal and avoid interference is completely desirable and justified.

This work will be carried out using United Microelectronics Corporation 130 nm technology, using the Cadence® design framework. Cadence® provides a platform for circuit design, allowing engineers to focus on precision-crafting their custom Integrated Circuit (IC) design. Furthermore, the IC designed will have its size and layout optimized by the Electronic Design Automation (EDA) tool Analog IC Design Automation. AIDA allows for design optimization and porting using highly efficient searching methods combined with accurate circuit-level simulation, layout design rules, and parasitic extraction engines, and is being developed in Instituto de Telecomunicações.
1.2 Goals and Challenges

The main objective of this work is to develop a tunable LPF, for biomedical and healthcare devices. The main challenges in the realization of this circuit are:

- High energy efficiency;
- Low active-area;
- Low noise contribution;
- Effective gain.

The system specifications goal is presented in Table 1.1.

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</thead>
<tbody>
<tr>
<td>1.2</td>
<td>&lt; 1</td>
<td>2</td>
<td>Butterworth</td>
<td>0.13</td>
<td>0.01 - 2000</td>
<td>&gt; 0</td>
<td>&lt; 50</td>
<td>&lt; -60</td>
</tr>
</tbody>
</table>

The presented set of specifications is encompassed in an overviewed state-of-the-art, explored throughout. It is intended to design a µW filter, in order to minimize the impact on a sensor. The UMC 130 nm technology will be implemented, under a 1.2 V voltage supply, which means the current consumption will be in the order of hundreds of nA. The integrated noise must be low, in parallel with effective gain, which means the gain must be positive. Finally, a total harmonic of -60 dB relates with the difference between the fundamental component and a sine-wave third harmonic spectral power.

1.3 Document Organization

This report is organized as follows:

- Chapter 1 is an introduction about the purpose of the filter and its implementation. Furthermore the design specifications are presented.

- Chapter 2 is the state-of-the-art where some theory of LPFs is explained. In this chapter, basic concepts and important metrics are presented for a better understating of the work. Important circuit topologies are described and, finally, a summary of the related work is presented.

- In Chapter 3 the architecture of the proposed circuit is shown.

- In Chapter 5 the conclusions are presented along with the scheduling for future work.
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State-of-the-Art

This chapter presents the state-of-the-art of LPF, to provide context and give an overview of the topics presented in this dissertation. The basic concepts on LPF are presented in section 2.1, important metrics regarding the performance are presented in section 2.2, in section 2.3 some of the most common filter approximations are described and the most relevant circuit topologies in recently published literature are described in section 2.4.

2.1 Basic Concepts on Low-Pass Filters

Sometimes, it is desirable to have circuits capable of selectively filtering one frequency or range of frequencies out of a mix of different frequencies in a system. A LPF is a filter that lets through signals with frequency lower than its corner frequency and attenuates signals with higher frequency. A 1st-order, or one pole, LPF can be a passive RC circuit, which is composed of a resistor, and a capacitor in parallel with the load, as shown in Figure 2.1a. A second order, or two poles, filter can be as in Figure 2.1b. The reactance of the capacitor blocks lower frequencies forcing them through the load and at higher frequencies the capacitor has very low reactance working as a short circuit, filtering the frequency. The frequency at which the first-order filter cuts off is given by Equation 2.1, whereas the second-order filter at Equation 2.2. The transfer function of the first-order filter is given by Equation 2.3 while the second-order filter transfer function is given by Equation 2.4, where Q represents the quality factor of the filter. In both cases K represents the low frequency, or static, gain. In both cases K equals one.

![1st-order RC filter](image1)

![2nd-order RC filter](image2)

Figure 2.1: Example of passive filters.
$$f_{c1st} = \frac{1}{2\pi R_1 C_1},$$  \hspace{1cm} (2.1)$$

$$f_{c2nd} = \frac{1}{2\pi \sqrt{R_1 C_1 R_2 C_2}},$$  \hspace{1cm} (2.2)$$

$$H(s) = K \frac{1}{s R_1 C_1 + 1}.$$  \hspace{1cm} (2.3)$$

$$H(s) = K s^2 + \frac{1}{Q \sqrt{R_1 C_1 R_2 C_2}} + \frac{1}{R_1 C_1 R_2 C_2}.$$  \hspace{1cm} (2.4)$$

A passive LPF has certain limitations that impede its usage in more precise and complex circuits. The impedance creates a loss in the amplitude and more filter stages can result in a greater loss of amplitude. Amplification cannot be done by a passive LPF alone, so, attenuating this problem is impossible. Finally, the filter’s characteristics depend on a considerable amount on the load impedance. An active LPF introduces, usually, an Operational Amplifier (OPAMP) in its design. An OPAMP is mostly chosen for its high input impedance and introduces little noise, and will be described further in this document. In the example of Figure 2.2 the corner frequency is given by $f_c = 1/(2\pi R_2 C)$ \cite{2}, working in a similar way to the passive filter, but in this design, the filter has an adjustable gain that is given by $-R_2/R_1$, as shown in Equation 2.5.

![Active low-pass filter](image)

**Figure 2.2:** Active low-pass filter.

$$H(s) = -\frac{R_2}{R_1 R_2 Cs + 1}$$  \hspace{1cm} (2.5)$$

### 2.1.1 Ideal Operational Amplifier

An ideal OPAMP, in its ideality, is a circuit approximation that has differential input, infinite voltage gain, infinite input resistance, and zero output resistance. In a real OPAMP, the gain depicted in Figure 2.3, $A_v$, refers only to the differential gain, or the gain applied to the differential voltage at the input of the amplifier. Furthermore, a real OPAMP also amplifies the common-mode voltage, $v_{cm}$, which is the
voltage value applied to both inputs of the amplifier at the same time. This gain is called common-mode gain and in reality, can be very small, but it is never zero. The real output of an OPAMP is given by Equation 2.6 [3], where $A_{dm}$ and $A_{cm}$ are the differential gain and common-mode gain respectively, $v_d$ the differential input defined in Equation 2.7 and $v_{cm}$ the common mode input, defined in Equation 2.8.

$$v_{out} = A_{dm}v_{in} + A_{cm}v_{cm} \tag{2.6}$$

$$v_d = v_{in} = v^+ - v^- \tag{2.7}$$

$$v_{cm} = \frac{v^+ + v^-}{2} \tag{2.8}$$

![Internal circuit of an ideal OpAmp.](image)

**Figure 2.3:** Internal circuit of an ideal OpAmp.

### 2.1.2 Operational Transconductance Amplifier

The OTA is an amplifier whose differential input voltage produces a current output with an active gain, how the basic electrical symbol demonstrates in Figure 2.4a. In some topologies, the gain can be tuned by adjusting a DC current, with significant ranges. OTAs can realize complex functions, same as their OPAMP counterparts, but with often r circuits, these circuits are also preferred when building components substantial resistance, such as capacitors. As a downside, the properties of these circuits are usually process and temperature dependent. The basic electrical OTA scheme is the symmetrical CMOS OTA show in Figure 2.4b.

The output current value of an ideal OTA is given by Equation 2.9. The cut-off frequency is given by Equation 2.10 [4].

$$I_{out} = gm \times (V^+ - V^-) = gm \times V_{in} \tag{2.9}$$

$$f_c = \frac{gm}{2\pi C_L\left(r_{0P0b}/r_{0N12}\right)} \tag{2.10}$$
2.1.3 Switched-Capacitor

A Switched-capacitor (SC) is a circuit that functions by moving charges in and out of capacitors with switches determining the order [5]. Normally, non-overlapping signals are used to control the switches, guaranteeing that all switches are not closed at the same time. A SC is represented in Figure 2.5a, which is composed of one capacitor C1 and two switches S1 and S2. At a given frequency, the switches alternately connect the SC to the output and input. When S1 is closed and S2 is open the capacitor C1 is charged and in the next cycle when S1 is open and S2 is open C1 is discharged. In DC terms, an equivalent resistor equals $1/f_s C$ where $f_s$ is the switching frequency.

2.1.4 Cascode Stage

The cascode configuration is beneficial as it increases output resistance and reduces unwanted capacitive feedback in amplifiers, as such, proper operation at higher frequencies is possible [6]. The basic cascode presented in Figure 2.5b is composed of a common-source transistor connected to a common-gate transistor. The gain expression resulting from this configuration is given by equation Equation 2.11. The gain is derived from the transconductance of N0 times the output resistance, which is also affected by the transconductance of N1, as shown in Equation 2.12.

$$ A_v = -g_{mN0} \times r_{out} \cong -g_{mN0} \times g_{mN1} \times r_{outN0} \times r_{outN1} $$ (2.11)

$$ r_{out} = (g_{mN1} \times r_{outN1} + 1)r_{outN0} \cong g_{mN1} \times r_{outN0} \times r_{outN1} $$ (2.12)
2.1.5 Gyrator Circuit

An OTA-C filter based on a passive LC ladder can be achieved by substituting the inductors by their OTA-C equivalents. The gyrator, with a grounded capacitor represented in Figure 2.5c, will simulate an inductor with inductance \( L = C/g_{m1}g_{m2} \) [7].

![Gyrator Circuit Diagram](image)

(a) Example of a Switched Capacitor.
(b) Cascode Stage.
(c) Grounded Gyrator.

Figure 2.5: Switched Capacitor, Cascode Stage and a Grounded Gyrator.

2.2 Performance Metrics

In this section, the most relevant performance metrics of the LPF are described, in order to provide a better understanding and more comfortable reading of the developed work.

2.2.1 Frequency Response

The gain represents the increase in voltage when a signal is transmitted from one point to another. Gain, as shown in equation Equation 2.13 is determined by the ratio of the output voltage by the input voltage, for a system or circuit. Typically, this metric is represented in terms of decibels, calculated in the second part of the equation Equation 2.13, or V/V or dimensionless. The corner frequency is the frequency at which a 3 dB attenuation occurs in the gain represented in Figure 2.6, which corresponds to a drop of approximately 70.7\% in linear terms. The bandwidth is the difference between the upper and lower frequencies in a continuous band of frequencies, typically measured in Hertz. Passband bandwidth is the difference between the upper and lower cut-off frequencies for example, in a band-pass filter. Baseband bandwidth applies to a LPF, the bandwidth is equal to its cut-off frequency, once again, viewing Figure 2.6 the bandwidth coincides with \( f_c \) represented. The Gain–bandwidth Product (GBW) for an amplifier, as shown in Figure 2.6 is the product of the bandwidth and the gain. The resulting product is a constant, for a single pole OPAMP, and allows for the determination of the circuit gain for a given frequency (or bandwidth) and vice-versa.
\[ \text{gain} = \frac{v_{\text{out}}}{v_{\text{in}}} = 20 \log\left(\frac{v_{\text{out}}}{v_{\text{in}}}\right) \quad \text{(2.13)} \]

Figure 2.6: Gain and \( f_c \).

### 2.2.2 Noise

The sensitivity of communications systems is limited by noise. One predominant type of noise is the flicker noise, that follows a \( 1/f \) characteristic [8]. This noise, as the therm \( 1/f \) suggests, increases with the decreasing of the frequency of the system, limiting the bandwidth. In higher frequencies, the thermal noise is more predominant compared to the shot noise. The thermal noise comes from the thermally agitated charge carriers in a conductor that constitutes a randomly varying current that gives rise to a random voltage. Shot noise occurs when there is a DC current flow and a potential barrier for the charge carriers to overcome, it is the randomness of the arrival that generates shot noise. Shot noise is more important in TJBs. To convert the value of noise in the common unit of \( V_{\text{rms}} \) it would be necessary to integrate the squared Spectral Density (SD) graph in the desired bandwidth, as shown in Equation 2.14. This way would be too time-consuming so a common approximation is to approximate the area of integration by geometry and the final value would be given by \( V_{\text{rms}} = SD \times \sqrt{\mathcal{F}} \times F \), where \( F \) is a factor associated with the filter approximation and order it is available in dedicated technical literature applied to this field [9].

\[ V_{\text{rms}} = \sqrt{\int_{f_{\text{LOW}}}^{f_{\text{HIGH}}} SD(f)^2 df} \quad \text{(2.14)} \]

Figure 2.7: Flicker, thermal and shot noise.
2.2.3 CMRR and PSRR

The Common-Mode Rejection Ratio (CMRR) is an important metric of a differential circuit, such as an OPAMP and an OTA, since most analog systems transmit their signals deferentially. The CMRR, defined in Equation 2.15 [6], quantifies the ability of the system to reject common-mode signals in both inputs. A low CMRR in an OPAMP would result in undesired signals, like noise that is common on both inputs, to also be amplified. Ultimately, this can result in the saturation of the circuit or system.

The PSRR is a term used to describe the capability of an electronic circuit to attenuate any power supply variations to its output signal, and is usually expressed in decibels. Ideally, the power supply and the ground would be constant and not introduce variations in the output. Therefore, the PSRR, defined in Equation 2.16 [10] where $A_v$ is the differential gain and $A_{dd}$ is the gain when the input is zero, is used to evaluate the capability of rejecting these variations.

$$CMRR = 20 \log \left| \frac{A_{dm}}{A_{cm}} \right| \quad (2.15)$$

$$PSRR = 20 \log \left| \frac{A_v}{A_{vdd}} \right| \quad (2.16)$$

2.2.4 Transconductance

The transconductance is measured in Siemens $S$, and is represented by $g_m$. It is the characteristic that relates the voltage at the input of a device with a current at the output of a device. In a typical CMOS transistor, the transconductance is given by Equation 2.17 [4], where $I_D$ is the DC current at bias point and $V_{OV}$ is the overdrive voltage, or the difference between the gate-source voltage $V_{GS}$, and the threshold voltage of the device, $V_{th}$.

$$g_m = \frac{2I_D}{V_{ov}} = \frac{2I_D}{V_{GS} - V_{th}} \quad (2.17)$$

2.2.5 THD

The Total Harmonic Distortion (THD) measures the ratio of fundamental signal amplitude to that of all harmonics. Harmonics are caused by distortions to the underlying perfect sinusoidal component of any signal, produced by the action of non-linear behaviour. The THD of a signal is defined by the weight of all harmonics in comparison to the fundamental. It is usually measured in percentage or dB according to Equation 2.18 [2].

$$THD = 10 \log \left( \frac{V_{D2}^2 + V_{D3}^2 + V_{D4}^2 + ...}{V_{D1}^2} \right) \quad (2.18)$$
2.3 Filter Approximations

In this section the Butterworth, Chebyshev, Elliptic and Bessel filter approximations will be presented and described.

2.3.1 Butterworth

The Butterworth filter approximation transfer function of the $n^{th}$-order is given by Equation 2.19, where $n$ is the order of the filter and $G_0$ is the DC gain at zero frequency. The frequency response of the Butterworth filter is maximally flat. It has no ripple in the passband and rolls off towards zero in the stopband. When viewed on a logarithmic scale, the response slopes of linearly towards negative infinity. Finally, the frequency response of a 5$^{th}$-order Butterworth filter is represented in Figure 2.8a.

\begin{equation}
|H_n(j\omega)| = \frac{G_0}{\sqrt{1 + (j\omega/\omega_0)^{2n}}} \tag{2.19}
\end{equation}

2.3.2 Chebyshev

In the Chebyshev filter approximation the transfer function of the $n^{th}$-order low-pass filter is given by Equation 2.20, where $s$ is equal to $j\omega$, $\epsilon$ is the ripple factor, $\omega_0$ the cut-off frequency and $T_n$ is a Chebyshev polynomial of $n^{th}$-order. Chebyshev filters have a steeper roll-off and more passband ripple or stopband ripple than Butterworth filters. Chebyshev filters are able to minimize the error between the idealized and the actual filter characteristic over the range of the filter, which means that this approximation is more likely to be righteously implemented in practical terms. Finally, the frequency response of a 5$^{th}$-order Chebyshev filter is represented in Figure 2.8b.

\begin{equation}
|H_n(j\omega)| = \frac{1}{\sqrt{1 + \epsilon^2 + T_n^2(\omega/\omega_0)}} \tag{2.20}
\end{equation}

2.3.3 Elliptic

In the Elliptic filter approximation the transfer function of the $n^{th}$-order low-pass filter is given by Equation 2.21, where $\epsilon$ is the ripple factor, $\omega_0$ the cut-off frequency, $\zeta$ is a selectivity factor and $R_n$ is an elliptic rational function of the $n^{th}$-order. An elliptic filter is a filter with equalized ripple behaviour in both the passband and the stopband. The amount of ripple in each band is independently adjustable, and no other filter of equal order can have a faster transition in gain between the passband and the stopband, for the given values of ripple. Finally, the frequency response of a 5$^{th}$-order Elliptic filter is represented in Figure 2.8c.
\[ |H_n(\omega)| = \frac{1}{\sqrt{1 + \epsilon^2 + R_n^2(\zeta, \omega/\omega_0)}} \] (2.21)

### 2.3.4 Bessel

The Bessel filter approximation transfer function of the n\textsuperscript{th}-order is given by Equation 2.22, \( \theta_n \) is a reverse Bessel polynomial, they are defined and have different forms depending on the filter order. A Bessel filter is an analog linear filter with a maximally flat group, or phase delay, which is the maximally linear phase response, which preserves the wave shape form of the signals in the passband. Finally, the frequency response of a 5\textsuperscript{th}-order Bessel filter is represented in Figure 2.8d.

\[ |H_n(s)| = \frac{\theta_n(0)}{\theta_n(s/\omega_0)} \] (2.22)

**Figure 2.8:** Filter approximations frequency response.
2.4 Circuit Topologies

In this section several circuit architectures relevant to the work in this dissertation are presented and described.

2.4.1 High Ground-Noise Rejection

The paper [8] presents a second order Bessel low-pass filter based on the $G_m - C$ architecture, represented in Figure 2.9a. The current-division technique is used to reduce the $G_m$. The filter contains a differential amplifier into the negative loop to obtain the very low corner frequency and to eliminate the coupling from the ground. The ground-noise rejection requires only one extra amplifier independent of how many stages of $G_m - C$ filters are in cascade. The design of the 2$^{nd}$-order Bessel, represented in Figure 2.9a, has a transfer function as presented in Equation 2.23. Where $\omega_p$ is equal to $G_{m1}/C_1$. The filter’s corner frequency is given by $\omega_p/2\pi$. The authors [8] applied a current division technique to reduce $G_m$ and so the transconductance is given by equation Equation 2.24, where $N$ is the number of transistors in parallel and $M$ the number of transistors in series, as shown in Figure 2.9b. For the final equality in Equation 2.24, the author considered the calculations done in Equation 2.25 and took into account that the transconductance of the transistors in series is inversely proportional to $M$ and the transconductance of the transistors in series is proportional to $N$. This work managed to obtain adjustable corner frequencies between 1 and 50 Hz, the frequency depends on the $G_m$ and this value is adjustable by the $I_{BIAS}$, a power supply of 1.2 $\mu$W and ground-noise rejection of -64 dB (at 60 Hz).

\[ H(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{1}{1 + \frac{s}{\omega_p} + \frac{1}{3}\left(\frac{s}{\omega_p}\right)^2} \]  

Figure 2.9: Proposed OTA based filter and respective OTA schematic.
\[ G_m = g_{m1} \frac{g_{m2B}}{g_{m2A}} = g_{m1} \frac{\sqrt{\frac{1}{2} \frac{I_{BIAS} W/L_{m2B}}{W/L_{m2A}}}}{\sqrt{\frac{1}{2} \frac{I_{BIAS} W}{L_{m2A}}}} = \frac{g_{m1}}{MN} \] (2.24)

\[ \sqrt{\frac{1}{2} \frac{I_{BIAS} W/L_{m2B}}{W/L_{m2A}}} = \sqrt{\frac{(W/L)^2_{m2B}}{(W/L)^2_{m2A}}} = \frac{W/L_{m2B}}{W/L_{m2A}} = \frac{1}{N} = \frac{1}{MN} \] (2.25)

### 2.4.2 Tow-Thomas, Gm-C Biquad Filter

For a better understanding of the Tow-Thomas Biquad configuration a variation is shown in Figure 2.10. This configuration can be used as a low-pass or bandpass filter depending on where the output is taken from. The 2\textsuperscript{nd}-order low-pass transfer function is given by Equation 2.26 and the 2\textsuperscript{nd}-order band-pass transfer function is given by Equation 2.27. Where in both equations the natural frequency is \( \omega_0 = 1/\sqrt{R_2 R_4 C_1 C_2} \) and the quality factor \( Q = \sqrt{\frac{R_2 C_1}{R_3 R_4 C_2}} \).

\[ H_{LPF}(s) = -\frac{R_2}{R_1} \times \frac{\omega_0^2}{s^2 + \frac{\omega_0^2}{Q} s + \omega_0^2} \] (2.26)

\[ H_{BPF}(s) = -\frac{R_3}{R_1} \times \frac{\omega_0^2}{s^2 + \frac{\omega_0^2}{Q} s + \omega_0^2} \] (2.27)

![Figure 2.10: Basic Tow-Thomas based architecture.](image)

The authors of [11] utilize a \( G_m - C \) biquad filter with Tow-Thomas configuration, represented in Figure 2.11. The same OTA schematic was used for OTAs 1 to 4. For the low frequencies desired, the \( G_m - C \) filter is preferred over the switched capacitor due to the leakage issue. The OTA topology permits an increase in gain without more power consumption. The transconductance of the OTA is linearly dependent on the current, this allows for an almost linear control over the cut-off frequency. A Tow-Thomas biquad structure is selected due to the ease of cascading and due to this structure gives a second order low-pass filter and a second order band-pass in the outputs of OTA3. The \( f_c \) of this OTA is given by Equation 2.28, as the equation demonstrates the \( f_c \) is directly related to \( G_m \).
transconductance of the OTA. The $G_m$ can be determined by Equation 2.29, where $M$ is the number of transistors in series and $N$ the number in parallel. Furthermore, $g_m$, in the subthreshold region, $g_m$ can be approximated by Equation 2.30, where $U_t$ is the thermal voltage, giving the dependence on $I_{BIAS}$ of $f_c$. Finally, the transfer function of the biquad filter is given by Equation 2.31 [11], where $g_{m1}$ to $g_{m4}$ are the transconductance of OTA1 to OTA4, respectively, and $C_1$ and $C_2$ are the capacitors represented in Figure 2.11.

![Figure 2.11: Fully differential Tow-Thomas based architecture.](image)

\[ f_c = \frac{G_m}{2\pi C} \quad (2.28) \]

\[ G_m = \frac{g_m}{MN} \quad (2.29) \]

\[ g_m \approx \frac{I_D}{2U_t} \quad (2.30) \]

\[ H_{LP}(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{g_{m1} g_{m4}}{g_{m3} g_{m4} s^2 + s \left( \frac{g_{m2}}{C_1} \right) + \frac{g_{m3} g_{m4}}{C_1 C_2}} \quad (2.31) \]

### 2.4.3 Band-pass Filter using Switched-Capacitors

A band-pass filter can be implemented in biomedical systems since it is able to reject very low frequency noise, offering the same benefits of the Tow-Thomas configuration band-pass output. The filter implemented in [12] is a tunable band-pass filter, using a SC with a two-stage series to parallel topology, in substitution of the large resistor observable in Figure 2.12. A large resistor implemented in technology would result in an impractical surface area used to design it, the switched-capacitor technique uses periodic switching of the connections of on-chip and small-valued capacitors to substitute very high resistances, it can be designed to minimize on-chip area. The equivalent resistance is given by Equation 2.32, where the $k$ is the number of stages of capacitor pairs. However, due to leakage and
parasitic capacitance, only gigaohm resistance can be achieved. As such, the n-stage resistor ladder technology is used to implement the teraohm equivalent resistor, the new resistance value is defined in Equation 2.33, a teraohm resistance can be obtained with only two or three stages. As a result the lower corner frequency is given by Equation 2.34 [12]. The authors of [12] use the topology shown in Figure 2.12, choosing $f_s = 1$ kHz, $n = 2$, $C_1 = 25$ fF, $C_2 = 75$ fF, and with $C_{fb} = 1$ pF to obtain a low corner frequency of approximately 0.25 Hz. The authors of [13] use the same topology, choosing $f_s = 1$ kHz, to obtain a low corner frequency of 0.01 Hz and a high corner frequency of 309 kHz. This circuit is most useful when very low corner frequencies are desired.

Figure 2.12: Bandpass filter with Switched-Capacitor.

$$R = \frac{k(k^2C_1 + C_2)}{f SC_1C_2}$$  
(2.32)

$$R = \left(1 + \frac{C_2}{C_1}\right)^n \frac{1}{f SC_1}$$  
(2.33)

$$f_{\text{lower}} = \frac{f SC_1}{2\pi C_{fb}(1 + C_2/C_1)^n}$$  
(2.34)

### 2.4.4 Low-Pass Butterworth Filter using Ladder Topology

The goal of the works [14] and [15] was to develop a low-pass OTA-C filter to be implemented in a portable Electrocardiography (ECG) detector. The authors opted for a 5th-order ladder-type low-pass Butterworth, with the objective of reducing the influence of sensitivity and decreasing distortion to the bio-signal. The circuit was developed in 0.18 µm CMOS technology, operating in the subthreshold region in order to save power. According to [16], the ladder type is inherently insensitive to component
variations, as such, a better topology for high-order filters. The authors of [14] and [15] both used the topology shown in Figure 2.13, where the resistors and inductors of the LPF are replaced by an OTA, based on their functions [17]. The grounded resistors are replaced by OTA2 and OTA7 and the inductors are replaced by two gyrators. The OTA’s utilize current division transistors $M_M$ and current cancellation transistors $M_N$. The transistor represented by $M_R$ is a source-degeneration, included to improve linearity. The value of $G_m$ for this OTA is given by Equation 2.35, where $G_S$ is the admittance of the source of the input stage and is equal to $(1 + N + M)g_m$ and $g_{o,M_R}$ is the small signal drain-source transconductance of $M_R$. To realize a very small transconductance, by looking to Equation 2.35, the denominator must be designed to be much larger than the denominator and the dimension and channel current can also be designed so that $g_m >> g_{o,M_R}$, this way $G_m$ can be approximated by Equation 2.36.

![Figure 2.13: 5th order Butterworth with ladder topology.](image)

$$G_m = \frac{i_{out}}{v_{in}} = \frac{1 - N}{1 + N + M} \times \frac{G_S}{1 + G_S/g_{o,M_R}}$$ (2.35)

$$G_m = \frac{i_{out}}{v_{in}} = \frac{1 - N}{1 + N + M} \times g_{o,M_R}$$ (2.36)

### 2.4.5 Buffer-Based Biquadratic Cell

Paper [18] presents the development of a compact power efficient CMOS buffer to operate as a nano power low-pass biquadratic cell. This biquad obtains a $\approx 0 \text{ dB}$ passband gain without gain compensation. It is beneficial for the accomplishment of a cascade higher order LPF since it acquires the same levels of input and output $v_{cm}$. The biquadratic cell developed was adapted from [19], as Figure 2.14 shows each cell of the filter contains three Metal–Oxide–Semiconductor Field-effect Transistors (MOSFETs) and two capacitors. Transistors P1 and P2 and the current source $2I_B$ form a source coupled pair, that functions as a transconductor. The active load is transistor N1 and current source $I_B$, $I_B$ guaranties a large resistance necessary to established the DC current bias condition of the transconductor, while
N1 acts as an inverting transconductor. C1 and C2 provide the dynamics to create a 2\textsuperscript{nd}-order transfer function. The biquad’s transfer function as shown in Equation 2.37 conveys a second order low-pass characteristic. The DC gain is 1, the natural frequency is given by Equation 2.38 and the quality factor by Equation 2.39. From these equations, it’s concluded that the natural frequency can be tuned by adjusting $I_{BIAS}$. The parameters of the biquad filter shown in Figure 2.14 are presented in Table 2.1. The parameters have been optimized to obtain a flat passband response and maintain signal swing within the low internal nodes and so maximizing the filter’s linear range [20]. As such, the authors of this article managed to obtain a 100 Hz bandwidth, a gain of -0.05 dB and an output noise measured at 80.5 $\mu$V\textsubscript{rms}, all with a $V_{DD}$ of 0.9 V and total input power of 4.26 nW.

$$H(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{\frac{g_{mA}g_{mB}}{C_1C_2}}{s^2 + \left(\frac{1}{C_1C_2}\right) + \frac{g_{mB}g_{mA}}{C_1C_2}}$$ \hspace{1cm} (2.37)

$$\omega_C = \sqrt{\frac{g_{mA}g_{mB}}{C_1C_2}} = \frac{I_B}{U_T} \times \sqrt{\frac{1}{2n_mn_pC_1C_2}}$$ \hspace{1cm} (2.38)

$$Q = \sqrt{\frac{g_{mA}C_2}{g_{mB}C_1}} = \sqrt{\frac{n_mC_2}{2n_pC_1}}$$ \hspace{1cm} (2.39)

### Table 2.1: Parameters for the proposed Biquad filter.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$V_{DD}$ [V]</th>
<th>$I_B$ [pA]</th>
<th>Power [nW]</th>
<th>$f_C$ [Hz]</th>
<th>$g_{mA}, g_{mB}$ [nS]</th>
<th>$C_1, C_2/2$ [pF]</th>
<th>Quality factor (Q)</th>
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<tr>
<td>Biquad1</td>
<td>0.9</td>
<td>430</td>
<td>1.548</td>
<td>100</td>
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<td>17, 13.5</td>
<td>0.7</td>
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<tr>
<td>Biquad2</td>
<td>0.9</td>
<td>430</td>
<td>1.548</td>
<td>100</td>
<td>11.7, 13.3</td>
<td>7, 11</td>
<td>1.2</td>
</tr>
</tbody>
</table>
2.4.6 Subthreshold-Source-Follower

Paper [21] proposes a Subthreshold-Source-Follower (SSF) Biquad, it provides some beneficial characteristics such as the small number of active components reducing the noise and improving linearity, no feedback and ease of cascading. A Gain-compensation (GC) scheme is implemented to compensate for the gain-loss problem of NMOS-based SSF Biquad. For testing this technology, a 4th-order Butterworth LPF was fabricated. In Figure 2.15, on the left side, the GC comes from the cross coupled differential pair \( P_p \). The resistor \( R_{\text{deg}} \) is used as a source-degenerator and serves to influence the gain-linearity trade off. The ideal parameters for the Biquad are given by Equation 2.40 and Equation 2.41. The transfer function of the circuit is given by Equation 2.42, where \( g_{mc} = g_{mp} / (1 + g_{mp} R_{\text{deg}}) \), reducing the current through \( N_1 \) the cut-off frequency is also reduced. For the LPF design, it is necessary a cascade of two SSF Biquads a NMOS-based and a PMOS-based, to match their \( V_{\text{BIAS}} \). Since the body effect is avoided in the PMOS-based Biquad, there’s no need for GC. For the best optimization, the capacitors of the first stage are to be large in order to reduce noise and the capacitors of the second stage are to be optimized for low distortion. The total capacitance is of 59.2 pF. The LPF draws 15 nW at 3 V and manages a bandwidth of 100 Hz, a gain of 0 dB and an output noise of 29 \( \mu \text{V}_{\text{rms}} \).

\[
\omega_0 = \sqrt{\frac{g_{mN_1}g_{mN_2}}{C_1C_2}} \tag{2.40}
\]

\[
Q = \frac{g_{mp}}{1 + g_{mp} R_{\text{deg}}} \tag{2.41}
\]

\[
H(s) = \frac{v_{\text{out}}(s)}{v_{\text{in}}(s)} = \frac{(g_{mN_1} + g_{mN_2})g_{mN_2}}{s^2 + s\left(\frac{C_1g_{mN_1} + C_2(g_{mN_1} - g_{mN_2})}{C_1C_2} + \frac{g_{mN_1}g_{mN_2}}{C_1C_2}\right)} \tag{2.42}
\]

Figure 2.15: 4th-order GC LPF using SSF Biquads.
2.5 Related Work Summary

The work [8] presented a low cut-off frequency and the topology was specifically designed to attenuate the effect of ground-noise in the frequency response and a zero DC gain.

The authors of the work [11] implemented a Biquad filter with a Tow-Thomas approximation. This type of topology does not suffer from the same leakage problem of the SC topology. Furthermore, this topology has two different outputs depending on the OTA used as an output, which can give more options in the type of selectivity desired, also the cut-off frequency is easily adjusted to the pretended value just by adjusting the bias current.

The use of SC techniques [12, 13] can be suitable for medical applications, alongside many other CMOS technologies. For low frequencies among the active filters, $G_m - C$ filters are preferred since they do not suffer from the leakage problem of the SC filters. SC also occupies a much larger area compared to the $G_m - C$ filters, because of the passive components, usually requires more power.

The works presented in [14, 15] are developed around the technique of a fifth-order Butterworth approximation, where the typical inductors present are substituted by gyrators and the grounded resistors by OTA, this way it is able to reduce the area necessary to implement this filter.

The authors of work [18] designed a buffer-based biquadratic cell this developed filter manages to obtain an approximately 0 dB DC gain without gain compensation. The combination of a transductor and an inverting transconductor with the capacitors $C_1$ and $C_2$ allows this filter to designed with the same level of input and output common-mode voltage, meaning a DC gain of 1.

Table 2.2: Comparative analyses with relevant work.

<table>
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<th>Factor</th>
<th>[8]</th>
<th>[11]</th>
<th>[12]</th>
<th>[13]</th>
<th>[14]</th>
<th>[15]</th>
<th>[16]</th>
<th>[17]</th>
<th>[18]</th>
<th>[21]</th>
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<td>SC</td>
<td>Butterworth</td>
<td>SC</td>
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<td>2013</td>
<td>2013</td>
<td>2015</td>
<td>-</td>
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</tr>
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<td>0.18</td>
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<td>0.35</td>
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<td>0.35</td>
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<td>0.015</td>
<td>0.1134</td>
<td>&lt; 1</td>
<td></td>
</tr>
<tr>
<td>Cut-off Frequency [Hz]</td>
<td>3.44</td>
<td>52</td>
<td>0.3 - 270</td>
<td>0.01 - 308</td>
<td>250</td>
<td>243</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>50/60</td>
<td>0.01 - 2000</td>
<td></td>
</tr>
<tr>
<td>Gain [dB]</td>
<td>0</td>
<td>6</td>
<td>36.7</td>
<td>62.3</td>
<td>-10</td>
<td>-4</td>
<td>-0.05</td>
<td>-4</td>
<td>0</td>
<td>153</td>
<td>&gt; 0</td>
<td></td>
</tr>
<tr>
<td>Noise [µVrms]</td>
<td>-</td>
<td>24.4</td>
<td>17.5</td>
<td>-</td>
<td>340</td>
<td>-</td>
<td>80.5</td>
<td>36</td>
<td>29</td>
<td>-</td>
<td>&lt; 50</td>
<td></td>
</tr>
<tr>
<td>THD [dB]</td>
<td>-</td>
<td>-40</td>
<td>-</td>
<td>-</td>
<td>48.6</td>
<td>-40</td>
<td>-50</td>
<td>-55</td>
<td>-61</td>
<td>-</td>
<td>&lt; 60</td>
<td></td>
</tr>
</tbody>
</table>

The work developed in paper [21] presents a Biquad with SSF, that with a small number of active components allows for a small area and ease of cascading. This topology presents a GC technique to compensate for the gain loss associated with this type of filter, this technique comes from the cross-coupled differential pair.

The authors of [22] designed a notch filter in order to attenuate the noise coming from the power-lines 50 Hz or 60 Hz, which are a major source of noise in low frequency applications, the technique used is based on current-cancellation, where in the elliptic filter designed is composed of OTA and capacitors.
3

Circuit Topology

Contents

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3.3 Current-Mirroring Factor H ............................................. 32
Circuit Topology

The proposed LPF topology chosen for this work is presented in Figure 3.1, it is a biquad filter with a 2\textsuperscript{nd}-order Tow-Thomas configuration. The OTA\textsubscript{1} has an innovative topology designed to improve DC gain, presented in Figure 3.3b, while OTAs 2 to 4 are in current biased configuration, presented in Figure 3.4. This OTA will provide a gain enhancement of the overall circuit without a penalty in power consumption. The biquad structure allows to obtain a higher order filter, a more selective filter, just by cascading the structure. Moreover, it is able to provide low-pass characteristics and also band-pass at the output of the third and forth OTAs, respectively. This paper [1] presents a gain enhancing technique without the need for cascading, positive-feedback or feed-forward techniques.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig3.1.png}
\caption{Proposed Filter Topology.}
\end{figure}

The design of OTA\textsubscript{1} is based on VCs, which are simply a N-type Metal-Oxide Semiconductor (NMOS) in common-drain configuration and an NMOS in common-source configuration as Figure 3.2 shows. The transfer function of this circuit was extracted using SapWin [23], for better comprehensibility, some aspects were simplified, and is presented in Equation 3.1, where $g_{dsA+B} = g_{dsA} + g_{dsB}$ and $c_{dbA+B} = c_{dbA} + c_{dbB}$. From this transfer function is is possible to obtain the DC gain expression that is presented in Equation 3.2. Considering a $g_{mA}$ and $g_{mB} \gg g_{dsA+B}$ Equation 3.2 can be approximated.

\begin{equation}
H(s) = \frac{g_{mB} + g_{mA} + (c_{gsA} - c_{gdB}) \times s}{g_{mA} + g_{dsA+B} + (c_{dbA+B} + c_{gsA} + c_{gdB}) \times s}
\end{equation}
\[ A_{VC} = \frac{g_{mA} + g_{mB}}{g_{mA} + g_{dsA} + g_{mB}} \approx 1 + \frac{g_{mB}}{g_{mA}}, |A_{VC}| > 1 \]  

(3.2)

**Figure 3.2:** Voltage-combiner circuit.

The OTA presented in Figure 3.3a is composed of an a differential-pair (E and F), two P-type Metal-Oxide Semiconductor (PMOS) basic current-mirrors (A, B and C, D) and an NMOS current mirror (K, L). The innovation in this circuit is the fact that the typical NMOS current-source that biases the differential-pair has been substituted by two VCs in a cross coupled configuration (G, I and H, J). The authors managed to obtain a gain of 47 dB and a GBW of 170.6 MHz with a \( I_{DD} \) of 1 mA and a load of 6 pF all in 130 nm technology. By observing Equation 3.2 an additional 6 dB gain is easily obtained by sizing the circuit so that \( g_{mA} \approx g_{mB} \).

**Figure 3.3:** Studied OTA, proposed implementation and VC circuit.
Following the VCs biased OTA, in the schematic, three identical DC current biased OTAs are implemented. These OTAs allow a further control of the $f_c$, since the transconductance present in the pole of the transfer function is dependent on the drain current applied. The circuit is designed for Electrooculography (EOG) and Electromyography (EMG) signals, that have low frequency, then a very low power implementation is further needed to keep the drain current and consequently the $f_c$ low. The schematic of OTAs 2 to 4 is shown in Figure 3.4.

![Figure 3.4: Current biased OTA.](image)

The varactor structure, represented in Figure 3.1 by $C_1$ and $C_2$, allow for a tuning of $f_c$, by representing a significant capacitance that moves the pole in the transfer equation. A single MOSFET can be used to implement a varactor by connecting the drain, source and bulk to a single DC voltage source, while the gate is connected where the capacitance is to be applied. The varactor’s capacitance is given by Equation 3.3 [24], where $\epsilon_{ox}$ is the electron mobility, $t_{ox}$ is the oxide thickness and $S$ is the transistor’s channel area. $\epsilon_{ox}$ is dependent on $V_{CTRL}$, the voltage applied between the gate and bulk/drain/source, therefore the capacitance is adjustable as needed.

$$C_{MOS} = C \times S = \frac{\epsilon_{ox}}{t_{ox}} \times S$$ (3.3)
3.1 Biasing Strategy

This section presents the biasing strategy of the OTAs that make up the filter. The biasing strategies developed for the VCs biased OTA and the current biased OTA are depicted in Figure 3.5a and Figure 3.5b, respectively. Some considerations taken into account while developing the biasing strategy are to have the transistors in the saturation region, preferably in the weak to moderate inversion, if possible. The $V_{DS}$ of the NMOS N7 (or $V_{SD}$ of the PMOS P1 around 700 mV) in the output branch is dimensioned to be around 500 mV, because the OTAs are connected to each other.

![Biasing strategy](image)

Figure 3.5: Biasing strategy.

3.2 Small-signal Equivalent Circuit

In this section the small-signal equivalent circuits of the components of the filter are presented along with the gain and transconductance equations.

3.2.1 Voltage-Combiners

The small signal equivalent circuit of the VCs is presented in Figure 3.6, both the $v_{out}$ and gain expressions are presented in Equation 3.4.

\[
v_{out} = \frac{v_{in}g_{mCS} + v_{in}g_{mCD}}{r_{oCS} + r_{oCD} + g_{mCS}}
\]

\[
Av_{VCs} = \frac{v_{out}}{v_{in}} = \frac{g_{mCS} + g_{mCD}}{r_{oCS} + r_{oCD} + g_{mCS}}
\]
3.2.2 Current Biased OTA

The small-signal equivalent circuit of the current biased OTA is presented in Figure 3.7, to obtain this circuit the Bartlett’s bisection theorem [25] was applied. Through the circuit it is possible to determine both the transconductance, in Equation 3.5, and the gain, in Equation 3.6.

\[ v_{in} = v_{gsP3} \]

\[ v_A = -g_{mP3} \times \left( r_{oP3} / g_{mN6} \right) = v_{gsN1} = ... = v_{gsN5} \]

\[ i_{out} = -g_{mN5} \times v_A \]

\[ G_m = \frac{i_{out}}{v_{in}} = g_{mN5} \times g_{mP3} \times \left( r_{oP3} / g_{mN6} \right) \]

\[ v_{out} = B \times v_{in} \times g_{mN5} \times g_{mP3} \times \left( r_{oP3} / g_{mN6} \right) \times \left( r_{oP1} / r_{oN7} \right) \]

\[ Av = \frac{v_{out}}{v_{in}} = B \times g_{mN5} \times g_{mP3} \times \left( r_{oP3} / g_{mN6} \right) \times \left( r_{oP1} / r_{oN7} \right) \]
3.2.3 VCs Biased OTA

The transconductance of the VCs biased OTA can be obtained through the combination of the calculations done for the VCs and for the current biased OTA. As such, the result is based on the transconductance and gain of the OTA with the added gain provided by the VCs, as demonstrated in Equation 3.7, for the transconductance, and Equation 3.8, for the gain.

\[ G_m = \frac{i_{out}}{v_{in}} = g_{mN5} \times g_{mP3} \times (\frac{r_{oP3}}{g_{mN6}})(1 + A_{VCs}) \]  

(3.7)

\[ Av = \frac{v_{out}}{v_{in}} = B \times g_{mN5} \times g_{mP3} \times (\frac{r_{oP3}}{g_{mN6}}) \times (\frac{r_{oP1}}{r_{oN7}})(1 + A_{VCs}) \]  

(3.8)

3.3 Current-Mirroring Factor H

In MOSFET based current sources, like the basic PMOS current mirror shown in Figure 3.8, all the transistors must operate in the saturation region, P1 due to the drain-gate connection always has \( V_{SD} = V_{SD} \), therefore, verifying the saturation condition. By analysing the circuit it is verifiable that \( I_{D1} = I_{REF}, I_{D2} = I_{OUT1} \) and \( V_{SG1} = V_{SG2} \) and obtain the relation in Equation 3.9. This process, in an ideal environment, can be repeated indefinitely, as shown by transistor P3.

\[ H = \frac{I_{OUT}}{I_{REF}} = \frac{W_2}{L_2} \left( V_{SG2} - V_{TH} \right)^2 = \frac{W_2}{L_2} \]  

\[ = \frac{W_1}{L_1} \]  

(3.9)

Figure 3.8: Current-mirror factor H.
Implementation and Simulations

Results

Contents

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Implementation and Simulations

Results

This chapter presents the design stages of the filter from the biasing and sizing to design the layout in the Cadence software. First, in section 4.1 a polarization strategy was defined for both OTAs. In section 4.2, the strategy to increase the filter’s gain is presented and the steps to tune the filter’s cut-off frequency are explained. In section 4.3 the schematics, sizing and the transistor’s working region are shown and in section 4.4 the filter’s and OTAs’ simulations and test-benches are described. In section 4.5 the results obtained are presented in comparison with the specified parameters. Finally, in section 4.6 the circuits at a layout level and the post-extraction simulations are presented.

4.1 OTAs DC Biasing

This section presents the final biasing of the OTAs that makes up the filter. The biasing developed for the VCs biased OTA and the current biased OTA are presented in Table 4.1 and Table 4.2, respectively. These results show the DC voltage parameters and current present in all transistors that make up both OTAs.

To extract the values a DC simulation is done with both inputs having a DC bias voltage of 500 mV, this value derives from the DC voltage output of the low-noise amplifier that precedes the filter in the monitoring system and from the connections between each other when assembled in the filter keeping the DC offset along the circuit. Observing the tables and the values of $V_{DS}$ for N7 (501.553 mV) and $V_{SD}$ for P1 (698.447 mV), for both OTAs, the DC offset is balanced throughout the circuit. Most of the transistors operate in the subthreshold region, but none reach the triode or breakdown regions.
Table 4.1: VCs Biased OTA biasing.

<table>
<thead>
<tr>
<th></th>
<th>$V_{DS}$ [mV]</th>
<th>$V_{GS}$ [mV]</th>
<th>$V_{TH}$ [mV]</th>
<th>$V_{DSAT}$ [mV]</th>
<th>$I_D[nA]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCS</td>
<td>367.2</td>
<td>700.0</td>
<td>241.6</td>
<td>356.9</td>
<td>221.5</td>
</tr>
<tr>
<td>PCD</td>
<td>832.8</td>
<td>332.8</td>
<td>318.6</td>
<td>66.1</td>
<td>95.9</td>
</tr>
<tr>
<td>P1</td>
<td>698.5</td>
<td>100.3</td>
<td>250.7</td>
<td>36.7</td>
<td>2.4</td>
</tr>
<tr>
<td>P2</td>
<td>100.3</td>
<td>100.3</td>
<td>249.8</td>
<td>36.6</td>
<td>1.1</td>
</tr>
<tr>
<td>P3</td>
<td>772.8</td>
<td>332.8</td>
<td>318.3</td>
<td>65.6</td>
<td>125.6</td>
</tr>
<tr>
<td>N1</td>
<td>1.0 V</td>
<td>13.8</td>
<td>252.1</td>
<td>43.1</td>
<td>1.1</td>
</tr>
<tr>
<td>N2</td>
<td>20.2</td>
<td>34.0</td>
<td>249.5</td>
<td>43.0</td>
<td>1.1</td>
</tr>
<tr>
<td>N3</td>
<td>11.5</td>
<td>45.5</td>
<td>247.9</td>
<td>43.0</td>
<td>1.1</td>
</tr>
<tr>
<td>N4</td>
<td>8.1</td>
<td>53.6</td>
<td>246.8</td>
<td>43.0</td>
<td>1.1</td>
</tr>
<tr>
<td>N5</td>
<td>6.2</td>
<td>59.9</td>
<td>245.9</td>
<td>43.0</td>
<td>1.1</td>
</tr>
<tr>
<td>N6</td>
<td>59.9</td>
<td>59.9</td>
<td>214.8</td>
<td>43.0</td>
<td>125.6</td>
</tr>
<tr>
<td>N7</td>
<td>501.5</td>
<td>59.9</td>
<td>223.5</td>
<td>42.5</td>
<td>2.3</td>
</tr>
</tbody>
</table>

Table 4.2: Current Biased OTA biasing.

<table>
<thead>
<tr>
<th></th>
<th>$V_{DS}$ [mV]</th>
<th>$V_{GS}$ [mV]</th>
<th>$V_{TH}$ [mV]</th>
<th>$V_{DSAT}$ [mV]</th>
<th>$I_D[pA]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>698.4</td>
<td>75.1</td>
<td>250.5</td>
<td>36.3</td>
<td>1.0 nA</td>
</tr>
<tr>
<td>P2</td>
<td>75.1</td>
<td>75.1</td>
<td>249.7</td>
<td>36.2</td>
<td>494.4</td>
</tr>
<tr>
<td>P3</td>
<td>763.3</td>
<td>298.2</td>
<td>323.8</td>
<td>51.9</td>
<td>49.7 nA</td>
</tr>
<tr>
<td>N1</td>
<td>1.1 V</td>
<td>9.4</td>
<td>252.0</td>
<td>43.0</td>
<td>494.4</td>
</tr>
<tr>
<td>N2</td>
<td>20.1</td>
<td>10.7</td>
<td>249.4</td>
<td>42.9</td>
<td>494.4</td>
</tr>
<tr>
<td>N3</td>
<td>11.4</td>
<td>22.2</td>
<td>247.9</td>
<td>42.9</td>
<td>494.4</td>
</tr>
<tr>
<td>N4</td>
<td>8.0</td>
<td>30.2</td>
<td>246.8</td>
<td>42.9</td>
<td>494.4</td>
</tr>
<tr>
<td>N5</td>
<td>6.2</td>
<td>36.5</td>
<td>245.9</td>
<td>42.9</td>
<td>494.4</td>
</tr>
<tr>
<td>N6</td>
<td>36.5</td>
<td>36.5</td>
<td>241.8</td>
<td>42.9</td>
<td>49.7 nA</td>
</tr>
<tr>
<td>N7</td>
<td>501.5</td>
<td>36.5</td>
<td>223.4</td>
<td>42.3</td>
<td>1.0 nA</td>
</tr>
</tbody>
</table>
4.2 Increase Gain and Tune Cut-off Frequency

The gain of the filter depends heavily on the proposed OTA, since the current biased OTA contributes only with a slight decrease in gain. The proposed OTA gain is given by Equation 4.1, where \( B \) is given by the ratio of widths of transistors N6 and N5 \( (W_{N6}/W_{N5}) \). The VCs gain equation can be simplified as Equation 4.2, the transconductances \( g_{mP3}, g_{mCS} \) and \( g_{mCD} \) is given by Equation 2.17, and finally \( g_{ds_{out}} \) is given by Equation 4.3.

Taking into consideration that the transistors drain current, in the saturation region, is given by Equation 4.4 the strategy to increase the gain to the desired value is to adjust the width and length of the transistors to increase or decrease the drain current as necessary according to the previously shown equations. As a start-off point the ratio \( W/L \) of the transistor \( P_{CS} \) is designed to be greater than the ratio of \( P_{CD} \) in order to have \( g_{mCS} \) greater than \( g_{mCD} \) and increase \( Av_{VC} \). The transconductance of transistor \( P_{3} \) is increased as the gain equation shows. The value of \( B \) is increased by maintaining the same length in both transistors involved in the current mirror and increasing the width of \( N_{6} \) to 45 \( \mu m \) keeping the width of \( N_{5} \) at 1 \( \mu m \). And finally, the current in the output branch is kept at a minimum to keep \( g_{ds_{out}} \) low and not decrease the gain.

\[
Av = \frac{Bg_{mP3}(1 + Av_{VC})}{g_{ds_{out}}} \tag{4.1}
\]

\[
Av_{VC} = 1 + \frac{g_{mCS}}{g_{mCD}} \tag{4.2}
\]

\[
g_{ds_{out}} = \frac{1}{\lambda I_{D}} \tag{4.3}
\]

\[
I_{D} = \frac{1}{2}\mu pC_{ox} \frac{W}{L}(V_{GS} - V_{th})^{2} \tag{4.4}
\]

The filter’s cut-off frequency is adjusted to the desired value using the tuning methods available. Firstly, the cut-off frequency can be derived as Equation 4.5, from the transfer function and relating with the known transfer function of a 2\(^{nd}\)-order LPF. By observing the equation, the OTAs bias current allows for a fine adjustment of \( f_{c} \), by controlling the transconductance of OTAs 3 and 4. The transconductance is already low from the MN structure. Using the varactor structure, \( C_{1} \) and \( C_{2} \) represent significant capacitances, a broader tuning is possible.

\[
\omega_{0}^{2} = \frac{g_{m3}g_{m4}}{C_{1}C_{2}} \tag{4.5}
\]
4.3 Cadence Schematic Implementation

In this section, it is shown the filter’s components sizing and schematics. All the components are
designed with 130 nm technology and are built with PMOS transistors P_{12 \text{HSL130E}} and NMOS tran-
sistors N_{12 \text{HSL130E}}. The components’ biasing region is also presented and the description of the
numbers used is shown on Table 4.3, which are obtained via DC simulation on the Cadence program.

<table>
<thead>
<tr>
<th>Region</th>
<th>Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Cut-off</td>
</tr>
<tr>
<td>1</td>
<td>Triode</td>
</tr>
<tr>
<td>2</td>
<td>Saturation</td>
</tr>
<tr>
<td>3</td>
<td>Subthreshold</td>
</tr>
<tr>
<td>4</td>
<td>Breakdown</td>
</tr>
</tbody>
</table>

4.3.1 Schematic and Sizing of VCs Biased OTA

The electric schematic is presented in Figure 4.1 and the size of the transistors that make the OTA are
presented in Table 4.4. After obtaining the desired gain value some transistors are in the subthreshold
or weak-inversion region, but are in the border of the region closer to saturation and as such still work
as being in the saturation region, meaning assemblies such as the current mirror work as intended.

<table>
<thead>
<tr>
<th>Device</th>
<th>$P_{CS}$</th>
<th>$P_{CD}$</th>
<th>$P_1$</th>
<th>$P_2$</th>
<th>$P_3$</th>
<th>$N_1$</th>
<th>$N_2$</th>
<th>$N_3$</th>
<th>$N_4$</th>
<th>$N_5$</th>
<th>$N_6$</th>
<th>$N_7$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W [\mu m]$</td>
<td>0.25</td>
<td>1.4</td>
<td>4.33</td>
<td>2</td>
<td>3.5</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>45</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>$L [\mu m]$</td>
<td>9</td>
<td>1.8</td>
<td>3</td>
<td>3</td>
<td>3.5</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>8</td>
</tr>
<tr>
<td>Region</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>
4.3.2 Schematic and Sizing of Current Biased OTA

The electric schematic is presented in Figure 4.2 and the size of the transistors that make the OTA are presented in Table 4.5. The transistors present in this OTA work as intended although they are in the subthreshold or weak inversion region because they are also in the border between the regions.

Table 4.5: Sizing and working regions of the current biased OTA transistors devices.

<table>
<thead>
<tr>
<th>Device</th>
<th>$P_1$</th>
<th>$P_2$</th>
<th>$P_3$</th>
<th>$N_1$</th>
<th>$N_2$</th>
<th>$N_3$</th>
<th>$N_4$</th>
<th>$N_5$</th>
<th>$N_6$</th>
<th>$N_7$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W \ [\mu m]$</td>
<td>4</td>
<td>2</td>
<td>3.5</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>45</td>
<td>4</td>
</tr>
<tr>
<td>$L \ [\mu m]$</td>
<td>3</td>
<td>3</td>
<td>3.5</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>8.58</td>
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<tr>
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<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>
4.3.3 Schematic and Sizing of Varactor

The electric schematic is presented in Figure 4.3a where the drain, source and bulk are connected to achieve higher capacitance and lower the cut-off frequency. The size and working region of the transistors that make the Varactor structure are presented in Table 4.6.

![Varactor schematic and testing bench.](image)

(a) Varactors C1 and C2 cadence schematic.  
(b) Test-bench for varactor’s capacitance.

Table 4.6: Sizing of the Varactor devices.

<table>
<thead>
<tr>
<th>Device</th>
<th>W [µm]</th>
<th>L [µm]</th>
<th>Region</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_1$</td>
<td>20</td>
<td>20</td>
<td>1</td>
</tr>
<tr>
<td>$C_2$</td>
<td>50</td>
<td>50</td>
<td>1</td>
</tr>
</tbody>
</table>
4.4 Test-benches and Simulations

In this section, the filter’s final schematics and test-benches used are presented, along with the test-benches designed to simulate both OTAs. A simulation that presents the varactors’ capacitance dependency on the voltage applied and the transistor’s size is described. The simulations are done for both the low-pass and band-pass outputs and consist of a FFT analysis, where a brief introduction is done to coherent sampling necessary for it, AC simulation and noise analysis of the input referred noise. Just in the case of the filter a PSRR and the variation of the cut-off frequency with the varactors and bias current analysis are done.

4.4.1 Coherent Sampling

For the FFT a coherent sampling is implemented to avoid spectral leakage, meaning that the frequency components of the input signal will be contained at a FFT bin. By following the Equation 4.6, where \( M_{cycles} \) is the number of cycles in the implemented set and \( N_{samples} \) is the number of samples, and starting with a \( f_{in} \), that respects the \( f_c \) of the component, a \( f_s \) of 5 kHz and 4096 samples gives \( M_{cycles} \), this number has to be a prime number, so it is round to the closest prime number. Returning to Equation 4.6 with \( M_{cycles} \) gives the \( f_{in} \) necessary for the coherent sampling. To plot the FFT on the transient responses’ calculator the Discrete Fourier Transform (DFT) function is picked with an interval of 0.8192 s (starting after allowing the signal to stabilize), 4096 samples and a Hamming window.

A window function is a mathematical function that is generally zero outside a chosen interval, this function allows control over the spectral leakage, such as minimize it. The Hamming window has a narrow main lobe and is optimized to minimize the nearest side lobe [26], which is optimal for the EOG and EMG signals, composed of sine waves fairly close in frequency.

\[
\frac{f_{in}}{f_s} = \frac{M_{cycles}}{N_{samples}}
\]

4.4.2 OTA Test-benches and Simulations

The test-bench present in Figure 4.4 is designed to obtain the transient response of both OTAs (the current source is connected in the case of the current biased OTA). From the transient response, it is possible to plot an FFT and determine the THD. In a time-domain simulation, such as this, is done in a closed-loop, so there is negative feedback from the differential outputs to the inputs. The circuit has a unit gain since all resistors (R1 to R4) have a resistance of 1 kΩ. The capacitors represent the capacitance of the circuit the OTA will be connected and all have a capacitance of 500 fF. The voltage sources feed the \( V_{DD} \), the positive input with a 500 mV DC bias voltage and an AC magnitude of 5 mV.
and the negative input with 500 mV bias voltage. The voltage-controlled voltage source has a unit gain and converts the differential output to a single output.

Starting with Equation 4.6 a $f_{in}$ of 9 Hz, that respects the $f_c$ of the OTA, a $f_s$ of 5 kHz and 4096 samples gives $M_{cycles}$ equal to 7.3728. This number has to be a prime number, rounding it gives $M_{cycles}$ equal to 7. Returning to Equation 4.6 with $M_{cycles}$ equal to 7 gives that $f_{in}$ is equal to 8.544921875 Hz. To plot the FFT on the transient responses' calculator the DFT function is picked with an interval from 0.1 s to 0.9192 s, 4096 samples and a Hamming window. The plots are shown in Figure 4.5 and Figure 4.6, for the VCs biased OTA and current biased OTA respectively. Finally the THD of the VCs biased OTA is -58.7 dB and of the current biased OTA is -55.5 dB.

![Test-bench for both OTA’s FFT simulations.](image)

**Figure 4.4:** Test-bench for both OTA’s FFT simulations.

![VCs biased OTA FFT simulation.](image)

**Figure 4.5:** VCs biased OTA FFT simulation.
To analyze the AC output of the OTAs an AC simulation was implemented. This type of simulation corresponds to a linearization around the DC bias point. To obtain this simulation in the input fin+ is applied a 1 V and in input fin- 0 V, because the gain is obtained from a slope calculation of the OTA's outputs. As Equation 4.7 shows it is a ratio of the difference of the outputs over the difference of inputs and having 1 V in the difference of inputs (any relation of x and y whose difference results in 1 V) results the real gain of the circuit. From this simulation results a gain relative to the frequency as well as important frequency parameters, the frequency range is 0.1 Hz to 100 kHz. These simulations are in the frequency domain and done in an open-loop, the capacitors, current source and the voltage-controlled voltage source serve the same purpose. The outputs of the simulation are shown in Figure 4.8 and Figure 4.9 and the significant values represented in Table 4.7, where is significant to refer that the gain of the VCs biased OTA is greater than the current biased OTA.

\[
Gain = \frac{f(y) - f(x)}{y - x}
\]  

(4.7)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Gain [dB]</th>
<th>( f_c ) [Hz]</th>
<th>GBW [kHz]</th>
<th>Phase Margin [°]</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCs</td>
<td>58.62</td>
<td>35.81</td>
<td>29.99</td>
<td>82.47</td>
</tr>
<tr>
<td>Current</td>
<td>57.55</td>
<td>15.21</td>
<td>11.34</td>
<td>84.37</td>
</tr>
</tbody>
</table>

Figure 4.6: Current biased OTA FFT simulation.
Figure 4.7: Test-bench for OTA’s noise and AC simulations.

Figure 4.8: VCs biased OTA gain and phase simulation.

Figure 4.9: Current biased OTA gain and phase simulation.
The noise simulations are executed in the same test-bench and plot the input referred noise of the output in relation to the positive input of the OTA. Maintaining the same frequency sweep the plots are presented in Figure 4.10 and Figure 4.11. For the VCs biased OTA the circuit introduces a flicker noise of 12.99 $\mu V_{rms}$ and a thermal noise of 98.02 $\mu V_{rms}$. For the current biased OTA the circuit introduces a flicker noise of 11.86 $\mu V_{rms}$ and a thermal noise of 99.92 $\mu V_{rms}$.

**Figure 4.10:** VCs biased OTA input referred noise.

**Figure 4.11:** Current biased OTA input referred noise.
4.4.3 Varactor Test-bench and Simulations

The varactor structure represents a capacitance applied to the circuit to adjust the poles of the circuit in the transfer function. To measure the capacitance of the varactor a parametric analysis of the ccg parameter is done in the test-bench present in Figure 4.3b, where a voltage source has a 500 mV DC voltage, that is present in the filter’s circuit, and a second voltage source varies from 0 V to 1.2 V. The results are present in Figure 4.12, where four different combinations of W and L were done (20 µm, 30 µm, 40 µm and 50 µm), to demonstrate the variance of capacitance both with $V_{CTRL}$ and the transistor’s area. As the capacitance equation ($C = \epsilon_0 A/d$), demonstrates the capacitance of the capacitor is directly proportional to the area, the same occurs with the varactor structure and $V_{CTRL}$ allows for control of one order of magnitude of capacitance.

(a) Transistor length and width of 20 µm.

(b) Transistor length and width of 30 µm.

(c) Transistor length and width of 40 µm.

(d) Transistor length and width of 50 µm.

Figure 4.12: Varactor’s capacitance simulation.
4.4.4 Filter Test-Bench and Simulations

The final technology schematic of the LPF is shown in Figure 4.13a, where OTAs are replaced with their symbol equivalents. The schematic presented is then used to form the symbol present in the test-bench shown in Figure 4.13b. The test-bench is composed of two input voltage sources for fin+ and fin-, a voltage source for $V_{DD}$, a fourth one for the $V_{CTRL}$ of the varactors, three current sources to bias the OTAs and finally the outputs for low-pass and band-pass. The inputs for $V_{CTRL}$ and $I_b$ allow to, from the test-bench, tune the cut-off frequency.

![LPF Cadence schematic.](image)

![LPF test-bench schematic.](image)

Figure 4.13: Filter’s Cadence schematic and test-bench.

In this stage of the filter’s schematic design, the technology bias current sources were replaced by PMOS based current-mirrors, the PMOS structures were chosen as the goal of the current-mirrors is to inject current into the circuit. The resulting schematic took into account the need to adjust $f_c$ through $I_{b2}$, as such the final result has two current-mirrors. Both technology current sources need to be replaced. The one biasing $I_{b2}$ by an external potentiometer, that gives the ability to adjust $f_c$, it would be externally
welded to the Printed Circuit Board (PCB). The fixed resistor in the second current-mirror is a precision resistor to not affect the performance of the circuit.

The final step is to determine the value of the potentiometer and resistor, the first step is to determine the voltage in the current sources through a DC analysis and annotating the voltage drop or by calculating the difference of $V_{DD}$ (1.2 V) by $V_{DS, I2}$ (285.555 mV). The voltage value is 914.445 mV and the bias current is 100 nA, and the necessary resistance to force the bias current is given by Ohm’s law and the value is approximately 9.2 MΩ. The final schematic is shown in Figure 4.14a and the respective test-bench in Figure 4.14b. From a DC simulation performed in the test-bench shown below and with $V_{DD}$ and $V_{CTRL}$ with 1.2 V and the current-mirrors designed for 100 nA the circuit drains 787.62 nW.

![Filter's final schematic and test-bench.](image)

Figure 4.14: Filter’s final schematic and test-bench.
For the filter's FFT simulation, contrary to the OTA's, a negative feedback is not implemented on the test-bench because as seen in Figure 4.14b the schematic already has as part of it's circuit assembly. The calculations done for the OTA hold true for the filter's low-pass output, so using $f_{in}$ of 8.544921875 Hz, an interval of 1.1 s to 1.9192 s (for signal stabilization), 4096 samples and a Hamming window the plot is shown in Figure 4.15 and the THD is -54.36 dB. For the band-pass output a new $f_{in}$ has to be determined, since the current is cut by the filter. Using the previous calculations with Equation 4.6, an initial frequency of 430 Hz, $f_s$ of 5 kHz and 4096 samples gives $M_{cycles}$ equal to 352.256 that rounds to a prime number 353 and a $f_{in}$ of 430.908203125 Hz. The band-pass FFT plot is shown in Figure 4.16 and the THD is -48.56 dB.

![Figure 4.15: Filter's low-pass output FFT simulation.](image1)

![Figure 4.16: Filter's band-pass output FFT simulation.](image2)
To analyze the AC output of the filter an AC simulation was implemented. This type of simulation corresponds to a linearization around the DC bias point. To realize this simulation in the input fin+ is applied a 1 V and in input fin- 0 V and the frequency range is 0.1 Hz to 100 kHz. The outputs of the simulation are shown in Figure 4.17 for the low-pass output and Figure 4.18 for the band-pass output. The important parameters of both outputs are presented in Table 4.8.

Table 4.8: Results of low-pass and band-pass AC simulation.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Low-pass</th>
<th>Band-pass</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>Gain [dB]</td>
<td>f_c [Hz]</td>
</tr>
</tbody>
</table>

Figure 4.17: Filter’s low-pass output gain and phase simulation.

Figure 4.18: Filter’s band-pass output gain simulation.
The noise simulations are executed in the same test-bench and plot the input referred noise of the output in relation to the positive input of the filter. Maintaining the same frequency sweep the plots are presented in Figure 4.19 and Figure 4.20. For the low-pass output the circuit introduces a flicker noise of 10.38 $\mu V_{rms}$ and a thermal noise of 28.77 $\mu V_{rms}$. For the band-pass output the circuit introduces a flicker noise of 34.13 $\mu V_{rms}$ and a thermal noise of 75.41 $\mu V_{rms}$.

![Figure 4.19: Filter’s low-pass output input referred noise.](image1)

![Figure 4.20: Filter’s band-pass output input referred noise.](image2)
To test for the circuits PSRR an AC simulation is done with the same test-bench, where the positive input is fin+ with 1 V and the negative input is $V_{DD}$ with 0 V AC magnitudes. Both fin+ and fin- have 500 mV DC voltage to bias the circuit. The simulation sweeps from 1 mHz to 100 kHz and the outputs are presented in Figure 4.21 for the low-pass output and Figure 4.22 for the band-pass output. For the low-pass output removing the circuit’s gain (8.546 dB) gives a PSRR of 149.154 dB and for the band-pass gives a PSRR of 143.267 dB (gain of 8.533 dB).

![AC Response](image)

Figure 4.21: Filter’s low-pass output PSRR.

![AC Response](image)

Figure 4.22: Filter’s band-pass output PSRR.
To illustrate the filter’s variation of the cut-off frequency with $V_{CTRL}$ and $I_{BIAS}$ fixed at 100 nA a parametric analysis was done where a sweep from 0 V to 1.2 V, the results are present in Figure 4.23 for low-pass output and Figure 4.24 for band-pass output. For both outputs the variation of $V_{CTRL}$ has no influence on the gain as it stays the same through the changes. The variation of the cut-off frequency is not linearly dependent on $V_{CTRL}$ as the figures show the lowest cut-off frequency comes from 1.2 V and the highest from 0.6 V. For the low-pass output the lowest cut-off frequency is 55.53 Hz at 1.2 V and the highest is 313.2 Hz at 0.6 V. For the band-pass the lowest cut-off frequency is 8.83 Hz at 1.2 V and the corresponding high cut-off frequency at 2.757 kHz and the highest is 8.094 kHz at 0.6 V with its corresponding low cut-off frequency of 48.8 Hz.

Figure 4.23: Illustration of the tuning capability of the varactors (low-pass).

Figure 4.24: Illustration of the tuning capability of the varactors (band-pass).
To illustrate the filter’s variation of the cut-off frequency with $I_{BIAS}$ and $V_{CTRL}$ fixed at 1.2 V a parametric analysis was done. A sweep of $I_{BIAS}$ is done, from 60.16 nA to 175.85 nA, by sweeping the potentiometer value from 5.2 MΩ to 15.2 MΩ, the results are present in Figure 4.25 for low-pass output and Figure 4.26 for band-pass output. For both outputs the variation of $I_{BIAS}$ has no influence on the gain as it stays the same through the changes. The variation of the cut-off frequency is linearly dependent on $I_{BIAS}$, meaning inversely dependent to the resistance, as the figures show the lowest cut-off frequency comes from 15.2 MΩ and the highest from 5.2 MΩ. For the low-pass output the lowest cut-off frequency is 38.28 Hz and the highest is 92.23 Hz. For the band-pass the high cut-off frequency stays the same at 2.758 kHz, independent of the potentiometer’s resistance, the lowest is 6.03 Hz and the highest of the low cut-off frequency at 14.47 Hz.

Figure 4.25: Illustration of the tuning capability of the bias current (low-pass).

Figure 4.26: Illustration of the tuning capability of the bias current (band-pass).
4.5 Summary

This section presents the final results of the filter where, in general, all the specifications were fulfilled. The type Butterworth and 2\textsuperscript{nd}-order of the filter were defined in the chosen topology. In the case of $V_{DD}$, it had to be adjusted to 1.2 V because the Low-Noise Amplifier (LNA) that precedes it in the whole acquisition system increased it, to achieve all the bias criteria defined for it, and to have continuity in the system the filter adjusted too.

The cut-off frequencies are tuned according to the Electromyography signal with a frequency range of 20 - 2000 Hz that corresponds to the band-pass range of 21.5 to 1135 Hz and Electrooculography signal with DC to 10 Hz in a frequency range that corresponds to the low-pass range of DC to 22.37 Hz. With power consumption below 1 $\mu$W (787.62 nW) both outputs present a gain larger than 0 dB, around 8.5 dB for both. And accomplishing the specifications for noise and PSRR the filter introduces minimum noise to the signal. Finally, having achieved the THD specification it is guarantied that minimum disruption to the signal will occur from the harmonics.

<table>
<thead>
<tr>
<th>Performance Index</th>
<th>Specification</th>
<th>Final</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type of filter</td>
<td>Butterworth</td>
<td>Butterworth</td>
</tr>
<tr>
<td>Order</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>$V_{DD}$ [V]</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td>Power [$\mu$W]</td>
<td>&lt;1</td>
<td>0.78762</td>
</tr>
<tr>
<td>$f_c$ Low-pass [Hz]</td>
<td>20</td>
<td>22.37</td>
</tr>
<tr>
<td>$f_c$ Band-pass [Hz]</td>
<td>20 - 2000</td>
<td>21.5 - 1135</td>
</tr>
<tr>
<td>Gain Low-pass [dB]</td>
<td>$&gt;$0</td>
<td>8.546</td>
</tr>
<tr>
<td>Gain Band-pass [dB]</td>
<td>$&gt;$0</td>
<td>8.533</td>
</tr>
<tr>
<td>Noise Low-pass [$\mu V_{rms}$]</td>
<td>$&lt;$50</td>
<td>10.38 / 28.77</td>
</tr>
<tr>
<td>Noise Band-pass [$\mu V_{rms}$]</td>
<td>$&lt;$50</td>
<td>34.13 / 75.41</td>
</tr>
<tr>
<td>PSRR Low-pass [dB]</td>
<td>Maximum</td>
<td>149.154</td>
</tr>
<tr>
<td>PSRR Band-pass [dB]</td>
<td>Maximum</td>
<td>143.267</td>
</tr>
<tr>
<td>THD Low-pass [dB]</td>
<td>$&lt;$-60</td>
<td>-54.36</td>
</tr>
<tr>
<td>THD Band-pass [dB]</td>
<td>$&lt;$-60</td>
<td>-48.56</td>
</tr>
</tbody>
</table>
4.6 Layout and Post-Layout Simulations

This section presents the layout design of the VCs biased OTA and the current biased OTA post-layout simulations and comparison to the original schematic results, considering both both OTAs FFT, gain and phase and input referred noise simulations. Finally, a gain and phase and input referred noise simulations for both outputs of the filter are presented.

4.6.1 Initial Layout Design Considerations

For the development of the circuit’s layout, some initial considerations were taken to optimize the design and minimize the parasitic capacitances. Firstly, the transistor’s positions were kept symmetric, while grouping the PMOS separately from the NMOS. The disposition is similar to the schematic, done to minimize area and the length and number of paths. The rooting is designed to minimize overlaps between paths and not overlap with transistors. For the rooting, the width and area of the paths are kept almost all at value orders of magnitude above the minimum. To minimize parasitic capacitances the connections to \( V_{DD} \) are done with M2 metal, connections to \( gnd \) with metal M1 and connections between transistors metal M3 and above. To minimize the resistance and prevent complications from manufacturing several contacts are used. Finally, to improve short-circuit protection two rings are implemented around the transistors.

4.6.2 VCs Biased OTA Layout

In Figure 4.30 it is shown the layout core of the VCs biased OTA, from which the post-layout simulations will be done. Taking the circuit symmetry into account, an amplified version of the top of the circuit, containing the N-well and PMOS transistors, is shown in Figure A.3 and the bottom, containing the NMOS transistors, in Figure A.4.

The FFT output is presented in Figure 4.27, the AC plot of gain and phase are shown in Figure 4.28 and the input referred noise plot is in Figure 4.29. The comparison of the performance indexes between the post-layout and schematic is shown in Table 4.10, where it is most noticeable the improvement in THD, the noise at cut-off frequency increases from 968.6 \( \mu V/\sqrt{Hz} \) to 969.5 \( \mu V/\sqrt{Hz} \), along with the flicker and thermal noise, with the other performance indexes having a minimal decrease, less than 1.8\%, as seen in Table 4.10.
Table 4.10: Comparison of performance indexes of VCs biased OTA.

<table>
<thead>
<tr>
<th>Performance Index</th>
<th>Schematic</th>
<th>Post-Layout</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD [dB]</td>
<td>-58.7</td>
<td>-74.73</td>
</tr>
<tr>
<td>Gain [dB]</td>
<td>58.62</td>
<td>58.61</td>
</tr>
<tr>
<td>$f_c$ [Hz]</td>
<td>35.81</td>
<td>35.72</td>
</tr>
<tr>
<td>GBW [kHz]</td>
<td>29.99</td>
<td>29.6</td>
</tr>
<tr>
<td>Phase Margin [$^\circ$]</td>
<td>82.47</td>
<td>81.05</td>
</tr>
<tr>
<td>Noise [$\mu V_{rms}$]</td>
<td>12.99 / 98.02</td>
<td>13.0 / 98.1</td>
</tr>
</tbody>
</table>

Figure 4.27: Post-layout FFT simulation of VCs biased OTA.

Figure 4.28: Post-layout gain and phase simulation of VCs biased OTA.
4.6.3 Current Biased OTA Layout

In Figure 4.34 it is shown the layout core of the current biased OTA, from which the post-layout simulations will be done. Taking the circuit symmetry into account, an amplified version of the top of the circuit, containing the N-well and PMOS transistors, is shown in Figure A.1 and the bottom, containing the NMOS transistors, in Figure A.2.

The FFT output is presented in Figure 4.31, the AC plot of gain and phase are shown in Figure 4.32 and the input referred noise plot is in Figure 4.33. The comparison of the performance indexes between the post-layout and schematic is shown in Table 4.11, where it is most noticeable the improvement in THD, the noise at cut-off frequency increases from \(1.517 \mu V/\sqrt{Hz}\) to \(1.519 \mu V/\sqrt{Hz}\), along with the flicker and thermal noise, with the other performance indexes having a minimal decrease, in this case less than 1.5\%, as seen in Table 4.11.

Table 4.11: Comparison of performance indexes of current biased OTA.

<table>
<thead>
<tr>
<th>Performance Index</th>
<th>Schematic</th>
<th>Post-Layout</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD [dB]</td>
<td>-55.5</td>
<td>-61.70</td>
</tr>
<tr>
<td>Gain [dB]</td>
<td>57.55</td>
<td>57.55</td>
</tr>
<tr>
<td>(f_c) [Hz]</td>
<td>15.21</td>
<td>15.13</td>
</tr>
<tr>
<td>GBW [kHz]</td>
<td>11.34</td>
<td>11.23</td>
</tr>
<tr>
<td>Phase Margin [°]</td>
<td>84.37</td>
<td>83.25</td>
</tr>
<tr>
<td>Noise [(\mu V_{rms})]</td>
<td>11.86 / 99.92</td>
<td>11.9 / 100.0</td>
</tr>
</tbody>
</table>
Figure 4.30: Full layout of VCs biased OTA.
Figure 4.31: Post-layout FFT simulation of current biased OTA.

Figure 4.32: Post-layout gain and phase simulation of current biased OTA.

Figure 4.33: Post-layout input referred noise simulation of current biased OTA.
Figure 4.34: Full layout of current biased OTA.
4.6.4 Post-Layout Simulation Results

The post-layout simulations of the filter are present next, both low-pass and band-pass outputs. The filter’s layout is composed of the layout of the previous two OTAs, therefore, only the parasitic contributions of the OTAs will affect the simulations, the remaining components of the filter will remain as a technology schematic component.

For the low-pass output, a DC simulation shows that the DC offset remains the same at 510.358 mV, for the schematic and post-layout simulations. The gain and phase plot is presented in Figure 4.35 and the input referred noise is presented in Figure 4.36, in Table 4.12 it is shown significant performance indexes, where it is observable that the gain also remains the same, \( f_c \), GBW and the phase margin slightly decrease and the noise slightly increases, with the noise at \( f_c \) going from 1.461 \( \mu V/\sqrt{Hz} \) to 1.462 \( \mu V/\sqrt{Hz} \).

<table>
<thead>
<tr>
<th>Performance Index</th>
<th>Schematic</th>
<th>Post-Layout</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain [dB]</td>
<td>8.546</td>
<td>8.561</td>
</tr>
<tr>
<td>( f_c ) [Hz]</td>
<td>22.37</td>
<td>22.34</td>
</tr>
<tr>
<td>GBW [Hz]</td>
<td>55.53</td>
<td>55.56</td>
</tr>
<tr>
<td>Phase Margin [°]</td>
<td>108.99</td>
<td>108.94</td>
</tr>
<tr>
<td>Noise [( \mu V_{rms} )]</td>
<td>10.38 / 28.77</td>
<td>10.4 / 28.8</td>
</tr>
</tbody>
</table>

Figure 4.35: Post-layout gain and phase simulation of the low-pass output.
For the band-pass output, a DC simulation shows that the DC offset decreases from 501.553 mV to 501.549 mV, from the schematic to the post-layout simulations, this change still fulfills the 500 mV specified. The gain plot is presented in Figure 4.37 and the input referred noise is presented in Figure 4.38, in Table 4.13 it is shown significant performance indexes, where it is observable that the gain has a minimal increase, $f_c$ and GBW margin slightly decrease and the noise slightly increases, with the noise at $f_c$ going from $1.485 \mu V/\sqrt{Hz}$ to $1.486 \mu V/\sqrt{Hz}$.

Table 4.13: Comparison of performance indexes of the band-pass output.

<table>
<thead>
<tr>
<th>Performance Index</th>
<th>Schematic</th>
<th>Post-Layout</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain [dB]</td>
<td>8.533</td>
<td>8.534</td>
</tr>
<tr>
<td>$f_c$ [Hz]</td>
<td>21.57 - 1135</td>
<td>21.54</td>
</tr>
<tr>
<td>GBW [Hz]</td>
<td>8.83 - 2760</td>
<td>8.818</td>
</tr>
<tr>
<td>Noise [$\mu V_{rms}$]</td>
<td>34.13 / 75.41</td>
<td>34.2 / 75.5</td>
</tr>
</tbody>
</table>

Overall the circuit shows improvement in THD, this is a result of the parasitic capacitances from the layout composition. The Power Factor (PF) is a metric applicable to circuits where there is an AC voltage source that provides an AC current for some specific of load. It is the nature of the load that determines the nature of the current and therefore the PF. PF is given by Equation 4.8 where it depends on the circuits power. THD is given by Equation 4.9 [27], given that the voltage source and current is the same for the schematic and post-layout simulations the difference in THD comes from a difference in the phases between voltage and current ($\theta_v - \theta_i$), from the parasitic capacitances.

$$PF = \frac{\text{Real Power}}{\text{Apparent Power}} \tag{4.8}$$
\[ THD = \sqrt{\frac{\cos(\theta_v - \theta_i)^2}{PF^2} - 1} \] (4.9)

Figure 4.37: Post-layout gain simulation of the band-pass output.

Figure 4.38: Post-layout input referred noise simulation of the band-pass output.
4.7 Design Optimization and Optimized Results

This section presents the optimization and results for the first stage of the filter architecture, i.e., the voltage-combiners biased OTA. This chapter offers a detailed description of the automatic framework in which the optimization was carried out, as well as the test-bench, voltage and temperature conditions and the complete set of specifications and objectives to achieve. In order to achieve the most competitive design solutions and completely explore the tradeoffs between the gain and the noise performance of the first stage of the filter, a multi-objective and multi-constraint circuit optimization framework denominated AIDA was used, to automatically optimize the circuit at sizing level [28].

4.7.1 Optimization Framework

The optimization tool AIDA is based on an evolutionary computation kernel, and implements automatic synthesis, where the robustness of the solutions can be enhanced by considering process, voltage and temperature (PVT) corners, and the circuit performance is evaluated using electrical circuit simulators. In this work, the AIDA’s native simulator ELDO® was used. There are minor and negligible differences between the results in ELDO® and any other simulator, e.g., Cadence’s Spectre, which are mainly due to differences in terms of device models that are not relevant. ELDO® is able to deal with all the analyses needed with relative ease and speed, hence its choice. The robustness of the design can also be enhanced by considering Monte Carlo yield optimization [29]. The output of AIDA is a Pareto Optimal Front (POF) of feasible solutions. A POF is a list of completely sized circuits that meet the specifications, however representing different performance compromises between contradictory optimization objectives, hence providing a larger insight and wider perception of the considered circuit.

The complete AIDA framework, depicted in Figure 4.39 is composed by two main modules: a sizing module AIDA-C [30] and a layout module AIDA-L [31], which was not considered in this work. The layout module can be partially activated to include layout data, e.g., geometric and parasitic effects, inside the sizing optimization for a layout-aware sizing optimization. AIDA-L takes the device sizes and the best floor-plan for selected circuit sizing, and generates the layout by placing and routing the devices. The layout is then saved as a geometric data stream (GDS-II) graphical format, and the evaluation of the results is performed. It is provided to the designer operating AIDA, the freedom to choose which solution fits best the requirements or specifications of a given design project and targeting a specific application [32]. The sizing module AIDA-C receives the circuit and test-benches in netlist format with: free variables, i.e., design parameters to be optimized automatically; a complete set of specifications for both DC and AC, e.g., overdrive voltages and gain correspondingly; and also the optimization objectives, i.e., the specifications to be maximized or minimized, e.g., maximization of gain and minimization of noise contribution, that represent a design tradeoff. The AIDA-C is shown in Figure 4.40.
The AIDA-C engine solves multi-objective multi-constraint optimization problems defined in Equation 4.10, where $x$ is a vector of $N$ input variables (to optimize), $f_m(x)$ is a fitness function, i.e., set of $M$ objective functions to minimize, $g_j(x)$ is the set of $J$ constraints and, finally, $x_i^L \leq x_i \leq x_i^U$ is the range for the optimization variable $x_i$. The formulation of this problem is adapted to the analog IC design by using the circuit parameters as design variables, defining the $N$-dimensions search space. The objectives are handled and defined as performance figures or fitness functions $f_m$. In this case, the ones that are to be minimized are used directly, while the ones being maximized are multiplied by -1, for normalization purposes. The design specifications are normalized and the circuit characteristics are evaluated through.

$$\text{find } x \text{ that minimizes } f_m(x) \quad m = 1, 2, \ldots, M$$

subject to $g_j(x) \quad j = 1, 2, \ldots, J$

$x_i^L \leq x_i \leq x_i^U \quad i = 1, 2, \ldots, N$  \hspace{1cm} (4.10)

![Diagram](image_url)

**Figure 4.39:** Analog IC Design Automation complete framework (AIDA).
The multi-objective optimization kernel implemented by the NSGA-II, is described in the algorithm shown in Figure 4.41. The implementation of the NSGA-II algorithm follows the reference first proposed in [33], using simulated binary crossover and mutation operators, tournament selection, and constrained based solution dominance check.

**input:** Population Size, Max Generation

 initialization

 while (generation < Max Generation) {
   apply operators //Mutation and Crossover
   evaluate
   non-dominated sorting
   selection
 }

 return pareto

**Figure 4.41:** Simplified pseudo-code of the NSGA-II algorithm in AIDA-C.

The optimization of the amplifier is carried out using UMC 130 nm CMOS design kit, with standard-VT 1.2 V devices. In order to achieve the most competitive design solutions and completely explore the tradeoffs between the gain and output noise, the multi-objective multi-constraint automatic IC sizing and optimization framework AIDA-C, is used to automatically synthesize the circuit at sizing level.

Simulation results of a properly optimized amplifier using AIDA-C, demonstrate that a gain above 58 dB can be achieved while an output noise of 1.2 mV_{RMS} can also be achieved. The process was carried
out considering two contradictory objectives: the maximization of the gain and the minimization of the output noise. All the measures were taken under an open-loop test-bench with an output capacitive load of 500 fF. This resulted in several sizing solutions constituting a POF of properly sized circuits, as described further. The extension to deeper nanoscale nodes, e.g., 65 nm is relatively straightforward.

A set of specifications is considered in the optimization process. The specifications are, on the one hand, related to the overdrive voltage of the devices, i.e., the gate-source voltage minus the threshold voltage (in the case of the NMOS) or the source-gate voltage minus the absolute value of the threshold voltage (in the case of the PMOS which have negative threshold voltages); and to their minimal saturation margin, i.e., the drain-source voltage minus the overdrive (in the case of the NMOS) or the source-drain voltage minus the overdrive (in the case of the PMOS); while other specifications are related with the performance metrics of the circuit, e.g., current consumption, the gain, 3 dB bandwidth, gain-bandwidth product, phase margin, output noise and output offset voltage. The overdrive voltages and saturation margins are according to the manual design process. The set of the other specifications is listed in Table 4.14. In this optimization, the bandwidth was comprehended between 20 and 30 Hz, which is lower than what was achieved manually. This is expected to have an impact on the overall architecture performance, lowering the bandwidth and allowing a lower value for baseband signals, improving the tuning of the filter. The gain was set to be higher than 56 dB and was one of the objectives (to maximize) to verify the potential of this architecture. A phase margin higher than $50^\circ$ ensures stability. The output noise voltage was set lower than $1.5 \text{ mV}_R$ and was the other objective (to minimize). The current consumption was set lower than 440 nA which was less than the value achieved manually, and the output offset voltage, being the difference between the DC voltage at the output and the DC voltage at the input, was set lower than 1 % of the supply voltage, which was 1.2 V in this work.

**Table 4.14:** Optimization specifications.

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<td>Gain [dB]</td>
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<tr>
<td>Bandwidth [Hz]</td>
<td>$20 \leq \text{Bandwidth} \leq 30$</td>
</tr>
<tr>
<td>Gain-bandwidth Product [Hz]</td>
<td>$\geq 5000$</td>
</tr>
<tr>
<td>Phase Margin [°]</td>
<td>$\geq 50$</td>
</tr>
<tr>
<td>Output Noise [mV\text{\text{RMS}}]</td>
<td>$\leq 1.5$</td>
</tr>
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<td>Current Consumption [nA]</td>
<td>$\leq 440$</td>
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<tr>
<td>Output Offset Voltage [mV]</td>
<td>$\leq 10$</td>
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</table>
The optimization process took approximately 12 hours in an i7-3770 Intel® CPU with 16 GB-RAM. A population of 128 elements evolved over 2000 generations, establishing a steady POF and demonstrating that, for the presented specifications, it is possible to achieve a gain over 58 dB or an output noise of 1.2 mV_{RMS} with this topology, under typical PVT conditions, i.e., typical process models, 1.2 V supply voltage and 25 ° of temperature. The output POF is shown in Figure 4.42. All the project files are in Appendix B.

Figure 4.42: Optimization results.
5

Conclusions and Future Work
Conclusions and Future Work

This chapter presents the conclusions of this dissertation work, emphasising on the most important metrics improved in this work. Future work on this dissertation is also proposed.

In this work we considered the development of a low-power LPF to be integrated inside a portable biomedical device. Important metrics and basic concepts were studied to better understand the operation of a low pass filter. Filter approximations were analyzed to comprehend the different options available and understand the most suitable. Finally, relevant work was examined to ascertain the optimal solution for the objectives established. Taking the existing work into consideration, this dissertation presented a new perspective in the creation of a biquad filter with a 2nd-order Tow-Thomas configuration for biomedical equipment. This configuration allowed for a very low and tunable cut-off frequency, also provided a band-pass output. For a better fulfillment of the specifications, a new OTA configuration designed for better overall gain was presented. The layout core of both OTAs was developed and implemented in the filter. Finally, the VCs biased OTA sizing was optimized using the AIDA tool. The complete circuit was implemented using the UMC 130 nm technology, biased by a 1.2 V supply source, consuming approximately 788 nW. The post-layout simulations showed that the filter achieved a cut-off frequency of 22.34 Hz when used as a low-pass filter with an effective gain of approximately 8.561 dB and a bandwidth of 21.4 Hz when used as a band-pass filter with a maximum gain of 8.534 dB.

5.1 Future Work

The following tasks are proposed as future work for this dissertation:

- Optimize all the filter components with the AIDA tool for maximum gain versus maximum energy-efficiency;
- Develop the remaining components layout, fabricate and validate the circuit at a experimental level.
Bibliography


Figure A.1: Top layout of VCs biased OTA.

Figure A.2: Bottom layout of VCs biased OTA.
Figure A.3: Top layout of current biased OTA.

Figure A.4: Bottom layout of current biased OTA.
Appendix - Optimization Files
Optimization Files

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View name: schematic

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v0 net1 0 DC=1.2 AC 0
e3 vout 0 VCVS vop vom 1
c2 vout 0 500e-15
c0 vop 0 500e-15
c1 vom 0 500e-15

Analysis

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.NOISE v(vop,von) v2 100
.OPTION BRIEF=0

.Performance Measures

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.EXTRACT AC label=BW XDOWN(VDB(VOUT),G3DB,1,500000,1)

.Overdrives

.MEASURE AC vov_mpm2b = param('((\text{lv9 (xi0.mpm2b)} - \text{VGS(xi0.mpm2b)})')
.MEASURE AC vov_mpm1b = param('((\text{lv9 (xi0.mpm1b)} - \text{VGS(xi0.mpm1b)})')
.MEASURE AC vov_mpm2a = param('((\text{lv9 (xi0.mpm2a)} - \text{VGS(xi0.mpm2a)})')
.MEASURE AC vov_mpm1a = param('((\text{lv9 (xi0.mpm1a)} - \text{VGS(xi0.mpm1a)})')
.MEASURE AC vov_mptop = param('((\text{lv9 (xi0.mptop)} - \text{VGS(xi0.mptop)})')
.MEASURE AC vov_mptop0 = param('((\text{lv9 (xi0.mptop1)} - \text{VGS(xi0.mptop1)})')
.MEASURE AC vov_mpmdowna = param('((\text{lv9 (xi0.mpmdowna)} - \text{VGS(xi0.mpmdowna)})')
.MEASURE AC vov_mpm0a = param('((\text{lv9 (xi0.mpm0a)} - \text{VGS(xi0.mpm0a)})')

Performs a behavioral simulation of the OTA circuit with the specified parameters and analysis options.
122 .MEASURE AC vov_mpmtopb = param('(lv9(xi0.mpmtopb)-VGS(xi0.mpmtopb))')
123 .MEASURE AC vov_mpmdownb = param('(lv9(xi0.mpmdownb)-VGS(xi0.mpmdownb))')
124 .MEASURE AC vov_mpm0b = param('(lv9(xi0.mpm0b)-VGS(xi0.mpm0b))')
125 .MEASURE AC vov_mnmza = param('(VGS(xi0.mnmza)-lv9(xi0.mnmza))')
126 .MEASURE AC vov_mnmwa = param('(VGS(xi0.mnmwa)-lv9(xi0.mnmwa))')
127 .MEASURE AC vov_mnmxa = param('(VGS(xi0.mnmxa)-lv9(xi0.mnmxa))')
128 .MEASURE AC vov_mnmqa = param('(VGS(xi0.mnmqa)-lv9(xi0.mnmqa))')
129 .MEASURE AC vov_mnm1a = param('(VGS(xi0.mnm1a)-lv9(xi0.mnm1a))')
130 .MEASURE AC vov_mnm0a = param('(VGS(xi0.mnm0a)-lv9(xi0.mnm0a))')
131 .MEASURE AC vov_mnm0b = param('(VGS(xi0.mnm0b)-lv9(xi0.mnm0b))')
132 .MEASURE AC vov_mnm1b = param('(VGS(xi0.mnm1b)-lv9(xi0.mnm1b))')
133 .MEASURE AC del_mpm2b = param('(VDSAT(xi0.mpmtopb)-VDS(xi0.mpmtopb))')
134 .MEASURE AC del_mpm1b = param('(VDSAT(xi0.mpmdownb)-VDS(xi0.mpmdownb))')
135 .MEASURE AC del_mpm0a = param('(VDSAT(xi0.mpmtopb)-VDS(xi0.mpmtopb))')
136 .MEASURE AC del_mpm0b = param('(VDSAT(xi0.mpmdownb)-VDS(xi0.mpmdownb))')
137 .MEASURE AC del_mnmza = param('(VDSAT(xi0.mnmza)-VDS(xi0.mnmza))')
138 .MEASURE AC del_mnmwa = param('(VDSAT(xi0.mnmwa)-VDS(xi0.mnmwa))')
139 .MEASURE AC del_mnmxa = param('(VDSAT(xi0.mnmxa)-VDS(xi0.mnmxa))')
140 .MEASURE AC del_mnmqa = param('(VDSAT(xi0.mnmqa)-VDS(xi0.mnmqa))')
141 .MEASURE AC del_mnm1a = param('(VDSAT(xi0.mnm1a)-VDS(xi0.mnm1a))')
142 .MEASURE AC del_mnm0a = param('(VDSAT(xi0.mnm0a)-VDS(xi0.mnm0a))')
143 .MEASURE AC del_mnm0b = param('(VDSAT(xi0.mnm0b)-VDS(xi0.mnm0b))')
144 .MEASURE AC del_mnm1b = param('(VDSAT(xi0.mnm1b)-VDS(xi0.mnm1b))')
145 .MEASURE AC del_mnmxb = param('(VDSAT(xi0.mnmxb)-VDS(xi0.mnmxb))')
146 .MEASURE AC del_mnmwb = param('(VDSAT(xi0.mnmwb)-VDS(xi0.mnmwb))')
147 .MEASURE AC del_mnmqb = param('(VDSAT(xi0.mnmqb)-VDS(xi0.mnmqb))')

********************** SAT MARGINS ******************************
148 .MEASURE AC del_mpm2b = param('(VDSAT(xi0.mpmtopb)-VDS(xi0.mpmtopb))')
149 .MEASURE AC del_mpm1b = param('(VDSAT(xi0.mpmdownb)-VDS(xi0.mpmdownb))')
150 .MEASURE AC del_mpm0a = param('(VDSAT(xi0.mpmtopb)-VDS(xi0.mpmtopb))')
151 .MEASURE AC del_mpm0b = param('(VDSAT(xi0.mpmdownb)-VDS(xi0.mpmdownb))')
152 .MEASURE AC del_mnmza = param('(VDSAT(xi0.mnmza)-VDSAT(xi0.mnmza))')
153 .MEASURE AC del_mnmwa = param('(VDSAT(xi0.mnmwa)-VDSAT(xi0.mnmwa))')
154 .MEASURE AC del_mnmxa = param('(VDSAT(xi0.mnmxa)-VDSAT(xi0.mnmxa))')
155 .MEASURE AC del_mnmqa = param('(VDSAT(xi0.mnmqa)-VDSAT(xi0.mnmqa))')
156 .MEASURE AC del_mnm1a = param('(VDSAT(xi0.mnm1a)-VDSAT(xi0.mnm1a))')
157 .MEASURE AC del_mnm0a = param('(VDSAT(xi0.mnm0a)-VDSAT(xi0.mnm0a))')
158 .MEASURE AC del_mnm0b = param('(VDSAT(xi0.mnm0b)-VDSAT(xi0.mnm0b))')
159 .MEASURE AC del_mnm1b = param('(VDSAT(xi0.mnm1b)-VDSAT(xi0.mnm1b))')
160 .MEASURE AC del_mnmxb = param('(VDSAT(xi0.mnmxb)-VDSAT(xi0.mnmxb))')
161 .MEASURE AC del_mnmwb = param('(VDSAT(xi0.mnmwb)-VDSAT(xi0.mnmwb))')
162 .MEASURE AC del_mnmqb = param('(VDSAT(xi0.mnmqb)-VDSAT(xi0.mnmqb))')

*****************************************************************************
163 .END