Abstract: Machine learning and data analytics continue to expand the fourth industrial revolution and affect many aspects of our lives. The talk will explore hardware accelerator architectures for deep neural networks (DNNs). I will present a brief review of history of neural networks. I will talk about our recent work on Perm-DNN based on permuted-diagonal interconnections in deep convolutional neural networks and how structured sparsity can reduce energy consumption associated with memory access in these systems (MICRO-2018). I will then talk about reducing latency and memory access in accelerator architectures for training DNNs by gradient interleaving using systolic arrays (ISCAS-2020). Then I will present our recent work on LayerPipe, an approach for training deep neural networks that leads to simultaneous intra-layer and inter-layer pipelining (ICCAD-2021). This approach can increase processor utilization efficiency and increase speed of training without increasing communication costs.

Bio: Keshab K. Parhi received the B.Tech. degree from the Indian Institute of Technology (IIT), Kharagpur, in 1982, the M.S.E.E. degree from the University of Pennsylvania, Philadelphia, in 1984, and the Ph.D. degree from the University of California, Berkeley, in 1988. He has been with the University of Minnesota, Minneapolis, since 1988, where he is currently Distinguished McKnight University Professor and Edgar F. Johnson Professor of Electronic Communication in the Department of Electrical and Computer Engineering. He has published over 650 papers, is the inventor of 32 patents, and has authored the textbook VLSI Digital Signal Processing Systems (Wiley, 1999) and coedited the reference book Digital Signal Processing for Multimedia Systems (Marcel Dekker, 1999). His current research addresses VLSI architecture design of machine learning systems, hardware security, data-driven neuroscience and molecular/DNA computing. Dr. Parhi is the recipient of numerous awards including the 2017 Mac Van Valkenburg award and the 2012 Charles A. Desoer Technical Achievement award from the IEEE Circuits and Systems Society, the 2004 F. E. Terman award from the American Society of Engineering Education, and the 2003 IEEE Kiyo Tomiyasu Technical Field Award. He served as the Editor-in-Chief of the IEEE Trans. Circuits and Systems, Part-I during 2004 and 2005. He is a Fellow of IEEE, ACM, AAAS and the National Academy of Inventors.