Modular Single Stage Smart Transformer with DC Link

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***Abstract*—The growing evolution both in terms of electricity consumption and production is followed by a growing need for the evolution of the energy distribution and supply network, with greater control and quality. The Low-Frequency Transformers, LFT, which currently compose the electrical grid have several limitations such as poor voltage regulation, large dimensions and the use of oil for cooling the transformer, which is an important aspect with a negative impact in environmental terms.**

Due to the limitations of LFTs, the main objective of this dissertation is to study and propose a Smart Transformer (ST) that could be implemented in the electrical grid, between the MV and LV network, and offer a DC link for charging electric vehicles (EV).

The ST features a modular topology, consisting of single-phase matrix converters and high-frequency transformers. The LV side voltage and current control is performed using Lyapunov's stability theory and the Predictive Control Method, respectively. It is shown the ST operation in normal MV/LV connection operation functions, simultaneous operation with DC load and also under the influence of voltage dips/overvoltages in the MV network.

The ST simulations are carried out in MATLAB/Simulink and confirm the good operation of the ST in the MV/LV network, as well as during DC loading, and the dimensioning of the input and output filters that integrate it. The transformer core does not saturate, because of the control strategies applied to the ST and has an adjustable output voltage under load.

***Index Terms*—Smart Transformer, High Frequency Transformer, Single Phase Matrix Converter, Lyapunov Stability, Predictive Control**

I. Introduction

In recent years, with the integration of renewable energies and new loads (e.g electric vehicles), the concept of smart grid has gained increasing relevance. The electrical grid, with the contribution of new associated loads, has undergone major changes, which are expected to continue to happen, and the impact of this evolution will be increasingly felt in the quality of service.

The need for greater automation and control over the electrical grid has led to a constant study and search for solutions in order to meet the needs that arise and to improve the quality of the electricity distribution service. The introduction of STs in the connection between the medium and low voltage grid, in place of LFTs, is a solution that allows us to respond to many of the current and future challenges. LFTs have several limitations that motivate the study and development of technologies such as Solid State Transformers , (SST), which are more capable and with more functionalities than those presented by the type of transformers that currently compose the electrical grid. All the features that the study of this new solution demonstrates that can be implemented, motivates an increasingly deeper study and the desire to take this type of transformers to be incorporated into the grid.

The concept of Solid State Transformer (SST) appeared in 1968 [4]. This transformer works at high frequencies unlike the LFT, which in itself brings great weight and volume advantages [1]. The SST concept and later ST concept have been studied over the years [2]. ST is a transformer that offers possibilities for controlling and managing the electrical grid in an easy, fast and intelligent way. Recently, a lot of work has been devoted to the study of STs and its application in the electrical grid.

II. Proposed Modular ST

The proposed system is an ST to be installed in the distribution network, connecting the MV and LV network. The ST consists of single-phase matrix converters on the input and output stages, whose semiconductors are switched at high frequency. Between the input and output converters are the high frequency transformers. In the case under study, the working frequency of the transformers is $50kHz$.

In addition to the three output phases for the LV network, the ST also features a DC link that is very useful in various applications such as charging electric vehicles. The general scheme of the dimensioned topology is shown in Fig. 1.

At the output, 4 single-phase matrix converters can be observed, represented by blue rectangles, one for each AC phase of the LV network and another for the DC link. For each of these output converters we have at the input the corresponding set of 3 modular single-phase matrix converters that allow the division of the input voltage on the MV side by the semiconductors that make up these converters by their modular configuration. The dashed rectangle shown on the upper part of the ST identifies the first of the 4 conversion stages that make up the ST.

The first stage of the ST conversion is presented in greater detail in Fig. 2, where the modular composition of this transformer can be observed. This Figure details the first set

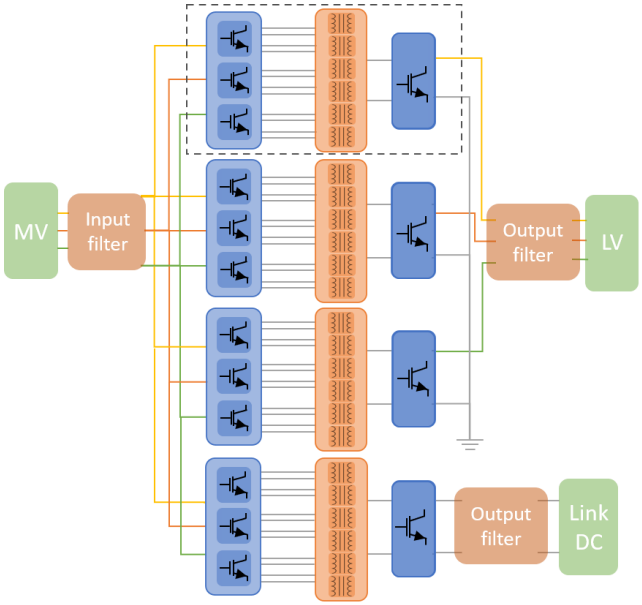

Fig. 1. ST's simplified topology

of 3 converters of the ST input stage, connections between the high frequency transformers and the respective output converter that characterizes each of the ST output phases.

For the purpose of understanding what will be explained below, it should be noted that the status of switches S_{a11}, S_{a12}, S_{a13} and S_{a14} corresponds to the status of switches S_{a15}, S_{a16}, S_{a17} and S_{a18} respectively. The same reasoning applies to the other converters on each ST conversion stage. Thus, for purpose of simplification, the states of S_{a11}, S_{a12}, S_{a13} and S_{a14} will always be considered, which correspond by default to the states of the other 4 switches of that same converter.

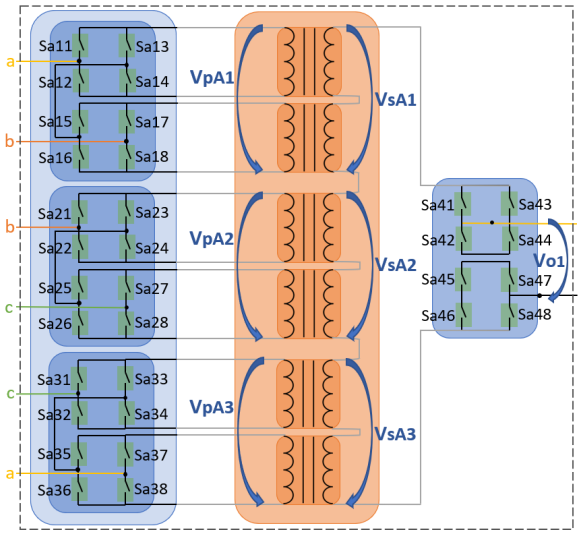

Fig. 2. Detailed representation for the conversion stage of an ST output phase, specifically the first phase

According to the status of the switches, they can be associated with the voltages obtained at the output of the converter, depending on their input. In Table I you can see this same association for the first converter of the set of 3 input converters in Fig. 2, which corresponds to the same possible states for each of the converters on this floor.

TABLE I
POSSIBLE COMBINATIONS OF SWITCH STATES OF THE FIRST INPUT CONVERTER IN FIGURE 2

S_{a11}	S_{a12}	S_{a13}	S_{a14}	V_{pA1}
1	0	0	1	V_{ab}
1	1	0	1	0
0	1	1	0	$-V_{ab}$
0	0	1	1	0

The second and third input converters of each of the 3 ST conversion stages have the same possible combinations as those represented in Table I. The output voltages for these second and third converters of the conversion stage are V_{bc} and V_{ca} for the states that indicate the voltage V_{ab} in the table, respectively.

III. Filters Sizing

The sizing of the ST input filter presented in this section intends to minimize the dissipated power, the lag between the grid voltages and those applied to the ST and the lag between the input voltages and currents by a unitary power factor [7]. The filter applied to the ST input is a second order filter and can be represented by the Figure 3.

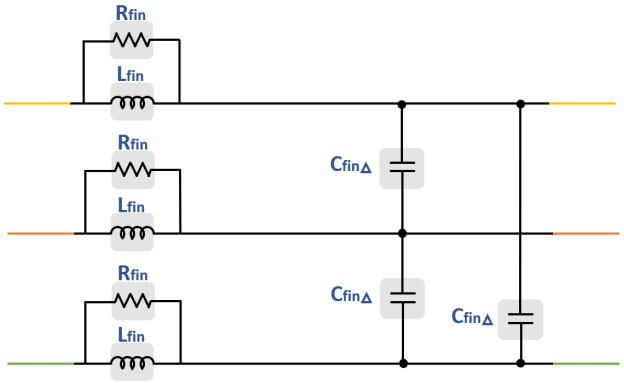

Fig. 3. ST input filter

In order to simplify the filter sizing, the equivalent single-phase scheme shown in Figure 4 is considered. It is based on this equivalent scheme that all filter components are dimensioned.

$$C_{f_{inY}} = \frac{I_{fmin}}{\omega_i V_{f_{max}}} tan(cos^{-1}(P_f)) \quad (1)$$

To obtain the value of the coil, the equation (2) is applied, where the value of the capacitor calculated previously and the value of the cutoff frequency f_c, that is, ω_c, are necessary. This cut-off frequency must correspond to a value between the grid frequency and the switching frequency, more

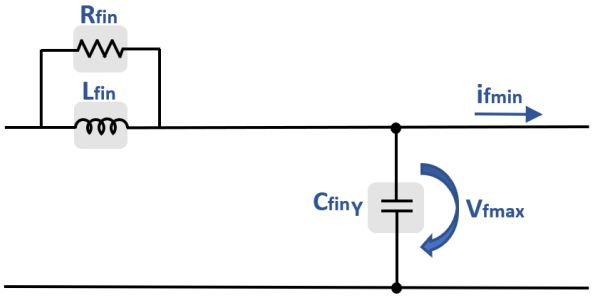

Fig. 4. Equivalent circuit of the AC input filter

properly a decade above the grid frequency and a decade below the switching frequency $f_i << f_c << f_s$, that is, $\omega_i << \omega_c << \omega_s$. This aspect is important for the filter to minimize the attenuation of high frequency harmonics and the resonant effect resulting from the cutoff frequency.

$$L_{f_{in}} = \frac{1}{\omega_c C_{f_{inY}}} \tag{2}$$

The damping resistance that is connected in parallel with the coil is dimensioned according to (3). Note that $Z_{f_{in}}$ corresponds to the input filter impedance which is given by (4).

$$R_{f_{in}} = \frac{1}{2\zeta} Z_{f_{in}} \tag{3}$$

$$Z_{f_{in}} = \frac{L_{f_{in}}}{C_{f_{inY}}} \tag{4}$$

As stated above, with the calculated values, conditions are met to size the input filter. The single-phase equivalent scheme coil and damping resistance values correspond to the values applied to these same components in the ST input filter. The capacitor capacity value of the ST input filter is related to the capacitor capacity value present in the equivalent scheme through (5).

$$C_{f_{in\Delta}} = \frac{C_{f_{inY}}}{3} \tag{5}$$

The table II presents the values of the components of the ST input filter under study.

TABLE II
VALUES OF THE INPUT FILTER

$C_{f_{in\Delta}}$ $[\mu F]$	$L_{f_{in}}$ $[mH]$	$R_{f_{in}}$ $[\Omega]$
0.65	1.1	382

The output filter that is applied to the ST output corresponds to the representation shown in Figure 5. The filter is characterized as a low pass that allows obtaining a better quality LV side current by filtering high frequency harmonics.

In order to dimension the ST output filter, it is simplified according to the equivalent single-phase scheme represented in Figure 6.

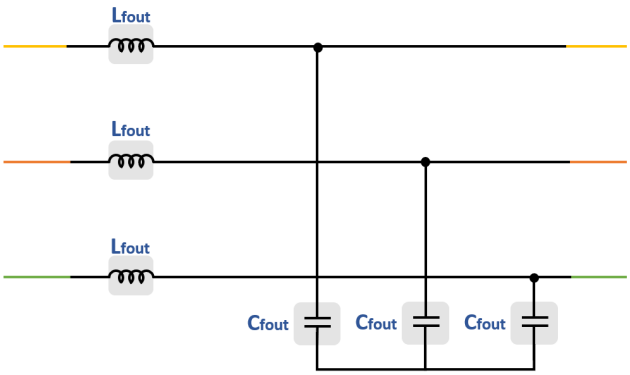

Fig. 5. ST AC output filter

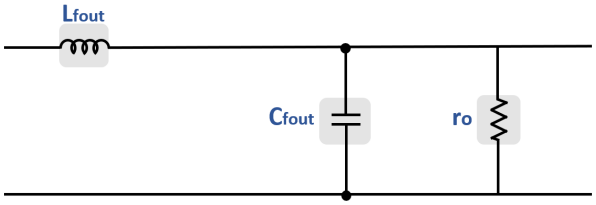

Fig. 6. Equivalent circuit of the AC output filter

All calculations of the components of the ST output filter correspond to the components represented in the equivalent single-phase circuit. The output filter capacitor capacity should be obtained through the formula (6), where $Z_{f_{out}}$ is the characteristic impedance of the output filter and is obtained by (7). In this last expression r_o corresponds to the resistance value equivalent to the filter output obtained by the LV side output voltage and power values and ζ corresponds to the filter damping coefficient.

$$C_{f_{out}} = \frac{1}{\omega_c Z_{f_{out}}} \tag{6}$$

$$Z_{f_{out}} = \frac{r_o}{2\zeta} \tag{7}$$

The value of ω_c, similarly to the one presented for the input filter, is related to the cutoff frequency f_c to be chosen. The coil value can be obtained by the expression (8) according to the value of the characteristic impedance of the output filter and the cutoff frequency, similarly to what was considered above.

$$L_{f_{out}} = \frac{Z_{f_{out}}}{\omega_c} \tag{8}$$

The ST DC link output filter is composed of a coil and a capacitor similar to the one dimensioned for the AC filter. The values are exactly the same for its components.

According to the aforementioned, the values of the filtering components that make up the output filter are thus obtained. The components are shown in Table III.

TABLE III
VALUES OF THE OUTPUT FILTER

$C_{f_{out}}[mF]$	$L_{f_{out}}[\mu H]$
0.23	440

IV. ST CONTROL

A. BT Current Control

In order to control the ST output current, the Predictive Control Method, MCP, is applied, based on the *Euler-Backward* method as a control strategy. It is possible to predict the best combination of states of the semiconductors that make up the ST input and output converters based on a cost function, in order to obtain a current on the LV side according to a reference current. There is also the *Euler-Forward* method, but the first one mentioned is more stable and gives better results, [8] . The expression (9) corresponds to the integration method of *Euler-Backward*, where x_{k+1} is the variable to predict in the future instant $t = k + 1$ e h the time interval, which correspond respectively in the case presented below to the current and calculation step, T_s.

$$x_{k+1} \approx x_k + h \left(\frac{dx}{dt} \right)_{k+1} \tag{9}$$

Figure 7 represents one of the ST phases, through which the voltages and output current for the calculation of the output voltage of the first output phase of the ST are represented, v_{o1}.

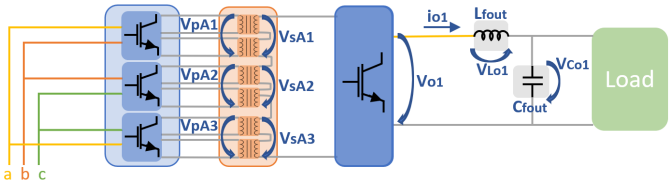

Fig. 7. Representation of the first output ST phase and its voltages and output current

By a mesh analysis applied to Figure 7, the equation (10) can be written, where the ST output voltage is obtained as a function of the secondary voltages of the transformers corresponding to each of the 3 input converter. The values that the variable γ_{s_A} can have are -1, 0 or 1 depending on the state of the semiconductors that make up the ST output converter.

$$v_{o1} = (v_{s_A1} + v_{s_A2} + v_{s_A3})\gamma_{s_A} \tag{10}$$

Based on the relationship between the voltages at the primary of the transformers v_{s_A1}, v_{s_A2} and v_{s_A3} and the input voltages at the input converters of the ST V_{ab}, V_{bc} and V_{ca}, (which also correspond to the voltages of the input filter capacitors), are obtained (11). The possible values for each of the gamma, γ_{1_A}, γ_{2_A} and γ_{3_A} are -1, 0 or 1, as for γ_{s_A}.

$$v_{o1} = (\gamma_{1_A} V_{ab} + \gamma_{2_A} V_{bc} + \gamma_{3_A} V_{ca})\gamma_{s_A} \tag{11}$$

By analyzing Figure 7, more specifically for the mesh corresponding to the ST output, the expression (12) can be written.

$$v_{o1} = L\frac{di_o}{dt} + v_{Co1} \Leftrightarrow \frac{di_o}{dt} = \frac{v_{o1}}{L} - \frac{v_{Co1}}{L} \tag{12}$$

From this equation, the expression for the calculation of the output current of the first phase of the ST at the future instant $t = k + 1$, $i_{o1}(k + 1)$, is obtained (13). $v_{o1}(k + 1)$ corresponds to the possible values of the output voltage at the instant $t = k + 1$, T_s to the calculation step, L to the value of the coil of the output filter $L_{f_{out}}$, v_{Co1} at the output filter capacitor voltage $C_{f_{out}}$ and $i_{o1}(k)$ is the output current of the ST at the instant K, when the calculation is performed.

$$i_{o1}(k + 1) = \frac{(v_{o1}(k + 1) - v_{Co1})T_s}{L} + i_{o1}(k) \tag{13}$$

The voltage $v_{o1}(k + 1)$ is a vector composed of 81 values corresponding to the 81 possible values for the output voltage of the ST obtained by (11), by the values that each γ can take. Thus, the possible values of $i_{o1}(k + 1)$ are also 81, as in the case of the other two ST output phases, $i_{o2}(k + 1)$ and $i_{o3}(k + 1)$.

With the various predicted current values associated with each possible combination of semiconductor states, it is possible to obtain an error between each of these currents and the reference current. In this sense, and as it is want an error closest to zero, either positive or negative, the cost function corresponding to (14) is defined in an initial phase, where α_1 is a constant.

$$f_{i_{o1}} = \alpha_1 (i_{o1_{ref}}(k + 1) - i_{o1}(k + 1))^2 \tag{14}$$

The minimization of the cost function allows the selection of the semiconductors state combinations that lead to the existence of a smaller error, in modulus, between the reference current and the possible current at a future time, through the values of γ_{1_A}, γ_{2_A},γ_{3_A} and γ_{s_A}.

To obtain an average value of the voltages in the transformers as low as possible, so as not to saturate them, new terms are added to the cost function according to the possible input voltages in the ST. With this strategy it is intended that this average value is also minimized, ideally being zero. Since each ST output phase comes from 3 input converters, the new terms to add to the cost function are 3, corresponding to the possible combinations of input voltages for each converter. Based on the above, and in order to obtain the average value of the input voltages at each instant for the converters of the first ST conversion stage, the expression (15) is written. The value of $V_{mem_{A1}}$ corresponds to the sum of the output voltage values prior to the instant in which $V_{tr_{A1}}$ is calculated, in this case for the first converter of the first conversion stage of the ST. $V_{tr_{A2}}$ and $V_{tr_{A3}}$ corresponds to the second and third converters of the first conversion stage of the ST.

$$\begin{cases} V_{tr_{A1}} = V_{mem_{A1}} + T_s \gamma_{1_A} V_{ab} \\ V_{tr_{A2}} = V_{mem_{A2}} + T_s \gamma_{2_A} V_{bc} \\ V_{tr_{A3}} = V_{mem_{A3}} + T_s \gamma_{3_A} V_{ca} \end{cases} \quad (15)$$

At $t = 0$, the value of $V_{mem_{A1}}$ is zero, both with $V_{mem_{A2}}$ and $V_{mem_{A3}}$. The value of $V_{mem_{A1}}$ to be used at the instant $t = k + 1$ corresponds to (16), where $\gamma_{1_{A_{min}}}$ corresponds to value of γ_{1_A} that minimizes the cost function that weighs the new terms of the mean value of the voltage at the instant of calculation. For the second and third input converters of the conversion stage, the expression is identical, with the gamma and voltages corresponding with the ones of the respective conversion stage.

$$V_{mem_{A1}}(k+1) = \gamma_{1_{A_{min}}} V_{ab} + V_{mem_{A1}} \quad (16)$$

The new cost function that contains the terms corresponding to (15) for each of the input voltages multiplied by a constant α_2 is presented in (17).

$$\begin{aligned} f_{i_{01}} &= \alpha_1 \left[i_{o1_{ref}}(k+1) - i_{o1}(k+1) \right]^2 + \\ &+ \alpha_2 \left[(\gamma_{1_A} V_{tr_{A1}})^2 + (\gamma_{2_A} V_{tr_{A2}})^2 + (\gamma_{3_A} V_{tr_{A3}})^2 \right] \end{aligned} \quad (17)$$

The cost functions to be applied to the second and third stages of conversion of the ST are, respectively, $f_{i_{02}}$ and $f_{i_{03}}$ (18).

$$\begin{aligned} f_{i_{02}} &= \alpha_1 \left[i_{o2_{ref}}(k+1) - i_{o2}(k+1) \right]^2 \\ &+ \alpha_2 \left[(\gamma_{1_B} V_{tr_{B1}})^2 + (\gamma_{2_B} V_{tr_{B2}})^2 + (\gamma_{3_B} V_{tr_{B3}})^2 \right] \\ f_{i_{03}} &= \alpha_1 \left[i_{o3_{ref}}(k+1) - i_{o3}(k+1) \right]^2 + \\ &+ \alpha_2 \left[(\gamma_{1_C} V_{tr_{C1}})^2 + (\gamma_{2_C} V_{tr_{C2}})^2 + (\gamma_{3_C} V_{tr_{C3}})^2 \right] \end{aligned} \quad (18)$$

The flowchart representing the ST current control is shown below in Figure 8. It is only by minimizing the cost function that the gamma values required for the selection of the ST switch states are obtained.

The ST output current control presented in this section and summarized in the flowchart is repeated for the other two conversion stages corresponding to the other two ST output phases. The reference current for each of the other phases is different only in the phase shift. This reference is obtained by the voltage control which will be explained in the next section. The current control applied to the ST DC bus is based on the method applied to the AC current, with the difference only in the reference current and the respective γ of each converter, similarly to what happens for the other output AC phases.

B. BT Voltage Control

To control the voltage on the LV side, a method based on the Lyapunov control theory is applied. A great advantage of applying this method lies in the fact that it is not necessary to solve differential equations to infer the stability conditions of the equilibrium state of the system [9].

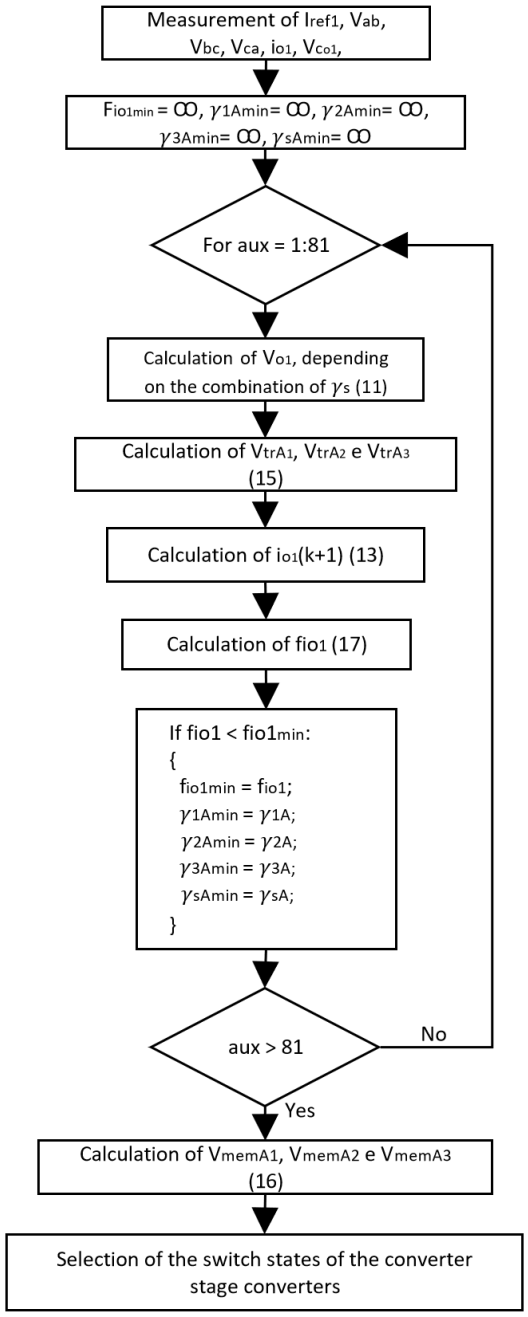

Fig. 8. Representative flowchart of the LV side current control of the first phase of the ST

The Lyapunov function, which is called $V_L(y)$, is a positive definite function and it defines a continuous D region that contains the origin. If its derivative, $V'_L(x)$, with respect to the system $x' = f(x)$ is less than or equal to zero, it implies the stability of the null solution of $x' = f(x)$. If $V'_L(x)$ is negatively defined in this same region D, it implies the asymptotic stability of the null solution of $x' = f(x)$. In this last condition and being $x = 0$ an equilibrium point - PE, PE is said to be asymptotically stable, that is, in addition to being stable, $\exists\ r(t0) > 0$, such that $||x(t0)|| < r \Rightarrow ||x(t)|| \to 0, t \to \infty$

[11]. The asymptotic stability condition can thus be defined as represented in (19).

$$V_L'(x) = \frac{dV_L(x)}{dt}(x \neq 0) < 0 \tag{19}$$

It is intended to ensure a monitoring of the voltage on the LV side, $v_{dq0_{BT}}$, according to a reference voltage, $v_{dq0_{ref}}$, both voltages being expressed in coordinates dq0. Thus, the equality $v_{dq0_{BT}} = v_{dq0_{ref}}$ is applied, where the error between these two voltages is expressed by (20).

$$e_{dq0} = v_{dq0_{ref}} - v_{dq0_{BT}} \tag{20}$$

The tension $v_{dq0_{ref}}$ corresponds to $\begin{bmatrix} V_{d_{ref}} & V_{q_{ref}} & V_{0_{ref}} \end{bmatrix}$ and e_{vdq0} a $\begin{bmatrix} e_d & e_q & e_0 \end{bmatrix}$. According to Lyapunov's theory, a Lyapunov function can be defined as (21) and, in order to guarantee asymptotic stability, the derivative of V_{L_v} must be negative.

$$V_{L_v} = \frac{1}{2} e_{vdq0}^2 \tag{21}$$

The asymptotic stability condition represented in (19) can be thus translated to the Lyapunov function defined in (21) and obtains for the case under study the stability condition (22).

$$\frac{V_{L_v}}{dt}(e_{vdq0} \neq 0) = e_{vdq0}\frac{e_{vdq0}}{dt} < 0 \tag{22}$$

In order for this equation to be satisfied, and being α_3 a positive constant, it can be written (23), whereby the equation (24) is obtained by replacing (20) in (23).

$$\frac{e_{vdq0}}{dt} = -\alpha_3 e_{vdq0} \tag{23}$$

$$\frac{v_{dq0_{ref}}}{dt} - \frac{v_{dq0_{BT}}}{dt} = -\alpha_3 e_{vdq0} \tag{24}$$

Through (24) the current $i_{vdq0_{ref}}$ can be obtained knowing that the current on the LV side corresponds to the capacitor current and, therefore, $i_{dqo_{BT}} = C_{f_{out}} \frac{v_{dq0_{BT}}}{dt}$.

$$i_{vdq0_{ref}} = C_{f_{out}} \alpha_3 e_{vdq0} + i_{dqo_{BT}} \tag{25}$$

The equation (25) allows the calculation of the reference current that is later used in the current predictive controller, I_{0ref}.

Regarding the DC bus output voltage control, the same reasoning explained for the AC control is applied, apart from the transformations between coordinates abc and $dq0$ and the inverse that are not applied.

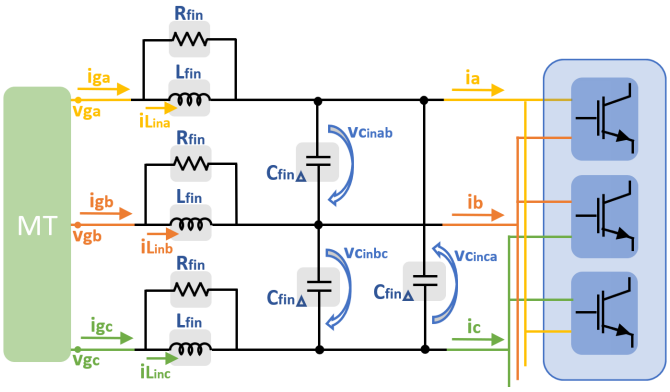

Fig. 9. Currents and voltages associated with the MV network, filter and ST input converters

V. MT Current Control

By the Predictive Control Method introduced in the section IV-A, it is possible to control the current of the MV network. This control is achieved by adding a new term in the cost function (17), [10]. Figure 9 represents the connection of the MV network, the input filter and the ST input currents and voltages.

In order to model the MV network, we start by obtaining the dynamics of the currents of the coils $L_{f_{in}}$, followed by the currents of the MV network and the voltages of the capacitors $C_{f_{in\ Delta}}$. Based on this dynamics, the currents in the input filter coils at the instant $t = k+$ are obtained, as well as the voltages of the input filter capacitors and the grid currents at that instant. It is based on the minimization of the component q of the current in the MV network at the instant $t = k+$, by the cost function, that a control of this current is obtained, similarly to the control of the LV current.

The currents in the coils in phase a, b and c of the MV network, that are $i_{L_{ina}}$, $i_{L_{inb}}$ and $i_{L_{inc}}$ respectively, contains the relation (26).

$$\begin{cases} v_{ga} = L_{f_{in}} \frac{di_{L_{ina}}}{dt} + v_{C_{inab}} - \frac{di_{L_{inb}}}{dt} + v_{gb} \\ v_{gb} = L_{f_{in}} \frac{di_{L_{inb}}}{dt} + v_{C_{inbc}} - \frac{di_{L_{inc}}}{dt} + v_{gc} \\ v_{gc} = L_{f_{in}} \frac{di_{L_{inc}}}{dt} + v_{C_{inca}} - \frac{di_{L_{ina}}}{dt} + v_{ga} \end{cases} \tag{26}$$

This relation, after simplified, written as a matrix and in $dq0$ coordinates corresponds to (27).

$$\begin{bmatrix} \frac{di_{L_{ind}}}{dt} \\ \frac{di_{L_{inq}}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix} \begin{bmatrix} i_{L_{ind}} \\ i_{L_{inq}} \end{bmatrix} + \\ + \begin{bmatrix} -\frac{1}{2L_{f_{in}}} & -\frac{\sqrt{3}}{6L_{f_{in}}} \\ \frac{\sqrt{3}}{6L_{f_{in}}} & -\frac{1}{2L_{f_{in}}} \end{bmatrix} \begin{bmatrix} v_{C_{ind}} \\ v_{C_{inq}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{f_{in}}} & 0 \\ 0 & \frac{1}{L_{f_{in}}} \end{bmatrix} \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix} \tag{27}$$

To obtain the currents of the MV network, we have (28).

$$\begin{cases} i_{ga} = i_{L_{ina}} + \frac{L_{f_{in}}}{R_{f_{in}}} \frac{di_{L_{ina}}}{dt} \\ i_{gb} = i_{L_{inb}} + \frac{L_{f_{in}}}{R_{f_{in}}} \frac{di_{L_{inb}}}{dt} \\ i_{gc} = i_{L_{inc}} + \frac{L_{f_{in}}}{R_{f_{in}}} \frac{di_{L_{inc}}}{dt} \end{cases} \tag{28}$$

Making the necessary approximations and the transformation to dq coordinates is obtained (29).

$$\begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \begin{bmatrix} i_{L_{ind}} \\ i_{L_{inq}} \end{bmatrix} + \begin{bmatrix} i_{L_{ind}} \\ i_{L_{inq}} \end{bmatrix} + + \begin{bmatrix} \frac{L_{f_{in}}}{R_{f_{in}}} & 0 \\ 0 & \frac{L_{f_{in}}}{R_{f_{in}}} \end{bmatrix} \begin{bmatrix} \frac{di_{L_{ind}}}{dt} \\ \frac{di_{L_{inq}}}{dt} \end{bmatrix} \tag{29}$$

The voltages at the input capacitors are (30).

$$\begin{cases} i_{ga} = C_{f_{in\Delta}} \frac{dv_{C_{inab}}}{dt} - C_{f_{in\Delta}} \frac{dv_{C_{inca}}}{dt} + i_a \\ i_{gb} = C_{f_{in\Delta}} \frac{dv_{C_{inbc}}}{dt} - C_{f_{in\Delta}} \frac{dv_{C_{inab}}}{dt} + i_b \\ i_{gc} = C_{f_{in\Delta}} \frac{dv_{C_{inca}}}{dt} - C_{f_{in\Delta}} \frac{dv_{C_{inbc}}}{dt} + i_c \end{cases} \tag{30}$$

The simplification of the voltages in the capacitors makes it possible to obtain (31).

$$\begin{bmatrix} \frac{dv_{c_{ind}}}{dt} \\ \frac{dv_{c_{inq}}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix} \begin{bmatrix} v_{c_{ind}} \\ v_{c_{inq}} \end{bmatrix} + \begin{bmatrix} \frac{1}{2C_{f_{in}}} & -\frac{\sqrt{3}}{6C_{f_{in}}} \\ \frac{\sqrt{3}}{6C_{f_{in}}} & \frac{1}{2C_{f_{in}}} \end{bmatrix} \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} + + \begin{bmatrix} -\frac{1}{2C_{f_{in}}} & \frac{\sqrt{3}}{6C_{f_{in}}} \\ -\frac{\sqrt{3}}{6C_{f_{in}}} & -\frac{1}{2C_{f_{in}}} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{31}$$

By the equations (27), (29) and (31) we obtain the respective voltages and currents at the instant $t = k+1$ and after working and simplified these equations, (32) is obtained.

The T_s value corresponds to the calculation step and $C_{f_{in\Delta}}$, $L_{f_{in}}$ and $R_{f_{in}}$ to the value of the capacitor, coil and resistance sized for the input filter. The current and voltage $i_{gdq}(k)$ and $v_{gdq}(k)$ are the MT current and MT voltage. $v_{gdq}(k+1)$ isthe voltage at the instant $K+1$ that, because it is not expected a large voltage variation, it is considered in the calculation equal to $v_{gdq}(k)$. $v_{C_{fin\Delta d}}(k)$ and $v_{C_{fin\Delta q}}(k)$ are the components d and q of the voltage of the input filter capacitors. The current $i_{dq}(k+1)$ corresponds to the input current of the ST input converters. This current can take several possible values through a set of combinations of the γ associated with the ST semiconductor states. Possible values of ST input currents are related to ST output current and semiconductor states as represented in (32).

$$\begin{cases} i_a &= i_{o1}\gamma_{s_A}(\gamma_{1_A} - \gamma_{3_A}) + i_{o2}\gamma_{s_B}(\gamma_{1_B} - \gamma_{3_B}) + \\ &\quad + i_{o3}\gamma_{s_C}(\gamma_{1_C} - \gamma_{3_C}) \\ i_b &= i_{o2}\gamma_{s_A}(\gamma_{2_A} - \gamma_{1_A}) + i_{o2}\gamma_{s_B}(\gamma_{2_B} - \gamma_{1_B}) + \\ &\quad + i_{o3}\gamma_{s_C}(\gamma_{2_C} - \gamma_{1_C}) \\ i_c &= i_{o3}\gamma_{s_A}(\gamma_{3_A} - \gamma_{2_A}) + i_{o2}\gamma_{s_B}(\gamma_{3_B} - \gamma_{2_B}) + \\ &\quad + i_{o3}\gamma_{s_C}(\gamma_{3_C} - \gamma_{2_C}) \end{cases} \tag{32}$$

The currents i_{o1}, i_{o2} and i_{o3} are the output currents of the first, second and third ST output phases and the gamma values corresponding to each ST converter. The γ_{1_A} and γ_{2_A} corresponds to the first and second input converters of the first conversion stage of the ST, respectively, and the γ_{3_B} and γ_{s_C} corresponds to the third input converter of the second conversion stage and the output converter of the third conversion stage of the ST, respectively.

From equation (33), the value of the component q of the MV network current, at the instant $k+1$, $i_{gq}(k+1)$, is obtained.

$$\begin{aligned} i_{gq}(k+1) = &\frac{3L_{fin}C_{fin\Delta}R_{fin}}{3L_{fin}C_{fin\Delta}R_{fin} + L_{fin}T_s + R_{fin}T_s^2} i_{gq}(k) \\ &- \frac{(\sqrt{3}C_{f_{in\Delta}}R_{f_{in}}T_s)\ v_{C_{fin\Delta d}}(k)}{6L_{f_{in}}C_{f_{in\Delta}}R_{f_{in}} + 2L_{f_{in}}T_s + \ 2R_{f_{in}}T_s^2} \\ &+ \frac{(3C_{fin\Delta}R_{finT_s})\ v_{C_{fin\Delta q}}(k)}{6L_{fin}C_{fin\Delta}R_{fin} + 2L_{fin}T_s + 2R_{fin}T_s^2} \\ &+ \frac{(L_{f_{in}} + R_{f_{in}}T_s)T_s}{3L_{f_{in}}C_{f_{in\Delta}}R_{f_{in}} + L_{f_{in}}T_s + R_{f_{in}}T_s^2} i_q(k+1) \\ &\frac{3C_{fin\Delta}(L_{f_{in}} + R_{f_{in}}T_s)}{3L_{f_{in}}C_{f_{in\Delta}}R_{f_{in}} + L_{f_{in}}T_s + R_{f_{in}}T_s^2} v_{gq}(k+1) \\ &- \frac{3C_{fin\Delta}L_{f_{in}}}{3L_{f_{in}}C_{f_{in\Delta}}R_{f_{in}} + L_{f_{in}}T_s + R_{f_{in}}T_s^2} v_{gq}(k) \end{aligned} \tag{33}$$

The cost function to be applied in the control of the first ST conversion stage with the new term associated with the ST input current control is (34), where α_4 is a constant.

$$\begin{aligned} f_{i_{o1}} = &\alpha_1 \left[i_{o1_{ref}}(k+1) - i_{o1}(k+1) \right]^2 + \\ &+ \alpha_2 \left[(\gamma_{1_A} V_{tr_{A1}})^2 + (\gamma_{2_A} V_{tr_{A2}})^2 + (\gamma_{3_A} V_{tr_{A3}})^2 \right] + \\ &+ \alpha_4 \left[i_{gq}(k+1) \right] \end{aligned} \tag{34}$$

Regarding the control of the ST input currents at the level of the DC bus, the same method explained for the control of the AC conversion stages is applied. The minimization of (33) is applied to the DC control cost function, which depends on the combinations of γ associated with the converters of this link. With γ_{1_D}, γ_{2_D} and γ_{3_D} associated with the first, second and third input converters of the DC link conversion stage, respectively, and γ_{s_D} associated with the output converter of that same stage, the cost function associated with the DC link control is represented in (35).

$$\begin{aligned} f_{i_{0_{DC}}} = &\alpha_1 \left[i_{oDC_{ref}}(k+1) - i_{o_{DC}}(k+1) \right]^2 + \\ &+ \alpha_2 \left[(\gamma_{1_D} V_{tr_{D1}})^2 + (\gamma_{2_D} V_{tr_{D2}})^2 + (\gamma_{3_D} V_{tr_{D3}})^2 \right] + \\ &+ \alpha_4 \left[i_{gq}(k+1) \right] \end{aligned} \tag{35}$$

VI. Results

This section presents the simulation of the ST in the electrical grid, its study and analysis of its operation. The results are obtained through the MATLAB/Simulink software and the LV current and voltage controls are applied.

A. ST operation on MT/BT connection

In order to simulate and study the ST performance in the electrical network, the parameters that characterize the ST are defined. The ST operates as a voltage converter for $10kV/400V$, thus connecting the MV and LV network. The work frequency of the transformer is $50000Hz$ and both ω_{MT} and ω_{BT} correspond to $2\pi.50$ $[rads^{-1}]$. The load used in the BT network simulations is resistive and has a value of 1Ω.

The three-phase voltages of the MV network side for the operating conditions presented are represented in Figure 10.

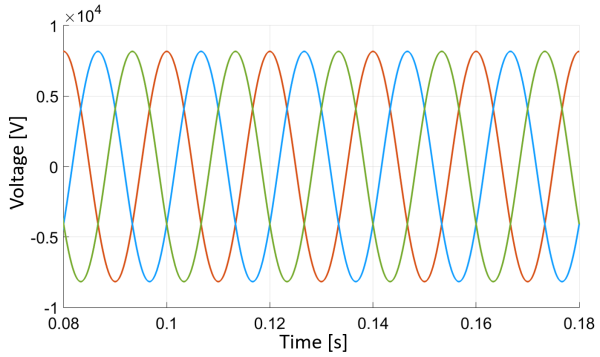

Fig. 10. Three-phase voltage on the MV side in normal MV/LV operation

As described in the ST control section, we ensured that the average value of the voltages at the input of the transformer was null so as not to saturate it. In Figure 11 it can be seen that the average value of the voltage at the input of the transformer corresponds to an approximately null value.

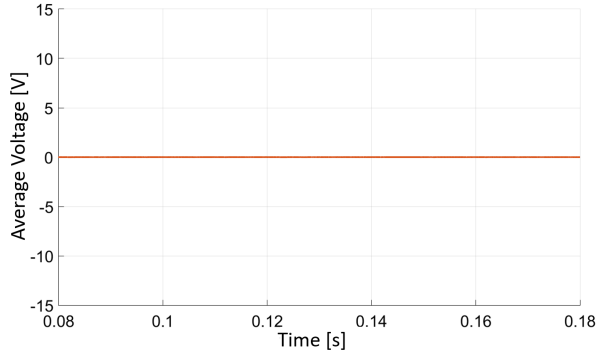

Fig. 11. Average value of the transformer input voltage for one of the ST input converters under normal MV/LV operation

The voltage obtained from the LV side is represented in Figure 12, where the good dimensioned and applied control can be confirmed. This good result is further supported by the error measured between the reference voltage and the voltage measured at each instant as shown in Figure 13.

The error associated with voltage corresponds to a value less than 1%, which is perfectly acceptable and demonstrates the good operation of the system. Furthermore, the load currents and respective reference currents are shown in Figure 14, where the good current tracking achieved with the applied control system is observed.

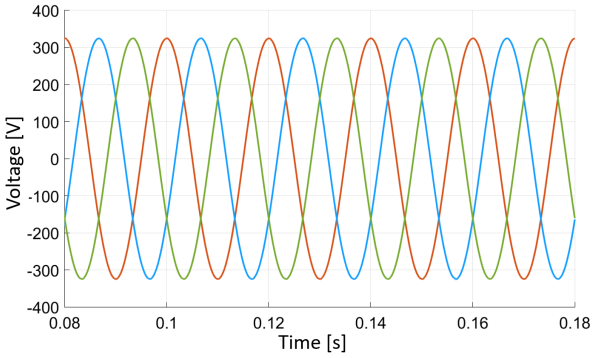

Fig. 12. Load voltage in normal MV/LV operating situation

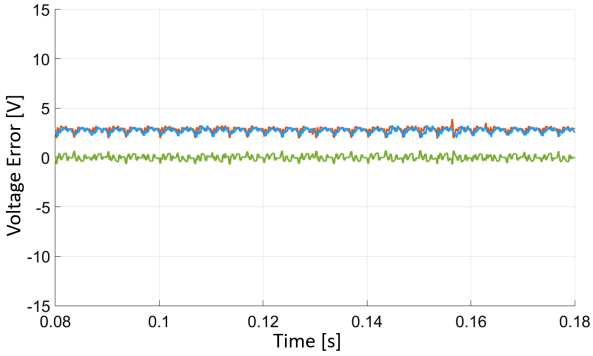

Fig. 13. LV voltage error, d (blue), q (orange) and 0 (green) components in normal MV/LV operation

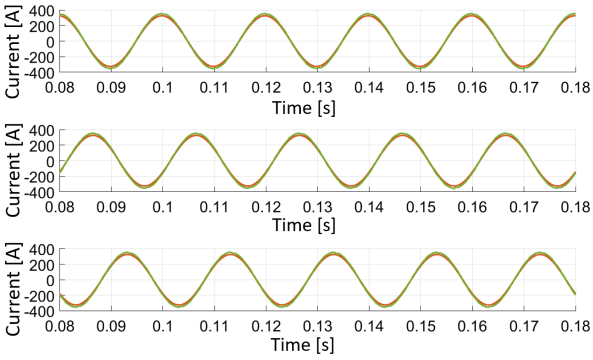

Fig. 14. Current on the LV side (orange) and its reference current (green) in normal MV/LV operation

B. EV Charging

In addition to its operation in the electrical grid, the ST has the possibility of simultaneous operation of its DC link. In this section is presented the charging of an EV while the ST performs its functions in the electrical grid.

In accordance with IEC 61851 standards and IEC 62196, 4 charging modes can be defined, where the fourth mode corresponds to DC charging whose voltage can go up to $600V$ and a maximum current of $400A$. Based on these values, a DC link on the ST was dimensioned for charging electric cars, EV, with a charging power of up to $240kW$. In Figure 15 it is possible to observe the evolution of the voltage and current

of the EV, which starts charging at the instant $0.1s$.

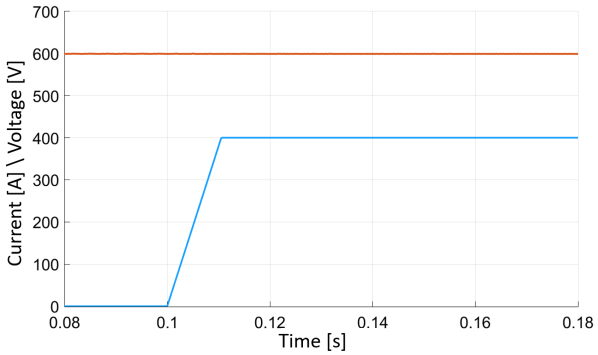

Fig. 15. Voltage (orange) and current (blue) during EV charging

While the EV is charging, the ST operation on the electrical grid remains identical to the one verified without any charging associated with the ST DC link. The Figure 16 shows the evolution of the voltage that is supplied by the ST to the LV network, which is shown not to be influenced by the use of the ST's DC link when charging an EV.

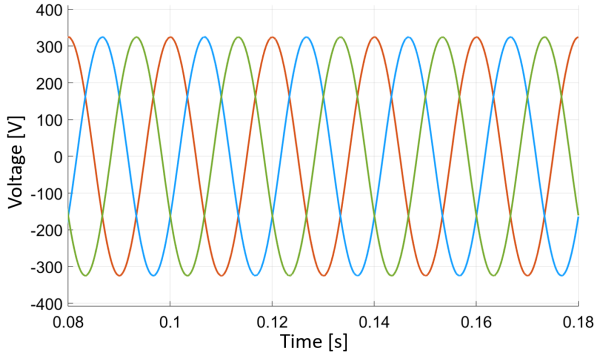

Fig. 16. BT voltage in MT/BT operation and simultaneous EV charging

The LV current with its tracking in relation to the reference current is almost the same as represented in the MT/BT operation. Regarding the error associated with the reference voltage and the voltage on the LV network load is reduced, corresponding to a value lower than 1%. The ST DC link voltage error is less than 0.5% and can be seen in Figure 17.

C. MT Voltage Dip

The ST has the ability to mitigate voltage disturbances that come from the MV side from passing to the LV side by continuously controlling the output voltage. In this way, it is expected that when there is a voltage dip, (sag), in the MV network, it will not be reflected on the LV side, contrary to what is expected with the application of LFTs. In Figure 18 it is possible to verify the disturbance applied to the MV voltage and that is applied to the ST. The presented sag is characterized by a reduction in wave amplitude of 25% compared to the initial voltage wave and the duration of 2 mains cycles.

The error between the LV reference voltage and the load voltage has a slight increase during the grid period in which

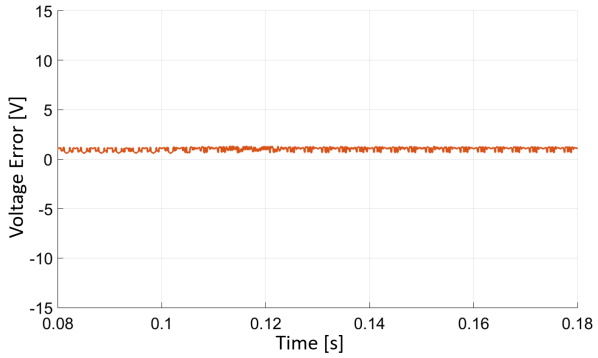

Fig. 17. DC voltage error in MT/LV operation and simultaneous EV charging

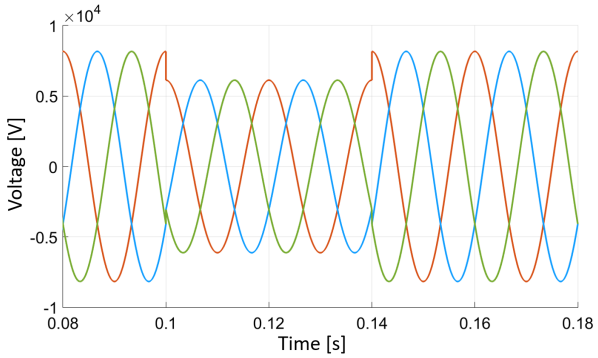

Fig. 18. MV tryphasic voltages with the presence of a voltage dip

the sag occurs. Even so, the error does not have a significant increase and remains below 1%. Thus, a load voltage is obtained that does not have any relevant influence of the existing disturbance on the MV network. In Figure 19 the LV voltage is shown.

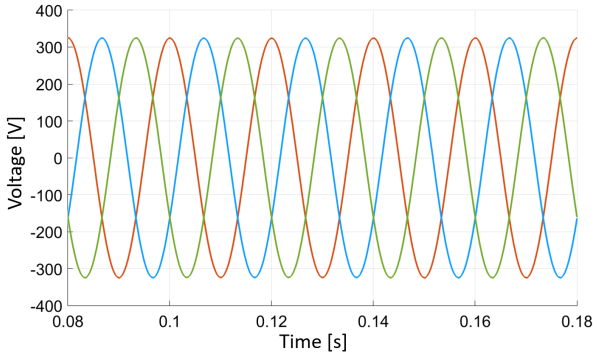

Fig. 19. Voltage on the LV side in the presence of a voltage dip in the MV network

As expected, after the disturbance in the MV network, the controller acts to correct this distortion. No disturbance is felt in the load and thus concludes the good operation of the system in the presence of sags in the MT.

D. Current injection into the MV network

In order to study the capacity of the ST to supply current from the DC bus to the MV network, a simulation of current

injection into the grid with the connection to the LV network disconnected was carried out. In this case it is simulated a voltage and current of $600V$ and $400A$, just like the charging voltage and current of an EV in the VI-B section and applied a second order double filter, that is, two of the ST-sized input filters in section III in series. In Figure 20 it is possible to observe the three-phase current supplied to the MV network.

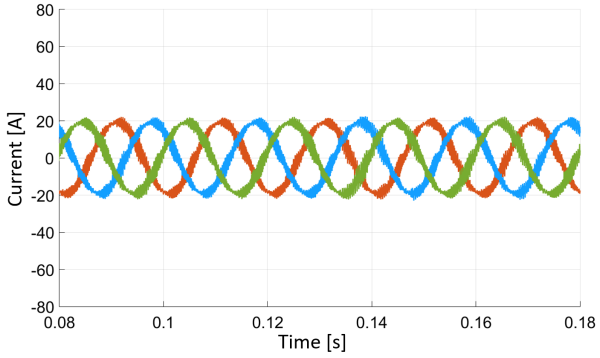

Fig. 20. Three-phase currents of the MV network injected through DC link

In Figure 21 it can still be observed a slight lag between the voltage and current MV resulting from the input filter. The waves represented are almost in phase opposition, as expected, as it is a current injection.

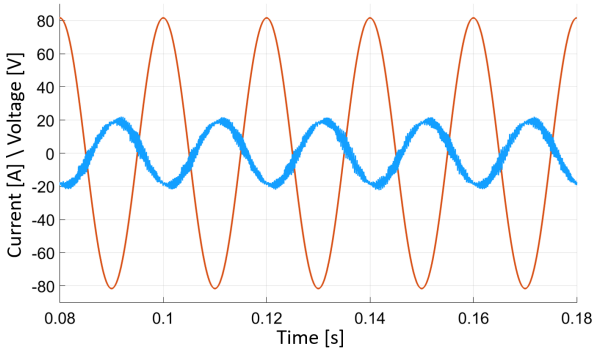

Fig. 21. Current (blue) in a phase of the MV network injected through the DC bus and voltage (orange) of the MV network scaled by a factor of $1/100$

With this last simulation, the good control of the MV network currents is proven, based on the suggested method to be applied in section V.

VII. Conclusion

The main objective of this work was the development of an ST, which could be integrated into the electrical grid. This would allow a greater control over the grid voltage and, with the DC link, offer the possibility of charging EV's. After planning the ST topology, dimensioning filters and defining control methods, the tests in a simulation environment allowed us to conclude that the ST responds to several limitations of the LFT's. The main aspects that were taken into account in the development of this work were the non-saturation of the high frequency transformer, as well as the correct supply of AC and DC voltage and current to the LV network so that the ST would a good candidate for implementation in the electrical grid in the future.

The simulations demonstrates the potential of the system proposed in this dissertation and some of the advantages that this ST brings to the electrical grid. With further study of the system and laboratory implementation of a prototype, the ST developed in this dissertation has all the conditions to be implemented in the electrical grid, with the control and autonomy of grid management that is not possible with the currently implemented transformers.

Acknowledgment

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