130 nm CMOS Temperature sensor front-end for IoT applications

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***Abstract*—Temperature is one of the most important physical parameters that must be carefully monitored and quantified. The temperature of a significant number of applications and environments can be controlled with temperature sensors. For example, the agriculture industry needs a constant and careful examination of the ambient temperature as it directly affects the environment, this temperature control can be done with sensors. The evolution of the Internet of Things (IoT) systems adds the extra capability of measuring anytime and almost anywhere.**

The CMOS technology evolution and development allows the development of low cost and ultra-low power sensors, using a single chip implementation. This work presents the development of a front-end circuit developed in UMC 130 nm CMOS technology for ambient temperature sensor with a 1 $^{\circ}C$ resolution. To design this circuit, a careful study of the temperature behaviour in the most commonly used devices and components like BJTs, MOSFETs and resistors, was made. The most common voltage and current reference circuits were also studied. Following this theoretical analysis, a prototype is presented to identify the best options for the circuit.

***Index Terms*—130 nm, BJT, CMOS, IoT, MOSFET, Temperature sensor, ultra-low power.**

I. Introduction

Temperature is one of the most important physical parameter, so it must be accurately quantified. Some applications, for example, biomedical, pharmaceutical and environmental control for agriculture require the monitorization of the temperature which can be made using sensors.

A smart temperature sensor can be designed with electronic components. The most common temperature sensors are designed with Bipolar Junction Transistor (BJT) or Metal Oxide Semiconductor Field Effect Transistor (MOSFET), using the temperature characteristics of the transistors junctions. When designing a temperature sensor the main focus should be on the resolution, size, accuracy, autonomy, process dispersion and supply voltage insensitivity.

The Complementary metal–oxide–semiconductor (CMOS) technology can be used to design these types of sensors with low cost and ultra-low power consumption. Additionaly, a single chip implementation can be done. This is a big advantage because there is no need for additional and external circuits.

As the temperature affects components each device must carefully be studied. Especially when designing a temperature sensor to guarantee its correct behaviour.

This work is divided in 3 sections. Section 2 will present the state of the art of some of the existing temperature sensors. In Section 3 the developed temperature sensor is presented. Finally, in Section 4 a conclusion and future work is presented.

A. Motivation

The evolution and development of the Internet of Things (IoT) has created the possibility of everything, located anywhere, to connect to the internet. A big part of the developed technology will be a node in a wireless sensor node for environment measurements applications. These systems must be carefully controlled to avoid malfunctions.

One of the many applications for these sensors is in agriculture where almost every production process has temperature dependencies. A sensor to monitor and control is highly useful. The sensor should focus on having a low power consumption and to be energy efficient. For its use in agriculture is important that the sensor has a long life time, even more because the temperature measurement will be made periodically. An important function of the sensor is also in fire detection. The sensor should sound an alarm if the temperature is above the chosen value of 65 $^{\circ}C$.

I was motivated to choose this thesis because I found nanotechnology the most interesting part in electronics. The application in which this project will be used also aroused my attention because I have become aware of the role of agriculture nowadays. This work allowed me to combine my interest in technology, most specifically nanotechnology, and applied it to my newly discovered interest in agriculture. I find it a funny coincidence that my middle name "Fazendeiro" some years ago was related to someone that a farm and therefore connected to agriculture.

B. Objectives

The objective of this work is to develop and design the front-end of an ultra-low power temperature sensor to be used in agriculture applications. The focus should be on energy consumption reduction, temperature range and resolution.

The sensor should be developed in 130 nm CMOS mixed-mode RF technology from UMC manufacturer. *Cadence Design Environment* software will be used. The ADC that will be is already available and has VLSB of 2.56 mV with a ENOB of 10.97 after layout extraction. Ideally the temperature sensor should have an inaccuracy of ± 0.25 $^{\circ}C$ over the range of -25 $^{\circ}C$ to 80 $^{\circ}C$, using a 1.2 V power supply. In a later stage of the project a 1-point calibration to improve the sensor is a possibility.

II. State of the Art

The wireless sensor nodes development is growing at a fast pace and so it is important to have ultra-low power to have long lifetime (years) systems. The temperature must be monitored to ensure the proper work of the devices. This work presents the development of a voltage-based temperature sensor. As the IoT applications begin to be more common a low supply voltage is needed to achieve ultra low power, as well as the circuits should be powered by nano-ampere currents.

The following table presents the comparison between the temperature sensors of the referenced articles:

TABLE I: State of the Art of the Temperature Sensors

Reference	[3] JSSC-2005	[4] ITCS-2018	[5] ISCC-2019	[6] ISSCC-2013	[7] ITCS-2020	[8] APMC-2019	[9] SSCL-2019	[12] JSSC-2019	[13] SSCL-2020	[14] SSCL-2020
Sensor Type	BJT	BJT	BJT	MOSFET	MOSFET	OSC	Resistor (PPF)	Resistor	Resistor	Resistor
Technology (um)	0,7	0,18	0,04	0,18	0,18	0,18	0,065	0,18	0,065	0,18
Area (mm2)	4,5	0,1	0,03	0,0003286	0,45	0,11	0,058	0,068	0,0017	0,12
Supply Voltage (V)	2,5-5	1,6-2	1,2	1,8	1,8	0,65	0,85-1,3V	1,8	0,6/1	1,6
Power Consumption (uW)	247,5 (*1)	0,864	13,5	1,026	1,99	1,3	32,5	1600	0,109	6,6
Temperature Range (ºC)	-55~125	-30~120	-20~100	-20~100	-20~ 80	-15~65	-50 ~125	-35~125	-20~120	27,5~47,5
Trimming points	1	1	Untrim,	1	2	2	1 or 2	2	2	1
Inaccuracy (ºC)	±0,1	±0,85	±0,8	0,17/-0,21	0,5/-0,44 (*2) 0,66/-0,73 (*3)	0,27/-0,3	±1,2 (*4) ±0,16 (*5)	±0,35	4,3/-2,5	0,2/-0,1
Energy/Conversion (nJ)	24750	6,9984	13,5	1026	49,75	130	32,5	528	0,00218	52,8

(*1) At 3.3 V. (*2) Min. value. (*3) Max. value. (*4) 1-point calibration. (*5) 2-point calibration.

The main focus when comparing the sensors were the temperature range, area, accuracy and energy/conversion power. The same sensor can not have a small area, good accuracy and a low energy for each conversion, there needs to be a trade off between one characteristic to benefit another.

The BJT-based temperature sensors are the most common because they are easier to develop due to the linear temperature characteristics. The sensor in [3] has the best accuracy of $\pm$ 0.1 $^{\circ}C$ at the cost of a larger area of 4.5 mm^2 and a high energy of 24750 nJ conversion. This sensor also has the largest range of temperatures and a single point calibration. In [4] and [5] the sensors consume the lowest energy for a temperature conversion and have a small area of 0.1 mm^2 and 0.03 mm^2. Both present almost the same inaccuracy of $\pm$ 0.85 $^{\circ}C$ and $\pm$ 0.8 $^{\circ}C$, respectively. However, the first sensor has a 1 point calibration point while the second does not need calibration. The sensor in [4] has a larger temperature range than the sensor in [5].

The MOSFET-based sensors do not have as linear temperature characteristics as the BJT-based sensors, so additional calibration is required as seen in [6] and [7] that need a 1 and 2 point calibration. With this calibration points these sensors present a good accuracy. These sensors have a larger conversion energy and do not have a temperature range as wide as the BJT sensors.

Every resistor-based sensor studied have calibration points and present a good accuracy except the sensor in [13]. Overall these sensors have a small area but it is consumed a lot of energy for a conversion.

III. Temperature Sensor Frontend

In this section it is presented the methodology behind the development of the final circuit. Following the previous studies it was decided to design the circuit using only PMOS transistors. It should be kept in mind that the final circuit will be globally optimized to obtain better results.

The final PTAT circuit can be made based on a voltage or current reference. Using a voltage reference, a transistor powered by this voltage will have the VSG almost stable and with the proper dimensions a CTAT output voltage will be generated. Combining two of these circuits the subtraction of the CTAT signals can be made to generate the desired PTAT signal. Using a current reference, a current mirror with a transistor can be made and both CTAT signals obtained.

Based on the method presented in article [17], it was decided to design a current reference circuit. This method consists in the generation of a stable current by controlling the body voltage of a transistor. Initially the circuit presented in Figure 1, with the dimensions in Table II, was designed to study the current behavior.

TABLE II: Figure 1 dimensions

Transistor	W; L
M1	W = 1 μm; L = 5 μm
M2	W = 100 μm; L = 1 μm

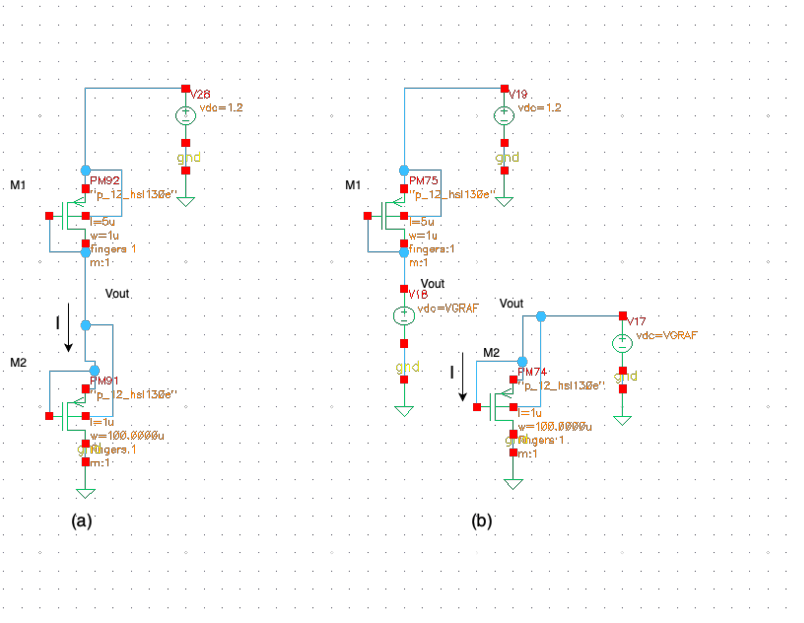

Fig. 1: Current behaviour: (a) global circuit, (b) partial circuits.

As a starting point a graphical study was made based on simulation results. The partial circuits were simulated for temperatures of 0 $^{\circ}C$, 27 $^{\circ}C$ (nominal temperature) and 50 $^{\circ}C$. For the given temperatures the current (I) and output voltage (Vout) were obtained in Figure 2.

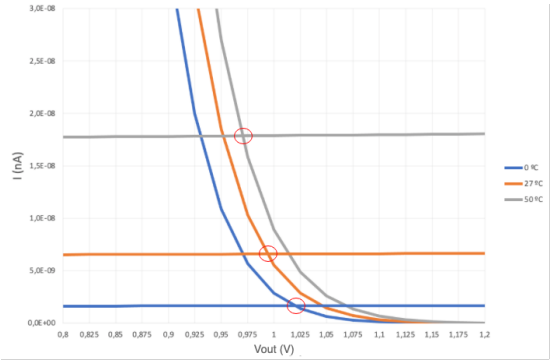

Fig. 2: Current (nA) in function of Vout (V).

By combining the obtained results each interception represents the current and output voltage for the given temperature. The top interception is for 50 $°C$ (represented in grey), the middle interception for 27 $°C$ (represented in orange) and the bottom interception is in 0 $°C$ (represented in blue). This means that the current will increase with temperature, as expected.

The output voltage is presented in Figure 3.

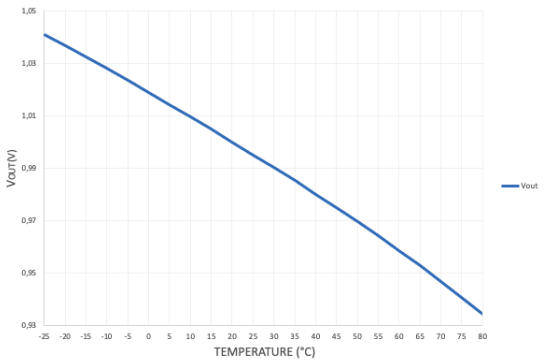

Fig. 3: Vout (V).

And the output current in Figure 4.

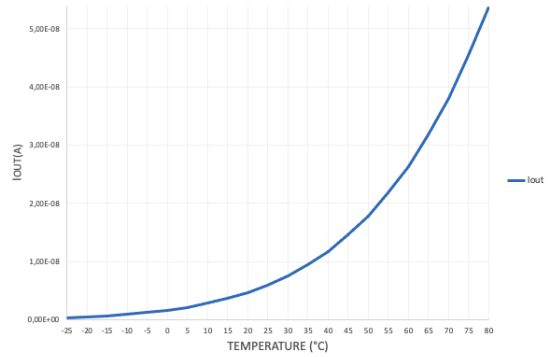

Fig. 4: Iout (A).

This circuit does not generate a stable current reference, nor voltage reference but Vout varies much less than Iout. Following the method presented in [17] an attempt was made to control the voltage of M2´s body to compensate the current variations. So, it was important to understand how the voltage at the body will impact the circuit current. The circuit of Figure 5 was simulated with new dimensions, presented in Table III.

TABLE III: Figure 5 dimensions

Transistor	W; L
M1	W = 1 μm; L = 20 μm
M2	W = 40 μm; L = 1 μm

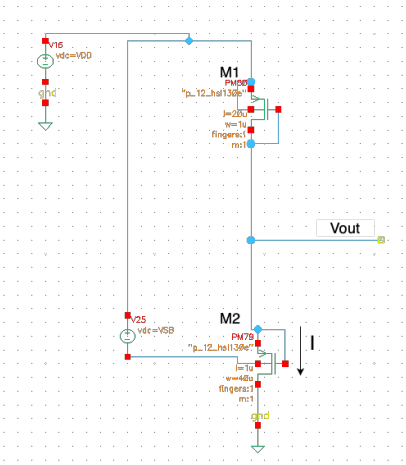

Fig. 5: Body effect study in circuit of Figure 1.

The simulations were made for the nominal temperature of 27 $°C$, 0 $°C$ and 50 $°C$ in terms of VDD. By specifying the temperatures it is easier to observe the different current (Iout) values of each one. The currents obtained are presented in Figure 6.

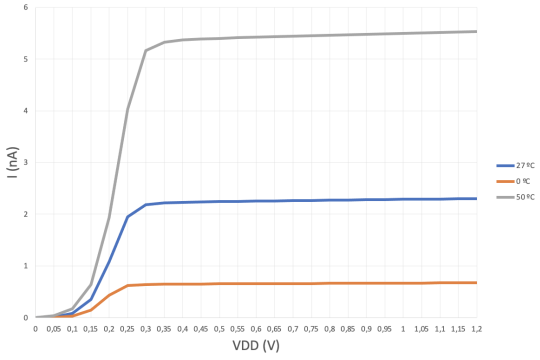

Fig. 6: I (nA) for temperatures of 0$°C$, 27$°C$ and 50 $°C$ in function of VDD.

It is easily observed that the current has a large increase with the temperature increment. In all simulations the current becomes stable with VDD around 0.3 V. So, as the temperatures become stable around the same value it is possible to match the currents values. A new simulation was made, fixing the VDD - Vbody = 0.2 V for the 27 $°C$ and changing this voltage for the other temperatures. The values of the currents match with VDD - Vbody = 0.43 V for 0 $°C$ and 0.02 V for 50 $°C$ were obtained. The results are presented in Figure 7.

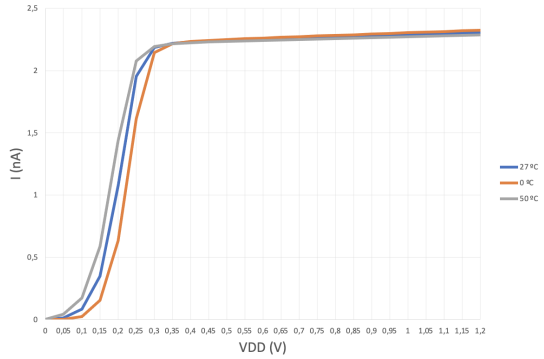

Fig. 7: I (nA) for a voltage VDD - Vbody = 0.2 V for 27 $°C$, 0.43 V for 0 $°C$ and 0.02 V for 50 $°C$.

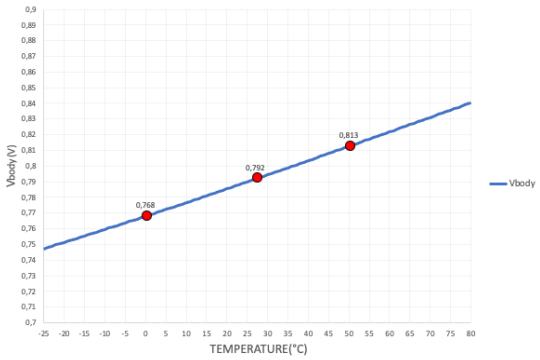

Fig. 9: Body voltage (Vbody) generated.

TABLE IV: Body voltage for each temperature

Temperature	Vbody voltage (Vbody)
0 $°C$	770 mV
27 $°C$	1 V
50 $°C$	1.18 V

These simulations concluded that the body effect changes the transistor´s temperature behaviour, and a stable current reference can be generated. The next step is to design the complete current reference circuit where Vbody should be generated in order to obtain the values of Table IV.

The designed circuit is presented in Figure 8. The method of [17] was followed for the the Vbody generation. In this circuit the Vbody is generated with transistors MP1, MP2, MPZ1 and MPZ2 that are connected as active charges.

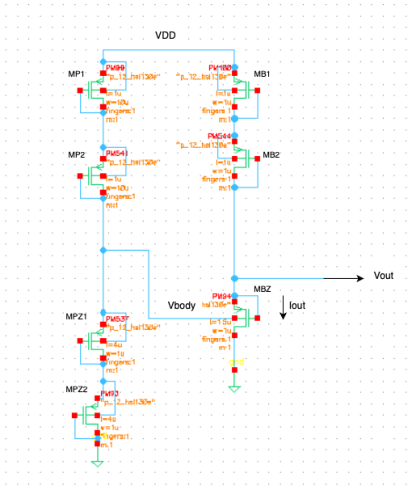

Fig. 8: Reference circuit.

The circuit was simulated with the dimensions in Table V.

TABLE V: Figure 8 dimensions

Transistor	W; L
MP1, MP2	W = 10 μm; L = 1 μm
MPZ1, MPZ2	W = 4 μm; L = 1 μm
MB1, MB2	W = 1 μm; L = 1 μm
MBZ	W = 1 μm; L = 1.5 μm

The generated Vbody is presented in Figure 9.

The Vbody increases with temperature accordingly with the previous study, where an increasing voltage at the body of MBZ is used to compensate the current of the transistor. However, the voltage values are not the ideal ones previously calculated. In 0 $°C$ the voltage is around 770 mV as desired but in the following temperatures, 27 $°C$ and 50 $°C$ the voltage cannot achieve the values necessary to properly affect the body. So it is expected that the currennt will not be stable.

The output current (Iout) was simulated in Figure 10.

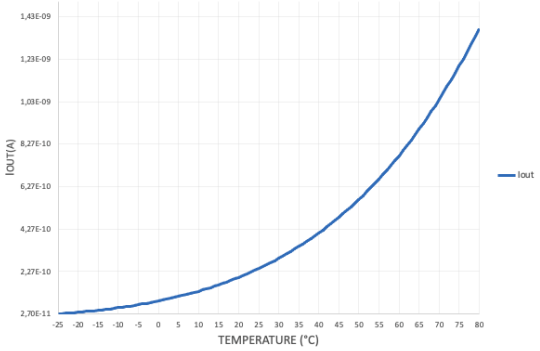

Fig. 10: Output current (Iout) generated.

The output current has an almost exponential growth with temperature, and so the Vbody generated cannot affect this current properly to make it a reference. The circuit was simulated with different dimensions and number of transistors and the current behaviour compensation was impossible to achieve.

With the current not behaving as expected the output voltage was simulated and represented in Figure 11.

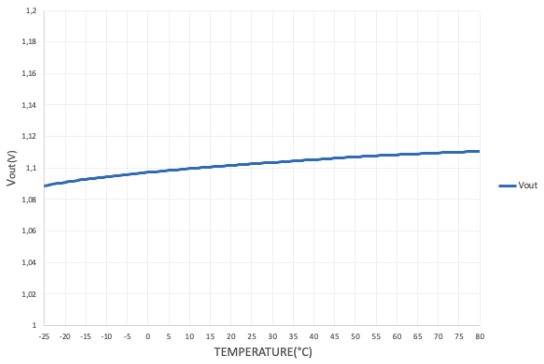

Fig. 11: Output voltage (Vout) generated.

The output voltage (Vout) approximately behaves as a voltage reference, at around 1.12 V. As the circuit is able to generate an approximate voltage reference it was decided to develop the circuit using this reference instead of the current reference initially thought.

At this point there are two options: the first one is to obtain a circuit that with this voltage reference directly generates the desired PTAT signal and the second one to design a circuit that generates two CTAT signals whose subtraction gives the desired PTAT signal. As the ADC that will be used has differential inputs the second approach will be chosen.

The two CTAT signals VSG1 and VSG2 were generated using the circuit presented in Figure 12.

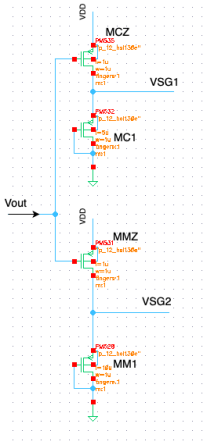

Fig. 12: CTAT generation circuit.

Using the dimensions presented in Table VII.

TABLE VI: Figure 12 dimensions

Transistor	W; L
MCZ	W = 1 μm; L = 1 μm
MC1	W = 1 μm; L = 5 μm
MMZ	W = 1 μm; L = 1 μm
MM1	W = 1 μm; L = 10 μm

the generated VSG1 and VSG2 are presented in Figure 13.

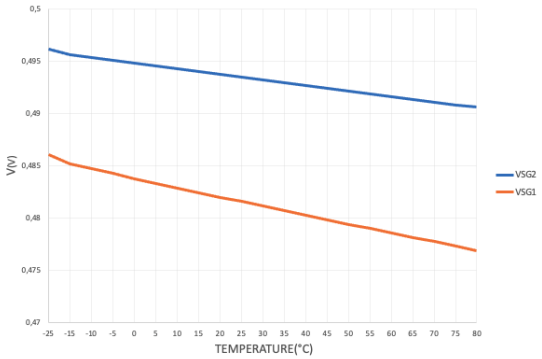

Fig. 13: VSG1 and VSG2 generated.

Both signals are CTAT with different slopes, the VPTAT signal will be given as the subtraction of the voltages and is presented in Figure 14.

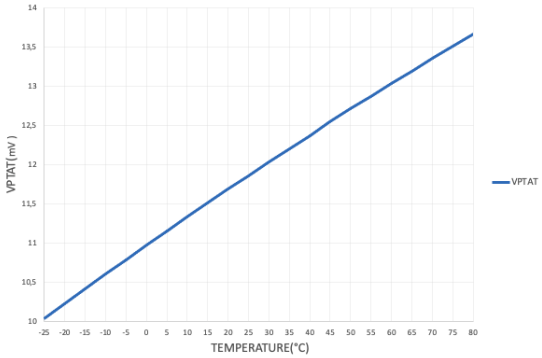

Fig. 14: VPTAT signal obtained.

This circuit was designed to show the technique to obtain the PTAT output voltage using the subtraction of two CTAT voltages. The transistors used and dimensions are not proper set to obtain the desired ΔVPTAT full range, because in this case a ΔVPTAT of around 4 mV is only obtained.

The VLSB of the ADC that will be used is 2.56 mV and so for a range of -25 $^{\circ}C$ to 80 $^{\circ}C$ (ΔT = 105 $^{\circ}C$) the required ΔVPTAT for 1 $^{\circ}C$ resolution should fulfill:

$$\frac{\Delta \text{VPTAT}}{\Delta \text{T}} > \text{VLSB} \tag{1}$$

so the ΔVPTAT range should be higher than 259 mV.

To increase the ΔVPTAT the complete front-end composed of Vbody generation, Vout generation and VCTAT generation, and additional transistors, was globally optimized. The final front-end is presented in Figure 15.

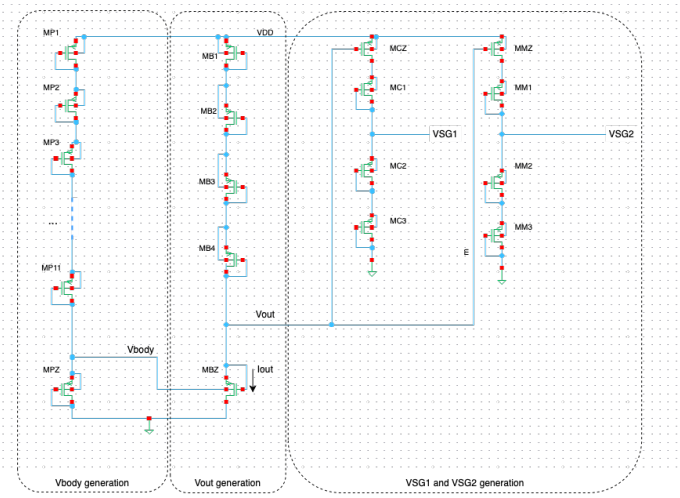

Fig. 15: Front-end circuit.

Using the dimensions presented in Table VII.

TABLE VII: Figure 15 dimensions

Transistor	W; L
MP1, ..., MP11	W = 100 μm; L = 1 μm
MPZ	W = 1 μm; L = 50 μm
MB1, ..., MB4	W = 100 μm; L = 1 μm
MBZ	W = 56 μm; L = 1 μm
MCZ	W = 1 μm; L = 1 μm
MC1, ..., MC3	W = 54 μm; L = 1 μm
MMZ	W = 1 μm; L = 1 μm
MM1, ..., MM3	W = 1 μm; L = 50 μm

The final body voltage generated is presented in Figure 16.

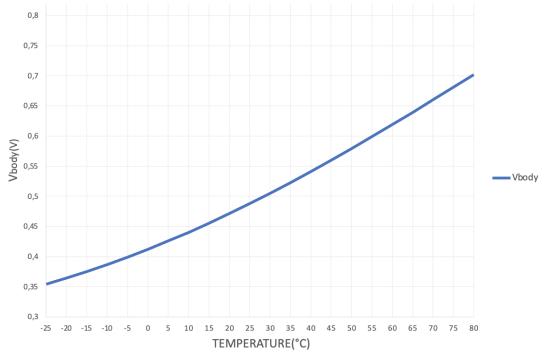

Fig. 16: Body voltage (Vbody) generated.

The nominal Vbody increases from around 350 mV to 700 mV and will affect the body of the MBZ transistor. The optimization results obtained this voltage instead of the previously presented in Figure 9 that was in the range around 750 mV to 850 mV.

The MBZ transistor is connected as a current source and with the addition of the diode connected transistors MB1 through MB4 is responsible to generate the output voltage (Vout) presented in Figure 17.

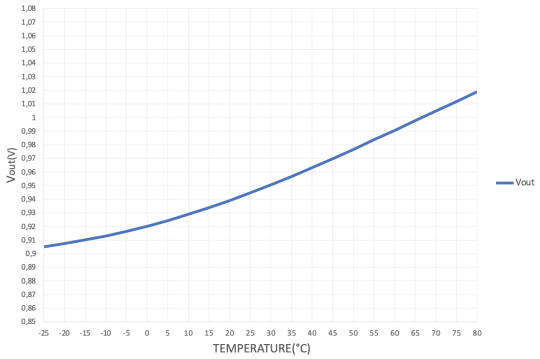

Fig. 17: Output voltage (Vout) generated.

The Vout has a variation of 100 mV around 900 mV to 1 V, instead of the previously obtained in Figure 11 that was more close to a reference voltage.

The circuit was simulated taking into account dispersion parameters (corners simulation). For each signal it is presented its nominal value as well as the result with the SS (slow-slow) and FF (fast-fast) corner as only PMOS transistors were used.

Finally for the CTAT voltage generation the VSG1 and VSG2 signals are obtained and presented in Figure 18 and Figure 19.

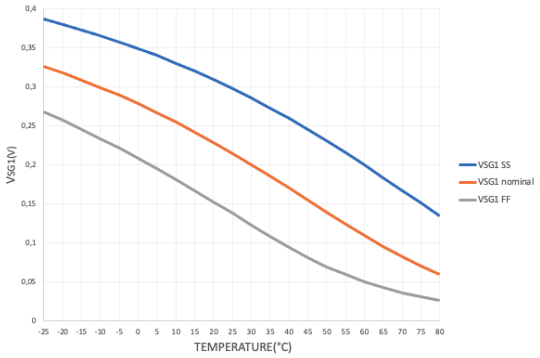

Fig. 18: VSG1 generated.

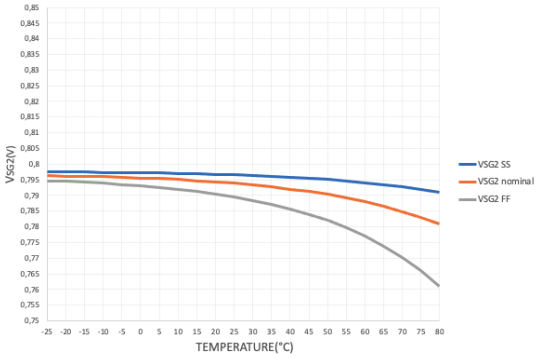

Fig. 19: VSG2 generated.

The VSG1 signal is clearly a CTAT signal and suffers from process dispersion. However, the VSG2 signal is almost stable with a small decrease with temperature. These signals were obtained to generate the PTAT signal with a ΔVPTAT

higher than 259 mV as previously mentioned. This result was obtained using the optimization functionality of the *Cadence Design Environment*. The optimization was tried with:

- an increasing Vbody from 500 mV to 900 mV
- a reference Vout around 800 mV
- the VSG1 and VSG2 CTAT voltages around 600 mV to 750 mV
- ΔVPTAT $>$ 259 mV

The simulator did not find any circuit that could match all of this requisites, so the final simulation was made only with ΔVPTAT $>$ 259 mV to meet the requirement needed to work with the ADC. The obtained VPTAT signal is presented in Figure 20.

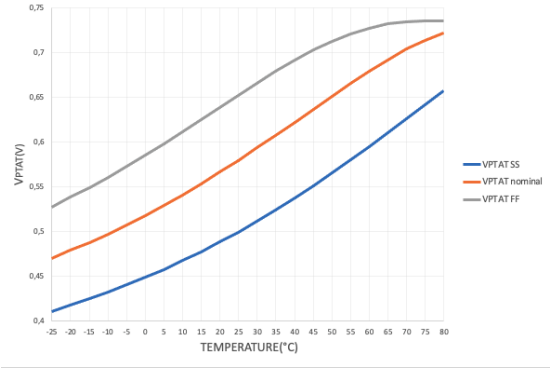

Fig. 20: VPTAT obtained.

The obtained VPTAT has a ΔVPTAT of 265 mV and so it checks the requisite. The voltage increases with temperature but is not linear in FF corner for higher temperature valies it also suffers from process dispersion. This was the best VPTAT voltage obtained. The way to improve this voltage and the process dispersion effect is through a 1-point calibration that can be digitally implemented.

To calculate the power consumption of the front-end circuit the current was simulated and is presented in 21

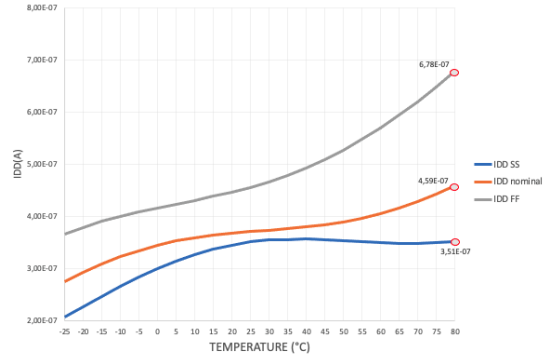

Fig. 21: Front-end circuit current (IDD).

The nominal current value of the circuit is 459 nA, meaning a power consumption of 550 nW. The current suffers from process dispersion so considering the maximum value of 678 nA the circuit will consume around 813 nW.

In Figure 22 the VPTAT in function of VDD was obtained, the voltage increases with VDD.

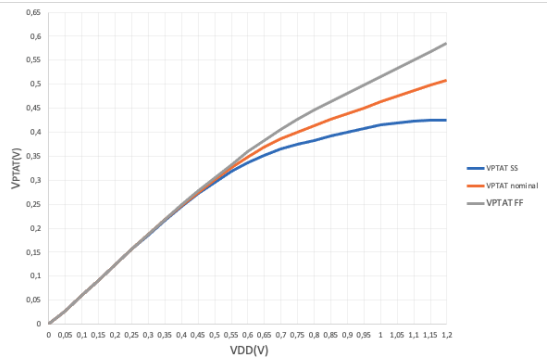

Fig. 22: VPTAT(V) in function of VDD.

The VDD dependency comes mainly from the Vbody generation. This voltage was generated using transistors connected as active charges meaning that there is a VDD dependency. Unfortunately, there was not enough time to eliminate this dependency but a possible solution would be to generate the Vbody using one transistor connected as a current source.

IV. Sensor System and Simulations

An analog-to-digital converter (ADC) is necessary to convert the measurements of the sensor to a digital temperature value. The most common type of ADC for low power consumption are the successive approximations ADC (SAR ADC) [3], [15], Sigma-Delta ADC ($\Sigma\Delta$ ADC) [7], and incremental ADC (IADC) [5]. The choice of the ADC for the sensor should rely on the resolution instead of the conversion speed because the temperature values are not expected to change of a sudden.

For this sensor the SAR ADC in [15] was chosen because of its ultra low-power consumption and the efficiency of the conversion process.

The parameters of the SAR ADC are presented in Table VIII.

TABLE VIII: SAR ADC characteristics.

Supply Voltage (V)	Resolution	ENOB
1.2	10 bit	$8.87^{(*1)}$

(*1) - After layout extraction.

The resolution of the ADC will affect the resolution of the sensor, a better resolution of the ADC would mean a better accuracy in the temperature reading.

In order to test the front-end circuit was added to this test bench as shown in Figure 23.

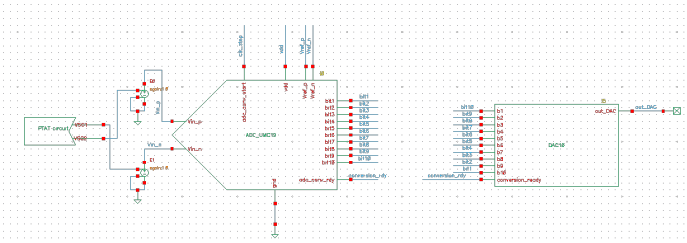

Fig. 23: Temperature sensor test bench.

The ideal DAC was developed in Verilog-A code to convert the 10-bit word from the ADC into an analogue voltage [15]. The input voltages V_{in+} and V_{in-} are the differential inputs of the ADC. The conversion ready signal indicates the ADC when to perform a conversion. And the out_Dac is the output analogue voltage. The VSG1 and VSG2 voltages are connected to the differential inputs of the ADC with the addition of two buffers due the high input impedance of the ADC. If the ideal buffers were not added the capacitors of the ADC would take more time to charge leading to a higher current consumption. Performing a full simulation for the temperature range of the -20 $°C$ to 80 $°C$ in the conversion time of 517 μs it was obtained the results of Figure 24.

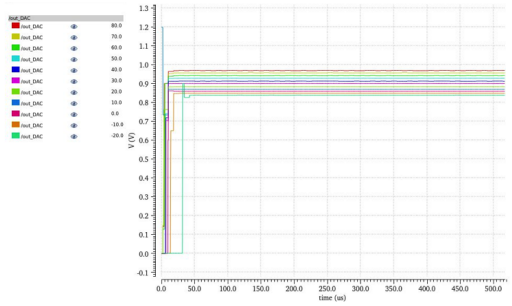

Fig. 24: Output analogue voltage (out_DAC) with temperatures -20 $°C$ to 80 $°C$.

Until 50 μs the ADC has a strange behaviour but during operation the expected result is obtained. As the temperature increases the output voltage also increases as desired with the PTAT circuit. The results are in more detail in Figure 26.

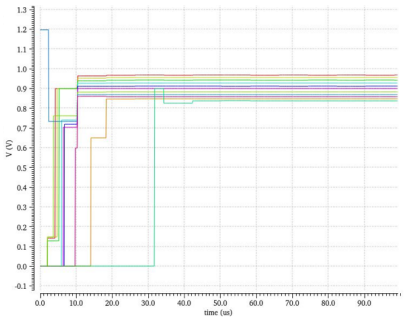

Fig. 25: Analogue voltage (out_DAC) at initial time.

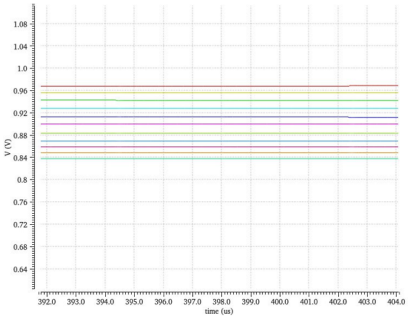

Fig. 26: Analogue voltage (out_DAC) final time.

In Table IX the out_Dac and the correspondent binary words for each temperature are presented.

TABLE IX: Temperatures of -20 $°C$ to 80 $°C$.

Temperature ($°C$)	out_DAC (mV)	Binary word	Binary word value	Increment
-20	837.891	1011001011	715	—
-10	848.438	1011010101	725	+10
0	858.984	1011011101	733	+8
10	869.531	1011100110	742	+9
20	883.592	1011110010	754	+12
30	900	1100000000	768	+14
40	912.891	1100001011	779	+11
50	928.125	1100011000	792	+13
60	942.188	1100100101	805	+13
70	956.250	1100110000	816	+11
80	969.141	1100111011	827	+11

Despite seeming that for the first instances of the conversion the ADC has a different behaviour for the negative and positive temperatures the results of the Table IX show that the results are similar. For temperature intervals of 10 $°C$ the ADC is able to do the conversion as observed with the voltage increase. For the range of -20 $°C$ to 80 $°C$ the output voltage increases from around 837 mV to 969 mV. The binary word for the first temperature is 715 and for the final temperature is 827 and the increment is around $+12$ for each 10 $°C$.

In the next simulation a temperature conversion was simulated for intervals of 1 $°C$ in the negative range of temperatures from -20 $°C$ to -10 $°C$. The result is presented in Figure 27.

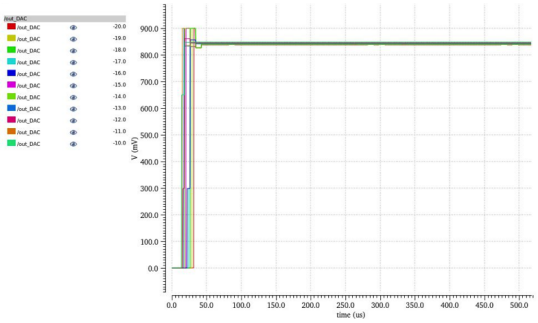

Fig. 27: Output analogue voltage (out_DAC) with temperatures -20 $°C$ to -10 $°C$.

The ADC seems to do the conversion but a detailed view is presented in Figure 29.

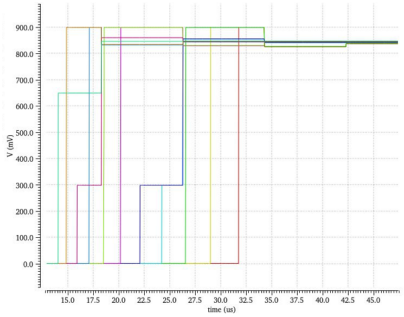

Fig. 28: Analogue voltage (out_DAC) at initial time.

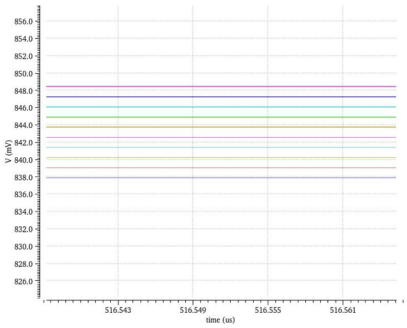

Fig. 29: Analogue voltage (out_DAC) final time.

In Table X the out_Dac and the correspondent binary words for each temperature are presented.

TABLE X: Temperatures of -20 $°C$ to -10 $°C$.

Temperature ($°C$)	out_DAC (mV)	Binary word	Binary word value	Increment
-20	837.891	1011001011	715	—
-19	839.063	1011001100	716	+1
-18	840.234	1011001101	717	+1
-17	841.406	1011001110	718	+1
-16	842.578	1011001111	719	+1
-15	843.750	1011010000	720	+1
-14	843.750	1011010000	720	+0
-13	844.921	1011010001	721	+1
-12	846.094	1011010010	722	+1
-11	847.265	1011010011	723	+1
-10	848.438	1011010101	725	+2

Through the Figure 29 it seems that for negative temperatures the ADC has a different behaviour in early stages. However, at around 40μs and during operation the ADC starts to work properly and the 1 $°C$ conversion can be achieved. This results are confirmed in Table X. The out_Dac goes from around 837 mV to 848 mV, an increase of 11 mV in 10 $°C$. In each 1 $°C$ there is a change of 1 bit in the binary word and in 10 $°C$ the decimal value increases 10 times from 715 to 725, for each 1 $°C$ the increment is almost always $+1$.

A new simulation was made for positive temperatures of 70 $°C$ to 80 $°C$. The result is presented in Figure 30.

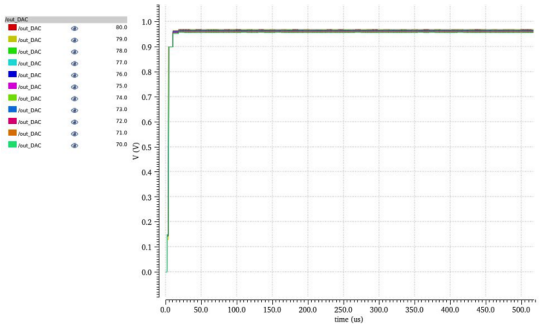

Fig. 30: Output analogue voltage (out_DAC) with temperatures 70 $°C$ to 80 $°C$.

The detailed view is presented in Figure 32.

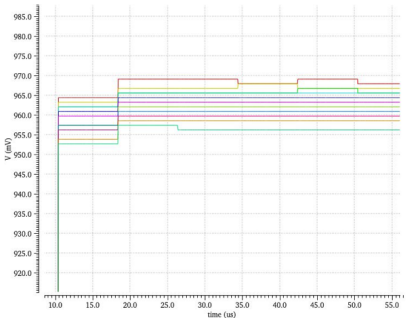

Fig. 31: Analogue voltage (out_DAC) at initial time.

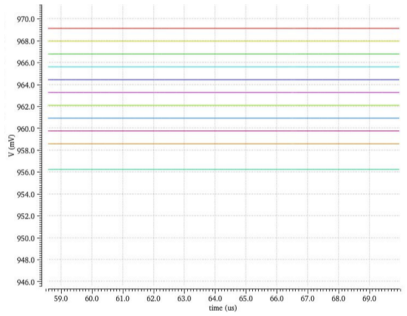

Fig. 32: Analogue voltage (out_DAC) final time.

In Table XI the out_Dac and the correspondent binary words for each temperature are presented.

TABLE XI: Temperatures of 70 $°C$ to 80 $°C$.

Temperature ($°C$)	out_DAC (mV)	Binary word	Binary word value	Increment
70	956.250	1100110000	816	—
71	958.594	1100110010	818	+2
72	959.766	1100110011	819	+1
73	960.938	1100110100	820	+1
74	962.109	1100110101	821	+1
75	963.281	1100110110	822	+1
76	964.453	1100110111	823	+1
77	965.625	1100111000	824	+1
78	965.625	1100111000	824	+0
79	966.797	1100111001	825	+1
80	969.141	1100111011	827	+2

It is clear that the ADC works properly for the positive temperatures. This results are confirmed in Table XI. It is observed that as the temperature increases the output voltage also increases so it is concluded that a 1 $°C$ conversion is possible. For this range the voltage increases from around 956 mV to 969 mV, a 13 mV increment. In each 1 $°C$ there is a change of 1 bit, and an increment in the binary word of around $+1$ for each 1$°C$.

Following this simulation is concluded that the front-end was correctly designed to work with the ADC and a 1$°C$ temperature conversion resolution is achieved.

V. Conclusion and Future Work

The goal of this thesis work was to develop and design the front-end circuit of an ultra-low power temperature sensor. The sensor will be used in precision agriculture and in fire detection, as it measures ambient temperature on a range of -25 $°C$ to 80 $°C$. The sensor should have the best possible

resolution, the goal was set for a 0.25 $^{\circ}C$ resolution with nano ampere current consumption.

Temperature sensors that had similar characteristics were studied and compared. It was concluded that most circuits were developed with BJTs and only more recently with MOSFETs. This is explained due the high linear temperature characteristics of the BJTs. MOSFETs are becoming an alternative because with 1 or 2-point calibration best results are obtained in terms of resolution. Resistor-based are not so commonly used because with the same calibration type the obtained results are not as good.

A better understanding of the temperature behaviour of the BJT, MOSFET and resistors was needed to study the best circuit choice. This study was complemented by simulating these components and circuits with UMC 130 nm CMOS technology, and finally decide the best option for the front-end circuit. After these tests and simulations it was decided to use PMOS transistors only with the possibility of a 1-point calibration in a later stage.

The design of the final front-end was based on the method presented in [17]. It was confirmed that the current has an exponential growth with temperature so it is not even close to a current reference but the output voltage obtained did not vary too much. The next step was trying to use the body effect to compensate the current variations. Despite simulating a lot of circuits and trying new options it was not possible to generate the necessary Vbody to compensate the current. The solution was to generate a VDD - Vout reference with the Vbody compensation circuit. The Vbody generation for the compensation, with active charges allowed to obtain the desired output voltage, but as a disadvantage this voltage will be VDD dependent. A possible solution was to generate the Vbody with one of the transistors connected as a current source instead of all transistors connected as active charges. Finnaly, the VDD - Vout will be used to obtain the two CTAT voltages responsible for the generation of the final ΔVPTAT voltage. The desired ΔVPTAT was obtained with a global optimization of the circuit. However, the constraints for the optimization were not detailed enough and despite having the desired ΔVPTAT behaviour the voltage is not linear and suffers a lot from process dispersion. It was hard to obtained the desired linear PTAT without using optimization and so there was not enough time to improve it. A possible solution can be the addition of more constraints in the optimization, for example an additional derivative constraint for the final PTAT to obtain the best linearity.

The final front-end circuit works in the range of -25 $^{\circ}C$ to 80 $^{\circ}C$, has an ultra-low power consumption of 550 nW and a 1 $^{\circ}C$ resolution. The circuit is designed only with PMOS transistors bringing the additional advantage of only having three corner analysis (FF, nominal and SS). However, the expected results for this work were not fully achieved, the fire detection was not developed and 0.25 $^{\circ}C$ resolution was not obtained. The final PTAT obtained is not linear and varies a lot with VDD.

Initially, the design of a humidity front-end circuit was also proposed but with the difficulties found while developing the temperature circuit there was not enough time to complete it. It is proposed as future work to complete the development of the circuit with the fire detection capability and the development of the circuit layout. The simulations made are not enough to validate the circuit for a real application, as the post layout extracted simulations are needed. In case of using the already exiting ADC the design of the buffers for the circuit integration is also needed. After the post layout simulations and validations the work can be concluded with the circuit fabrication.

REFERENCES

[1] C. W. Kok and W. S. Tam, "CMOS Voltage References an Analytical and Practical Perspective", John Wiley Sons Singapore Pte. Ltd., 2013.

[2] J. Oliveira, "CMOS Smart Temperature Sensors", IST, 2015.

[3] M. A. P. Pertijs, K. A. A. Makinwa and J. H. Huijsing, "A CMOS smart temperature sensor with a 3/spl sigma/ inaccuracy of /spl plusmn/0.1/spl deg/C from -55/spl deg/C to 125/spl deg/C," in IEEE Journal of Solid-State Circuits, vol. 40, no. 12, pp. 2805-2815, Dec. 2005.

[4] B. Wang, M. Law, C. Tsui and A. Bermak, "A 10.6 pJ·K2 Resolution FoM Temperature Sensor Using Astable Multivibrator," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 7, pp. 869-873, July 2018.

[5] T. Zhang and Y. Gao,"A BJT-Based Temperature Sensor in 40-nm CMOS With ±0.8 ºC (3σ) Untrimmed Inaccuracy",Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore,2020.

[6] C. Zhao, Y. Wang, D. Genzer, D. Chen and R. Geiger, "A CMOS on-chip temperature sensor with 0.21°C 0.17 °C inaccuracy from 20 °C to 100 °C," 2013 IEEE International Symposium on Circuits and Systems (ISCAS), Beijing, 2013, pp. 2621-2625.

[7] Y. Chen et al., "A +0.66/0.73 °C Inaccuracy, 1.99-W Time-Domain CMOS Temperature Sensor With Second-Order $\Sigma\Delta$ Modulator and On-Chip Reference Clock," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 11, pp. 3815-3827, Nov. 2020.

[8] Y. Tan et al., "A 1.3-μW 0.3/+0.27°C Inaccuracy Fully-integrated Temperature Sensor Based on a Pre-Charge Relaxation Oscillator for IoT applications," 2019 IEEE Asia-Pacific Microwave Conference (APMC), Singapore, Singapore, 2019.

[9] Y. Lee, W. Choi, T. Kim, S. Song, K. A. A. Makinwa and Y. Chae, "A 5800-μm2 Resistor-Based Temperature Sensor With a One-Point Trimmed Inaccuracy of ±1.2 °C (3σ) From 50 °C to 105 °C in 65-nm CMOS," ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC), Cracow, Poland, 2019.

[10] S. Pan, Y. Luo, S. H. Shalmany, and K. A. A. Makinwa, "A resistor-based temperature sensor with a 0.13 pJ · K2 resolution FoM," IEEE J. Solid-State Circuits, vol. 53, no. 1, pp. 164–173, Jan. 2018.

[11] W. Choi et al., "A compact resistor-based CMOS temperature sensor with an inaccuracy of 0.12 ºC (3σ) and a resolution FoM of 0.43 pJ·K2 in 65-nm CMOS," IEEE J. Solid-State Circuits, vol. 53, no. 12, pp. 3356–3367, Dec. 2018.

[12] J. A. Angevare and K. A. A. Makinwa, "A 6800- μ m2 Resistor-Based Temperature Sensor With ±0.35 °C (3 σ) Inaccuracy in 180-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 54, no. 10, pp. 2649-2657, Oct. 2019.

[13] Pelzers, Kevin Xin, Haoming Cantatore, E. Harpe, Pieter, "A 2.18pJ/conversion, 1656μm^2 Temperature Sensor with a 0.61pJK FoM and 52pW Stand-by Power", IEEE Solid-State Circuits Letters, 2020.

[14] S. Pan and K. A. A. Makinwa, "A 6.6-μW Wheatstone-Bridge Temperature Sensor for Biomedical Applications," in IEEE Solid-State Circuits Letters, vol. 3, pp. 334-337, 2020.

[15] R. Alves, "ADC Ultra-low Power for Micro-Sensors", IST, Nov. 2013.

[16] J. Santamaria, N. Cuevas, Luis E., Rueda G., J. Ardila and E. Roa, "A Family of Compact Trim-Free CMOS Nano-Ampere Current References", IEEE, 2019.

[17] Q. Dong, I. Lee, K. Yang, D. Blaauw and D. Sylvester, "A 1.02nW PMOS-only, trim-free current reference with 282ppm/°C from 40°C to 120°C and 1.6% within-wafer inaccuracy," ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference, 2017.