130 nm CMOS Temperature sensor front-end for IoT applications

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Declaration

I declare that this document is an original work of my own authorship and that it fulfills all the requirements of the Code of Conduct and Good Practices of the Universidade de Lisboa.

Declaração

Declaro que o presente documento é um trabalho original da minha autoria e que cumpre todos os requisitos do Código de Conduta e Boas Práticas da Universidade de Lisboa.

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Abstract

Temperature is one of the most important physical parameters that must be carefully monitored and quantified. The temperature of a significant number of applications and environments can be controlled with temperature sensors. For example, the agriculture industry needs a constant and careful examination of the ambient temperature as it directly affects the environment, this temperature control can be done with sensors. The evolution of the Internet of Things (IoT) systems adds the extra capability of measuring anytime and almost anywhere.

The CMOS technology evolution and development allows the development of low cost and ultra-low power sensors, using a single chip implementation. This work presents the development of a front-end circuit developed in UMC 130 nm CMOS technology for ambient temperature sensor with a 1 $^{\circ}C$ resolution. To design this circuit, a careful study of the temperature behaviour in the most commonly used devices and components like BJTs, MOSFETs and resistors, was made. The most common voltage and current reference circuits were also studied. Following this theoretical analysis, a prototype is presented to identify the best options for the circuit.

Keywords: 130 nm, BJT, CMOS, IoT, MOSFET, Temperature sensor, ultra-low power.

Resumo

A temperatura é um dos parâmetros físicos mais importante e deve ser cuidadosamente monitorizada e quantificada. A temperatura de um número significativo de aplicações e ambientes pode ser controlada com sensores de temperatura. Por exemplo, a indústria agrícola necessita de um controlo cuidadoso da temperatura ambiente, este controlo da temperatura pode ser feito com sensores. A constante evolução da Internet das Coisas (IoT) acrescenta uma vantagem com a capacidade de se poder medir a temperatura a qualquer altura e em qualquer lugar.

A evolução e desenvolvimento da tecnologia CMOS permite o desenvolvimento destes sensores com baixo custo e pouco consumo, ao usar a implementação em um único chip. Este trabalho apresenta o front-end de um circuito desenvolvido em tecnologia CMOS UMC 130 nm para um sensor de temperatura ambiente com uma resolução de 1 $^{\circ}C$. Para desenvolver este circuito, foi efeituado um estudo cuidadoso do comportamento da temperatura nos dispositivos e componentes mais utilizados, como BJTs, MOSFETs e resistências. Foram também estudados os circuitos mais comuns usados para gerar tensões e correntes de referência. Na sequência desta análise teórica, é apresentado um protótipo para identificar as opções mais viáveis para o circuito.

Keywords: 130 nm, BJT, CMOS, Consumo ultra-baixo, IoT, MOSFET, Sensor de temperatura.

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Nomenclature

2T 2-Transistor based voltage reference.

ADC Analog to digital converter.

BGR Bandgap reference circuit.

BJT Bipolar junction transistor.

BMCS Beta multiplier current source.

BPF Bandpass filter.

CMOS Complementary metal-oxide-semiconductor.

CTAT Complementary to absolute temperature.

DAC Digital to analog converter.

FDC Frequency to digital converter.

IoT Internet of Things.

MIM Metal-insulator-metal.

MOSFET Metal oxide semiconductor field effect transistor.

PDC Phase domain digital converter.

PPF Poly-phase filter.

PSRR Power supply rejection ratio.

PTAT Proportional to absolute temperature.

TC Temperature coefficient.

TDC Time to digital converter.

WB Wien-bridge.

WhB Wheatstone bridge.

ZTC Zero temperature coefficient.

Chapter 1

Introduction

Temperature is one of the most important physical parameter, so it must be accurately quantified. Some applications, for example, biomedical, pharmaceutical and environmental controls for agriculture require the monitorization of the temperature which can be made using sensors.

A smart temperature sensor can be designed with electronic components. The most common temperature sensors are designed with Bipolar Junction Transistor (BJT) or Metal Oxide Semiconductor Field Effect Transistor (MOSFET), using the temperature characteristics of the transistors junctions. When designing a temperature sensor the main focus should be on the resolution, size, accuracy, autonomy, process dispersion and supply voltage insensitivity.

The Complementary metal–oxide–semiconductor (CMOS) technology can be used to design these types of sensors with low cost and ultra-low power consumption. Additionally, a single chip implementation can be done. This is a big advantage because there is no need for additional and external circuits.

As the temperature affects components, each device must carefully be studied, especially when designing a temperature sensor to guarantee its correct behaviour.

This project is divided in 5 sections. Section 2 will present the state of the art of the existing temperature sensors. Section 3 will make a theoretical approach to the most commonly used components, and references generation. In the Section 4 a simulation study of the components in the UMC 130 nm technology is made. In Section 5 the front-end circuit for the temperature sensor is designed and presented. Concluding with Section 6 that will present the conclusion and future work.

1.1 Motivation

The evolution and development of the Internet of Things (IoT) has created the possibility of everything, located anywhere, to connect to the internet. A big part of the developed technology will be a node in a wireless sensor node for environment measurements applications. These systems must be carefully controlled to avoid malfunctions.

One of the many applications for these sensors is in agriculture where almost every production process has temperature dependencies. A sensor to monitor and control is highly useful. The sensor should

focus on having a low power consumption and to be energy efficient. For its use in agriculture is important that the sensor has a long life time, even more because the temperature measurement will be made periodically. An important function of the sensor is also in fire detection. The sensor should sound an alarm if the temperature is above the chosen value of 65 $^{\circ}C$.

I was motivated to choose this thesis because I found nanotechnology the most interesting part in electronics. The application in which this project will be used also aroused my attention because I have become aware of the role of agriculture nowadays. This work allowed me to combine my interest in technology, most specifically nanotechnology, and applied it to my newly discovered interest in agriculture. I find it a funny coincidence that my middle name ”Fazendeiro” some years ago was related to someone that a farm and therefore connected to agriculture.

1.2 Objectives

The objective of this thesis is to develop and design the front-end of an ultra-low power temperature sensor to be used in agriculture applications. The focus should be on energy consumption reduction, temperature range and resolution.

The sensor should be developed in 130 nm CMOS mixed-mode RF technology from UMC manufacturer. *Cadence Design Environment* software will be used. The ADC that will be used is already available and has VLSB of 2.56 mV with a ENOB of 10.97 after layout extraction. Ideally the temperature sensor should have an inaccuracy of $\pm$0.25 $^{\circ}C$ over the range of -25 $^{\circ}C$ to 80 $^{\circ}C$, using a 1.2 V power supply. In a later stage of the project a 1-point calibration to improve the sensor is a possibility.

Chapter 2

Temperature sensors overview

The wireless sensor nodes development is growing at a fast pace and so it is important to have ultra-low power systems. Temperature sensors are in almost every device from the medical equipment, gaming computers, smart devices, IoT devices and so many others that require a long lifetime (years). The temperature must be monitored to ensure the proper work of all these devices.

The main temperature sensors can be divided in 3 categories: voltage-domain, time-domain and phase-domain sensors. In Figure 2.1.

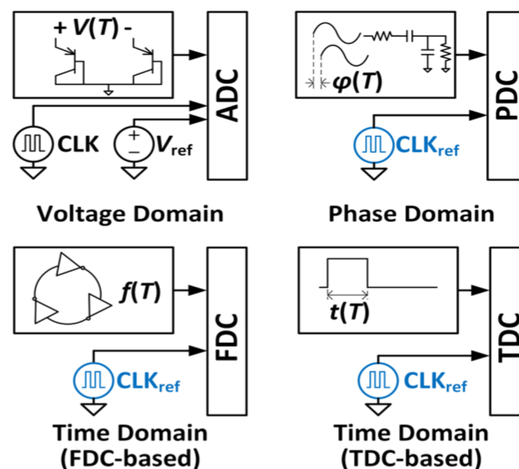

Figure 2.1: Operating principle of different temperature sensors [7].

Voltage-domain sensors use a proportional to absolute temperature (PTAT) voltage signal and a voltage ADC to convert the temperature signal into a digital word [2]. To perform the conversion the ADC also needs a reference (REF) signal. To obtain this reference signal it is also needed a complementary to absolute temperature (CTAT) signal that decreases with temperature. Combining the PTAT and CTAT signals the temperature independent reference V_{REF} is created and the temperature conversion can be made in the ADC. The accuracy of the final reading depends on the accuracy of the V_{REF} signal. A general voltage based temperature sensor can be made with three main circuits represented in Figure 2.2.

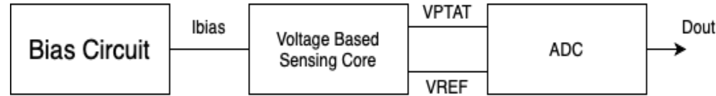

Figure 2.2: General Temperature Sensor Block diagram.

The three blocks are: the bias current circuit, the voltage base sensing core and the ADC. The bias current circuit is used to provide accurate currents. The voltage base sensing core generates the V_{PTAT} and V_{REF}, that will be later discussed in this thesis. The ADC, responsible for the conversion of the inputs to a digital value where the average is proportional to temperature.

Unlike the voltage-domain sensors, time-domain and phase-domain are clock (CLK_{REF}) dependent, so the accuracy of the final reading is dependent on the accuracy of the clock´s frequency. Time-domain sensors can be developed with a temperature dependent oscillator frequency and a frequency-to-digital converter (FDC) or with temperature dependent pulse width and a time-to-digital converter (TDC) [7]. In both cases the oscillator or the temperature dependent pulse will originate the VPTAT signal that will be converted by the FDC or TDC, respectively.

Phase-domain sensors rely on a phase-domain digital converter (PDC) that converts a temperature dependent phase shift generated by polysilicon resistors [7].

This work presents the development of a voltage-based temperature sensor. As the IoT applications begin to be more common a low supply voltage is needed to achieve ultra low power, as well as the circuits should be powered by nano-ampere currents.

2.1 State of the art

The following table presents the comparison between the temperature sensors of the referenced articles:

Table 2.1: State of the Art of the Temperature Sensors

Reference	[3] JSSC-2005	[4] ITCS-2018	[5] ISCC-2019	[6] ISSCC-2013	[7] ITCS-2020	[8] APMC-2019	[9] SSCL-2019	[12] JSSC-2019	[13] SSCL-2020	[14] SSCL-2020
Sensor Type	BJT	BJT	BJT	MOSFET	MOSFET	OSC	Resistor (PPF)	Resistor	Resistor	Resistor
Technology (um)	0,7	0,18	0,04	0,18	0,18	0,18	0,065	0,18	0,065	0,18
Area (mm2)	4,5	0,1	0,03	0,0003286	0,45	0,11	0,058	0,068	0,0017	0,12
Supply Voltage (V)	2,5-5	1,6-2	1,2	1,8	1,8	0,65	0,85-1,3V	1,8	0,6/1	1,6
Power Consumption (uW)	247,5 (*1)	0,864	13,5	1,026	1,99	1,3	32,5	1600	0,109	6,6
Temperature Range (ºC)	-55~125	-30~120	-20~100	-20~100	-20~80	-15~65	-50~125	-35~125	-20~120	27,5~47,5
Trimming points	1	1	Untrim,	1	2	2	1 or 2	2	2	1
Inaccuracy (ºC)	±0,1	±0,85	±0,8	0,17/-0,21	0,5/-0,44 (*2) 0,66/-0,73 (*3)	0,27/-0,3	±1,2 (*4) ±0,16 (*5)	±0,35	4,3/-2,5	0,2/-0,1
Energy/Conversion (nJ)	24750	6,9984	13,5	1026	49,75	130	32,5	528	0,00218	52,8

(*1) At 3.3 V. (*2) Min. value. (*3) Max. value. (*4) 1-point calibration. (*5) 2-point calibration.

The main focus when comparing the sensors was the temperature range, area, accuracy and energy/conversion power. In the same sensor it is not possible to have a small area, good accuracy

and a low energy for each conversion, there always needs to be a trade off between one characteristic to benefit another.

The BJT-based temperature sensors are the most common because they are easier to develop due to the linear temperature characteristics. The sensor in [3] has the best accuracy of $\pm$ 0.1 $^\circ C$ at the cost of a larger area of 4.5 mm^2 and a high energy of 24750 nJ conversion. This sensor also has the largest range of temperatures and a single point calibration. In [4] and [5] the sensors consume the lowest energy for a temperature conversion and have a small area of 0.1 mm^2 and 0.03 mm^2. Both present almost the same inaccuracy of $\pm$ 0.85 $^\circ C$ and $\pm$ 0.8 $^\circ C$, respectively. However, the first sensor has a 1 point calibration point while the second does not need calibration. The sensor in [4] has a larger temperature range than the sensor in [5].

The MOSFET-based sensors do not have as linear temperature characteristics as the BJT-based sensors, so additional calibration is required as seen in [6] and [7] that have a 1 and 2 point calibration. With this calibration points these sensors present a good accuracy. These sensors have a larger conversion energy and do not have a temperature range as wide as the BJT sensors.

Every resistor-based sensor studied has calibration points and presents a good accuracy except the sensor in [13]. Overall these sensors have a small area but it is consumed a lot of energy for a conversion.

Chapter 3

References generation

The temperature sensor is expected to work in a temperature range from -25 $°C$ to 80 $°C$. To design the sensor the temperature behaviour of the most commonly used devices must be studied. This section will present a theoretical approach to the temperature behaviour of components like BJTs, MOSFETs and resistors, to understand the best option for the sensor and present the most common circuits used to design voltage and current references.

3.1 Components behaviour

3.1.1 Bipolar junction transistor (BJT)

Bipolar Junction Transistor (BJT) are a commonly used device to obtain a temperature dependent voltage. In Figure 3.1 is presented a NPN BJT symbol,

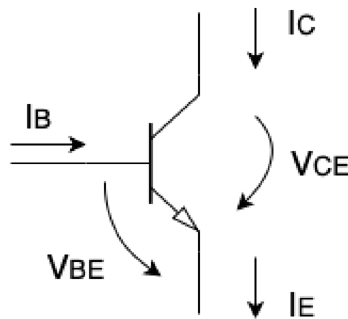

Figure 3.1: Single BJT.

where I_B is the base current, I_C the collector current, I_E the emitter current, V_{BE} the base-emitter voltage and V_{CE} the collector-emitter voltage. For the active region I_C is given as:

$$\mathrm{I_C(T) = I_S(T)(e^{\frac{V_{BE}}{V_T}} - 1)(1 + \frac{V_{CE}}{V_A})} \tag{3.1}$$

where I_S(T) is

$$\mathrm{I_S(T) = \frac{qA\bar{D}_n(T){n_i}^2(T)}{W_B N_A}} \tag{3.2}$$

in which q is the electron charge, A the emitter area, $\bar{D_n}$ the average diffusion constant for electrons, W_B the base width, N_A the acceptor atoms concentration at the base, V_A the early voltage and the thermal

voltage (V_T) is given by:

$$\mathrm{V_T = \frac{kT}{q}} \tag{3.3}$$

and n_i the intrinsic carrier concentration as:

$$\mathrm{n_i{}^2(T) = DT^3 exp[-\frac{V_G(T)}{V_T}]} \tag{3.4}$$

with the Einstein relation:

$$\mathrm{\bar{D_n}(T) = \frac{kT}{q}\bar{\mu_n}(T)} \tag{3.5}$$

and replacing it on equation 3.2 I_S(T) is obtained as:

$$\mathrm{I_S(T) = \frac{kTA\bar{\mu_n}(T)n_i{}^2(T)}{W_B N_A}} \tag{3.6}$$

It can be assumed that:

$$\mathrm{\bar{\mu_n} = CT^{-n}} \tag{3.7}$$

with C and n as constants. Finally the I_S(T) can be written as:

$$\mathrm{I_S(T) = ET^{\eta} exp[-\frac{V_G(T)}{V_T}]} \tag{3.8}$$

with η = 4 - n.

The V_{BE} can be written in function of I_C by negleting the Early effect as:

$$\mathrm{V_{BE}(T) = \frac{kT}{q} ln[\frac{I_C(T)}{I_S(T)}]} \tag{3.9}$$

For T = T_r being T_r a relative temperature:

$$\mathrm{V_{BE}(T_r) = \frac{kT_r}{q} ln[\frac{I_C(T_r)}{I_S(T_r)}]} \tag{3.10}$$

The temperature function of V_{BE} can be written as:

$$\begin{gathered} \frac{V_{BE}(T)}{T} - \frac{V_{BE}(T_r)}{T_r} = \frac{k}{q} ln[\frac{I_C(T)}{I_S(T)} \cdot \frac{I_S(T_r)}{I_C(T_r)}] \\ \Longrightarrow V_{BE}(T) = (\frac{T}{T_r})(V_{BE}(T_r) + \frac{kT}{q} ln[\frac{I_S(T_r)}{I_S(T)} \cdot \frac{I_C(T)}{I_C(T_r)}]) \end{gathered} \tag{3.11}$$

From equation 3.11, using equation 3.8:

$$\mathrm{V_{BE}(T) = V_G(T) - \frac{T}{T_r}V_G(T_r) + \frac{T}{T_r}V_{BE}(T_r) - \eta(\frac{kT}{q})ln(\frac{T}{T_r}) + (\frac{kT}{q})ln[\frac{I_C(T)}{I_C(T_r)}]} \tag{3.12}$$

If I_C(T) = I_C = constant, in equation 3.12 the terms V_G(T) is non linear and decreases with temperature, the term $\eta(\frac{kT}{q})ln(\frac{T}{T_r})$ is non linear but increases with temperature, if T = T_r the last term is 0, and the remaining terms also increase with temperature.

The expression can be further developed by assuming the V_G(T) as a straight line obtained with the derivative in T = T_r, V_G(T) can be approximated as:

$$\mathrm{\tilde{V_G}(T) = V_{G0} + \epsilon_r T} \tag{3.13}$$

The final V_{BE}(T) expression is obtained as:

$$\mathrm{V_{BE}(T) = V_{G0}(1 - \frac{T}{T_r}) + (\frac{T}{T_r})V_{BE}(T_r) - \eta(\frac{kT}{q})ln(\frac{T}{T_r}) + (\frac{kT}{q})ln[\frac{I_C(T)}{I_C(T_r)}]} \tag{3.14}$$

With $V_{G0}(1-\frac{T}{T_r})$ and $(\frac{T}{T_r})V_{BE}(T_r)$ the linear terms and $\eta(\frac{kT}{q})ln(\frac{T}{T_r})$ and $(\frac{kT}{q})ln[\frac{I_C(T)}{I_C(T_r)}]$ non linear terms. When the transistor is connected as a diode and assuming:

$$\begin{aligned} &V_{BE} >> V_T \\ &V_{CE} << V_A \end{aligned} \tag{3.15}$$

The voltage V_{BE} is temperature sensitive and is given by:

$$\mathrm{V_{BE}(T) = V_T ln\frac{I_C}{I_S(T)}} \tag{3.16}$$

The voltage V_{BE} is an almost CTAT voltage because the term $I_S(T)$ dominates the V_T.

3.1.2 MOSFET

The MOSFET operates in 3 regions: cut off region, triode region (Linear region) and saturation region. A single NMOS transistor is presented in Figure 3.2.

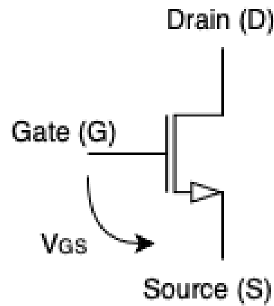

Figure 3.2: Single NMOS transistor.

The cut off region is where the current flowing through the transistor will be 0 A and so the transistor will be OFF. The cut off region is when the gate to source voltage (V_{GS}) is less than the threshold voltage (V_{TH}) and can be defined when:

$$\begin{aligned} &V_{GS} < V_{TH} \\ &I_D \approx 0 \end{aligned} \tag{3.17}$$

In the triode region:

$$\begin{aligned} &V_{GS} > V_{TH} \\ &V_{DS} < V_{GS} - V_{TH} \\ &I_D = \mu_0 C_{ox}(\tfrac{W}{L})[(V_{GS} - V_{TH})V_{DS} - \tfrac{{V_{DS}}^2}{2}] \end{aligned} \tag{3.18}$$

If these equations are verified a channel will be induced and the current will flow through the transistor. In the saturation region the current value will saturate, the transistor is in the saturation region if:

$$\begin{aligned} &V_{GS} > V_{TH} \\ &V_{DS} > V_{GS} - V_{TH} \\ &I_D = \tfrac{1}{2}\mu_0 C_{ox}(\tfrac{W}{L})(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \end{aligned} \tag{3.19}$$

The MOSFET operates in the subthreshold region when it operates below the threshold voltage. This region is very useful in order to reduce the power consumption. The current-voltage relationship equation can be expressed as:

$$\mathrm{I_0} = \mu_0 \mathrm{C_{ox}}(\frac{\mathrm{W}}{\mathrm{L}})\mathrm{V_T}^2 \exp(\frac{\mathrm{V_{GS}} - \mathrm{V_{th}}}{\eta \mathrm{V_T}})[1 - \exp(-\frac{\mathrm{V_{DS}}}{\mathrm{V_T}})] \tag{3.20}$$

with V_T as expressed in 3.4 and

$$\mathrm{C_{ox}} = \frac{\xi_{\mathrm{ox}}}{\Gamma_{\mathrm{ox}}} \tag{3.21}$$

where C_{ox} is the gate-oxide capacitance per unit area and η is the subthreshold slope factor.

3.1.3 Resistors

Resistors are commonly used devices in electronic circuits. Basically they can be used as voltage to current or current to voltage converters. To choose the most fitting resistor two paramenters must be taken into consideration:: the sheet resistance (R_{sheet}) in $\Omega\square$, which describes the resistance of a resistor with W = L, and the temperature and voltage sensitives [1] as:

$$\mathrm{R(T)} = \mathrm{R_{sheet}}(1 + \mathrm{T_{CR1}}(\mathrm{T} - \mathrm{T_r}) + \mathrm{T_{CR2}}(\mathrm{T} - \mathrm{T_r})^2 + ... + \mathrm{T_{CRn}}(\mathrm{T} - \mathrm{T_r})^{\mathrm{n}}) \tag{3.22}$$

and

$$\mathrm{R(V)} = \mathrm{R_{sheet}}(1 + \mathrm{V_{CR1}}(\mathrm{T} - \mathrm{T_r}) + \mathrm{V_{CR2}}(\mathrm{T} - \mathrm{T_r})^2 + ... + \mathrm{V_{CRn}}(\mathrm{T} - \mathrm{T_r})^{\mathrm{n}}) \tag{3.23}$$

where T_{CRi} is the i-th order temperature coefficient and V_{CRi} the i-th order voltage coefficient of the resistor. To have a stable resistance in most circuits a pair of resistors is used, in this way the absolute resistance of each resistor is not important but the ratio between the pair of resistors can be fine tuned. When using resistors it is also necessary to take into consideration the ”end-effect” that accounts for the enlargement of both ends of the resistor to accompany the contacts [1]. Due to this effect resistors with different length will not match and so to obtain the best matching, identical resistors must be used. When choosing what resistor to use it is important to analyse the sheet resistance and the first order temperature coefficients. In [1] typical available resistors of a 180 nm mixed signal CMOS technology are presented in Table 3.1.

Table 3.1: Sheet resistance and first order temperature coefficients (T_{CR}) of different resistors [1].

Resistor Type	Sheet Resistance ($\Omega/\square$)	T_{CR} (ppm/°C)
Non-Silicide *N*+ Diffused	56.1	1510
Non-Silicide *P*+ Diffused	114	1410
Non-Silicide *N*+ Poly	290	−1350
Non-Silicide *P*+ Poly	319	−163
N-well	890	2730
High Resistance Poly	1030	−852
Metal	0.078	3600

A low sheet resistance means that a large silicon area is needed to obtain a large resistance. A large temperature coefficient means a large temperature dependency which is not adequate for a voltage reference. The ideal resistor should have a large sheet resistance and a small temperature coefficient.

In the case of Table 3.1 the non-silicide P+ Poly resistor should be the choice to design temperature dependent circuits.

3.2 Voltage References

An important building block in the system is the voltage reference, used to generate a stable reference within a range of temperature with low power consumption. The voltage reference is always powered up in standby or active mode and so it has a big impact in the power consumption of the system. The voltage reference design is the key to extend the system´s lifetime. Bandgap references (BGR) are commonly used to generate the voltage reference by combining a proportional to absolute temperature (PTAT) voltage and a complementary to absolute temperature (CTAT) voltage. An alternative to the BGR is the use of 2-Transistor (2T) based voltage reference. This circuit uses two different sub-threshold-biased transistors to generate the stable voltage. A different approach can also be using a transistor near its zero temperature coefficient (ZTC) to obtain the temperature independent voltage.

3.2.1 Bandgap voltage reference (BGR) based

Bandgap references circuits (BGRs) are commonly used to generate stable reference signals insensitive to voltage, temperature and process variation [24]. In a temperature sensor every temperature dependent device must be carefully designed. These circuits generate and combine the PTAT and CTAT signals to eliminate the temperature dependency of the output voltage and obtain an accurate voltage reference. To easily identify each term in the equations the PTAT will be represented in blue and the CTAT in green.
A conventional Widlar bandgap circuit is shown in Figure 3.3 [21].

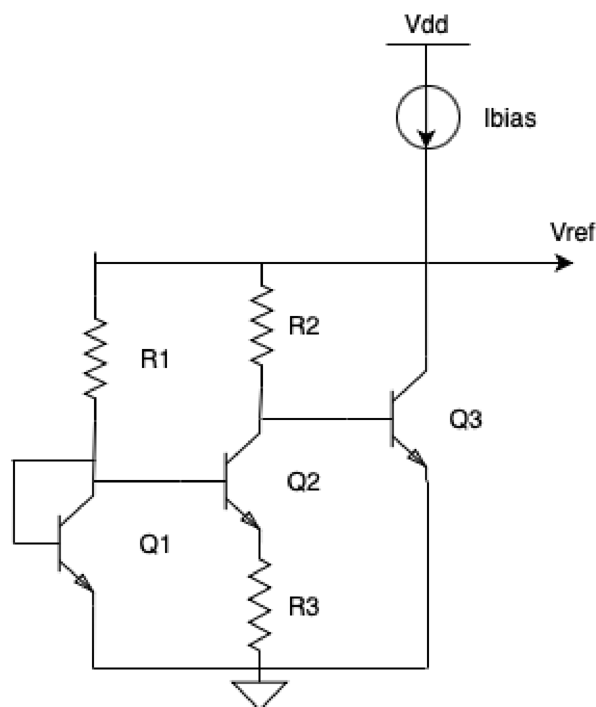

Figure 3.3: Widlar bandgap circuit [21].

The transistors Q1 and Q2 are responsible to generate temperature proportional voltages across R3 and consequently R2. Transistor Q3 V_{BE} will generate a CTAT voltage. Q3 will sense the output voltage

flowing through R2 and drive the output voltage that will be the sum of its V_{BE} and the voltage through R2. In this way the voltage across R2 will compensate the transistor´s V_{BE} by proper choice of R2 and R3 values generating a temperature stable output voltage. However, the effect of base current through R1 and R2 is neglected, the variability in the current will lead to an output voltage error [21]. And assuming that I_C = I_E:

$$\mathrm{V_{R3}} = \Delta \mathrm{V_{BE}} = \mathrm{V_{EB1}} - \mathrm{V_{EB2}} = \frac{\mathrm{kT}}{\mathrm{q}} \ln \frac{\mathrm{I_{C1}}}{\mathrm{I_{C2}}} \tag{3.24}$$

Assuming that $I_{C!}$ = I_{C2} is a an approximation to a constant the generated voltage in R3 (V_{R3}) is a PTAT voltage.
Also if I_{R3} = I_{R2}:

$$\frac{\mathrm{V_{R3}}}{\mathrm{R3}} = \frac{\mathrm{V_{R2}}}{\mathrm{R2}} \Longleftrightarrow \mathrm{V_{R2}} = \mathrm{V_{R3}} \frac{\mathrm{R2}}{\mathrm{R1}} \tag{3.25}$$

So the generated. voltage in R2 (V_{R2}) is a PTAT voltage. The reference voltage (Vout) is then obtained is obtained with:

$$\mathrm{Vout} = \mathrm{V_{R2}} + \mathrm{V_{BE3}} \tag{3.26}$$

An alternative circuit presented in Figure 3.4 is proposed by Brokaw to improve the previous circuit .

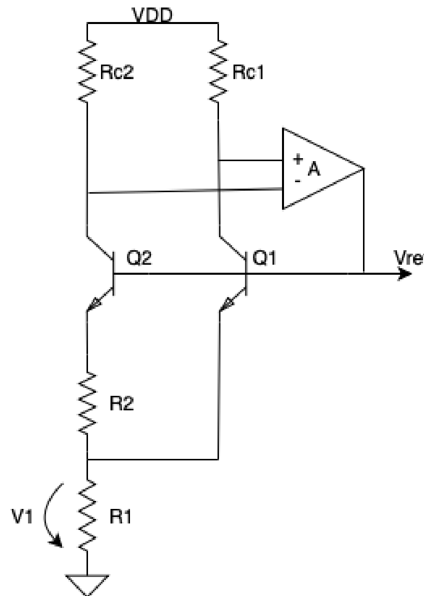

Figure 3.4: Brokaw bandgap circuit.

The op amp matches the collector currents of Q1 and Q2. Assuming the same value for Rc1 and Rc2 the collector current I_{C1} matches I_{C2}. The transistor Q2 and Q1 have different areas. As they are powered by the same current but have different areas the voltages V_{BE2} and V_{BE1} are different.
Assuming that the collector current (I_C) is equal to the emitter current (I_E) the voltage in R2 is given as:

$$\mathrm{V_{R2}} = \Delta \mathrm{V_{BE}} = \mathrm{V_{BE1}} - \mathrm{V_{BE2}} \tag{3.27}$$

The transistors current density is:

$$\mathrm{J_2} = \frac{\mathrm{I_{C2}}}{\mathrm{A_2}} : \mathrm{J_1} = \frac{\mathrm{I_{C1}}}{\mathrm{A_1}} \tag{3.28}$$

And so the ΔV_{BE}:

$$\Delta \mathrm{V_{BE}} = \frac{\mathrm{kT}}{\mathrm{q}} \ln \frac{\mathrm{J_1}}{\mathrm{J_2}} \tag{3.29}$$

With the previous assumptions that the values of R_{C2} and R_{C1} are equal, the values of the collector currents I_{C2} and I_{C1} and the values of the emitter currents I_{E2} and I_{E1} are equal and R2 (I_{R2}) is given as:

$$\mathrm{I_{R2}} = \frac{\Delta \mathrm{V_{BE}}}{\mathrm{R2}} \tag{3.30}$$

And the current I_{R1}:

$$\mathrm{I_{R1}} = 2\mathrm{I_{R2}} \tag{3.31}$$

these equations are used to obtain the voltage developed in R1 (V_1) given as:

$$\mathrm{V_1} = 2\mathrm{I_{R2}} \cdot \mathrm{R1} \Longleftrightarrow \mathrm{V_1} = 2\frac{\mathrm{R1}}{\mathrm{R2}}\frac{\mathrm{kT}}{\mathrm{q}} \ln \frac{\mathrm{A2}}{\mathrm{A1}} \tag{3.32}$$

The output voltage Vref generated is:

$$\mathrm{V_{ref}} = \mathrm{V_{BE1}} + \mathrm{V_1} \tag{3.33}$$

Being the reference voltage generated with the weighted sum of the complementary to absolute temperature voltage at the base of Q1 (V_{BE1}) and the proportional to absolute temperature voltage across R1 (V_1).
A diode connected voltage reference is presented in Figure 3.5.

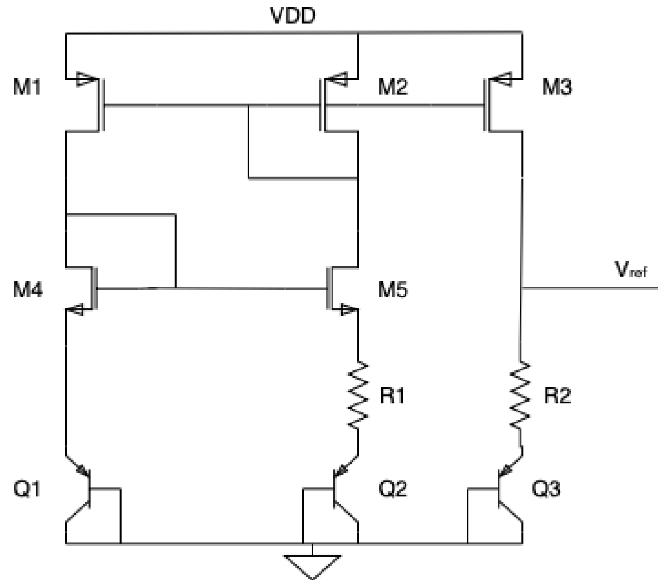

Figure 3.5: Diode connected bandgap reference circuit.

The output voltage V_{ref} is given by:

$$\mathrm{V_{ref}} = \mathrm{V_{EB3}} + \ln(\mathrm{N})\frac{\mathrm{R2}}{\mathrm{R1}} \cdot \mathrm{V_T} \tag{3.34}$$

where N is the ratio between Q2 and Q1 areas, V_T is the thermal voltage. The parameter V_{EB} is complementary to absolute temperature (CTAT) and the thermal voltage V_T is proportional to absolute

temperature (PTAT) [23]. By sizing the parameter N and R1 and R2 ratio the voltage output can be temperature independent [23].

To obtain a sub-1-V output voltage an alternate circuit is suggested in [23] presented in Figure 3.6.

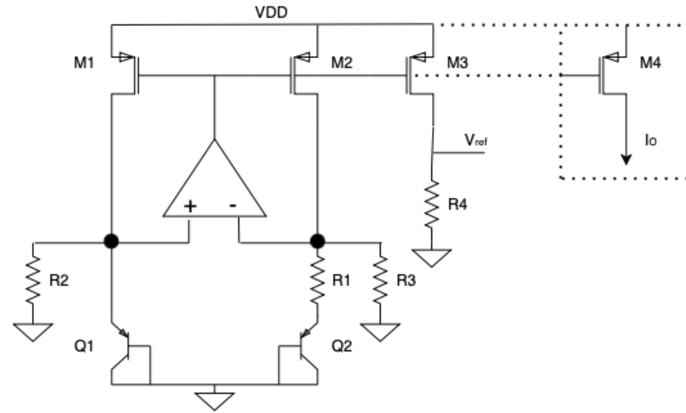

Figure 3.6: Ultra low power bandgap voltage reference.

In this circuit: R3 has the same value as R2 and the voltages V_{EB} and V_T are converted into currents and summed. The voltage output V_{ref} is now given as:

$$V_{\mathrm{ref}} = \frac{\mathrm{R4}}{\mathrm{R2}} V_{\mathrm{EB1}} + \ln(\mathrm{N}) \frac{\mathrm{R4}}{\mathrm{R1}} \cdot V_{\mathrm{T}} \tag{3.35}$$

In exchange for the voltage output reduction larger resistors are needed and additional components are added for the voltage to current conversion. So there is a trade off between power consumption and silicon area. Additionally in this circuit the transistor M4 can be added instead of the output resistor to generate a current reference.
An alternative MOSFET-based circuit is presented in [22], [28] where M3 is working as a current source and M4 as a diode. The circuit is presented in Figure 3.7.

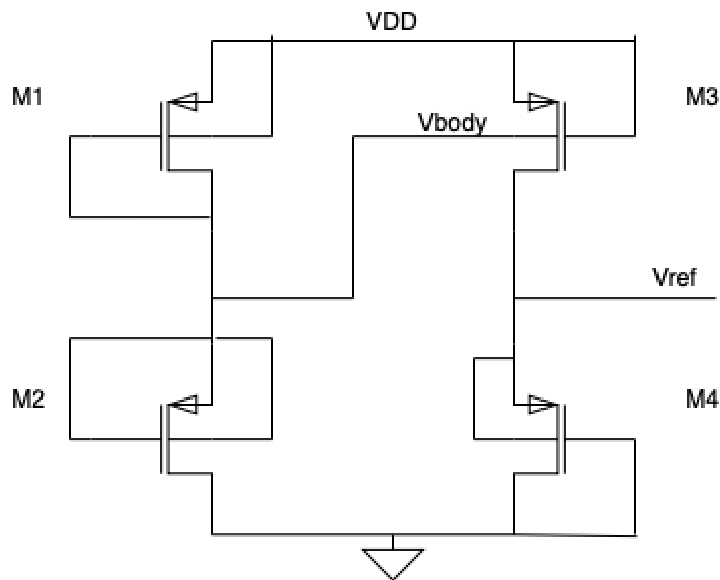

Figure 3.7: BGR PMOS-Only voltage reference schematic.

The circuit is designed with 4 PMOS transistors: M1, M2, M3 and M4. The transistors M1 and M2

generate the Vbody voltage for M3, where M1 is connected as a diode and M2 as a subthreshold current source. The generated voltage Vbody tracks Vdd. M3 is in the subthreshold mode resulting in the sub-threshold current source flowing through M4. As the M3 and M4 transistors are the same type of PMOS the difference between $V_{t_{h1}}$ and $V_{t_{h2}}$ comes from the body effect on M3. The current equations for the transistors M1 and M2 are expressed in (3.36) and for the transistors M3 and M4 in (3.37) [22].

$$\mathrm{I = u_pC_{ox}\frac{W1}{L1}nV_T{}^2exp(\frac{V_{body} - V_{dd} - V_{th1}}{mV_T}) = u_pC_ox\frac{W2}{L2}nV_T{}^2exp(\frac{0 - V_{th2}}{mV_T})} \tag{3.36}$$

$$\mathrm{I = u_pC_{ox}\frac{W3}{L3}nV_T{}^2exp(\frac{0 - V_{th1}}{mV_T}) = u_pC_ox\frac{W4}{L4}nV_T{}^2exp(\frac{0 - V_{ref} - V_{th2}}{mV_T})} \tag{3.37}$$

By solving equation (3.37) [22]:

$$\mathrm{V_{ref} = V_{th3} - V_{th4} + mV_Tln(\frac{W3L4}{W4L3})} = \gamma(\sqrt{2\phi_b - \mathrm{mV_Tln\frac{W2L1}{W1L2}}} - \sqrt{2\phi_b}) + \mathrm{mV_Tln\frac{W3L4}{W4L3}} \tag{3.38}$$

As in [22] a proper sizing and dimension of the transistors will result in a Vref signal. It is also possible to increase the generated voltage by increasing the number of stacked transistors in the place of M4.

3.2.2 2-Transistor (2T) based

With the objective of reducing the area and power consumption a new circuit is proposed in [25] named the 2-Transistor (2T) based voltage reference. The circuit uses two transistors in the subthreshold region with different threshold voltages (V_{th}). The circuit schematic is presented in Figure 3.8.

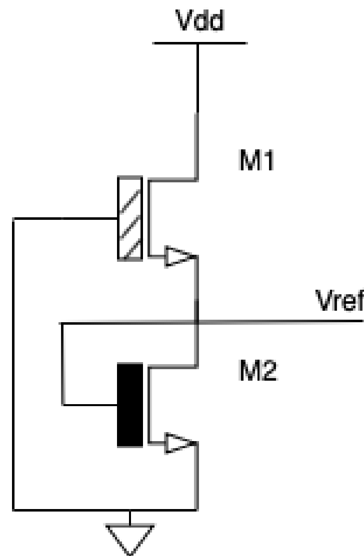

Figure 3.8: 2-Transistor based voltage reference.

As mentioned the circuit is designed with two transistors connected in series, M1 and M2. In [25] the transistor M1 is a native device, identical to a common MOSFET but with the threshold voltage near zero, and M2 a thick oxide input/output (I/O) device with an higher V_T. Assuming a subthreshold regime the transistor currents I_{M1} and I_{M2} are expressed as:

$$\mathrm{I_{M1} = u_1C_{ox1}\frac{W1}{L1}(m1 - 1)V_T{}^2exp(\frac{0 - V_{ref} - V_{th1}}{m1V_T})} \tag{3.39}$$

$$I_{M2} = u_2 C_{ox2}\frac{W2}{L2}(m2-1)V_T{}^2 \exp(\frac{V_{ref}-V_{th2}}{m2V_T}) \tag{3.40}$$

And the voltage reference equation can be obtained from equation 3.39 and 3.40:

$$V_{ref} = \frac{m1m2}{m1+m2}(V_{th2}-Vt_{h1}) + \frac{m1m2}{m1+m2}V_T \ln(\frac{u_1 C_{ox1} W_1 L_2}{u_2 C_{ox2} W_2 L_1}) \tag{3.41}$$

where m parameter is the subthreshold slope factor. The terms in equation 3.41 are either proportional or complementary to temperature, with a proper sizing of the transistors the terms will cancel out and the voltage reference is obtained. As all terms are insensitive to V_{DD} to first order this method offers good power supply rejection ratio (PSRR) [25]. However, this method suffers in temperature sensitivity because of the V_{th} variation suffering from process variations. This circuit was not simulated because the different V_{th} transistors are not available in the technology used.

3.2.3 Zero-temperature coefficient (ZTC) based

A zero-temperature coefficient (ZTC) in most transistors can be achieved due to the mutual temperature cancellation of the threshold voltage and carrier mobility. The transistor´s drain current in a ZTC bias point is nearly temperature independent. The work in [26] discusses and derives the important equations for the circuit. Firstly, a linear temperature model for the transistor´s threshold voltage (V_{th}) is assumed as [26]:

$$V_{th}(T) = V_{th}(T_0) + \alpha_{Vth}(T - T_0) \tag{3.42}$$

where T is the absolute temperature, T_0 is a reference temperature usually set to 300K, the temperature coefficient α_{Vth} is negative value between -3 mV/K and -0.5 mV/K and V_{th} decreases with rising temperature according to [26].
The transistor´s carrier mobility can be expressed as:

$$\mu(T) = \mu(T_0)(\frac{T}{T_0})^{\alpha_\mu} \tag{3.43}$$

where α_μ is constant with temperature. The MOSFET´s equations when operating in the saturation region are defined as:

$$I_D(T) = I_s(T) * i_D(T) \tag{3.44}$$

where I_s is the specific current:

$$I_s(T) = 2n\frac{W}{L}C_{ox}\mu(T)(\frac{kT}{q})^2 \tag{3.45}$$

i_D the normalized drain current:

$$i_D(T) = [\ln(1+e^{\frac{v(T)}{2}})]^2 \tag{3.46}$$

and v the normalized gate-source voltage:

$$v(T) = \frac{V_{GS} - V_{th}(T)}{\frac{nkT}{q}} \tag{3.47}$$

where n is the slope factor, W the channel width, L the channel length, C_{ox} is the oxide capacitance per unit area, k the Boltzmann constant, q the elementary charge, and V_{th} is (3.42) and $\mu(T)$ is (3.43) [26].

The article derives the gate-source bias as

$$\mathrm{V_{GS0}}(T) = (\frac{\alpha_\mu + 2}{\mathrm{C}})\frac{nkT}{\mathrm{q}} + \mathrm{V_{th}}(T_0) - \alpha_{\mathrm{Vth}} T_0 \tag{3.48}$$

The voltage V$_{GS0}$ is temperature independent if α_μ = -2 and the ZTC gate-source voltage is [26]

$$\mathrm{V_{GSF}} = \mathrm{V_{th}}(T_0) - \alpha_{\mathrm{V_{th}}}(T_0) - \alpha_{\mathrm{Vth}} T_0 \tag{3.49}$$

By considering α_μ = -2 the specific current I$_s$ can be simplified to:

$$\mathrm{I_{sF}} = 2\mathrm{n}\frac{\mathrm{W}}{\mathrm{L}}\mathrm{C_{ox}}\mu(T_0)(\frac{kT_0}{\mathrm{q}})^2 \tag{3.50}$$

The zero-temperature coefficient current can be obtained by substituting the equation 3.48 into 3.44 together with (3.46) and (3.47) as [26]:

$$\mathrm{I_{DF}} = \mathrm{I_D}(\mathrm{V_{GSF}}) = \mathrm{I_{sF}}[\ln(1 + \mathrm{e}^{-\frac{\mathrm{q}\mu_{\mathrm{V_{th}}}}{2\mathrm{nk}}}] \tag{3.51}$$

It is also important to mention the impact of the drain-source voltage on the ZTC region of operation. The drain-source voltage can influence the ZTC in two aspects: the drain current will change as the transistor goes from the off state through the triode state into the saturation region of operation and the impact of channel length modulation. In the theoretical analysis presented it was assumed that a transistor biased at its ZTC gate-source voltage (V$_{GSF}$) has α_μ = -2 and so the drain current is always temperature dependent as long as the drain-source voltage is not larger than the thermal voltage. So, for the ideal case there is no ZTC condition in the triode region. But as it was previously mentioned the drain current varies with temperature due to the non-ideal behavior of the mobility. The channel modulation can be described by:

$$\mathrm{I_{DCLM}} = \mathrm{I_D} * (1 + \lambda \mathrm{V_{DS}}) \tag{3.52}$$

where λ is the channel modulation coefficient. If the terms in equation 3.52 are temperature independent the channel length modulation term will cancel the derivation of V$_{GS0}$ [26]. Concluding that the channel length modulation will not influence the transistor in ZTC.

The circuit of a ZTC based voltage reference is presented in Figure 3.9.

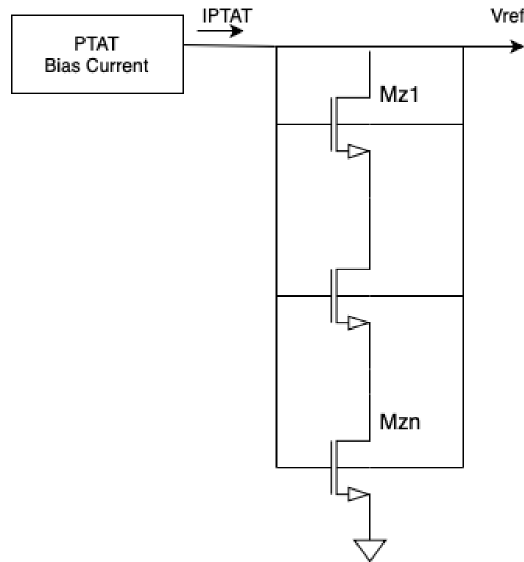

Figure 3.9: ZTC based voltage reference circuit.

The circuit used in [26] and presented in Figure 3.9 was designed to generate a Vref of 0.5 V and shows the concept of this method. The ZTC voltage from equation (3.49) is set by the threshold voltage. For low power operation of the common CMOS devices the V_{GSF} is too high in comparison with a typical threshold voltage around 0.45 V [26]. By biasing the transistors in its CTAT range and with a negative $\alpha_{V_{GS}}$ the transistor will be slightly outside the ZTC point, and will have the gate-source voltage lower than the ZTC voltage. The reference output voltage is obtained by having transistors biased by a PTAT current that will cancel the CTAT.

3.3 Current references

Another important block is the current reference, the complete sensor node will be powered by a 1.2 V battery whose leakage current is 240 nA. So the sensor should spend the minimum current possible, at least half of the battery leakage current. This way the power consumption allows the sensor to be powered for the longest time. The sensor will only make a few temperature readings per day so the current will not be always on. However, for fire detection the sensor must be always reading the temperature and, if the temperature is above a reference value, an alert signal will be generated. To achieve this, the current that is always being consumed should be even lower. Ideally the current used for the regular temperature readings and the fire alert readings should be the same.

A possible circuit can use a previously generated voltage reference and a resistor to obtain the current reference, however, the use of resistors is not ideal to obtain nano-ampere currents. A different circuit based on the subtraction of two PTAT or two CTAT signals can be used to generate the current reference. An alternative to the common beta-multiplier based circuit without resistors is also presented.

3.3.1 Voltage reference based

An ideal current reference should operate in a wide range of temperatures without having variations and impact the precision of the circuits. A conventional way of getting a current reference (Iref) is by using an already existing voltage reference (Vref). This can be achieved by using a voltage to current converter as described by the circuit presented in Figure 3.10.

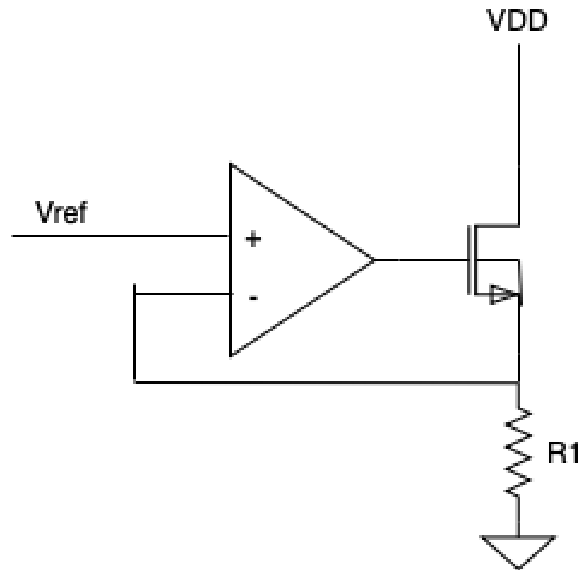

Figure 3.10: Voltage Reference circuit.

This circuit has an amplifier that will force V$_{ref}$ to be applied to R1 and if R1 is a reference resistor, its current will be a reference current. The use of resistors is not suitable for the nano-ampere domain due to area and power constraints as discussed in section 3.1. The voltage reference needs to be generated by a bandgap circuit which also occupies more area and draws more current.

3.3.2 PTAT current (IPTAT) + CTAT current (ICTAT) based

The work in [27] presents a resistor less circuit for a micro-ampere current reference. The circuit is presented in Figure 3.11.

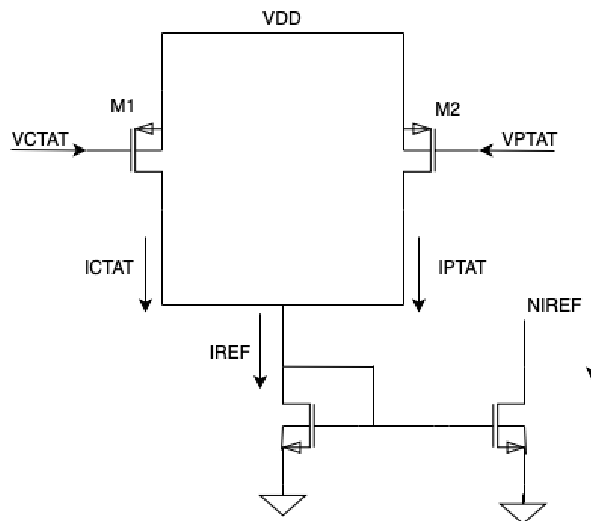

Figure 3.11: IPTAT + ICTAT based circuit.

In this circuit the VCTAT and VPTAT are generated in a different circuit. As the VCTAT flows through M1 a CTAT current (ICTAT) is obtained, and as VPTAT flows through M2 a PTAT current (IPTAT) is obtained. Ths current reference is obtained by the adding the two currents ICTAT and IPTAT. Unlike other circuits, the current reference is obtained with currents and not voltages.

3.3.3 Beta multiplier (BMCS) based

With a Beta Multiplier based current source (BMCS) it is possible to obtain a current in the order of nano-amperes. A schematic of the BMCS circuit is presented in Figure 3.12.

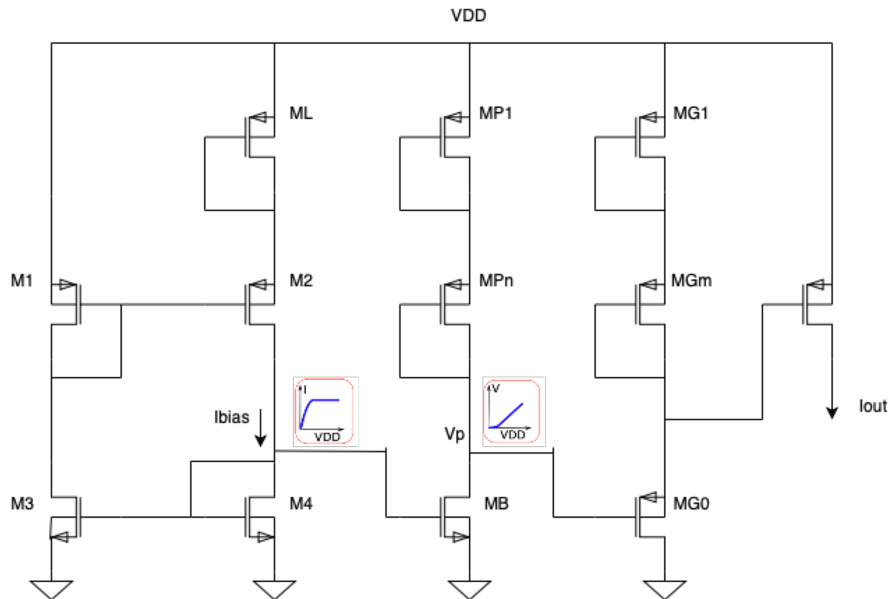

Figure 3.12: Beta Multiplier based current source circuit.

In theory this circuit should result in a supply-independent current Ibias and a voltage that tracks the supply voltage as shown in the graphics of the Figure 3.12. The circuit has a lower power supply dependence than stronger inversion biased source. By considering that the V_{DS} voltages of the transistors are larger than the thermal-voltage of a given temperature, the currents are expected to be insensitive to the supply variations [27] as:

$$\mathrm{I_{bias}} = \mu_\mathrm{p}\mathrm{C_{ox}}\mathrm{K}\frac{\mathrm{W_L}}{\mathrm{L_L}}\mathrm{n}\mathrm{V_T}^2\exp(\frac{-|\mathrm{V_{th}}|}{\mathrm{mV_T}}) \tag{3.53}$$

where K is the beta gain of the left to right devices ratio in the beta multiplier [27].

3.4 BJT, MOS and Resistor bandgap circuits

A temperature sensor needs to generate a VPTAT and a VREF signal to obtain the temperature. This section describes how to obtain this signals with the commonly used devices BJT, MOSFET and resistors.

A bangap voltage reference can also be designed with a BJT-based circuit to generate both the PTAT and CTAT voltages. The circuit can be designed with two vertical PNPs biased at different collector current densities (Figure 3.13) or with different dimensions in the transistors with the same current density.

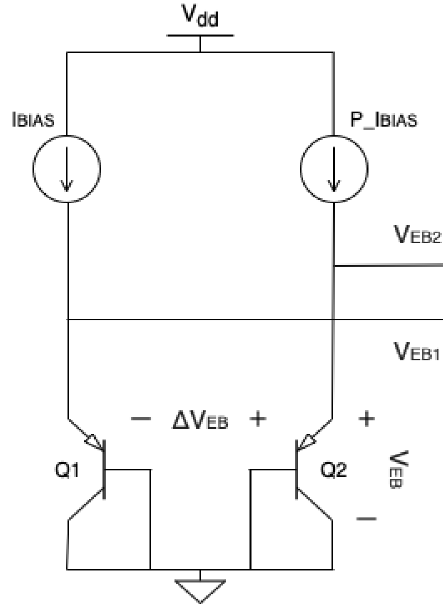

Figure 3.13: BJT-based.

The V_{BE} of a BJT in the active region is [3]

$$V_{EB}(T) = \frac{kT}{q} \ln \frac{I_C}{I_S} \tag{3.54}$$

where k is Boltzmann´s constant, q is the electron charge, T is the absolute temperature, I_S the inverse saturation current, and I_E is the emitter current imposed by a bias current. The V_{EB} has a nonlinear dependence with temperature. This voltage is temperature sensitive and complementary to temperature, being the CTAT signal.

The difference between the two transistors V_{EB} is expressed as:

$$\Delta V_{EB}(T) = \frac{kT}{q} \ln \frac{(I_C)}{(I_S)} - \frac{kT}{q} \ln \frac{(pI_C)}{(I_S)} = \frac{kT}{q} \ln(p) \tag{3.55}$$

The ΔV_{EB} depends on the ratio p and is proportional to the absolute temperature, serving as the PTAT signal.

The bandgap reference is created by combining both PTAT and CTAT signals: [2]

$$V_{REF} = V_{EB} + \alpha \Delta V_{EB} \tag{3.56}$$

With gain α.

Recently the MOSFET-based core became an alternative to the BJTs-based. The transistors of Figure 3.13 can be replaced by MOSFETs as shown in Figure 3.14.

Figure 3.14: NMOS-based.

In this architecture, the difference of the V_{GS} in the sub-threshold is low order function of the temperature *T*, which depends on transistors V_{TH} and the sub-threshold slope ξ [2].

Resistor-based sensors have proven to be stable, accurate and energy efficient [12], but lack in the sensor area. The temperature dependencies of these sensors are determined by the temperature coefficient (TC) of the resistor. In standard CMOS the resistors available are: metal resistors, diffusion resistors, poly resistor and silicided resistors [10]. The resistor should be chosen so that the voltage generated by it is as invariant with temperature as possible.
These sensors can be designed using a Wheatstone bridge (WhB) or by combining the temperature-dependent resistor *R(T)* with a low TC capacitor in order to get a temperature dependent circuit response, like a poly-phase filter (PPF) or a Wien-bridge (WB) sensor.
When using a Wheatstone bridge the value of *R(T)* is compared with a stable resistor, or with a different resistor whose temperature dependency is also different [12],[15]. As shown in Figure 3.15, there are two different types of resistors *R1* and *R2* that have different temperature coefficients.

Figure 3.15: Wheatstone-Bridge circuit.

The *Vdd* temperature dependencies will make the bridge output to be a temperature-dependent current I_{WhB}, which can be converted for example with a resistor DAC [12]. However, this design suffers twice from process spreading because it uses two different types of resistors.

A common RC filter used in temperature sensors is the Wien-bridge (WB) RC filter, whose phase shift can be digitized using a stable time reference [10] - [12]. A resistor-based temperature sensor needs to be able to generate a stable reference, which is hard to achieve with the standard CMOS technology. For the WB sensor the metal-insulator-metal (MIM) capacitors are an alternative for this reference because of the very low TC values (10 ppm/ºC [10]). In Figure 3.16 a WB *RC* filter circuit is shown.

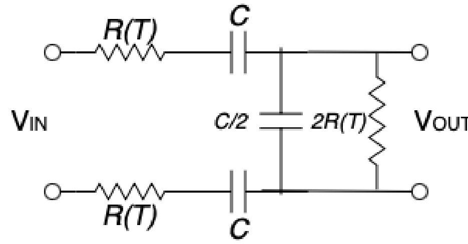

Figure 3.16: WB *RC* filter circuit.

The circuit works as a second-order bandpass filter (BPF), whose voltage gain magnitude function can be written as [10]

$$\mathrm{H}(\omega) = \frac{\mathrm{R}^2\mathrm{C}^2\omega}{1 - \mathrm{R}^4\mathrm{C}^4\omega^4 + 9\mathrm{R}^2\mathrm{C}^2\omega} \tag{3.57}$$

and phase transfer function

$$\gamma_{\mathrm{WB}}(\omega) = -\tan^{-1}(\frac{\mathrm{R}^2\mathrm{C}^2\omega^2 - 1}{3\mathrm{RC}\omega}) \tag{3.58}$$

where the frequency is normalized by $f_0 = 1/(2\pi\mathrm{RC})$ [10].

However, the filter´s phase γ_{WB} and center frequency f_0 are temperature dependent. When the γ_{WB} is fixed at 0 the frequency will vary, and for a fixed f_0 the phase γ_{WB} will vary. At least one additional circuit, for example, a digital phase/frequency detector is necessary. The resistors and capacitors are responsible for determining the phase of the WB, for a fixed driving frequency f_d. However, as previously mentioned the temperature sensitivity of MIM capacitors is not very high, so the resistors will determine the phase shift. That can be determined either by measuring the voltage across the output resistor 2*R(T)* or by measuring the current flowing through it [10].

An RC poly-phase filter (PPF) can be an alternative to the WB filters because of the higher frequency-to-phase gain and larger voltage swing [11], that allow a simpler way to determine the phase shift. Figure 3.17 shows the circuit of the PPF filter that is designed with a pair of resistors and capacitors.

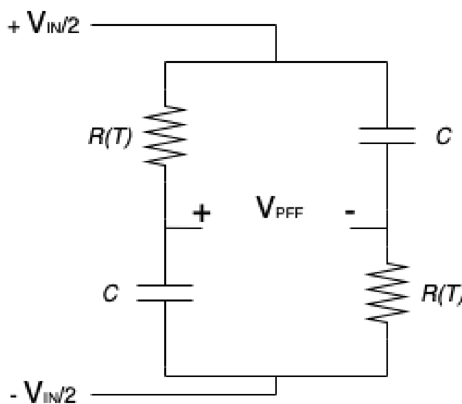

Figure 3.17: PPF *RC* filter circuit.

The gain voltage amplitude function can be written as

$$\mathrm{H}(\omega) = \frac{1 - \mathrm{R}^2\mathrm{C}^2\omega}{1 + \mathrm{R}^2\mathrm{C}^2\omega} \tag{3.59}$$

and phase transfer function [11]

$$\gamma_{\mathrm{PPF}}(\omega) = 2\tan^{-1}(-\mathrm{RC}\omega) \tag{3.60}$$

where the frequency is normalized by f_0 = 1/(2πRC) [11]. The PPF sensor´s phase γ_{PPF} and f_0 are temperature dependent therefore, as the WB sensor, an additional circuit, for example, a digital phase/frequency detector is necessary. The advantage of this sensor in comparison with the WB sensor is the area efficiency where it has fewer elements (2R and 2C).

Chapter 4

Devices temperature behaviour

In this section the behaviour with temperature of the most common components used in electronic circuits are studied and simulated in UMC 130 nm CMOS technology.

4.1 Bipolar Junction Transistor (BJT)

The bipolar junction transistors can be NPN (Figure 4.1 (a)) or PNP (Figure 4.1) (b)).

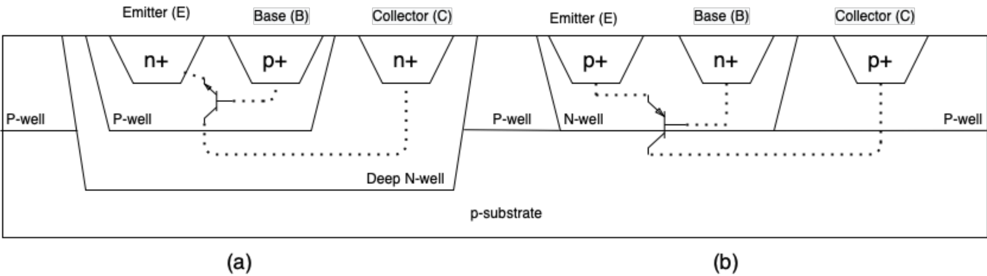

Figure 4.1: (a) NPN transistor. (b) PNP transistor.

Both transistors are formed in a p-substrate where the PNP transistor needs a n-well and the NPN transiros needs a deep n-well and a p-well. The PNP transistors can be developed in every CMOS technology while NPN transistors can only be designed in the CMOS technolog that has deep n-wells. This leads to the following simulations being made with PNP transistors.

The circuit in Figure 4.2 with a PNP transistor was simulated.

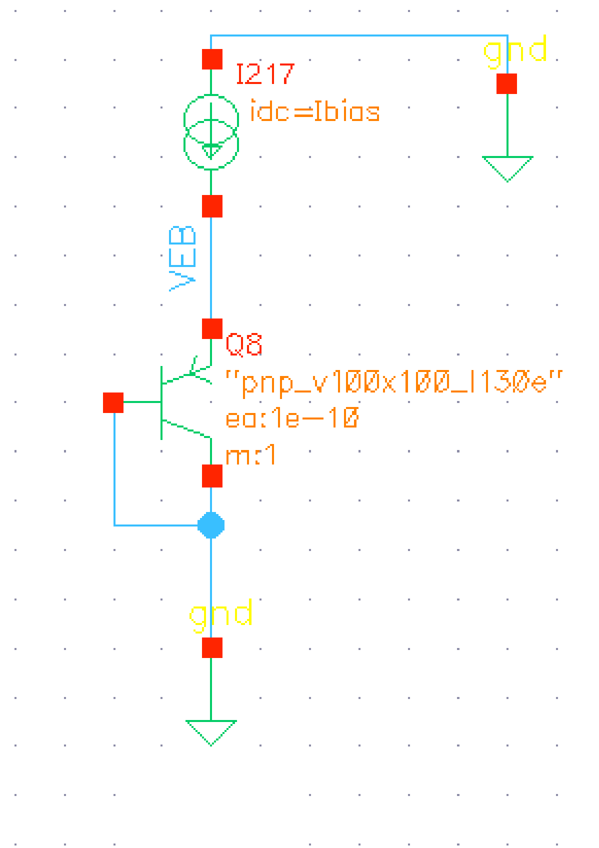

Figure 4.2: BJT in the active region.

The circuit was simulated with a current Ibias of 2 nA and 10 nA in Figure 4.3.

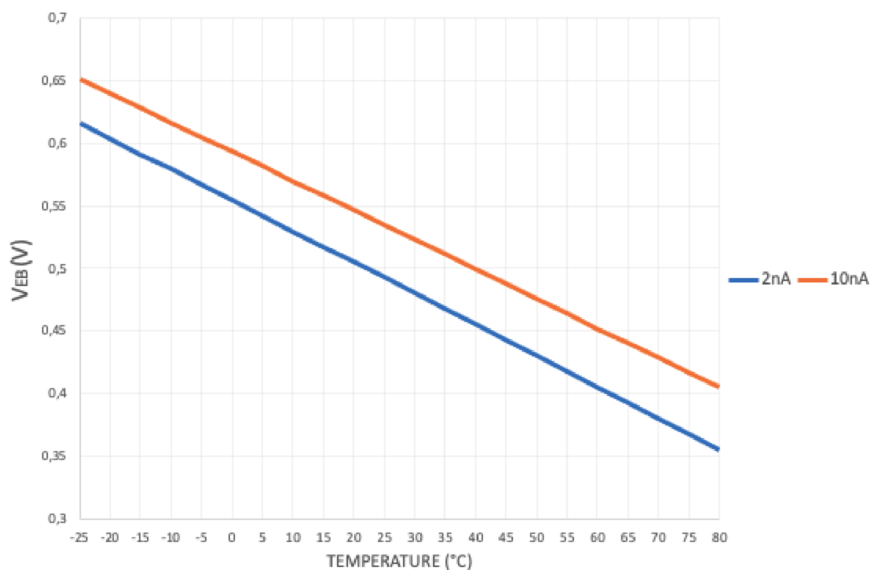

Figure 4.3: BJT behaviour for a current of 2 nA and 10 nA.

The results for both currents are similar and confirm the theoretical analysis being a CTAT signal. Despite the change in the current the voltage values are similar, initially around the 600/650 mV and ending around 300/400 mV. The V_{EB} will vary with different transistor sizes. The simulation shows an almost

linear CTAT signal which would be ideal, however when simulating the derivative of the obtained V_{EB} in Figure 4.4 it is shown that this voltage is not linear.

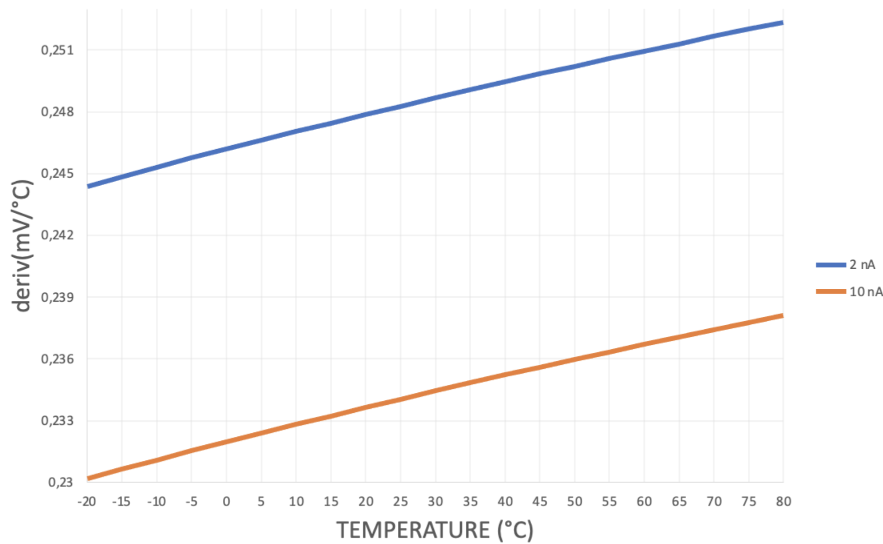

Figure 4.4: Derivative of the obtained V_{EB} with a current of 2 nA and 10 nA.

After the simulation of a single BJT the voltage circuits presented in 4.5 were tested and simulated.

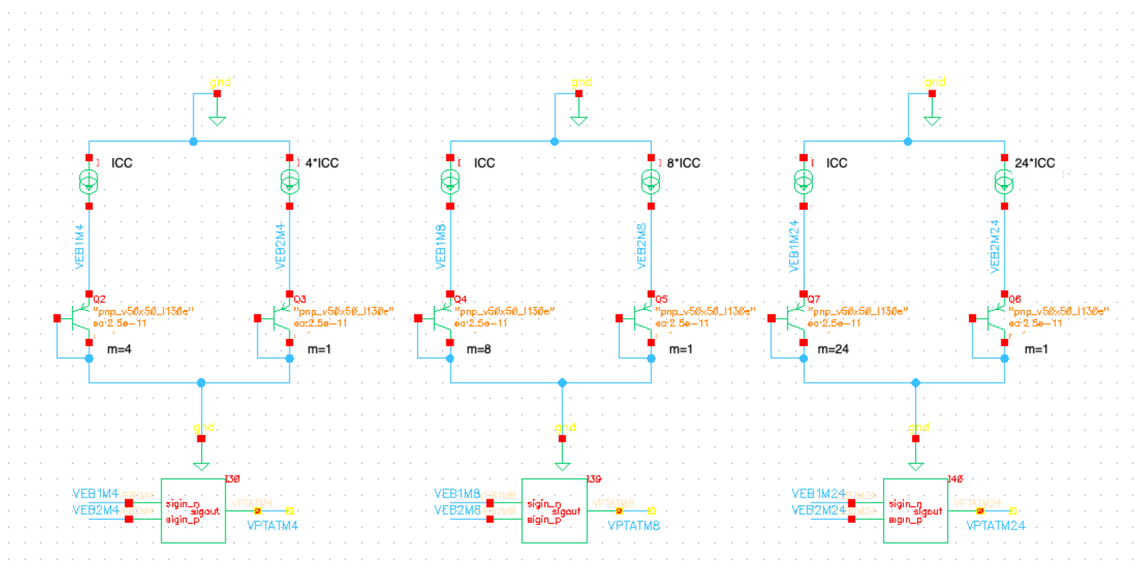

Figure 4.5: BJT voltage circuits simulated.

Each circuit is made with a pair of bipolar junction transistors (BJT) with a proportion of 4:1, 8:1 and 24:1, for example, the 4:1 means there are 4 transistors in parallel to 1 transistor. In Figure 4.5 the number of transistors is identified by the letter **m** next to each transistor. The transistor ratios were tested with these values due to the common centroid layout. In a further stage of the project the layout will be easier to design.

The bias currents ICC were also made with 1:4, 1:8 and 1:24 current ratio, identical to each transistor ratio. For example, the 1:4 current collector ratio corresponds to the 4:1 transistor ratio. The transistor and currents ratios were designed to be opposite to maximize the value of ΔV_{EB}. The simulated current values are 100 pA, 1 nA, 10 nA and 100 nA.

The VPTAT was calculated as in the BJT-based sensing cores:

$$\mathrm{VPTAT(V)} = \mathrm{V_{EB2}} - \mathrm{V_{EB1}} \tag{4.1}$$

This operation was made with a verilogA subtractor block.

In a first stage of the simulation the 1:4 collector current ratio and 4:1 transistor ratio were tested in Figure 4.6. Performing a temperature sweep from -25 $^{\circ}C$ to 80 $^{\circ}C$:

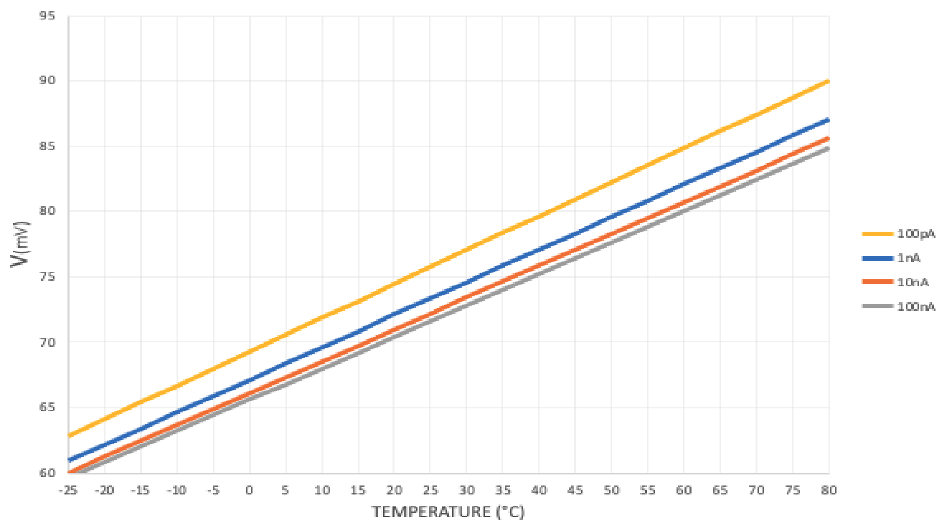

Figure 4.6: BJT VPTAT simulations with a 1:4 current collector ratio and 4:1 transistor ratio

As expected the VPTAT signal is almost linear with temperature. In Figure 4.7 it was plotted the derivative of the VPTAT signals obtained in Figure 4.6.

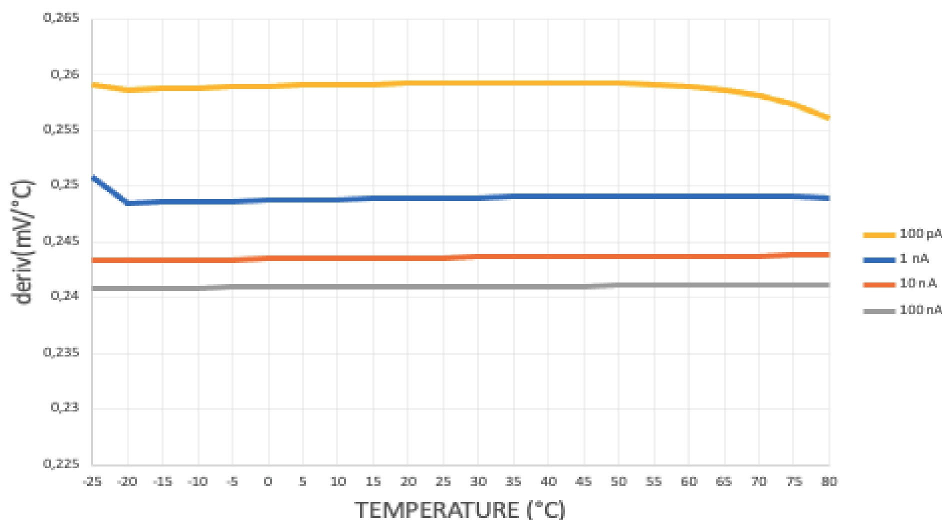

Figure 4.7: BJT VPTAT slope simulations for 100 pA, 1 nA, 10 nA, 100 nA

The most adequate current is obtained with 100 pA that has the biggest slope.

For the next simulation it was plotted the VPTAT for each of the collector current and transistor ratio for the 100 pA.

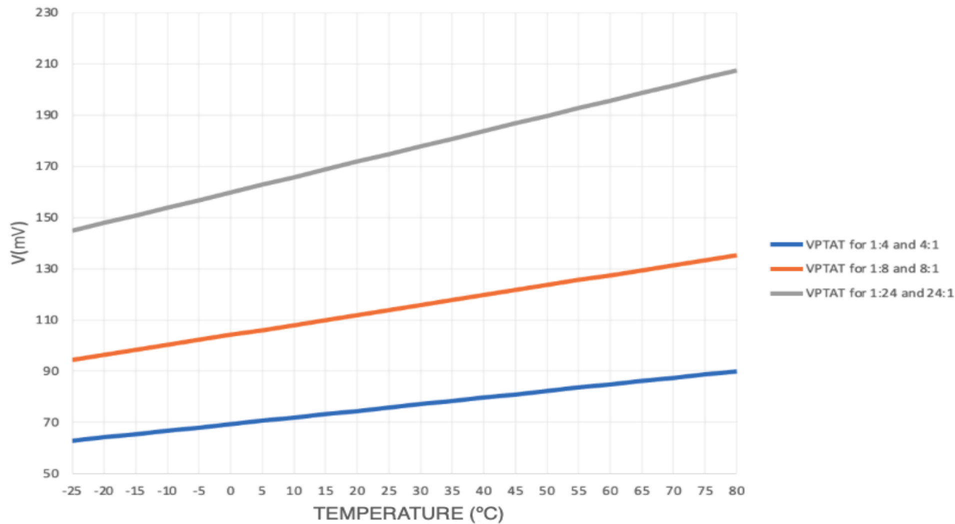

Figure 4.8: BJT VPTAT simulations for 100 pA

The maximum VPTAT values are obtained for the 1:24 collector current ratio and 24:1 transistor ratio. Table 4.1 shows the ΔVPTAT correspondent to 1 $°C$ in 100 pA.

Table 4.1: BJT voltage for 1 $°C$ with 100 pA.

Current collector - transistor ratio	V (mV)
1:4 - 4:1	1.454
1:8 - 8:1	2.18
1:24 - 24:1	3.35

The sensor resolution is obtained with the ΔVPTAT and the VLSB of the ADC. As previously mentioned the ADC [17] has a VLSB = 2.56 mV, and with a current of 100 pA and a ratio of 1:24 - 24:1 the ΔVPTAT = 3.35 mV. As the ΔVPTAT $>$ VLSB the resolution of 1 $°C$ can be achieved. For example, for the ratio of 1:8 - 8:1 and 1:4 - 4:1 with the ΔVPTAT = 2.18 mV and ΔVPTAT = 1.454 mV, respectively, the sensor could not be designed with the same resolution. The temperature sensor should have the best resolution possible and, for example, for a resolution of 0.25 $°C$ the ΔVPTAT calculations are presented in Table 4.2.

Table 4.2: BJT voltage for 0.25 $°C$ with 100 pA.

Current collector - transistor ratio	V (mV)
1:4 - 4:1	0.364
1:8 - 8:1	0.547
1:24 - 24:1	0.839

With these results it is not possible to design the sensor with this resolution. A possible solution would be to increase the resolution of the ADC, increasing the ENOB the VSLB value will be lower, for example, for 11 ENOB the VLSB = 0.585 mV. The resolution of 0.25 $°C$ of the temperature sensor would be possible with the ratio of 1-24 - 24:1.

The VREF signal was also plotted for these currents. In a BJT-based circuit:

$$\mathrm{VREF(V)} = \alpha(\mathrm{V_{EB2}} - \mathrm{V_{EB1}}) + \mathrm{V_{EB1}} \tag{4.2}$$

With a gain $\alpha = 8.6$, imposed using the verilogA block, the VREF signal was plotted in Figure 4.9

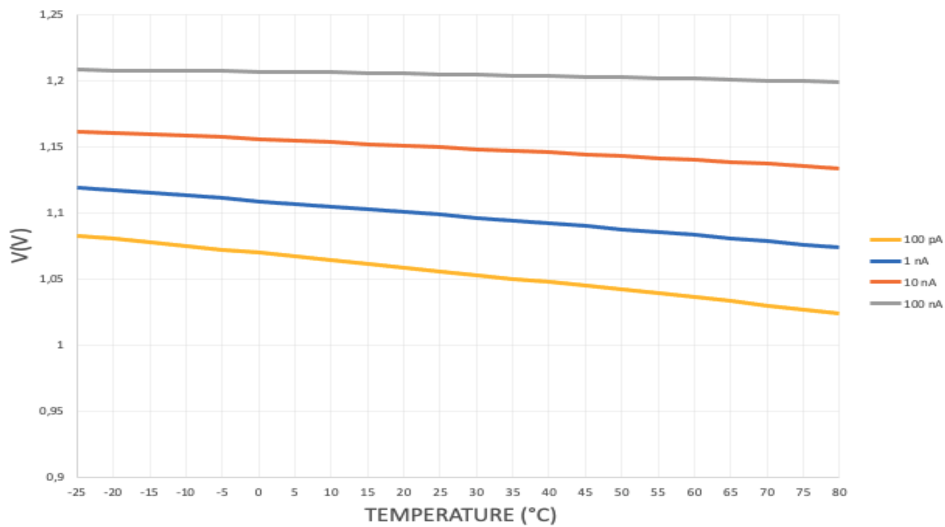

Figure 4.9: BJT VREF simulations with a 1:4 current collector ratio and 4:1 transistor ratio

The VREF plotted still shows a slight slope for all currents simulated. The best VREF is achieved with 100 nA with a variation of approximately 0.009 mV. However, the VREF voltage is around 1.2 V, because is generated with the difference of two voltages, that will be the supply voltage of the sensor, so an alternative to generate the VREF is needed.

4.2 MOSFET

Following the simulations with BJT circuits with MOSFET were simulated. The circuit presented in Figure 4.10 was simulated with 2 nA and 10 nA.

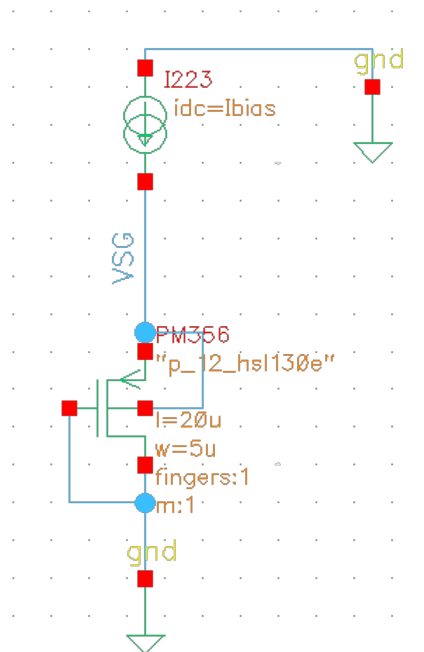

Figure 4.10: Single PMOS circuit.

The results are presented in Figure 4.11. The voltage decreases with the increase of the temperature as in the BJT circuit of Figure 4.2.

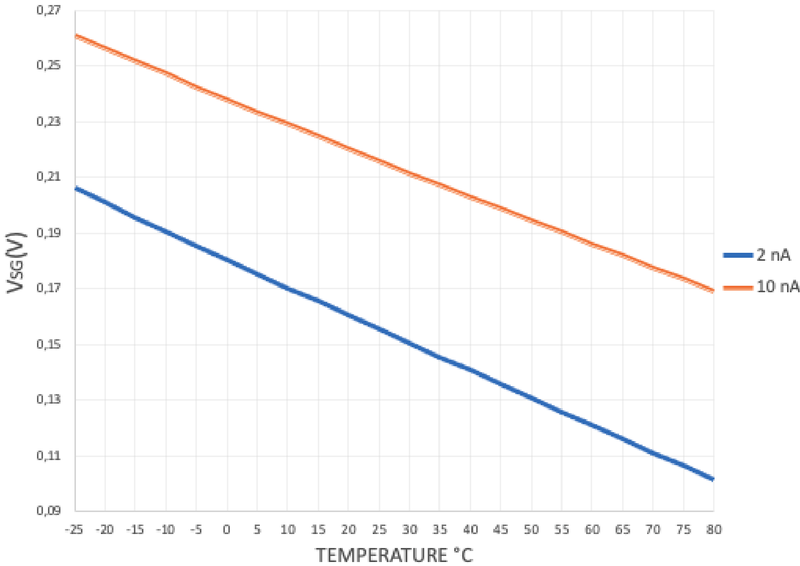

Figure 4.11: PMOS behaviour for a current of 2 nA and 10 nA.

As the V_{SG} obtained seemed almost linear the derivative of the signal was simulated and is shown in Figure 4.12.

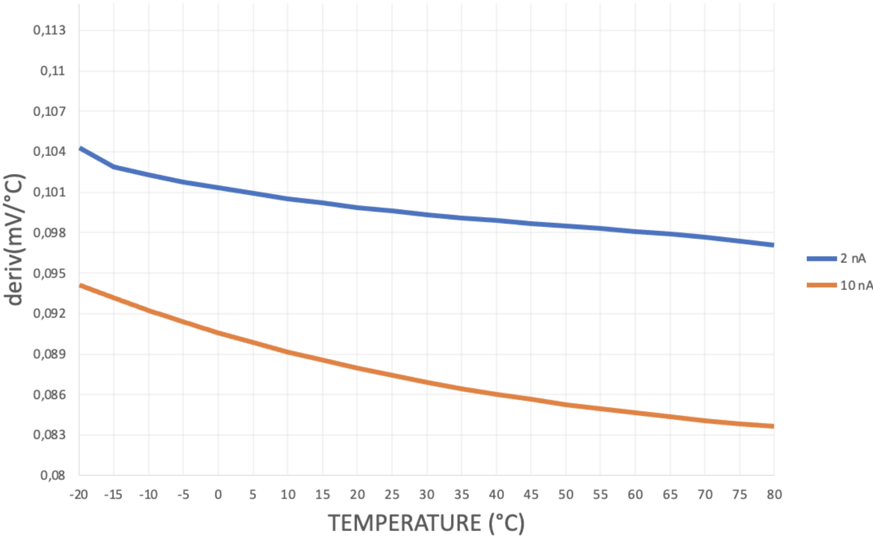

Figure 4.12: Derivative of the obtained V_{SG} with a current of 2 nA and 10 nA.

With the derivative it is shown that the voltage signal is not linear.

A further study was made with the circuits presented in Figure 4.13 with NMOS transistors.

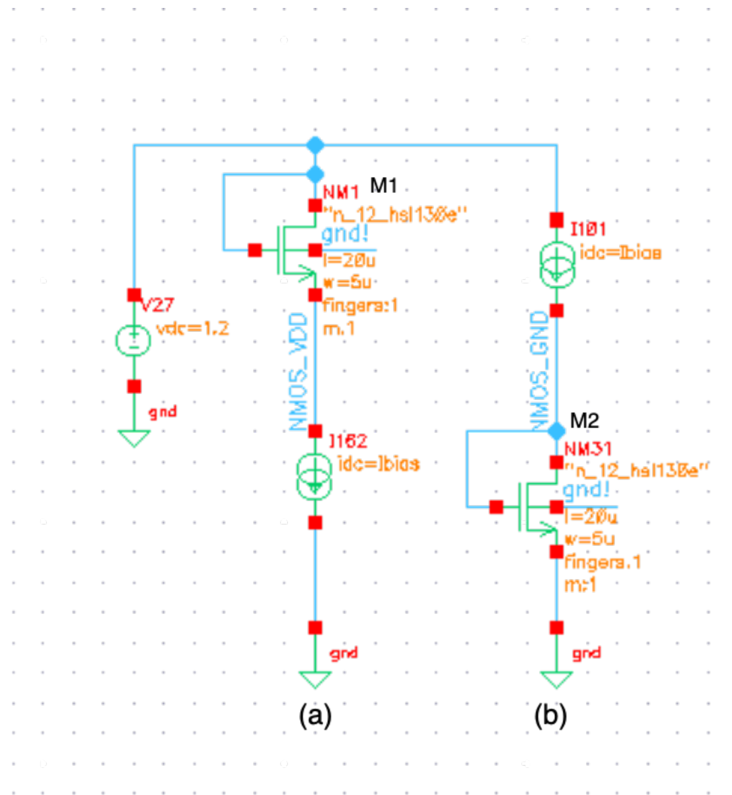

Figure 4.13: (a) NMOS connected to VDD; (b) NMOS connected to GND.

Table 4.3: Circuit 4.13 dimensions

Transistor	W; L
M1	W= 5 μm; L = 20 μm
M2	W= 5 μm; L = 20 μm

The circuit (a) has body effect and circuit (b) does not. The circuits were simulated with currents of 10 nA and 30 nA. In Figure 4.14 and 4.15 the NMOS circuits (a) and (b) simulated results are shown, respectively.

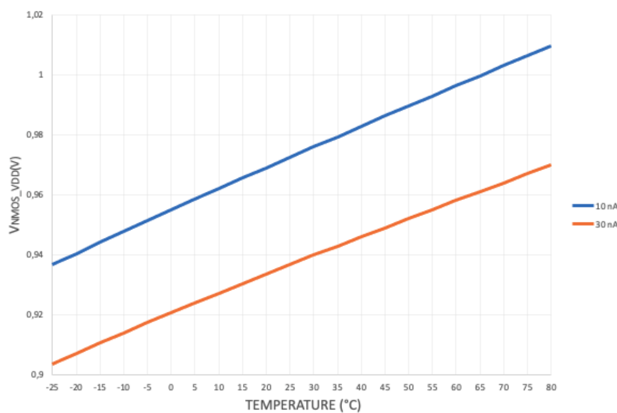

Figure 4.14: Circuit (a) simulated with 10 nA and 30 nA.

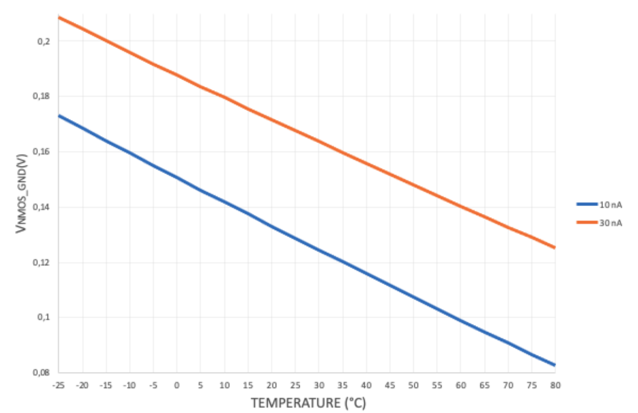

Figure 4.15: Circuit (b) simulated with 10 nA and 30 nA.

These simulations prove that is possible to get a proportional to temperature voltage with the circuit (a)

and an opposite to temperature voltage in circuit (b).

The same simulations were made for the circuits with PMOS transistors of Figure 4.16.

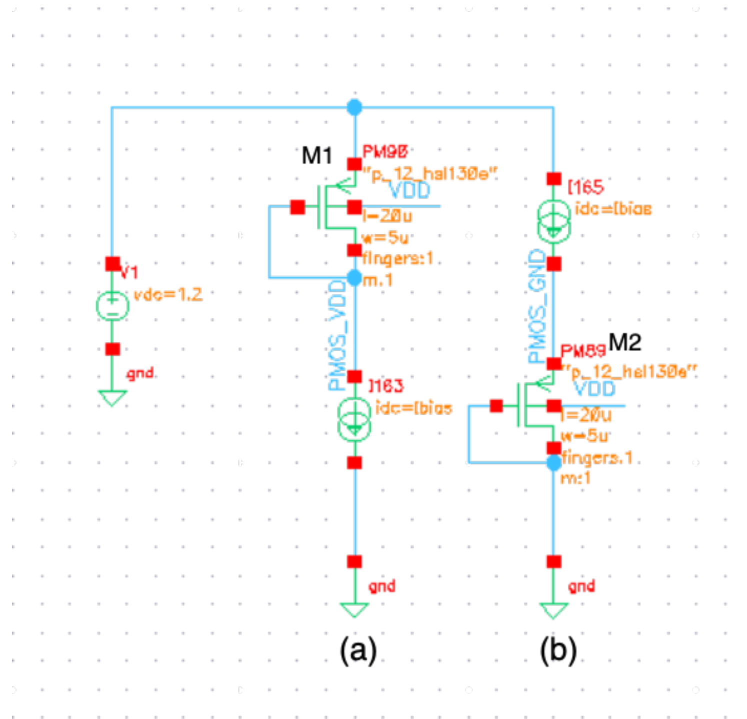

Figure 4.16: (a) PMOS connected to VDD; (b) PMOS connected to GND.

The results and conclusions were similar, as represented in Figure 4.17 with the circuit (a) and in Figure 4.18 with the circuit (b).

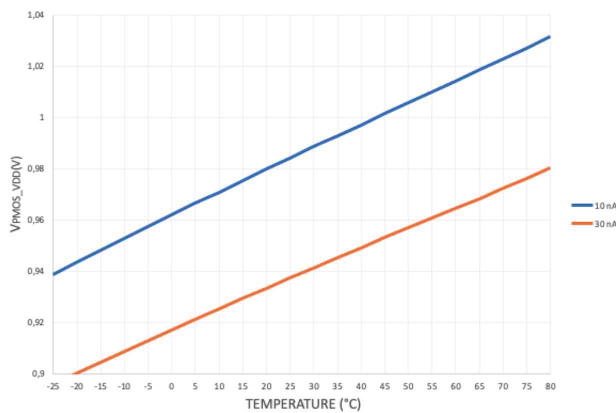

Figure 4.17: Circuit (a) simulated with 10 nA and 30 nA.

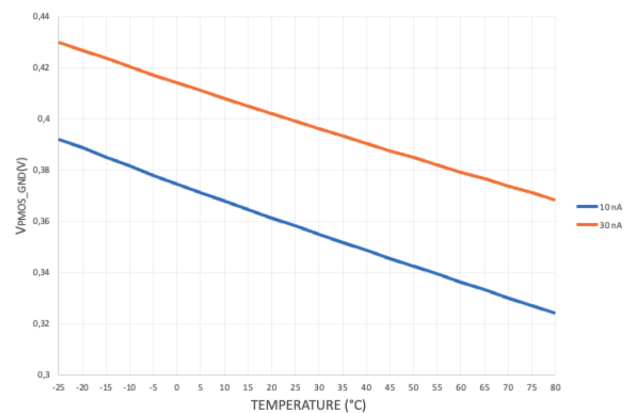

Figure 4.18: Circuit (b) simulated with 10 nA and 30 nA.

To start the development of the sensor MOSFET based bandgap circuits presented in Figure 4.19 were simulated.

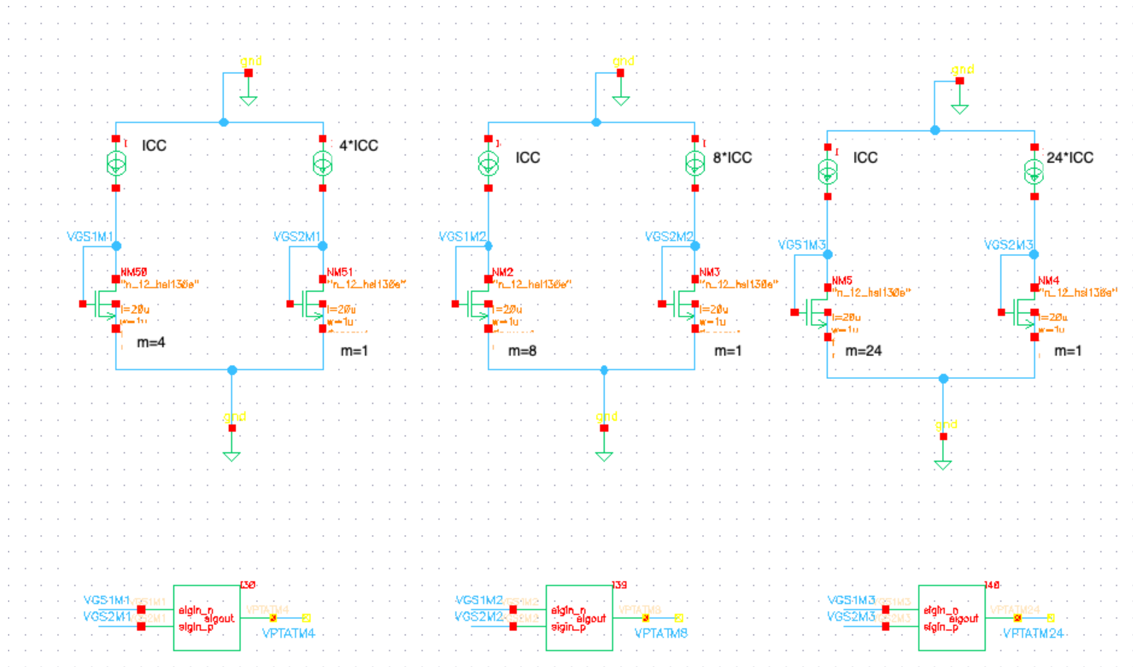

Figure 4.19: MOSFET voltage circuits simulated.

These circuits follow the same logic as the BJT circuits previously presented. The VPTAT is now calculated as:

$$\mathrm{VPTAT(V)} = \mathrm{V_{SG2}} - \mathrm{V_{SG1}} \quad (4.3)$$

In the first simulation the 1:4 current ratio and 4:1 transistor ratio circuit was simulated with 10 nA and 100 nA, presented in Figure 4.20.

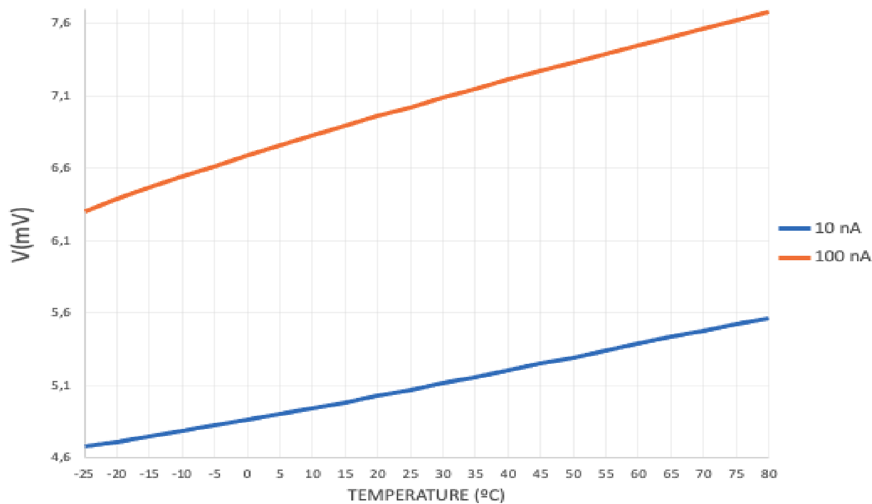

Figure 4.20: MOS VPTAT simulations with a 1:4 current collector ratio and 4:1 transistor ratio.

The VPTAT obtained seems to be almost linear and so the derivative of the signals was simulated and presented in Figure 4.21

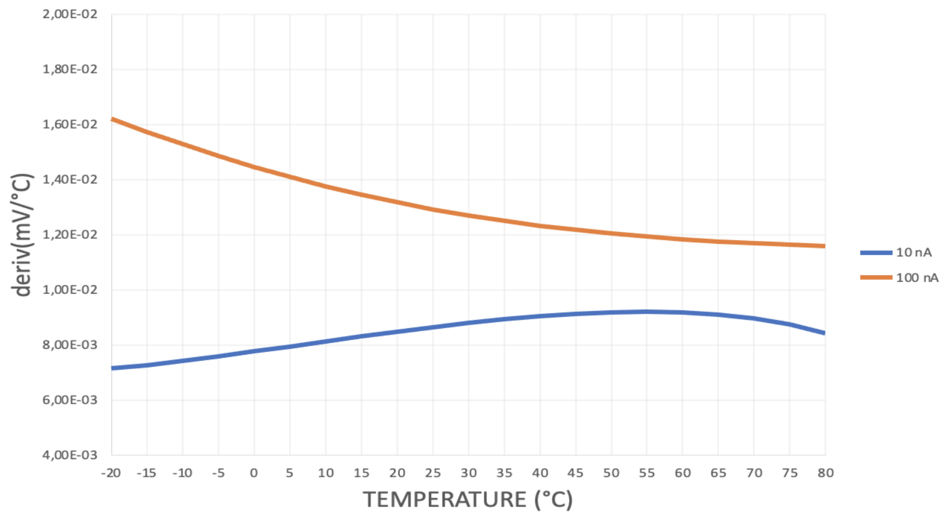

Figure 4.21: MOS VPTAT slope simulations for 10 nA and 100 nA.

As the most adequate current is 100 nA every circuit was simulated with this current and Figure 4.22 was obtained.

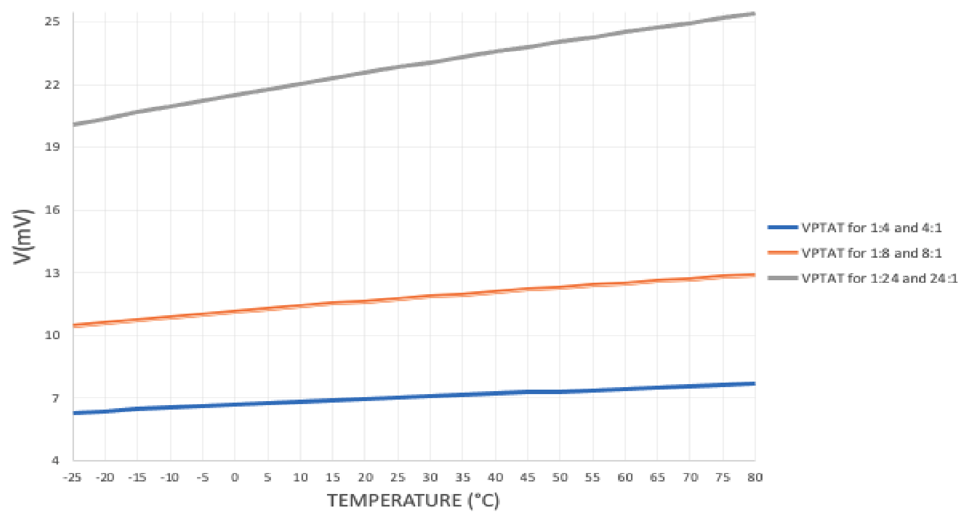

Figure 4.22: MOS VPTAT simulations for 100 nA.

It is possible to observe an almost linear signal. For this range of temperatures the voltage values obtained for 1 $°C$ are presented in Table 4.4.

Table 4.4: MOS voltage for 1 $°C$ with 100 nA.

Current - transistor ratio	V (mV)
1:4 - 4:1	0.013
1:8 - 8:2	0.022
1:24 - 24:1	0.05

With this results the sensor would not be possible to design because the ADC´s VLSB $>$ ∆VPTAT. Concluding that the transistors do not have the proper dimensions.
The VREF signal was plotted for the currents of 10 nA and 100 nA in the circuit with 1:4 and 4:1 ratios.

The VREF is now given as:

$$\mathrm{VREF(V)} = \alpha(\mathrm{V_{SG2}} - \mathrm{V_{SG1}}) + \mathrm{V_{SG1}} \tag{4.4}$$

With an imposed gain of $\alpha = 8.6$ the VREF obtained is presented in Figure 4.23

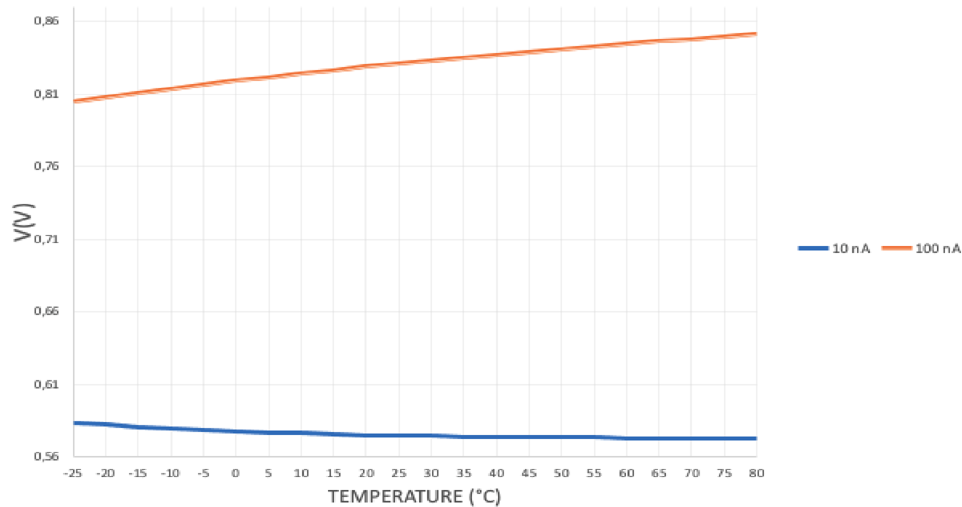

Figure 4.23: MOS VREF simulations with a 1:4 current ratio and 4:1 transistor ratio.

4.3 Resistors

The available resistors in UMC 130 nm technology are presented in Table 4.5.

Table 4.5: Available resistors in UMC 130 nm technology.

	Resistor Type
RN	Resistor without salicide (medium value)
RS	Resistor with salicide (lower value)
PPO	Poly1 resistor (over P+ inside n-well)
NPO	Poly1 resistor (over N+)
H	kohm high value poly resistance
PD	P+ resistor (over n-well)
ND	N+ resistor
RF	Capacitor with high frequency model

The silicide is used to reduce contact resistance between metal and active area and reduce the active area resistance. The objective was to simulate a resistor with high value and so the resistor H with kohm high value poly resistance was simulated in the circuit of Figure 4.24.

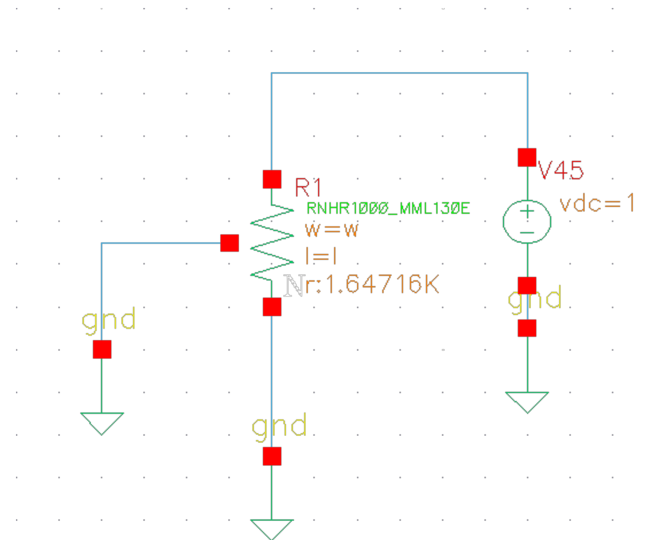

Figure 4.24: Resistor circuit.

The resistor with width and length values of 2u has a resistance value around the 800 Ω□ and the results for the temperature dependence are presented in Figure 4.25.

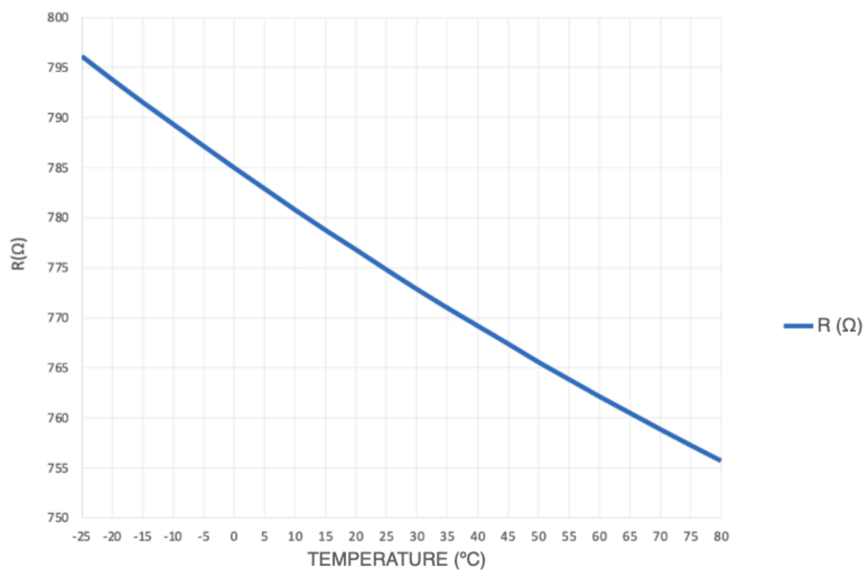

Figure 4.25: Resistor temperature behaviour.

It is noted that the resistor value has a large decrease with temperature, meaning that the temperature coefficient of the resistor is large. As previously mentioned this project aims for a low power and low area circuit, so because the use of resistors requires a larger area it was decided to minimize or avoid their use.

Chapter 5

Temperature sensor

In this section it is presented the methodology behind the development of the final circuit. Following the previous studies it was decided to design the circuit using only PMOS transistors. It should be kept in mind that the final circuit will be globally optimized to obtain better results.

5.1 Temperature sensor frontend

The final PTAT circuit can be made based on a voltage or current reference, as theoretically presented in Section 3. Using a voltage reference, a transistor powered by this voltage will have the VSG almost stable and with the proper dimensions a CTAT output voltage will be generated. Combining two of these circuits the subtraction of the CTAT signals can be made to generate the desired PTAT signal. Using a current reference, a current mirror with a transistor can be made and both CTAT signals obtained.

Based on the method presented in Section 3.7 article [28], it was decided to design a current reference circuit. This method consists in the generation of a stable current by controlling the body voltage of a transistor. Initially the circuit presented in Figure 5.1, with the dimensions in Table 5.1, was designed to study the current behavior.

Table 5.1: Figure 5.1 dimensions

Transistor	W; L
M1	W = 1 μm; L = 5 μm
M2	W = 100 μm; L = 1 μm

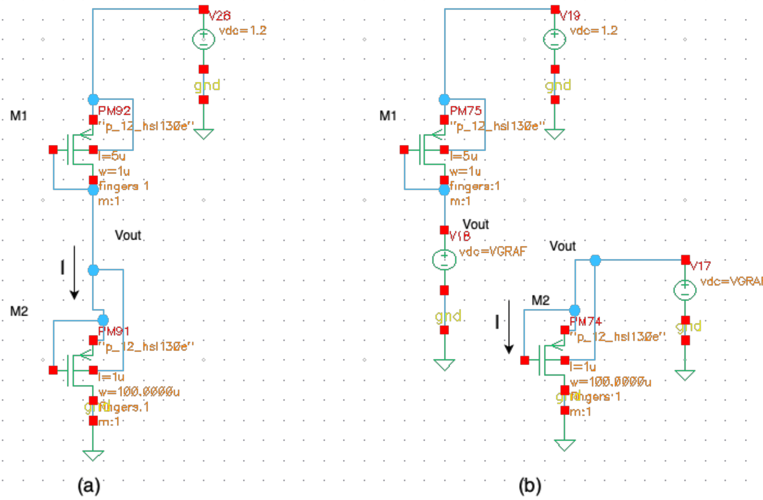

Figure 5.1: Current behaviour: (a) global circuit, (b) partial circuits.

As a starting point a graphical study was made based on simulation results. The partial circuits were simulated for temperatures of 0 $^{\circ}C$, 27 $^{\circ}C$ (nominal temperature) and 50 $^{\circ}C$. For the given temperatures the current (I) and output voltage (Vout) were obtained in Figure 5.2.

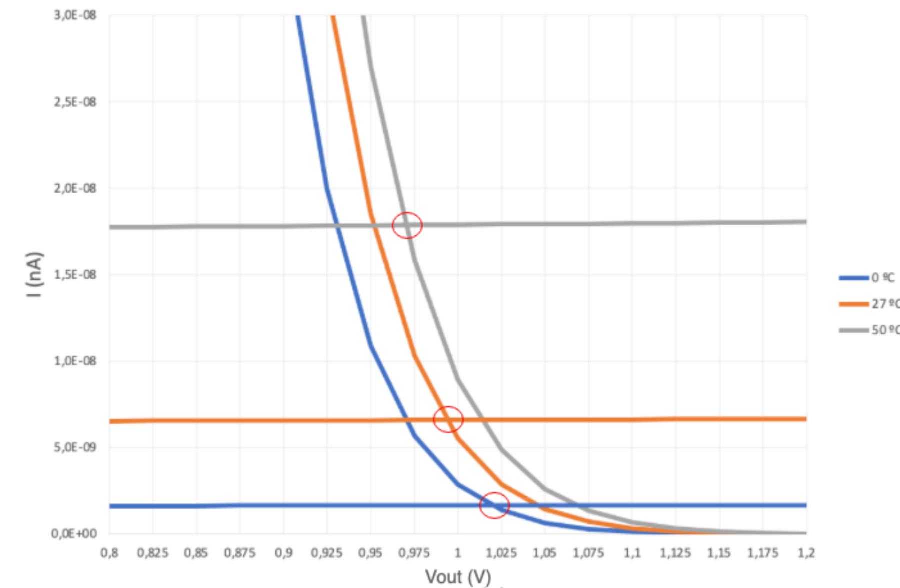

Figure 5.2: Current (nA) in function of Vout (V) for each temperature.

By combining the obtained results each interception represents the current and output voltage for the given temperature. The top interception is for 50 $^{\circ}C$ (represented in grey), the middle interception for 27 $^{\circ}C$ (represented in orange) and the bottom interception is in 0 $^{\circ}C$ (represented in blue). This means that the current will increase with temperature, as expected.
The output voltage and current obtained behaviour with temperature is presented in Figure 5.3 and Figure 5.4.

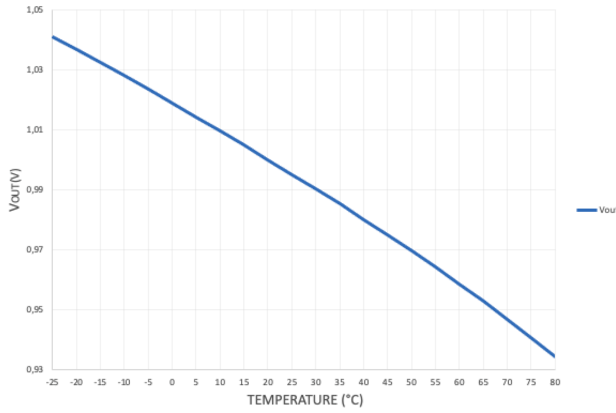

Figure 5.3: Vout (V).

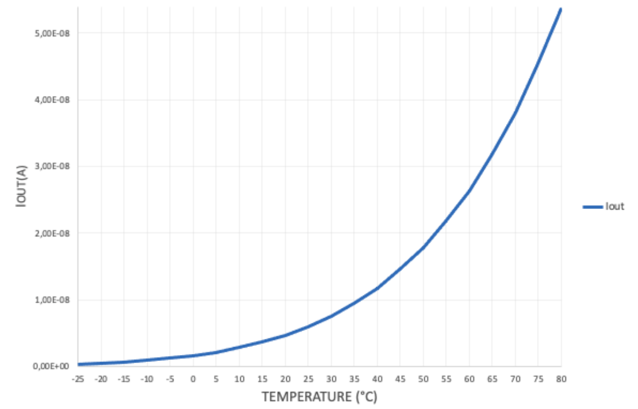

Figure 5.4: Iout (A).

This circuit does not generate a stable current reference, nor voltage reference but Vout varies much less than Iout. Following the method presented in [28] an attempt was made to control the voltage of M2´s body to compensate the current variations. So, it was important to understand how the voltage at the body will impact the circuit current. The circuit of Figure 5.5 was simulated with new dimensions, presented in Table 5.2.

Table 5.2: Figure 5.5 dimensions

Transistor	W; L
M1	W = 1 μm; L = 20 μm
M2	W = 40 μm; L = 1 μm

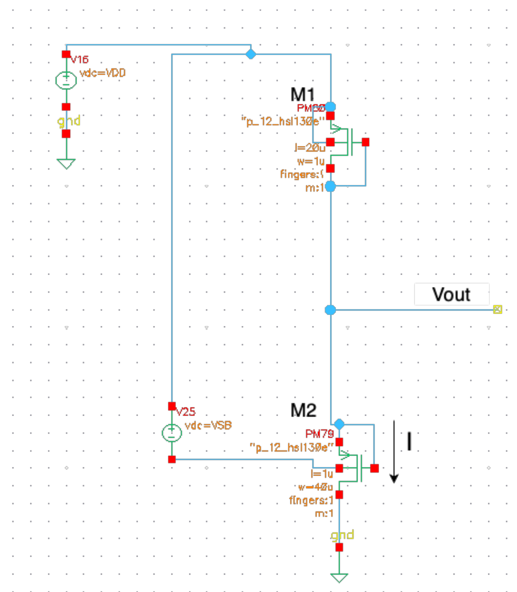

Figure 5.5: Body effect study in circuit 5.1.

The simulations were made for the nominal temperature of 27 $°C$, 0 $°C$ and 50 $°C$ in terms of VDD. By specifying the temperatures it is easier to observe the different current (Iout) values of each one. The currents obtained are presented in Figure 5.6.

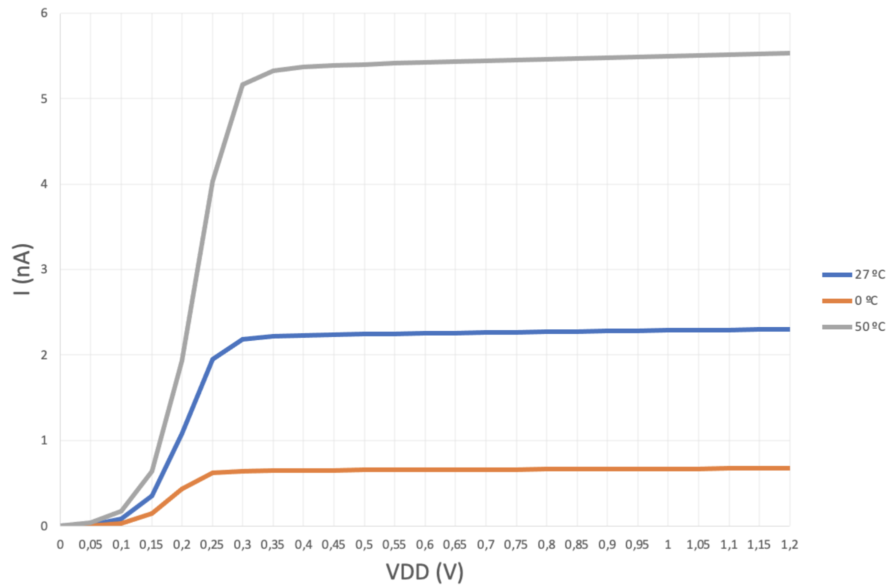

Figure 5.6: I (nA) for temperatures of 0°C, 27°C and 50 °C in function of VDD.

It is easily observed that the current has a large increase with the temperature increment. In all simulations the current becomes stable with VDD around 0.3 V. So, as the temperatures become stable around the same value it is possible to match the currents values. A new simulation was made, fixing the VDD - Vbody = 0.2 V for the 27 °C and changing this voltage for the other temperatures. The values of the currents match with VDD - Vbody = 0.43 V for 0 °C and 0.02 V for 50 °C were obtained. The results are presented in Figure 5.7.

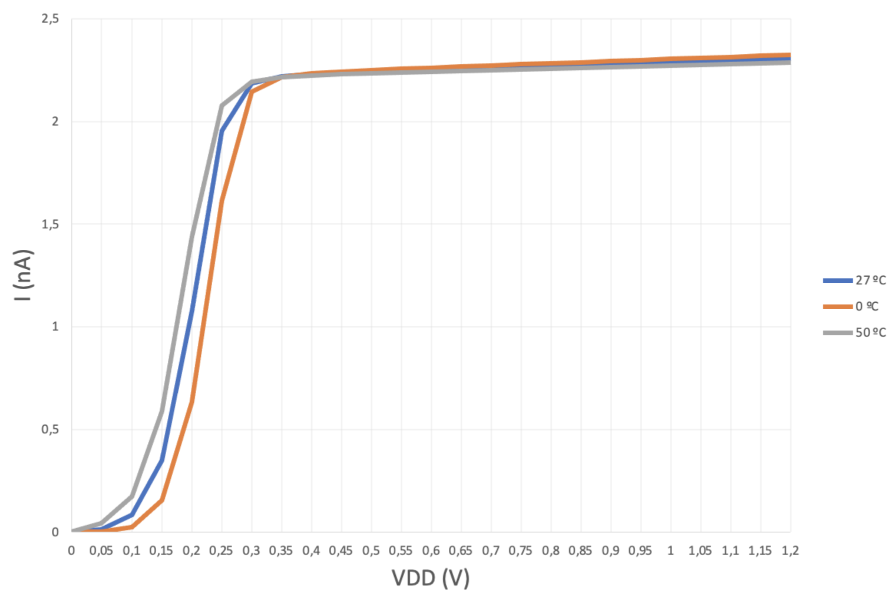

Figure 5.7: I (nA) for a voltage VDD - Vbody = 0.2 V for 27 °C, 0.43 V for 0 °C and 0.02 V for 50 °C.

Table 5.3: Body voltage for each temperature

Temperature	Vbody voltage (Vbody)
0 $^\circ C$	770 mV
27 $^\circ C$	1 V
50 $^\circ C$	1.18 V

These simulations concluded that the body effect changes the transistor´s temperature behaviour, and a stable current reference can be generated. The next step is to design the complete current reference circuit where Vbody should be generated in order to obtain the values of Table 5.3.

The designed circuit is presented in Figure 5.8. The method of [28] was followed for the the Vbody generation. In this circuit the Vbody is generated with transistors MP1, MP2, MPZ1 and MPZ2 that are connected as active charges.

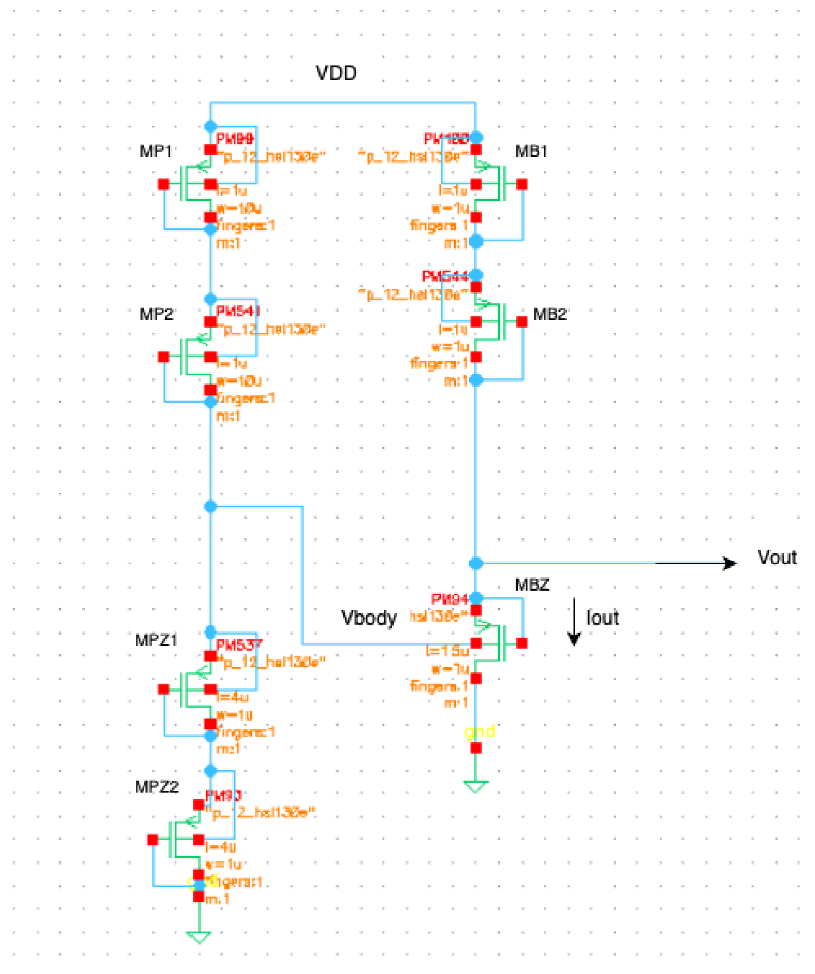

Figure 5.8: Reference circuit.

The circuit was simulated with the dimensions in Table 5.4.

Table 5.4: Figure 5.8 dimensions

Transistor	W; L
MP1, MP2	W = 10 μm; L = 1 μm
MPZ1, MPZ2	W = 4 μm; L = 1 μm
MB1, MB2	W = 1 μm; L = 1 μm
MBZ	W = 1 μm; L = 1.5 μm

The generated Vbody is presented in Figure 5.9.

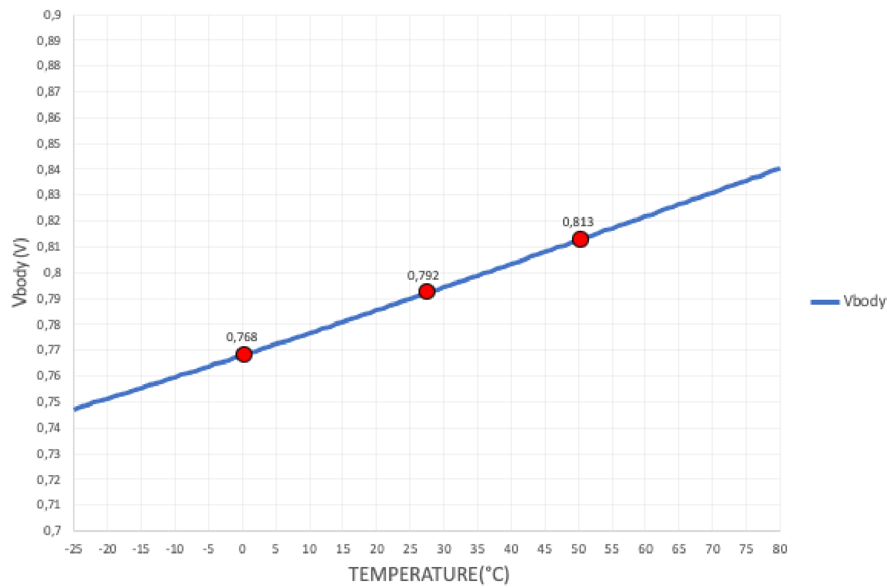

Figure 5.9: Body voltage (Vbody) generated.

The Vbody increases with temperature accordingly with the previous study, where an increasing voltage at the body of MBZ is used to compensate the current of the transistor. However, the voltage values are not the ideal ones previously calculated. In 0 $^\circ C$ the voltage is around 770 mV as desired but in the following temperatures, 27 $^\circ C$ and 50 $^\circ C$ the voltage cannot achieve the values necessary to properly affect the body. So it is expected that the current will not be stable.

The output current (Iout) was simulated in Figure 5.10.

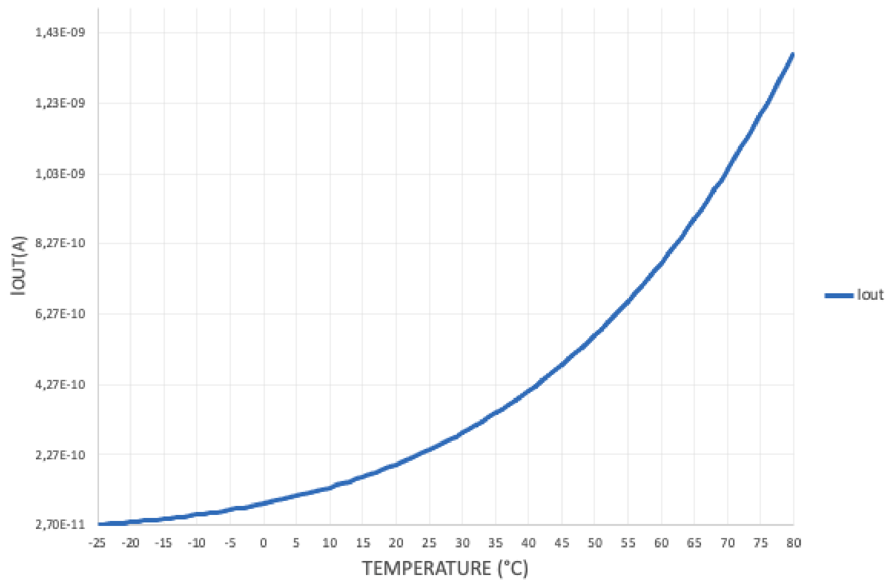

Figure 5.10: Output current (Iout) generated.

The output current has an almost exponential growth with temperature, and so the Vbody generated cannot affect this current properly to make it a reference. The circuit was simulated with different dimensions and number of transistors and the current behaviour compensation was impossible to achieve.

With the current not behaving as expected the output voltage was simulated and represented in Figure 5.11.

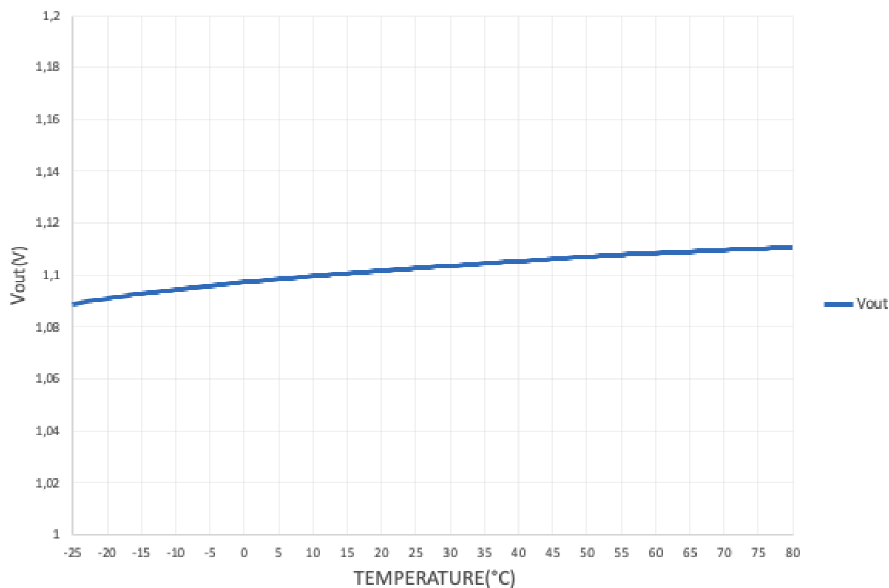

Figure 5.11: Output voltage (Vout) generated.

The output voltage (Vout) approximately behaves as a voltage reference, at around 1.12 V. As the circuit is able to generate an approximate voltage reference it was decided to develop the circuit using this reference instead of the current reference initially thought.

At this point there are two options: the first one is to obtain a circuit that with this voltage reference directly generates the desired PTAT signal and the second one to design a circuit that generates two CTAT signals whose subtraction gives the desired PTAT signal. As the ADC that will be used has differential inputs the second approach will be chosen.

The two CTAT signals VSG1 and VSG2 were generated using the circuit presented in Figure 5.12.

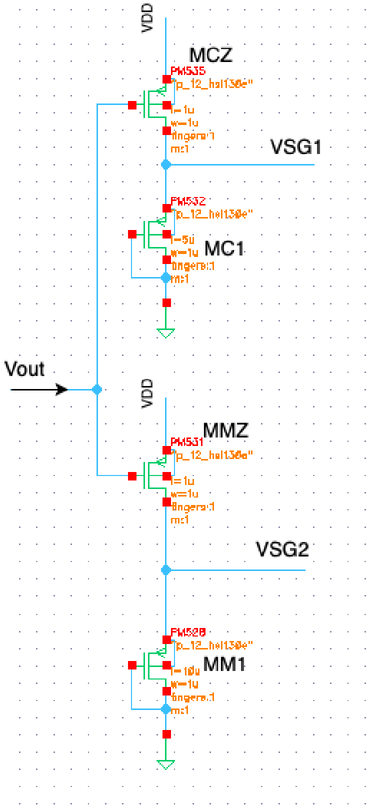

Figure 5.12: CTAT generation circuit.

Using the dimensions presented in Table 5.6.

Table 5.5: Figure 5.12 dimensions

Transistor	W; L
MCZ	W = 1 μm; L = 1 μm
MC1	W = 1 μm; L = 5 μm
MMZ	W = 1 μm; L = 1 μm
MM1	W = 1 μm; L = 10 μm

the generated VSG1 and VSG2 are presented in Figure 5.13.

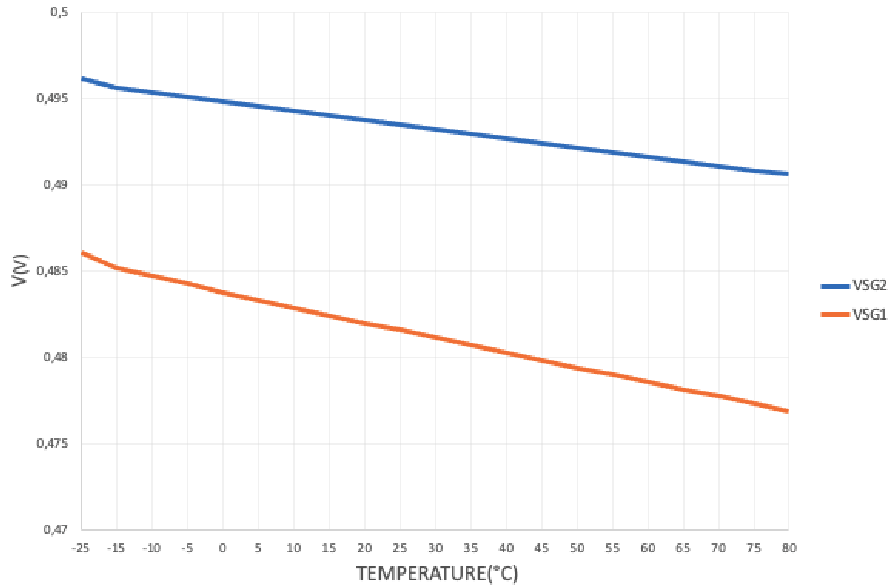

Figure 5.13: VSG1 and VSG2 generated.

Both signals are CTAT with different slopes, the VPTAT signal will be given as:

$$\mathrm{VPTAT(V)} = \mathrm{VSG2(V)} - \mathrm{VSG1(V)} \tag{5.1}$$

And is presented in Figure 5.14.

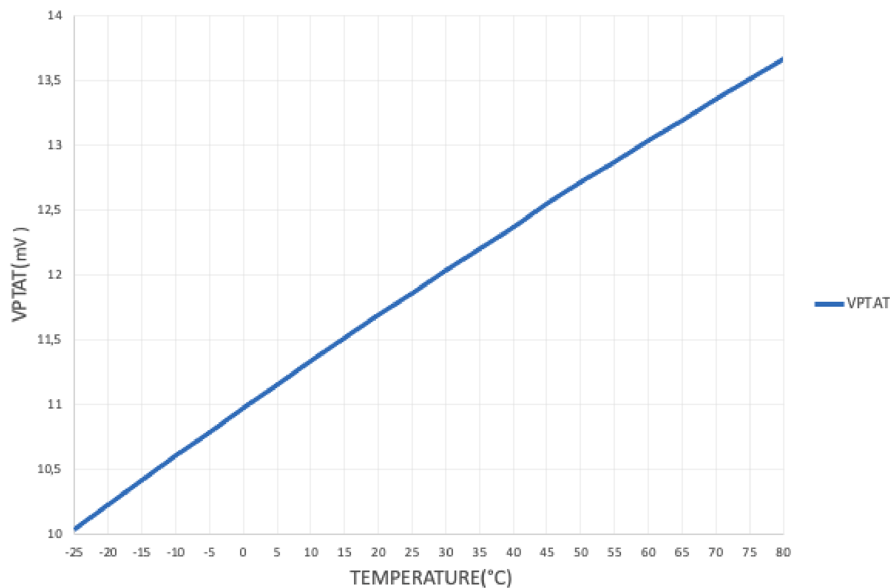

Figure 5.14: VPTAT signal obtained.

This circuit was designed to show the technique to obtain the PTAT output voltage using the subtraction of two CTAT voltages. The transistors used and dimensions are not proper set to obtain the desired ΔVPTAT full range, because in this case a ΔVPTAT of around 4 mV is only obtained.

The VLSB of the ADC that will be used is 2.56 mV and so for a range of -25 $^\circ C$ to 80 $^\circ C$ (ΔT = 105 $^\circ C$)

the required ΔVPTAT for 1 $^\circ C$ resolution should fulfill:

$$\frac{\Delta \mathrm{VPTAT}}{\Delta \mathrm{T}} > \mathrm{VLSB} \tag{5.2}$$

so the ΔVPTAT range should be higher than 259 mV.
To increase the ΔVPTAT the complete front-end composed of Vbody generation, Vout generation and VCTAT generation, and additional transistors, was globally optimized. The final front-end is presented in Figure 5.15.

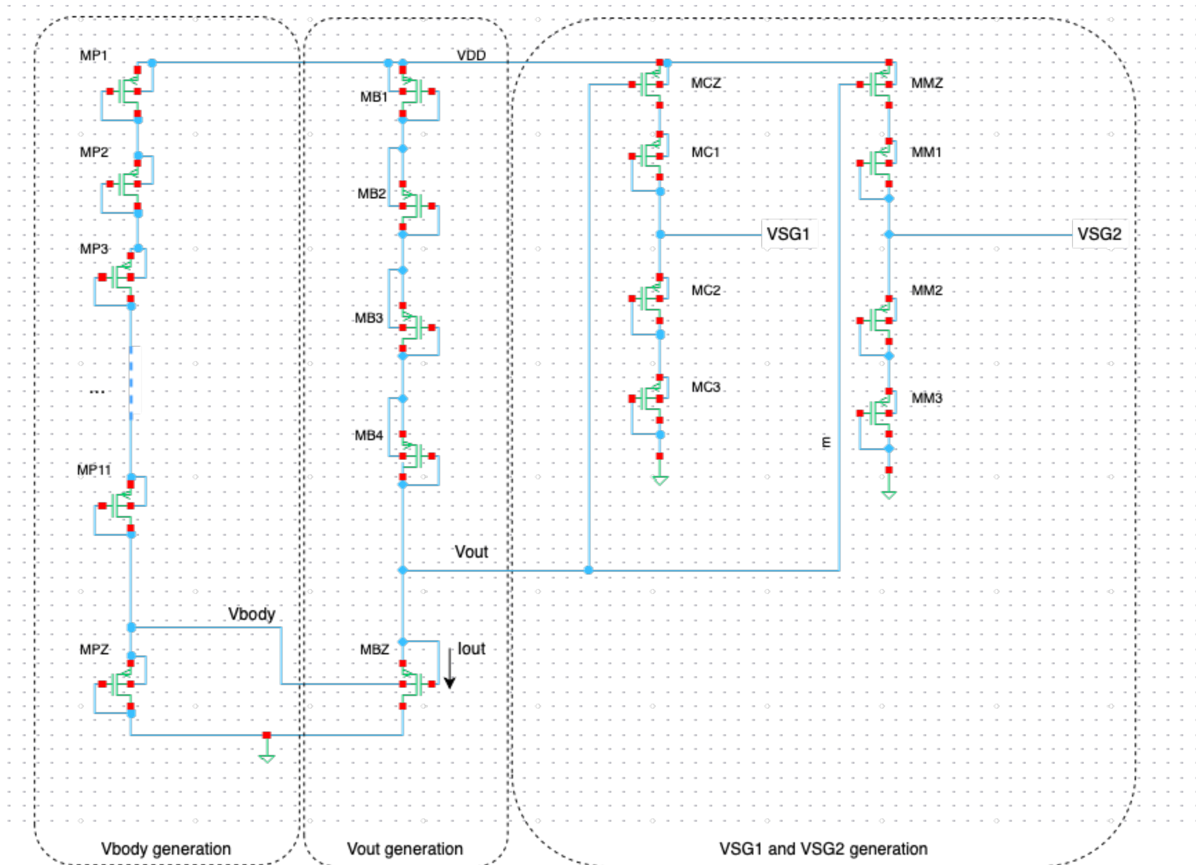

Figure 5.15: Front-end circuit.

Using the dimensions presented in Table 5.6.

Table 5.6: Figure 5.15 dimensions

Transistor	W; L
MP1, ..., MP11	W = 100 μm; L = 1 μm
MPZ	W = 1 μm; L = 50 μm
MB1, ..., MB4	W = 100 μm; L = 1 μm
MBZ	W = 56 μm; L = 1 μm
MCZ	W = 1 μm; L = 1 μm
MC1, ..., MC3	W = 54 μm; L = 1 μm
MMZ	W = 1 μm; L = 1 μm
MM1, ..., MM3	W = 1 μm; L = 50 μm

The final body voltage generated is presented in Figure 5.16.

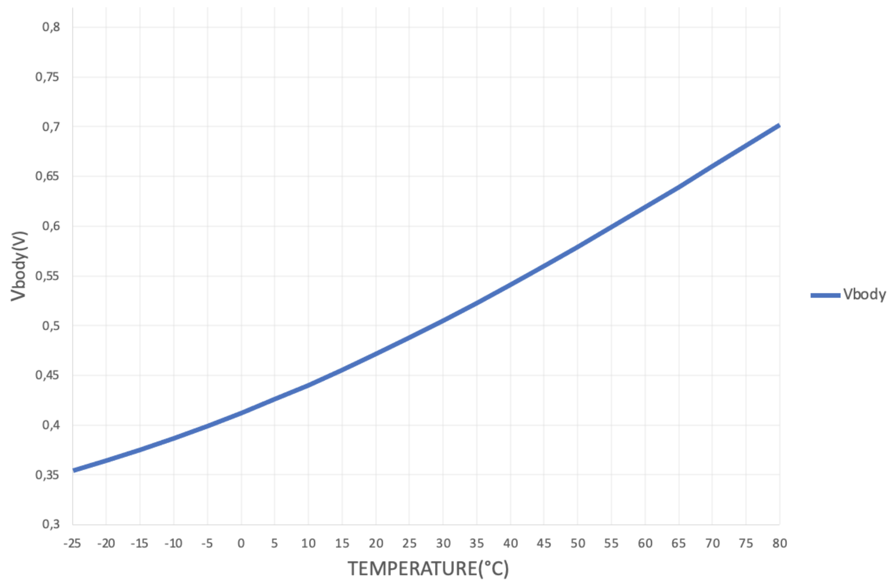

Figure 5.16: Body voltage (Vbody) generated.

The nominal Vbody increases from around 350 mV to 700 mV and will affect the body of the MBZ transistor. The optimization results obtained this voltage instead of the previously presented in Figure 5.9 that was in the range around 750 mV to 850 mV.
The MBZ transistor is connected as a current source and with the addition of the diode connected transistors MB1 through MB4 is responsible to generate the output voltage (Vout) presented in Figure 5.17.

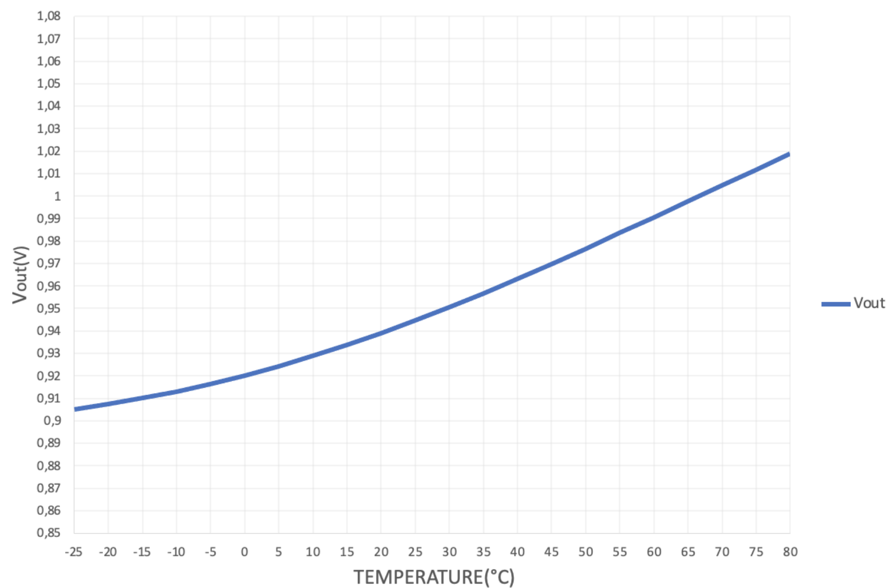

Figure 5.17: Output voltage (Vout) generated.

The Vout has a variation of 100 mV around 900 mV to 1 V, instead of the previously obtained in Figure 5.11 that was more close to a reference voltage.
The circuit was simulated taking into account dispersion parameters (corners simulation). For each signal it is presented its nominal value as well as the result with the SS (slow-slow) and FF (fast-fast) corner as only PMOS transistors were used.

Finally for the CTAT voltage generation the VSG1 and VSG2 signals are obtained and presented in Figure 5.18 and Figure 5.19.

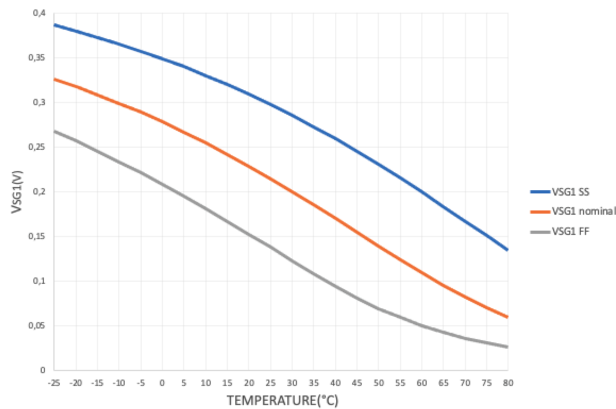

Figure 5.18: VSG1 generated.

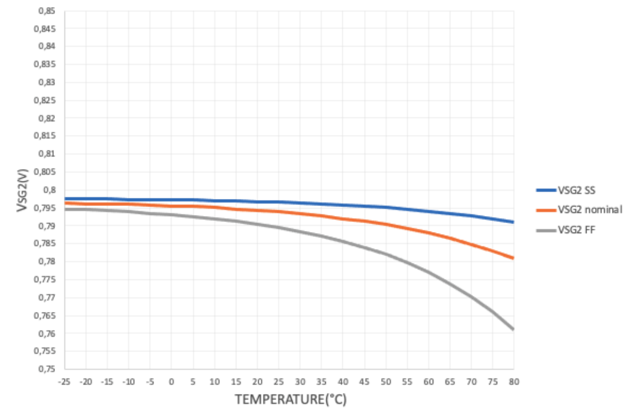

Figure 5.19: VSG2 generated.

The VSG1 signal is clearly a CTAT signal and suffers from process dispersion. However, the VSG2 signal is almost stable with a small decrease with temperature. These signals were obtained to generate the PTAT signal with a ΔVPTAT higher than 259 mV as previously mentioned. This result was obtained using the optimization functionality of the *Cadence Design Environment*. The optimization was tried with:

- an increasing Vbody from 500 mV to 900 mV
- a reference Vout around 800 mV
- the VSG1 and VSG2 CTAT voltages around 600 mV to 750 mV
- ΔVPTAT $>$ 259 mV

The simulator did not find any circuit that could match all of this requisites, so the final simulation was made only with ΔVPTAT $>$ 259 mV to meet the requirement needed to work with the ADC. The obtained VPTAT signal is presented in Figure 5.20.

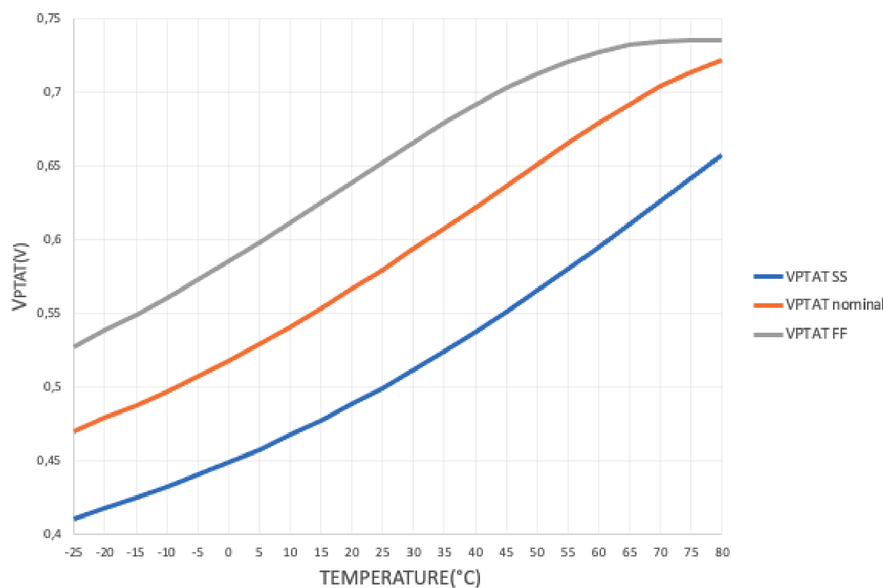

Figure 5.20: VPTAT obtained.

The obtained VPTAT has a ΔVPTAT of 265 mV and so it checks the requisite. The voltage increases

with temperature but is not linear in FF corner for higher temperature valies it also suffers from process dispersion. This was the best VPTAT voltage obtained. The way to improve this voltage and the process dispersion effect is through a 1-point calibration that can be digitally implemented.
To calculate the power consumption of the front-end circuit the current was simulated and is presented in 5.21

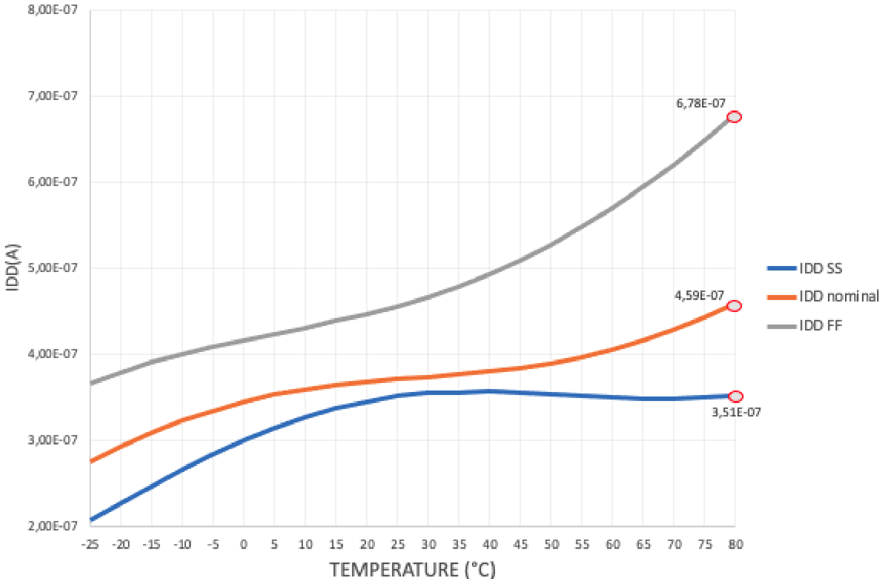

Figure 5.21: Front-end circuit current (IDD).

The nominal current value of the circuit is 459 nA, meaning a power consumption of 550 nW. The current suffers from process dispersion so considering the maximum value of 678 nA the circuit will consume around 813 nW.
In Figure 5.22 the VPTAT in function of VDD was obtained, the voltage increases with VDD.

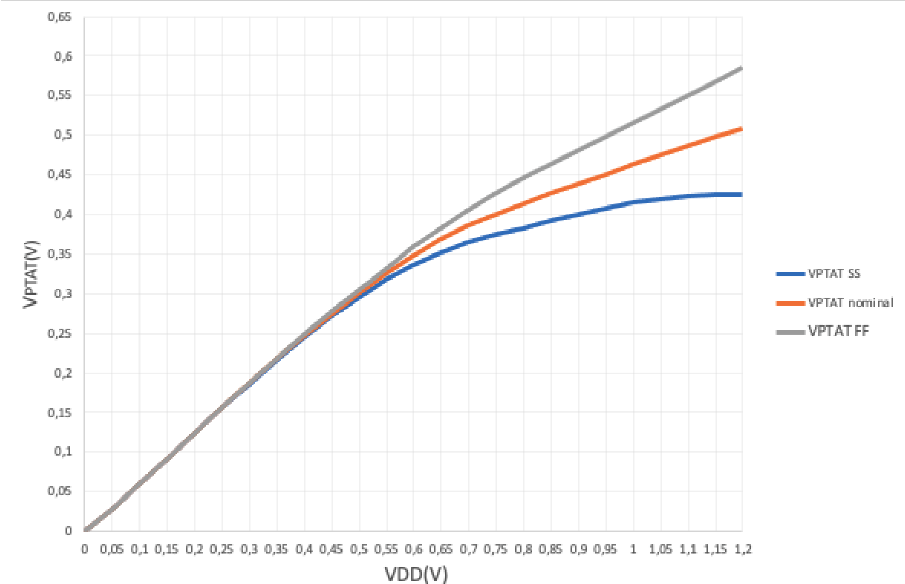

Figure 5.22: VPTAT(V) in function of VDD.

The VDD dependency comes mainly from the Vbody generation. This voltage was generated using

transistors connected as active charges meaning that there is a VDD dependency. Unfortunately, there was not enough time to eliminate this dependency but a possible solution would be to generate the Vbody using one transistor connected as a current source.

A Monte Carlo simulation was made to analyse the effects of mismatch and process dispersion in the circuit. The results of this simulation are presented in Figure 5.23 for the output voltage and in Figure 5.24 for the final VPTAT voltage.

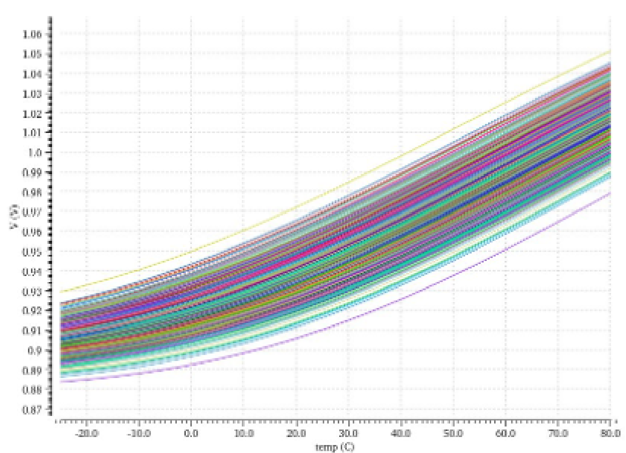

Figure 5.23: Output voltage Monte Carlo simulation.

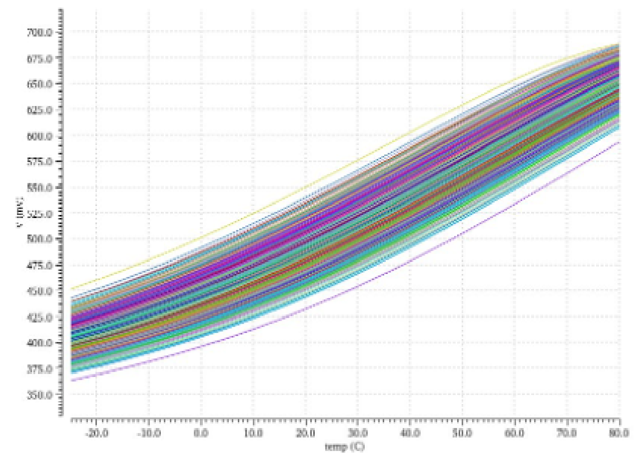

Figure 5.24: VPTAT Monte Carlo simulation.

The output voltage has a small variation but the most interesting result is obtained in the PTAT voltage. Unlike the corner analysis where the voltage suffered a lot from process variation, with the Monte Carlo simulation a better linearity is obtained in the VPTAT.

5.2 Sensor system and simulations

An analog-to-digital converter (ADC) is necessary to convert the measurements of the sensor to a digital temperature value. The most common type of ADC for low power consumption are the successive approximations ADC (SAR ADC) [3], [17], Sigma-Delta ADC ($\Sigma\Delta$ ADC) [7], [18] and incremental ADC (IADC) [5]. The choice of the ADC for the sensor should rely on the resolution instead of the conversion speed because the temperature values are not expected to change of a sudden.

For this sensor the SAR ADC in [17] was chosen because of its ultra low-power consumption and the efficiency of the conversion process. A common architecture for the SAR ADC (Figure 5.25) uses a comparator, capacitors, switches and a control logic block for the conversion [17].

A SAR ADC has three operating modes: sampling, hold and redistribution. A full conversion is made with a sequence of these operations. In the sampling mode, 5.26 the top plates of the capacitor are connected to ground and the bottom to the input voltage. In this configuration the capacitor top plates have a stored charge that is proportional to the input voltage V_{IN}, as shown in Figure 5.26.

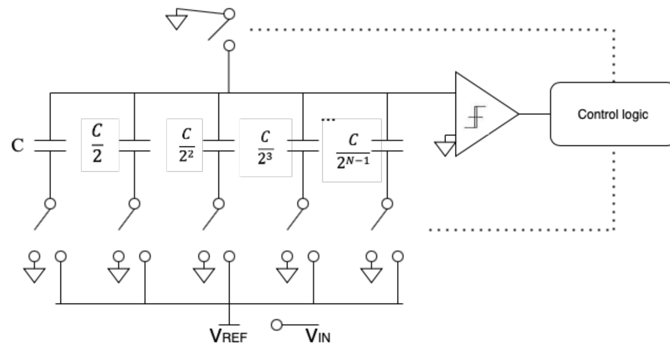

Figure 5.25: SAR ADC.

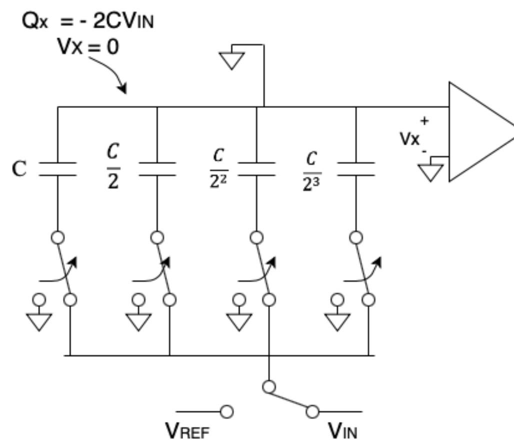

Figure 5.26: SAR ADC sampling mode.

The next step is the hold mode, in Figure 5.27, where the switch in the top plate is opened and the capacitor bottom plates are now connected to ground. Due to charge conservation the voltage in V_x is now $-V_{IN}$.

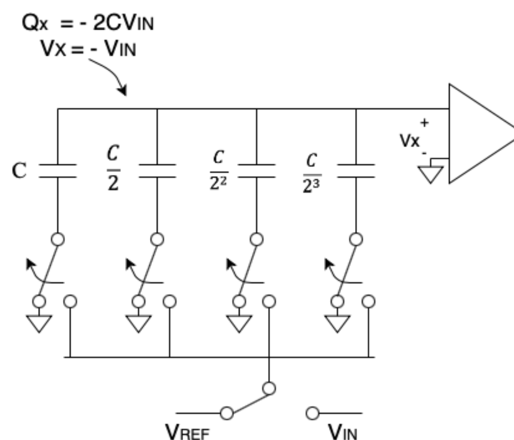

Figure 5.27: SAR ADC hold mode.

The final step is the redistribution mode where the conversion process starts. The largest capacitor C is used for finding the most significant bit (MSB) that is first converted. For this conversion the capacitor C bottom plate is connected to the V_{REF} voltage, and the remaining capacitors are still connected to ground. At this point the circuit is a simple voltage divider between two equal capacitors. In Figure 5.28

The V_x node now corresponds to the $-V_{IN}$ increased with half the reference voltage

$$\mathrm{V_x = -V_{IN} + \frac{V_{REF}}{2}} \tag{5.3}$$

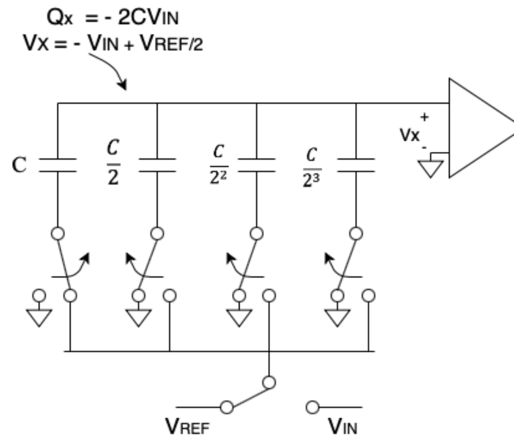

Figure 5.28: SAR ADC redistribution mode.

In each clock cycle a bit is determined, in the first period the most significant bit (b1), in the second period the second bit (b2) until all the converter N bits are determined [17]. For a N-bit conversion N clock cycles are needed to complete the conversion.

The logic for a conversion is for example to consider a random number between 1 to 64. Then a choice must be made if the number is greater or smaller than 32 (half scale). If it is greater, the next comparison is with 48, that is the mid range of [32,64]. If it is smaller, the next comparison is with 16, that is the mid range of [0,16]. By continuing these comparisons and dividing the scale by two the initial random number will be determined [17]. In terms of capacitors the comparison depends on the previously converted bit, for example, if the first bit is '0' in the next comparison it is only connected the capacitor C/2, if the bit is '1' it is connected the capacitor C and C/2 and so on.

The parameters of the SAR ADC are presented in Table 5.7.

Table 5.7: SAR ADC characteristics.

Supply Voltage (V)	1.2
Resolution	10 bit
ENOB	8.87$^{(*1)}$

(*1) - After layout extraction.

Having a supply voltage of 1.2V and 8.87 ENOB (Effective number of bits) the VLSB is calculated as:

$$\mathrm{VLSB = \frac{1.2}{2^{8.87}} = 0.00256V = 2.56mV} \tag{5.4}$$

The resolution of the ADC will affect the resolution of the sensor, a better resolution of the ADC would mean a better accuracy in the temperature reading.

The test-bench of the the ADC is presented in Figure 5.29.

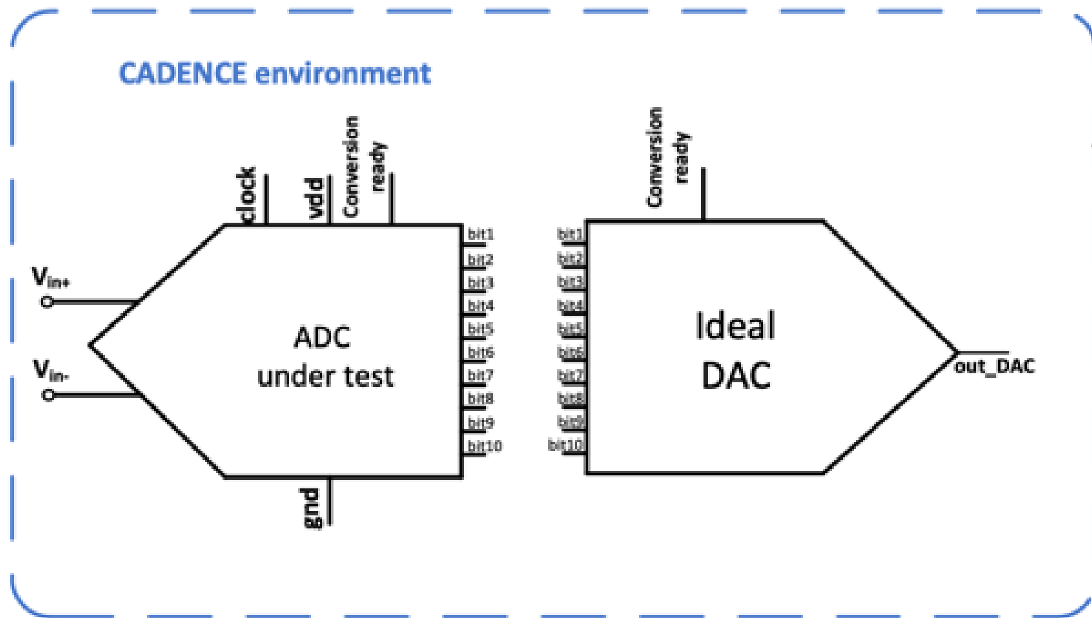

Figure 5.29: SAR ADC test bench [17].

The ideal DAC was developed in Verilog-A code to convert the 10-bit word from the ADC into an analogue voltage [17]. The input voltages V_{in+} and V_{in-} are the differential inputs of the ADC. The conversion ready signal indicates the ADC when to perform a conversion. And the out_Dac is the output analogue voltage.

In order to test the front-end circuit was added to this test bench as shown in Figure 5.30.

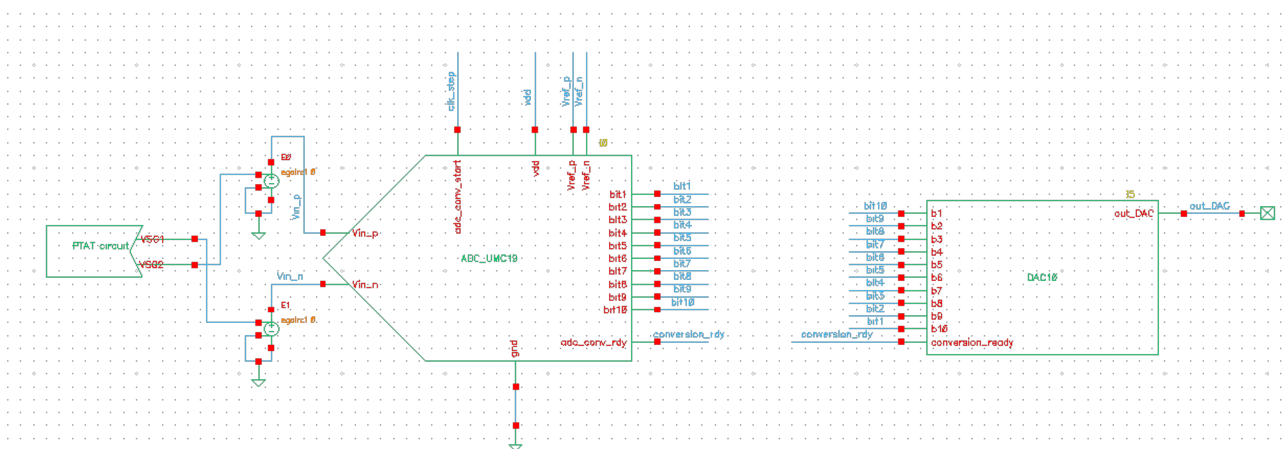

Figure 5.30: Temperature sensor test bench.

The VSG1 and VSG2 voltages are connected to the differential inputs of the ADC with the addition of two buffers due to the high input impedance of the ADC. If the ideal buffers were not added the capacitors of the ADC would take more time to charge leading to a higher current consumption. Performing a full simulation for the temperature range of the -20 $^{\circ}C$ to 80 $^{\circ}C$ in the conversion time of 517 μs it was obtained the results of Figure 5.31.

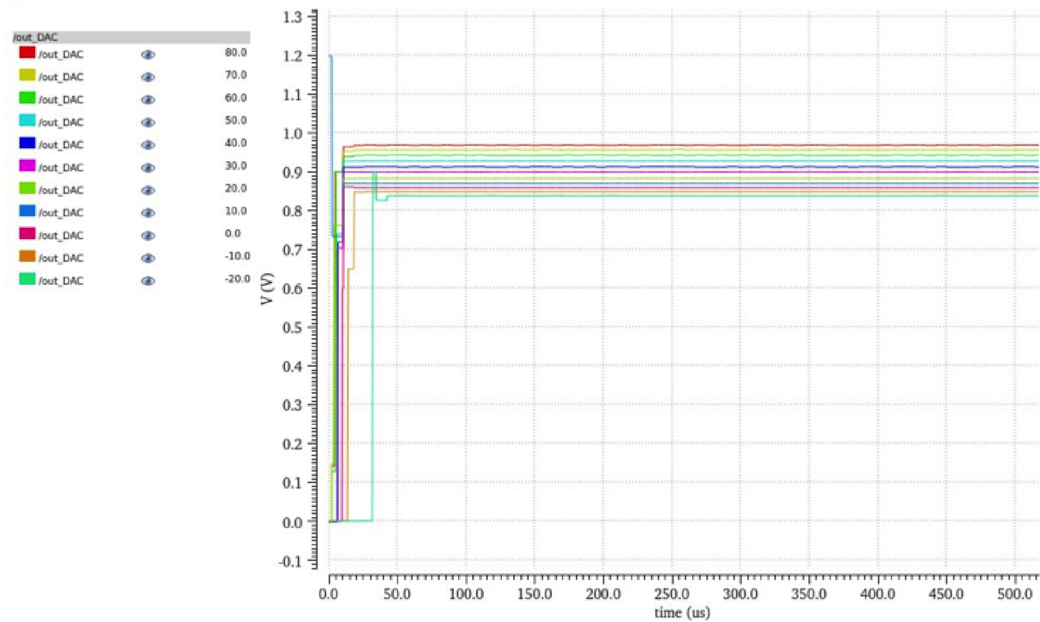

Figure 5.31: Output analogue voltage (out_DAC) with temperatures -20 $°C$ to 80 $°C$.

Until 50 μs the ADC seems to have a different behaviour but during operation the expected results are obtained. As the temperature increases the output voltage also increases as desired with the PTAT circuit. The results are in more detail in Figure 5.34.

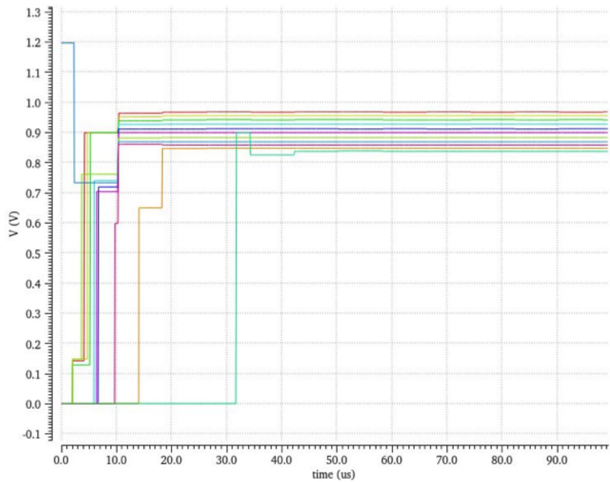

Figure 5.32: Analogue voltage (out_DAC) at initial time.

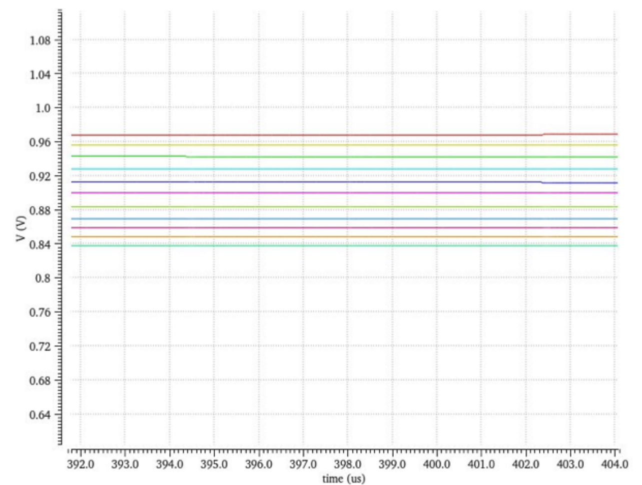

Figure 5.33: Analogue voltage (out_DAC) final time.

Figure 5.34: Detailed output analogue voltage (out_DAC) with temperatures -20 $°C$ to 80 $°C$.

In Table 5.8 the out_Dac and the correspondent binary words for each temperature are presented.

Table 5.8: Temperatures of -20 $^{\circ}C$ to 80 $^{\circ}C$.

Temperature ($^{\circ}C$)	out_DAC (mV)	Binary word	Binary word value	Increment
-20	837.891	1011001011	715	—
-10	848.438	1011010101	725	+10
0	858.984	1011011101	733	+8
10	869.531	1011100110	742	+9
20	883.592	1011110010	754	+12
30	900	1100000000	768	+14
40	912.891	1100001011	779	+11
50	928.125	1100011000	792	+13
60	942.188	1100100101	805	+13
70	956.250	1100110000	816	+11
80	969.141	1100111011	827	+11

Despite seeming that for the first instances of the conversion the ADC has a different behaviour for the negative and positive temperatures the results of the Table 5.8 show that the results are similar. For temperature intervals of 10 $^{\circ}C$ the ADC is able to do the conversion as observed with the voltage increase. For the range of -20 $^{\circ}C$ to 80 $^{\circ}C$ the output voltage increases from around 837 mV to 969 mV. The binary word for the first temperature is 715 and for the final temperature is 827 and the increment is around $+12$ for each 10 $^{\circ}C$.

In the next simulation a temperature conversion was simulated for intervals of 1 $^{\circ}C$ in the negative range of temperatures from -20 $^{\circ}C$ to -10 $^{\circ}C$. The result is presented in Figure 5.35.

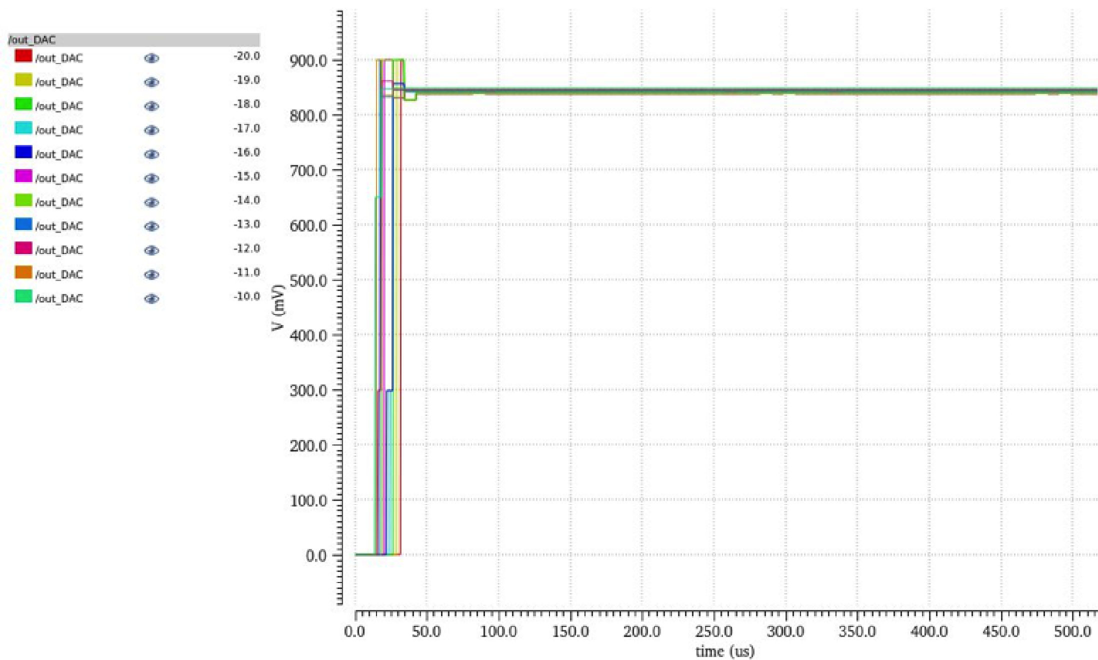

Figure 5.35: Output analogue voltage (out_DAC) with temperatures -20 $^{\circ}C$ to -10 $^{\circ}C$.

The ADC seems to do the conversion but a detailed view is presented in Figure 5.38.

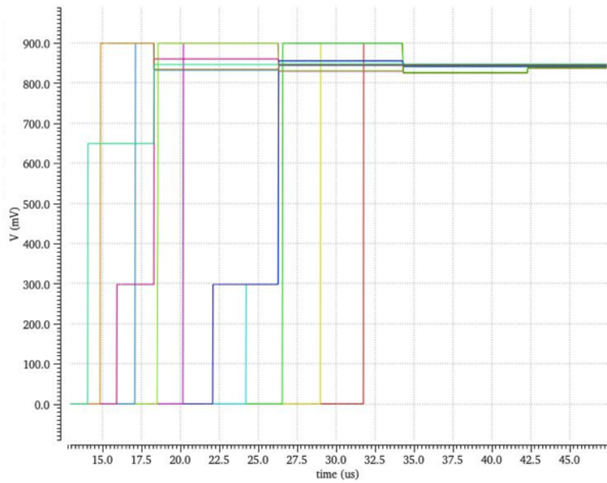

Figure 5.36: Analogue voltage (out_DAC) at initial time.

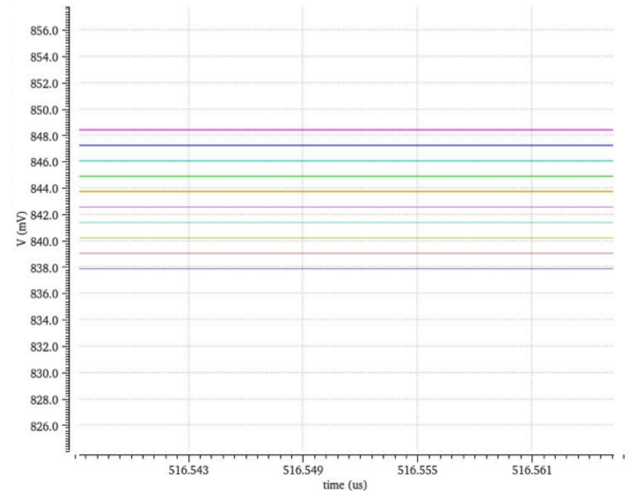

Figure 5.37: Analogue voltage (out_DAC) final time.

Figure 5.38: Detailed output analogue voltage (out_DAC) with temperatures -20 $^{\circ}C$ to -10 $^{\circ}C$.

In Table 5.9 the out_Dac and the correspondent binary words for each temperature are presented.

Table 5.9: Temperatures of -20 $^{\circ}C$ to -10 $^{\circ}C$.

Temperature ($^{\circ}C$)	out_DAC (mV)	Binary word	Binary word value	Increment
-20	837.891	1011001011	715	—
-19	839.063	1011001100	716	+1
-18	840.234	1011001101	717	+1
-17	841.406	1011001110	718	+1
-16	842.578	1011001111	719	+1
-15	843.750	1011010000	720	+1
-14	843.750	1011010000	720	+0
-13	844.921	1011010001	721	+1
-12	846.094	1011010010	722	+1
-11	847.265	1011010011	723	+1
-10	848.438	1011010101	725	+2

Through the Figure 5.38 it seems that for negative temperatures the ADC has a different behaviour in early stages. However, at around 40μs and during operation the ADC starts to work properly and the 1 $^{\circ}C$ conversion can be achieved. This results are confirmed in Table 5.9. The out_Dac goes from around 837 mV to 848 mV, an increase of 11 mV in 10 $^{\circ}C$. In each 1 $^{\circ}C$ there is a change of 1 bit in the binary word and in 10 $^{\circ}C$ the decimal value increases 10 times from 715 to 725, for each 1 $^{\circ}C$ the increment is almost always $+1$.

A new simulation was made for positive temperatures of 70 $^{\circ}C$ to 80 $^{\circ}C$. The result is presented in Figure 5.39.

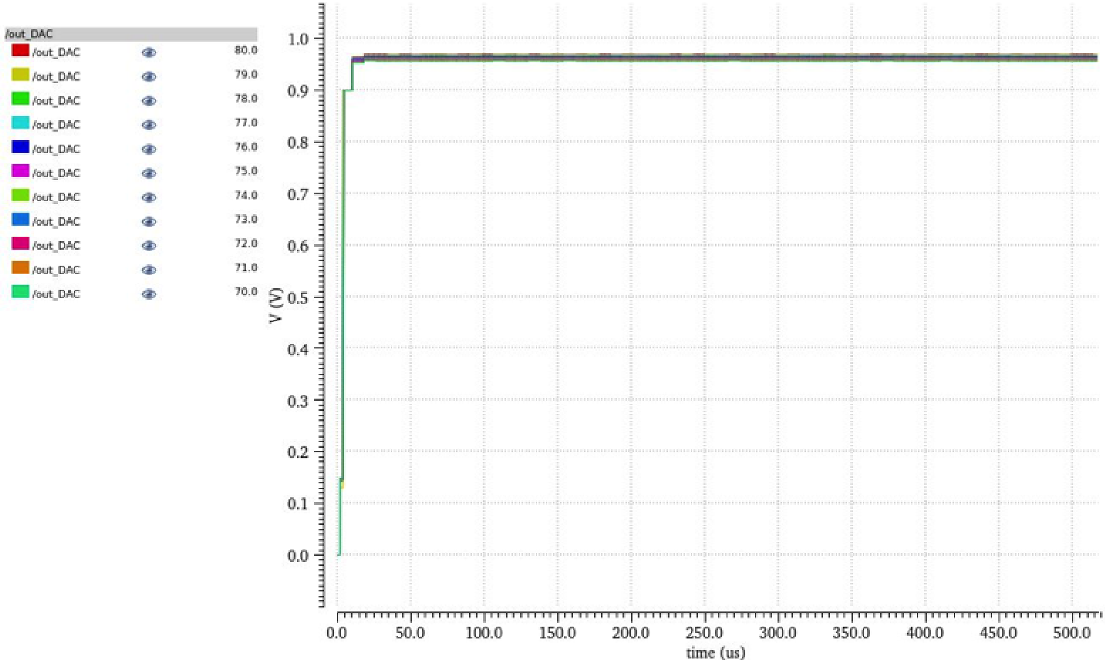

Figure 5.39: Output analogue voltage (out_DAC) with temperatures 70 $^{\circ}C$ to 80 $^{\circ}C$.

The detailed view is presented in Figure 5.42.

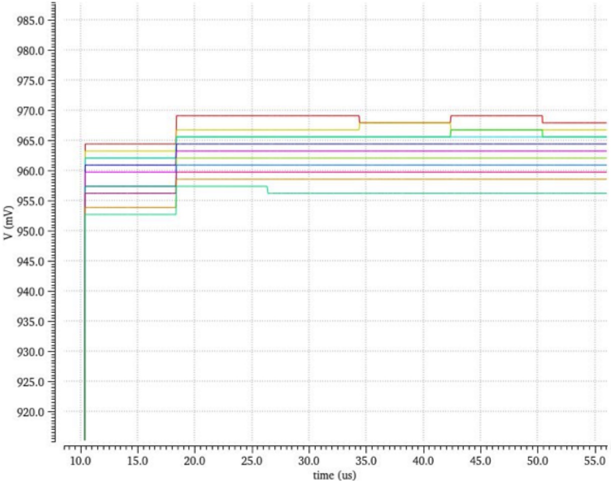

Figure 5.40: Analogue voltage (out_DAC) at initial time.

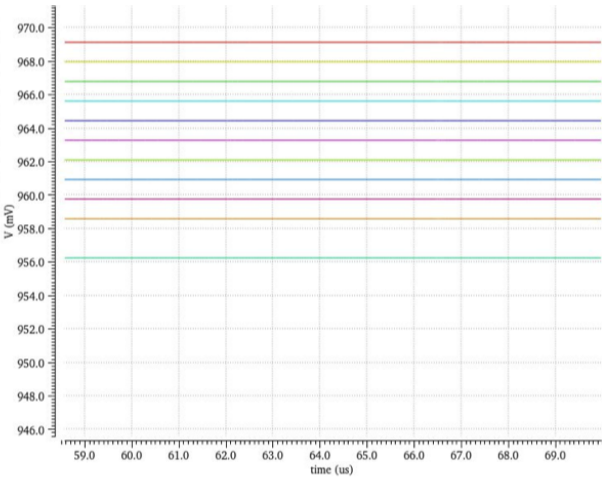

Figure 5.41: Analogue voltage (out_DAC) final time.

Figure 5.42: Detailed output analogue voltage (out_DAC) with temperatures 70 $^{\circ}C$ to 80 $^{\circ}C$.

In Table 5.10 the out_Dac and the correspondent binary words for each temperature are presented.

Table 5.10: Temperatures of 70 $^{\circ}C$ to 80 $^{\circ}C$.

Temperature ($^{\circ}C$)	out_DAC (mV)	Binary word	Binary word value	Increment
70	956.250	1100110000	816	—
71	958.594	1100110010	818	+2
72	959.766	1100110011	819	+1
73	960.938	1100110100	820	+1
74	962.109	1100110101	821	+1
75	963.281	1100110110	822	+1
76	964.453	1100110111	823	+1
77	965.625	1100111000	824	+1
78	965.625	1100111000	824	+0
79	966.797	1100111001	825	+1
80	969.141	1100111011	827	+2

It is clear that the ADC works properly for the positive temperatures. This results are confirmed in Table 5.10. It is observed that as the temperature increases the output voltage also increases so it is concluded that a 1 $^{\circ}C$ conversion is possible. For this range the voltage increases from around 956 mV to 969 mV, a 13 mV increment. In each 1 $^{\circ}C$ there is a change of 1 bit, and an increment in the binary word of around $+1$ for each 1$^{\circ}C$.

Following this simulation is concluded that the front-end was correctly designed to work with the ADC and a 1$^{\circ}C$ temperature conversion resolution is achieved.

Chapter 6

Conclusion and Future work

The goal of this thesis work was to develop and design the front-end circuit of an ultra-low power temperature sensor. The sensor will be used in precision agriculture and in fire detection, as it measures ambient temperature on a range of -25 $°C$ to 80 $°C$. The sensor should have the best possible resolution, the goal was set for a 0.25 $°C$ resolution with nano ampere current consumption.

Temperature sensors that had similar characteristics were studied and compared. It was concluded that most circuits were developed with BJTs and only more recently with MOSFETs. This is explained due to the high linear temperature characteristics of the BJTs. MOSFETs are becoming an alternative because with 1 or 2-point calibration best results are obtained in terms of resolution. Resistor-based are not so commonly used because with the same calibration type the obtained results are not as good.

A better understanding of the temperature behaviour of the BJT, MOSFET and resistors was needed to study the best circuit choice. The BJT temperature dependencies were presented and it was concluded that for a constant I_C the V_{BE} voltage is temperature sensitive, and behaves as a CTAT voltage. The MOSFET regions were presented and the behavior in the subthreshold region was identified as the best in order to reduce power consumption. Finally, resistors were studied and it was concluded that a larger silicon area is needed to obtain the large resistance value required for nA currrents. The most common voltage and current reference circuits were also studied.

This study was complemented by simulating these components and circuits with UMC 130 nm CMOS technology, and finally decide the best option for the front-end circuit. A single BJT in the active region and bandgap circuits were tested to obtain the PTAT voltage needed. In the bandgap circuits, different transistor to current ratios were used to maximize the obtained PTAT. This transistors were powered by an constant current and an almost linear PTAT voltage was obtained. However, the best voltage to temperature linear behaviour was achieved with a current in the order of pA, too close to noise levels. The same circuits were made with MOSFET but powered by a larger nA current, the PTAT obtained was not as linear as the previously ones. After these tests and simulations it was decided to use PMOS transistors only with the possibility of a 1-point calibration in a later stage.

The design of the final front-end was based on the method presented in [28]. It was confirmed that the current has an exponential growth with temperature so it is not even close to a current reference but the output voltage obtained did not vary too much. The next step was trying to use the body effect to compensate the current variations. Despite simulating a lot of circuits and trying new options it was not

possible to generate the necessary Vbody to compensate the current. The solution was to generate a VDD - Vout reference with the Vbody compensation circuit. The Vbody generation for the compensation, with active charges allowed to obtain the desired output voltage, but as a disadvantage this voltage will be VDD dependent. A possible solution was to generate the Vbody with one of the transistors connected as a current source instead of all transistors connected as active charges. Finally, the VDD - Vout will be used to obtain the two CTAT voltages responsible for the generation of the final ΔVPTAT voltage. The desired ΔVPTAT was obtained with a global optimization of the circuit. However, the constraints for the optimization were not detailed enough and despite having the desired ΔVPTAT behaviour the voltage is not linear and suffers a lot from process dispersion. It was hard to obtain the desired linear PTAT without using optimization and so there was not enough time to improve it. A possible solution can be the addition of more constraints in the optimization, for example an additional derivative constraint for the final PTAT to obtain the best linearity.

The final front-end circuit works in the range of -25 $^{\circ}C$ to 80 $^{\circ}C$, has an ultra-low power consumption of 550 nW and a 1 $^{\circ}C$ resolution. The circuit is designed only with PMOS transistors bringing the additional advantage of only having three corner analysis (FF, nominal and SS). However, the expected results for this work were not fully achieved, the fire detection was not developed and 0.25 $^{\circ}C$ resolution was not obtained. The final PTAT obtained is not linear and varies a lot with VDD.

It is proposed as future work to complete the development of the circuit with the fire detection capability and the development of the circuit layout. The simulations made are not enough to validate the circuit for a real application, as the post layout extracted simulations are needed. In case of using the already exiting ADC the design of the buffers for the circuit integration is also needed. After the post layout simulations and validations the work can be concluded with the circuit fabrication.

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