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Design and assessment of an MMC-HVDC system

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I declare that this document is an original work of my own authorship and that it fulfills all the requirements of the Code of Conduct and Good Practices of the Universidade de Lisboa.

Acknowledgments

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Abstract

The main aim of this dissertation is to design controllers and assess the response of an High Voltage Direct Current (HVDC) system. The focus of this work is to design linear and nonlinear controllers for the AC currents and to compare the obtained results.

An HVDC system is constituted by two AC/DC power electronic conversion systems connected by a DC cable. In this work, each converter is connected to an AC grid, one being operated at 50 Hz and the other at 60 Hz. Modular multilevel converters (MMC) with 24 submodules (SM) in each leg of the converter (12 in the upper arm and 12 in the lower arm) were used for each terminal of the HVDC system. The voltage in the DC link is 200kV and the peak value in the AC side is 100kV.

For the linear control approach, it is used a Phase Shift Carrier Pulse Width Modulation (PSC-PWM) and Proportional-Integral (PI) controllers. For the nonlinear controllers, a sliding mode control approach is used. In both cases a balancing control algorithm for the capacitors voltages in the submodules is developed.

The system is simulated in *Matlab*/*Simulink* and the obtained results show that nonlinear current controllers present better results than the linear controllers. Both present good performance in the output voltage control of the converters. The DC voltage control and the DC capacitors voltage balancing is successfully guaranteed as well as the mitigation of voltage sag or overvoltage events in the grid.

Keywords

High Voltage Direct Current (HVDC), Modular Multilevel Converter (MMC), Phase Shifted Carrier Pulse Width Modulation (PSC-PWM), Nonlinear current control (NLCC).

Resumo

O objetivo desta dissertação é o dimensionamento e avaliação de um sistema de transporte de energia em Alta Tensão Corrente Continua (HVDC – High Voltage Direct Current). O foco do trabalho é dimensionar controladores lineares e não lineares para as correntes AC e comparar os resultados obtidos.

Um sistema HVDC é constituído por dois sistemas de conversão eletrónica de potência AC/DC, ligados por um cabo DC, de transporte de energia. Cada sistema de conversão está ligado a uma rede AC. São utilizados conversores multinível modulares (MMC) constituído por 24 submódulos (SM) em cada braço do conversor (12 na zona superior e 12 na zona inferior). A tensão no andar DC é de 200 kV e a tensão máxima no lado AC são 100kV.

Para o controlo linear, o processo de modulação utilizado foi o processo de modulação por largura de impulso com desfasamento entre as portadoras (PSC-PWM) e controlo Proporcional-Integral (PI). No controlo não linear foi utlizada a estratégia de controlo por modo de deslizamento. Em ambos os casos foi executada uma estratégia de equilíbrio dos condensadores dos submódulos.

O sistema foi testado e os resultados mostraram que o controlador não linear da corrente apresenta melhores resultados nas formas de onda da corrente que o controlo linear e que ambos apresentam bons resultados na forma de onda da tensão à saída do conversor. O equilíbrio da tensão dos condensadores foi executado com sucesso bem como o controlo de cavas e sobretensões e o controlo no lado DC.

Palavras-chave

Alta Tensão Corrente Continua (HVDC), conversor multinível modular (MMC), modulação por largura de impulso com desfasamento entre as portadoras (PSC-PWM), controlo de corrente não linear.

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List of Acronyms

AAMMC	Alternate Arm Modular Multilevel Converter
AC	Alternating Current
CD	Clamp Double
CSC	Current Source Converter
DC	Direct Current
EU	European Union
FB-MMC	Full Bridge-Modular Multilevel Converter
HB-MMC	Half Bridge-Modular Multilevel Converter
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
LCC	Line Commutated Converter
LS-PWM	Level Shifted- Pulse Width Modulation
MMC	Modular Multilevel Converter
MTDC	Multiterminal Direct Current
NLCC	Nonlinear Current Control
NPC	Neutral Point Clamped
PI	Proportional-Integral
PSC-PWM	Phase Shifted Carrier-Pulse Width Modulation
PWM	Pulse Width Modulation
RMS	Root Mean Square
SM	Submodule
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	Static Synchronous Compensator
THD	Total Harmonic Distortion
UFB	Unipolar Voltage Full Bridge
VSC	Voltage Source Converter
3LCC/5LCC	3/5 Level Cross Connected

List of Symbols

[C]	Concordia Matrix
$C(s)$	Linear controllers
C	Capacitor in each submodule
C_{dc}	Capacitor in the DC side
[D]	Park transformation Matrix
e	error
f_{PWM}	Semiconductors switching frequency
G	Gain of the converter transfer function
G_{i}	Gain of the current controller transfer function
$H(s)$	Transfer function of the linear controller
H_{id}, H_{iq}	Output of the PI controllers for linear control
$i_{up\_a,b,c}$	Upper arm currents in the three phases
$i_{low\_a,b,c}$	Lower arm currents in the three phases
I_{DC}	Current in the DC side
i_{abc}	Three phase currents
$i_{circ\_a,b,c}$	Three phase circulating currents
i_{SM}	Submodule current
i_{ACmax}	Peak value of the semiconductor currents
i_c	Current in the capacitor
Δi	Current ripple in the coil
i_{dq}	Current in dq coordinates
i_{dqref}	Reference currents in dq coordinates
K_P	Proportional gain for the linear current controllers
K_I	Integral gain for the linear current controllers
K_{pv}	Proportional gain for the DC voltage controller
K_{iv}	Integral gain for the DC voltage controller
K_{AC}	Gain of the transfer function that relates V_{PCC} and i_{qref}
K_{pvAC}	Proportional gain for grid side voltage controllers
K_{ivAC}	Integral gain for grid side voltage controllers
l	Voltage level in the arm
L	Coil connected in each phase
L_{cable}	Inductance of DC cable
L_s	Series inductance connected to the grid
N	Number of modules in each arm
N_{up}	Number of SM in ON state in the upper arm
N_{low}	Number of SM in ON state in the lower arm
N_{red}	Number of redundancies in each level

P	Active power
P_d	Active power in d coordinates
$p_3(s)$	3rd order ITAE polynomial
Q	Reactive Power
R	Resistance in each phase
R_{on}	Conductor resistance
R_{grid}	Resistance connected to the grid
T_c	Switching period
T_d	Delay of the converter transfer function
T_p	Pole of linear control
T_z	Zero of the linear control
T_{dv}	Delay in the response of the current controller
T_{dvAC}	Delay in the response of the grid side voltage controller
S_{lowa}	State of the SM in the upper arm
S_{lowk}	State of the SM in the lower arm
V_{DC}	DC Voltage
$v_{upa,b,c}$	Voltage in the upper arms
$v_{lowa,b,c}$	Voltage in the lower arms
v_{abc}	Three phase voltages
v_{o_abc}	MMC three phase AC voltages
v_{SM}	Submodule voltage
v_c	Capacitor voltage in the submodule
$v_{\alpha\beta}$	MMC voltages in αβ coordinates
v_{dq}	MMC voltages in dq coordinates
$v_{o\,dq}$	Grid voltages in dq coordinates
V_{DCref}	Reference DC Voltage
V_{PCCd}	Voltage in the point of common coupling, in dq coordinates
$V_{PCCdref}$	Reference voltage in the point of common coupling, in dq coordinates
α_i	Current sensor
α_v	Voltage sensor
φ	Phase difference of the carrier waves

1. Introduction

One of the greatest challenges of the 21st century is to prevent climate change and its devastating effects. This awareness made governments to act and start creating incentives to promote the production of electricity through renewable energies.

In the last few years the grid integration of renewable energies as wind, solar, or hydro has been steadily growing. However, these sources of energy bring challenges to fulfil the demands of the consumers.

One of the characteristics of these renewable energy sources is their intermittence as they may not be available all the time and the generated power is highly dependent on the renewable energy resource (the wind or the sun). This problem results in the requirement for additional energy storage capabilities, either as hydro pump, when possible, or using large capacity flywheel energy systems or battery-based energy storage systems. These technologies have significantly evolved in the last few years but there is still a long way to go.

Additionally, they suffer from geographical limitations. The best areas for the optimal production of energy using the sun, wind or hydro resources may be located far away from the grid or from the most populated areas. The most promising renewable energy production in the next years may be the offshore wind power. Although the overall installation cost of these offshore wind farms is very high and they are located far away from the coastline, they can collect more energy than the onshore wind farms because they are bigger and the speed of the wind is higher and more constant, resulting in the generation of more energy.

High Voltage Direct Current (HVDC) transmission systems can be a good solution for this latter problem. In comparison with typical alternate current (AC) transmission systems, HVDC can transport more power over longer distances because only two cables are required, thus reducing the losses and the cost. However, the biggest advantage is the absence of reactive power absorption in the lines, and the minimization of losses in the cable capacitances.

Additionally, HVDC systems are a key technology to enable the stabilization and interconnection of AC networks, allowing increased energy trading, as a result of HVDC systems being highly stable and controllable [ABB, 2014], [Siemens, 2016].

The European Union (EU) wants to improve the interconnection between the countries to upgrade the security of electricity supply, to integrate more renewable energy sources and to have a more integrated energy market. Reliable connection with the EU countries reduces the risk of blackouts and reduces the need to build more power plants [EU, 2017], allowing the decommissioning of nuclear power plants.

The European council, in October of 2014 established a goal for all EU countries to have at least interconnection of 10% of their installed electricity production capacity in 2020 [EU, 2017]. As an example, Portugal has interconnection levels above 60%, while in Spain they are below 30%.

HVDC systems helped and will help to reach more ambitious goals in the integration of renewable energies. One of the most recent examples is the Baixas-Santa Llogaia interconnection HVDC transmission system between France and Spain and has started its operation in 2015. This interconnection doubled the interconnection capacity between the two countries [Siemens AG, 2016].

1.1. Objectives

The main aim of this thesis dissertation is to design and assess an MMC-HVDC system, focusing on the controllers design. The system rated DC voltage is 200 kV, being the AC side voltage equal to 100 kV. The grid frequency will be 50 Hz in one terminal and 60 Hz at the other terminal.

To accomplish these goals, this work will include:

- The presentation of the MMC-HVDC. Although the real systems are constituted by more than 200 submodules (SM) per arm, in this work, to allow the use of detailed models and avoid computational burden, the simulations will be carried out with only 12 SM.
- The design of linear and non-linear current controllers;
- The development of an algorithm to guarantee the DC capacitors voltages balancing;
- The design of a control system to guarantee the best system performance under voltage sag or overvoltage in the grid;
- The development of a simulation model in *Matlab/ Simulink,* to test the MMC-HVDC system under different operation conditions.

1.2. Outline

This dissertation is divided in six chapters and is organized as follows:

The chapter 1 is the introduction and describes the motivations and the relevance of the system to be studied. The objectives and outline are described.

The chapter 2 gives the overview and the theory of HVDC and a brief explanation of the possible solutions of these systems and technologies.

Chapter 3 describes the system which was used and the reasons of choice. The design of the system is performed.

In chapter 4 the controllers and the balancing DC voltages algorithms will be designed;

In chapter 5 the simulation results are presented and discussed.

Chapter 6 presents the conclusion and final remarks are made.

2. State of the art

HVDC have been a solid alternative for the more common AC transmission system. These systems provide advantages as being reliable and the cost over distance being reduced. However, they have higher maintenance and require more controllability and it is more difficult to have multiterminal systems as in the AC case [ABB, 2012].

HVDC systems may be the only way to connect two AC asynchronous networks as well functioning as a “firewall” of AC grids against cascading blackout as it was seen in the August 2003 northeast blackout. It is most appropriate for bulky power systems and mainly used when there is need of submarine cable (in offshore wind farms, for example). They can also increase the grid capacity in cases where they are less costly than introducing additional wires [ABB, 2012]. They can also connect two AC grids with different frequencies and will be a key technology in the future renewable transnational grid interconnection [ABB, 2012].

Since they can ease the problems of intermittence of renewable energies there are studies proving that Europe can be 100% renewable with the introduction of an HVDC grid [Czisch, 2009].

The EU commission proposed 300 million euros to subsidize HVDC grids and to the development between Ireland, UK, the Netherlands, Germany, Denmark, and Sweden in the North Sea with the construction of offshore wind and interconnection capability, in a 1.2 billion euros plan. These plans are not confined to connections between EU countries. The Union of Mediterranean wants to export to Europe energy through solar farms and a way to do it is using HVDC.

This “SuperGrid” has been seen with good eyes by the governments as it can surpass boundaries, reduces generation variability, connects wind farm and increases interconnection capabilities, helps the European energy market and reduces the costs for all of the countries involved [Gonzalez, et al, 2012].

An HVDC transmission system is constituted by a converter known as a rectifier which converts AC to DC, a cable that transmits in DC to another converter called an inverter that converts DC to AC. Figure 2.1 shows a simplified representation of an HVDC system.

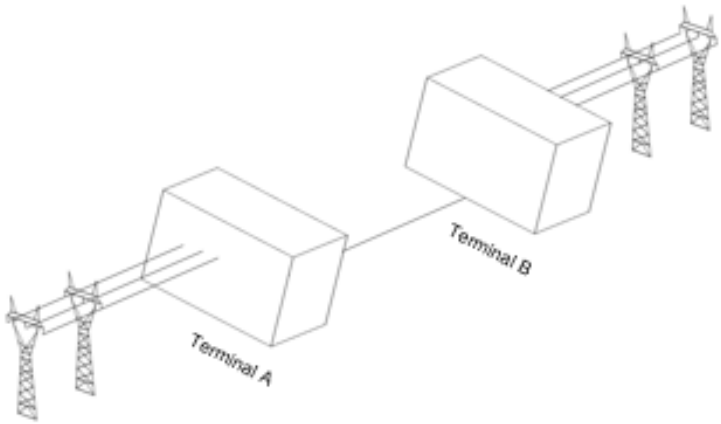

Figure 2.1: Scheme of an HVDC system with the two boxes representing the terminals of the HVDC system.

This DC transmission can be through undersea/underground or through an overhead line. The first have conductors surrounded by a thin level of the dielectric which results in having a high electrical capacitance. As it is a DC cable, the capacitance of the cable is charged only when the cable is first activated or the voltage levels change.

Overhead lines have not such a high electrical capacitance. Still, HVDCs may be more advantageous as in DC there is no skin effect (the skin effect results in the reduction of the useful current because it causes a nonuniform distribution of current over the cross section of the conductor).

2.1. History of HVDC technologies

Throughout the years there has been evolution in the topologies and technologies for DC power transmission. In the 19th century a swiss engineer called René Thury believed that power transmission using DC was a better option because only two cables were used instead of three. He created an electromechanical system composed by series of DC generators to increase the voltage and supply with a fixed current directly to the load [Deepak Tiku, 2014]. One of the most important examples was the Moutiers-Lyon system (150 kV, 20MW) operating between 1906 and 1937 [Black, 1983].

However, these systems were not adequate for higher power ratings. In the beginning of the 1920 mercury arc valve were the devices which enabled the conversion of AC to DC and DC to AC and had been invented in 1901 by Peter Cooper Hewitt. However, it was Dr. Uno Lamm who introduced it in HVDC systems in 1939 introducing grading electrodes, thus improving voltage balance and capability [Willys Long, 2019]. The valve would conduct if a pulse was provided in the positive polarity of the AC waveform. If the current was zero when the AC waveform reversed its polarity, then it wouldn't conduct. In these valves the area to support the blocking voltage was very thin which made these devices highly sensitive [Cory, et al, 1965].

One of the most important DC transmission systems was the connection between Sweden and the island of Gotland (96 km), considered to be the first modern HVDC link in 1954 [Willys Long, 2019]. The converters were constituted by two six-pulse valve groups (50kV 200A 10MW).

Until the 1970's this was the trending technology for HVDC. There were two types of valves: one developed by the Swedish that used many grading electrodes (mostly around 20) and the other designed by the Russians which used only four.

The difference is that the lower the grading electrodes, the higher is the current rating but it has a lower voltage blocking capability. The Russians used single anode mercury-arc valve while the Swedish used a multi anode with all anodes linked to the common cathode. The cooling was also different as the Swedish used water and Russian had chosen oil [Deepak Tiku, 2014].

Even though it was a great upgrade, the HVDC transmission cost is still high and it was only preferable when AC systems had natural connection barriers as the sea, or when long distance transmission was required. Also, these systems required high maintenance, had deterioration issues, a low flexibility in voltage ratings and environmental issues [Willys Long, 2019].

With the advances in power electronics these systems were overrun by semiconductors. In comparison with mercury valves, semiconductors have a higher switching capacity and can conduct higher currents.

The first semiconductor devices used in HVDC were the thyristors which need external commutation circuits. However, nowadays, the most common are the insulated-gate bipolar transistors (IGBT) due to their capability to block several kV, having the capability to be turned ON and OFF, still with relatively low conduction and switching losses.

2.2. Configuration of the converter

Interconnection of HVDC can be made in five ways depending on what the purpose of the interconnection is [Okba, et al, 2012], [Oni, 2016], [Bahrman, 2008]. In figure 1.2 the scheme for all configurations is presented.

The monopole configuration as the one represented in figure 2.2, (1) to (3), consists in a single DC line separating both converters, with the ground used for the path of current return. One of the terminals is connected to earth ground and the other connected to the transmission line. The ground can be connected to the other converter through an additional conductor. This configuration is in submarine environment.

Even though the monopole configuration has the advantage of being a cheaper configuration, it can cause problems such as corrosion of the cables. In the sea, unbalanced currents can create a magnetic field that can affect the ships that pass through. A simple way to resolve this issue would be the integration of a metallic return conductor as the one in figure 2.2 (2).

The back-to-back configuration (figure 2.2 (4)) has the rectifier and inverter in the same location as well as a small DC line. This configuration is mainly used for power transmission between neighbour AC grids that cannot be synchronized.

The bipolar connection, represented in figure 2.2 (5), is very similar to the homopolar but the polarities are different. Each pole is independent, and it can use a single pole with ground. It is the most popular configuration since it can split in two poles if there is need for higher energy availability and it has a lower cost than two monopoles.

In bipolar configuration there are three ways to design it: bipolar with ground return path, bipolar with dedicated metallic return path for monopolar operation, and bipolar without dedicated return path for monopolar operation.

The first is more common due to a higher flexibility concerning operation and reduced capacity during contingences. If there is a fault in a pole, that eventuality will be isolated because the current of the good pole will go to the ground return path.

The second one serves as an alternative to electrodes or if the distance is small. It can work as a monopole operation if there is loss of power resulting in bypass of switches.

The homopolar connection (figure 2.2 (9)) uses the ground as well as a current return path. It has two or more DC line connecting the converters all with the same polarity

Last but not least it is the multiterminal configuration. As the names indicates there are more than two converters connected by a power line. This configuration is not very common due to its complexity but with the consistent reduction in the price of semiconductors and the improvement in the performance capabilities of microprocessing systems these systems are more likely to appear. Nowadays, the biggest multiterminal project on operation is the 2000MW Quebec- New England transmission system and has started to operate in 1992.

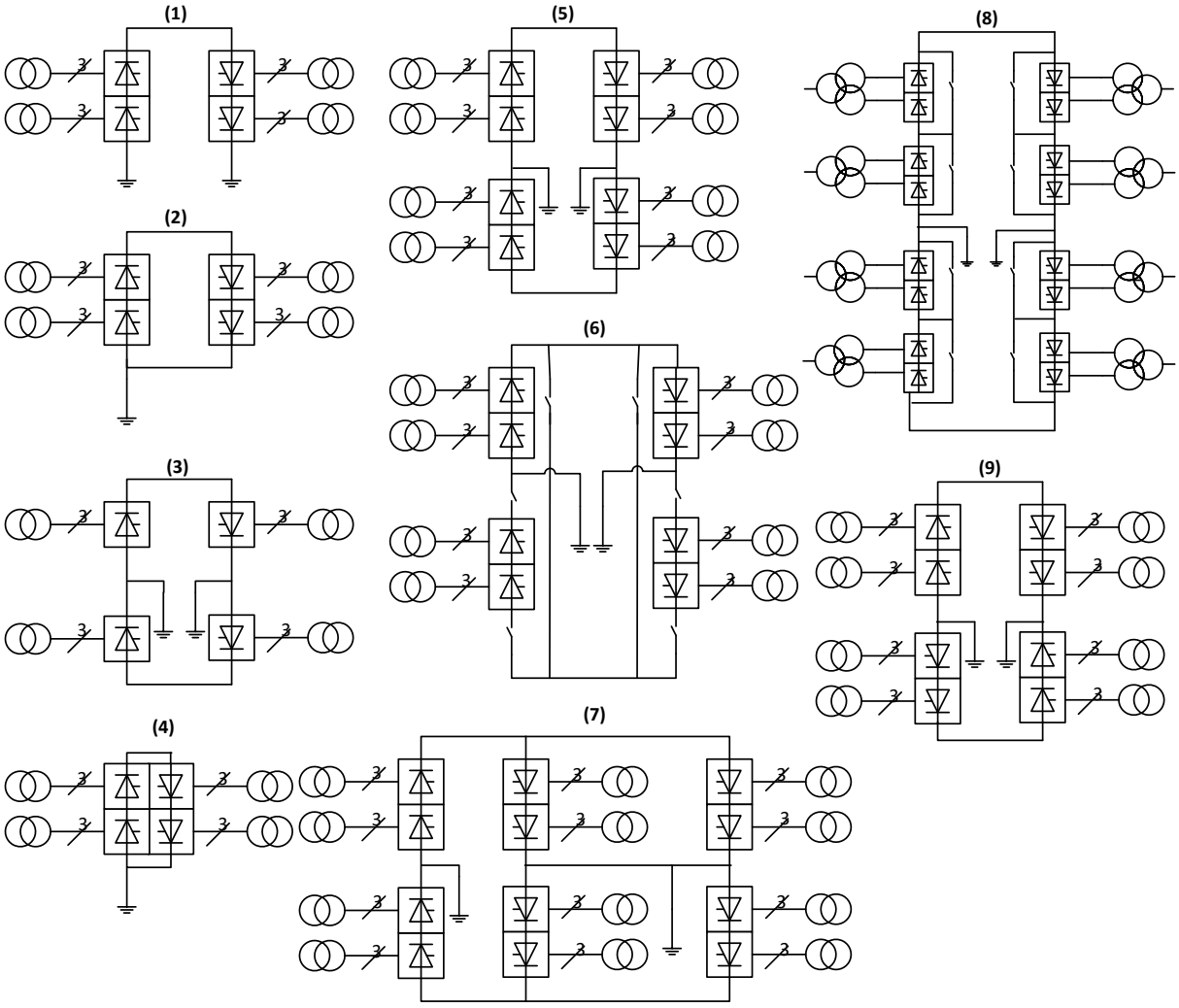

Figure 2.2: HVDC Configurations. (1) Monopole with ground return, (2) Monopole with metallic return, (3) Monopole with midpoint grounded, (4) Back-to-back, (5) Bipole, (6) Bipole with metallic return, (7) Multiterminal, (8) Bipole with series of connected converters, (9) Homopolar.

2.3. Methods of conversion

There are five different converter topologies used in HVDC systems: Line Commutated converters (LCC), Voltage source converters (VSC), Multilevel converters, Modular multilevel converter (MMC) and alternate arm modular multilevel converter (AAMMC).

2.3.1. Line Commutated Converters

This configuration uses thyristors and it had a big impact in the 1970's, when power electronics had a great advance. These semiconductors work as switches, turning on depending on the gate signal. However, they do not have turn OFF capability. The control is performed by changing the firing angle of the thyristors of both converters (AC to DC and DC to AC). When the firing angle is smaller than 90º degrees the converter acts as a rectifier. Otherwise it will work as an inverter [Zhang, 2002].

These LCC based systems need strong and high synchronous voltage source for the purpose of commutation which results from the firing of the thyristors being synchronized with the grid voltage. This aspect brings an inconvenience of these systems not being suitable for black start events, i.e., the process of restoring the energy after a blackout [Oni, 2016].

LCC demands reactive power during the process because the regulation of the DC current is done through the regulation of the fire angle, which introduces a delay between the AC currents and the corresponding voltages. This results in not having a good reactive power control which leads to the need of reactive power compensation [M. P. Bahrman, 2008].

It is possible to have reverse power flow of the system by changing the polarity of both converters, but it is not an easy solution for DC application [Kharade, et al, 2017].

LCC-HVDC systems are commonly used as they present advantages such as low losses per converter and lower cost for high voltage processing. It has drawbacks as generating low frequency harmonics in the AC grid currents which results in large converters and filtering requirements, as well as the necessity for a reactive power compensation and the lack of black start capability [Kharade, et al, 2017].

The basic topology of these systems is a three-phase thyristor bridge rectifier, as represented in figure 2.3. It is also referred as a 6-pulse converter since the fundamental frequency on the DC side is 6 times the grid frequency.

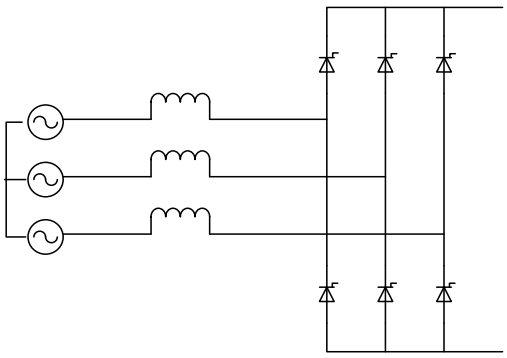

Figure 2.3: Three-phase full-wave thyristor bridge.

The common cathode connected thyristors are switched ON in a sequential way, as well as the common anode connected thyristors. The thyristors will be switched ON when they are forward biased and when they are fired. The firing angle is the delay from the moment when the thyristor is forward

biased until the time instant when it receives the gate current to be turned ON. In other words, it is the delay between the moment that it could be switched ON, and the time instant when it is actually switched ON [Bahrman, 2008].

When the bridge is operated as rectifier, the firing angle should be lower than 90º, the DC voltage should be positive, and the power flows from the grid to the DC side. When the bridge is operated as inverter, the firing angle should be higher than 90º, the DC voltage should be negative, and the power flows from the DC side to the grid.

In Line Commutated Converter based HVDC systems (LCC-HVDC) two three phase full-wave bridge converters are connected in series, resulting in a 12-pulse system, as the one in figure 2.4, in order to increase the DC voltage and to decrease the harmonic content of the DC voltage and the AC currents.

Using two transformers, one with a wye-connected secondary and the other with a delta connection, it is possible to obtain two three phase systems, with displacement factor of 30 degrees between one another. These transformers will then be connected to two three phase thyristor bridge converters connected in series on the DC side [M. P. Bahrman, 2008].

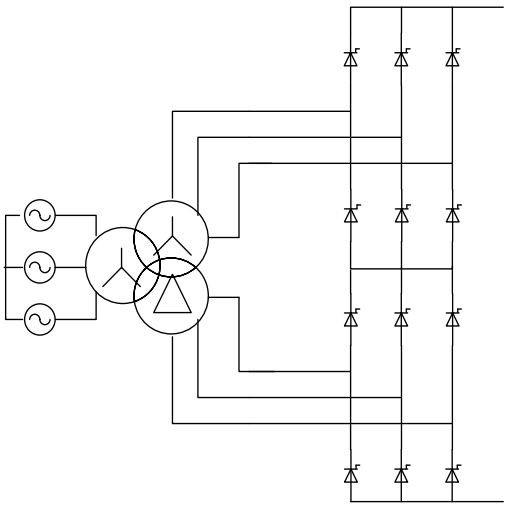

Figure 2.4: 12 pulse thyristor bridge.

The 12-pulse thyristor bridge is used instead of the 6-pulse thyristor bridge, due to its smaller filter components: in the 12-pulse thyristor bridge the 5^{th} and 7^{th} harmonics in the AC voltage and the 6^{th} in the DC voltage are cancelled. As a result, in the AC side, the most relevant harmonics are the 11^{th} and the 13^{th}, while in the DC side the most relevant harmonic is the 12^{th} [Bahrman, 2008].

However, even though the harmonic content of this topology is significantly lower than the one obtained with the 6-pulse bridge thyristor rectifier, it is still too high, and one of the main disadvantages of this solution is the high filtering requirements.

2.3.2. Voltage source converter

Even though LCC are a good and well-established solution for transmitting long distances and bulky power transmission operation, Voltage Source Converter (VSC) based topologies, and especially

modular multilevel converters (MMCs), have many advantages, as they present lower harmonic distortion, allow power factor regulation and have grid forming capability.

One of the great differences between LCC-HVDC and VSC-HVDC systems are the semiconductors: the first use thyristors, while the others use semiconductors, usually IGBTs, with turn ON and turn OFF capability. As a result, in VSC-HVDC systems, there is an additional degree of freedom as the semiconductors have the capability of turning OFF independently of the AC voltages. Additionally, with these semiconductors, VSC-HVDC systems can create its own three-phase AC voltage system, thus allowing black start capability [Oni, 2016].

The most usual process of modulation for these converters is the pulse width modulation (PWM), where the semiconductors are switched ON and OFF at high frequency (much higher than the grid frequency). With this modulation process, it is possible to regulate the amplitude and the phase of the AC voltage [Oni, 2016]. It also helps in reducing the harmonic content of the converter AC currents.

With this modulation process, these topologies allow the control not only of the active but also the reactive power in the connection to the grid [Oni, 2016], and the converter control signals act almost immediately in the converter AC voltage, and on the AC grid currents [Ackermann, 2005].

Active power transmission can be derived from the generation, and the HVDC reactive power is generated to compensate the need of the grid to which the HVDC is connected to [Ackermann, 2005]. Reactive power can be controlled at each HVDC terminal independently of the DC side. As a result, there is no restriction on the minimum short circuit capacity (capacity to interrupt a short circuit current), which was the case of the LCC topology [Ackermann, 2005].

Reactive power demand results from the AC filters, shunt banks (capacitor that improve power factor meaning a higher power transmission capability) or series capacitor. Any variation on reactive power must be hold by the AC network. The weaker the network or further away from generation, the smaller the variation is [Bahrman, 2008].

If there is no need for active power transmission, VSC can operate as a static compensator (STATCOM) to deal with the variation of reactive power.

Power can be controlled by changing the phase angle of AC voltage of the converter and the reactive by changing the magnitude of the fundamental component of AC voltage respecting to the AC filter.

The converter can be operated for the four quadrants of power (PQ). If the converter operates at near unity power factor, it can maintain dynamic reactive power reserve for contingencies. Furthermore, the transfer of power can be made in a fast way without altering reactive power exchange with the AC system [Ackermann, 2005].

The basic topology is the 2-level converter, as the one in figure 2.5. Depending on the switches state, two voltage levels (referred to the DC ground) at the AC side of the converter are possible.

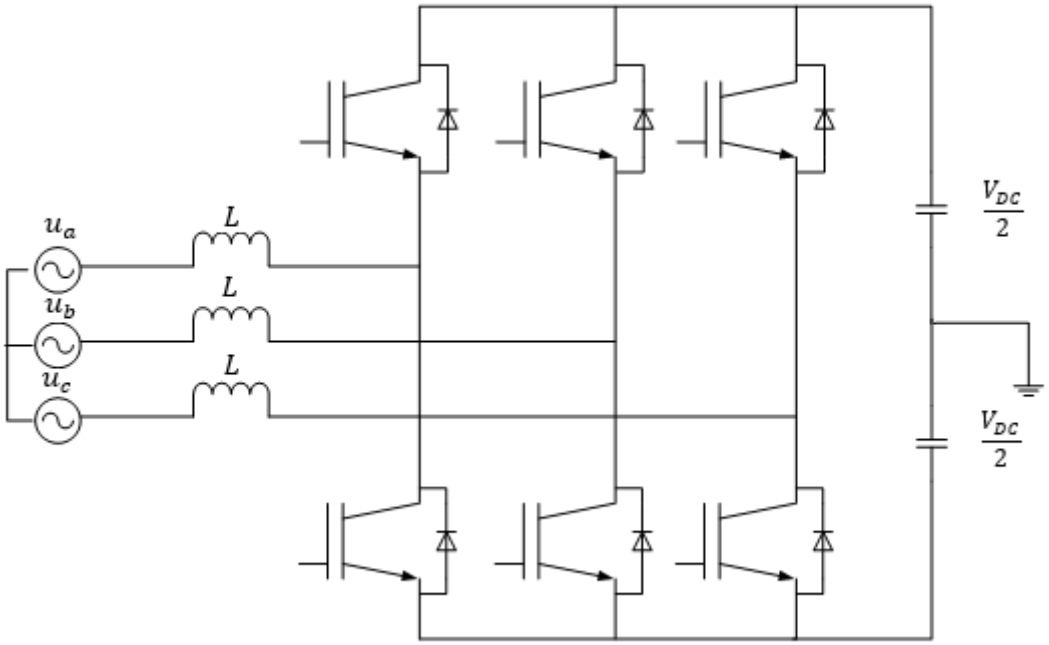

Figure 2.5: 2 level VSC scheme.

Even though this converter is suitable for medium voltage operation, for high voltage it has disadvantages and limitations. The high frequency switching of the semiconductors leads to a decrease of efficiency of the converter compared to an LCC. Also, there is electromagnetic interference for high voltage operation. The rate of change of voltage $\frac{dv}{dt}$ being very large demands high filtering values in the AC side, and the rate of change of current $\frac{di}{dt}$ in the DC side requires a bulky transformer to withstand high voltages for insulation, to handle switching voltage and high frequency operation [Kharade, et al, 2017]. To improve performance, AC filtering is required to mitigate high frequency harmonics.

VSC presents numerous advantages over LCC, as the decreased requirements for filtering components making the size of the converter smaller. They have an improved control capability and there is no need for reactive power compensation, as they are able to control active and reactive power with reduced low order harmonic content.

The change of power flow is much simpler because it can be done by changing the reference value in the controller. However, the losses are higher than in the LCC case (1.7% vs 0.7%) and the cost of these converters is higher than the LCC [Kharade, et al, 2017].

These systems are very common in transmitting power to remote isolated loads or even delivering power to urban areas through a multiterminal direct current (MTDC) [Manohart, et al, 2011].

However, in these topologies there are only two or three levels in the AC voltages, which contain a reasonably high number of high frequency harmonics. Additionally, due to the semiconductors maximum voltage blocking capability, there are limitations in the DC voltage increase. Consequently, in most cases, there is the need to use transformers, which increase the cost and scalability.

2.3.3. Multilevel converters

Another way to deal with the problem of high voltage operation is using the multilevel solution in order to have a high number of levels in the AC side. The main advantages are the reduction of the harmonic content on the AC side, the high efficiency of switching, lower losses and fewer number of components. Nonetheless with a high number of capacitors it results in problems of balancing the voltage in the capacitors.

There are many topologies of multilevel converter as the flying capacitor used in TGV systems or the neutral point clamped converters (NPC) [Kharade, et al, 2017].

NPC multilevel converters are n-level converters with clamping diodes to allow balancing of the capacitors voltages. NPCs do not have large filter requirements and allow reactive power control. However, the necessity of more diodes (for higher levels, it can be unbearable), the capacitors voltage cannot be sustained through switching pattern. It requires a neutral point voltage balancing control for more than three levels and because of the capacitor imbalance it is hard to control the active power of a single level of the converter [Dekka, et al, 2017] [Kharade, et al, 2017].

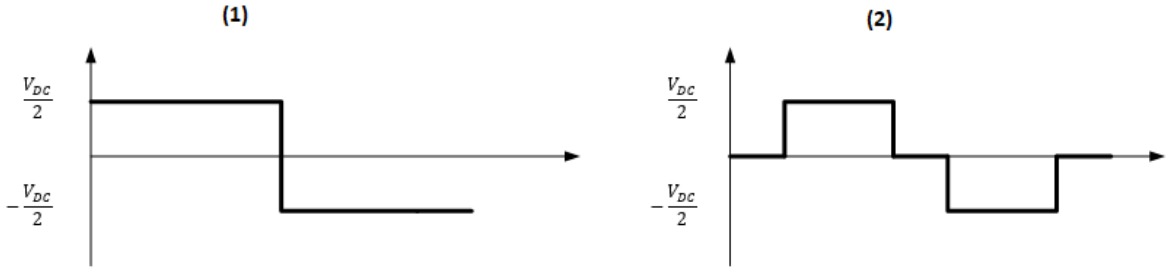

Figure 2.6: Voltage level for a (1) 2 level VSC and (2) 3 level VSC.

A 3-level converter can generate 3 voltage levels at its AC terminals: $\frac{V_{DC}}{2}$, 0 and $-\frac{V_{DC}}{2}$. In each converter leg only two consecutive IGBTs can be turned on because any other combination results in short circuit.

The flying capacitor multilevel is very similar to NPC but the capacitors share the voltage between switches. It uses pre-charged capacitors and it can have a lower harmonic distortion for higher number of levels. It can control active and reactive power flow and allows bidirectional power flow. It has a complex control system for higher levels as the number of capacitors increase with the number of levels. It results in increasing the size and the cost [Dekka, et al, 2017] [Kharade, et al, 2017].

There is a third case that is the cascaded H-bridge. It is the connection in series of H-bridge cells with separated DC sources. For three level output, it has three voltage levels: V_{DC}, 0 and $-V_{DC}$. As to N number of cells it has 2N+1 levels. Comparing to the other two systems, the cascaded H-bridge needs a lower number of semiconductors and capacitors which decreases the size and the cost. There is no need for additional capacitors, it is easily scalable and it works well for reactive power compensation. Nonetheless for a high number of cells the complexity increases dramatically. It is not very suitable for HV applications due to isolate DC sources [Dekka, et al, 2017] [Kharade, et al, 2017].

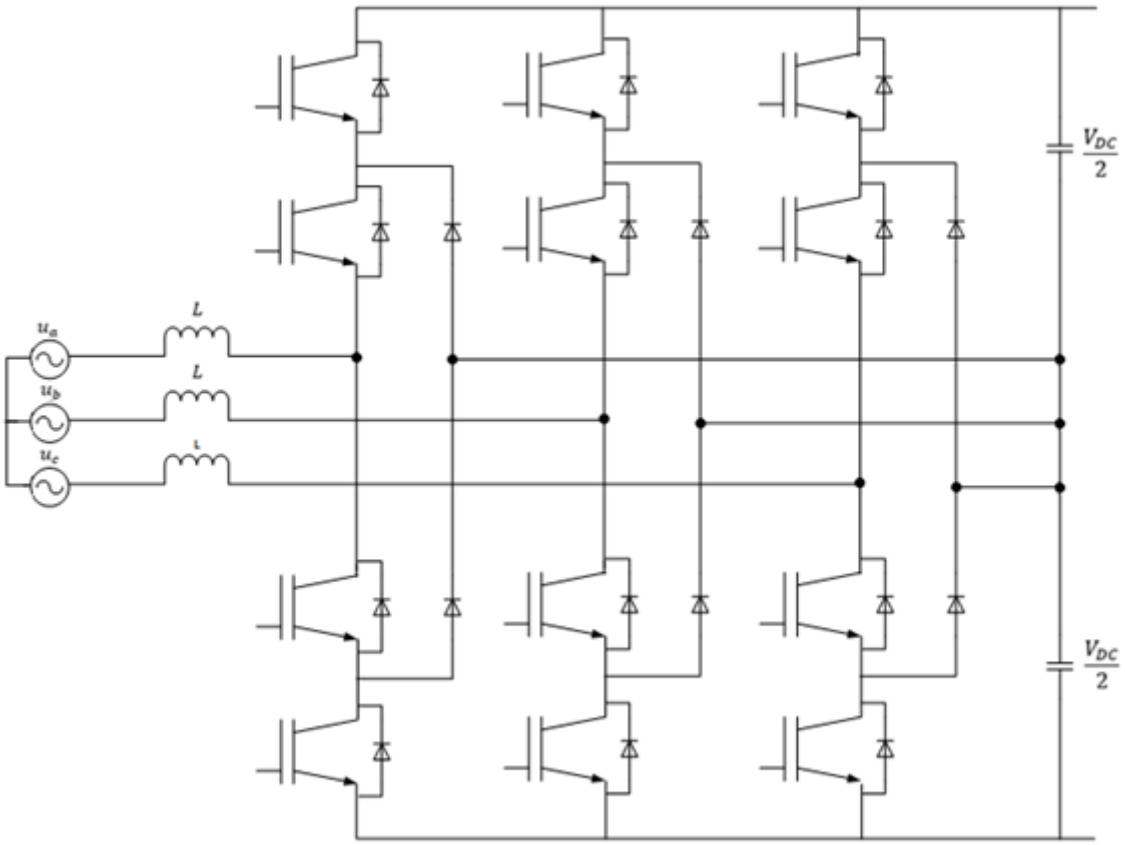

Figure 2.7: 3 level neutral point clamped multilevel converter.

Nevertheless, as these converters are not the best solution for high voltage operation in HVDC applications, other converters that guarantee redundancy, scalability and HV operation have been used [Kharade, et al, 2017].

2.3.4. Modular multilevel converter

In the early 2000's a new topology for High Voltage applications, based on a half bridge VSC has been proposed. This fundamental cell was first proposed by Marquart and Lesnicar in 2003 [Lesnicar, et al, 2003], allowed series connection of hundreds of cells in a modular multilevel topology, thus guaranteeing scalability. The first project using this modular multilevel topology was the San Francisco HVDC Trans Bay cable project [Davies, et al, 2008].

These systems have become very popular for large projects on renewable sources, being the connection of offshore wind farms and interconnection of AC systems the most relevant [Sapkota, 2017].

MMCs have a high number of levels which is ideal to connect to high voltage systems without increasing the switching frequency or transformers rating. Also, with high number of levels, the switching frequency can be lower which contributes to the decreasing of the size of filters and transformers.

These topologies have a better stored energy distribution, they have scalability properties, as they have a modular topology and due to high switching frequency, filters and transformers may be not necessary [Zhang, et al, 2017].

In comparison with the VSC, these topologies have lower converter losses and have better performance. The adversity of having big dv/dt can be avoided by increasing the number of levels as this converter is easily scalable [Zhang, et al, 2017]. There is an immediate disadvantage, that is the control system being much more complex than it was in the other topologies.

The DC side has two voltage sources that can be controlled using the redundant switching states of the multilevel converter [Angquist, 2009]. As the number of levels increases, the balancing of these capacitors voltages will become more complex.

One of the main principles is that the sum of the arm voltages must be always constant and equal do voltage of the DC side. In other words, if the upper arm has an increase/decrease of voltage, the lower arm must have a decrease/increase of the same proportion.

Concerning the control there must be a method of balancing the voltage in the capacitor and it must use a simple PWM modulation or similar as phase shift carrier PWM (PSC-PWM) or level shifted PWM (LS-PWM) for linear control.

To improve reliability for these systems, it should be used the principle of redundancy, periodic maintenance, fault detection and the control post fault [Zhang, et al, 2017].

The topology of this converter consists on each arm having a connection in series of several submodules, where each submodule contains 2 IGBT's and a capacitor. The energy stored in the capacitors can be used to damp power oscillation [Zhang, et al, 2017]. This capacitor is isolated and separated in each SM. This implies that DC voltage ripples cause circulating currents in each phase which creates ripple in the output current.

With MMC topologies there are two issues that every control must deal with: balancing the voltage in the capacitors and the problem with the circulating currents that can lead to instability problems.

A SM can be a half bridge of full bridge type which results on naming the two possible MMC systems: Half-bridge modular multilevel converter (HB-MMC) and the full-bridge modular multilevel converter (FB-MMC). There are other three types of SM: the unipolar-voltage full-bridge (UFB), the clamp-double (CD) and the three level / five-level cross-connected (3LCC/5LCC) but they are interesting only from an academic perspective [Zhang, et al, 2017].

The first presents an improvement, in comparison to the standard VSC, as it reduces the amplitude of the transient DC fault current. Also, with the addition of more SMs, the converters can have more levels which make them scalable for transmission of high voltage, decrease of harmonic content and no need for filters as they can eliminate the low order harmonics.

However, they cannot avoid the AC side influence on the DC fault current which results of having a fast circuit breaker. This requirement results from the fact that if the circuit breaker is not fast enough it

can damage the diodes. Each SM has a bypass switch to allow it to be removed form operation in the event of a semiconductor failure. Also, they have a thyristor to protect the lower diode from overcurrent in case of DC fault. The fault current flows through the diodes and that is why this topology cannot deal with DC faults without blocking IGBT. [Beddard, et al, 2015]

Nowadays most HVDC systems use underground or submarine cables. For overhead transmission HB-MMC is not very suitable [Song, et al, 2013]. Most systems use the blocking of IGBT to deal with the fault current. The process spends more time with the control synchronization due to the blocking and unblocking of the semiconductors. Methods that solve the problem without IGBT blocking can use reactive power when active power is lost due to weakness of the AC system. [Jovcic, et al, 2017].

The FB-MMC enables the four quadrants operation. It can block the current flow in the switches of the converter resulting in stopping the exchange of active and reactive power between the DC and AC side. It has a fault ride capability through AC to DC without blocking the IGBT. It can control DC power independently of DC voltage. In a way it gives more flexibility and robustness to the system [Jovcic, et al, 2017].

Nonetheless the most common has been the HB-MMC as the FB-MMC has a higher cost and switching losses. However, it is expected that the FB-MMC will be more used in the future.

2.3.5. Alternate arm modular multilevel converter

There are concepts in the future for hybrid MMC converter, a mix of multilevel and the two-level characteristics: switches (association of IGBT and diodes) and connection in series of H- bridge cells or SM. These switches are connected in series to choose the conduction sequence of the SM AC current. They generate various levels of voltage, so it can improve AC voltage level [Kharade, et al, 2017].

This topology has always DC fault blocking capability as it isolates the fault, as the FB-MMC, avoiding larger size circuit breakers. It also presents the same advantages, as the MMCs with low harmonic distortion and almost a pure sinusoid in the AC side with high number of levels [Merlin, et al, 2017].

It can control each converter independently because one controls the DC link voltage and the other determines the amount of active power in the link.

AAMMC is the newest topology to be discussed and it may have practical application in future as it is scalable and has multilevel characteristics, reduced components, filters and size in general, and mostly due to having a fast response to fault conditions.

3. Design of the MMC-HVDC model

The goal of this dissertation is the design and assessment of an MMC-HVDC. From the previous chapter it was concluded that this topology is the most common and it is more advantageous and the best compromise between cost and its characteristics.

To design the MMC-HVDC it is necessary to take in account the whole model including the ARM, the submodules, the number of semiconductors, the process of modulation, and sizing DC capacitors and inductors of the system connected to the grid.

In this thesis the MMC-HVDC to be design should be able to be connected to a 200 kV DC link, and 100kV in the AC side.

3.1. MMC-HVDC Model

The structure of the MMC-HVDC is shown in figure 3.1, consisting in three legs each one of them connected to one phase of the system.

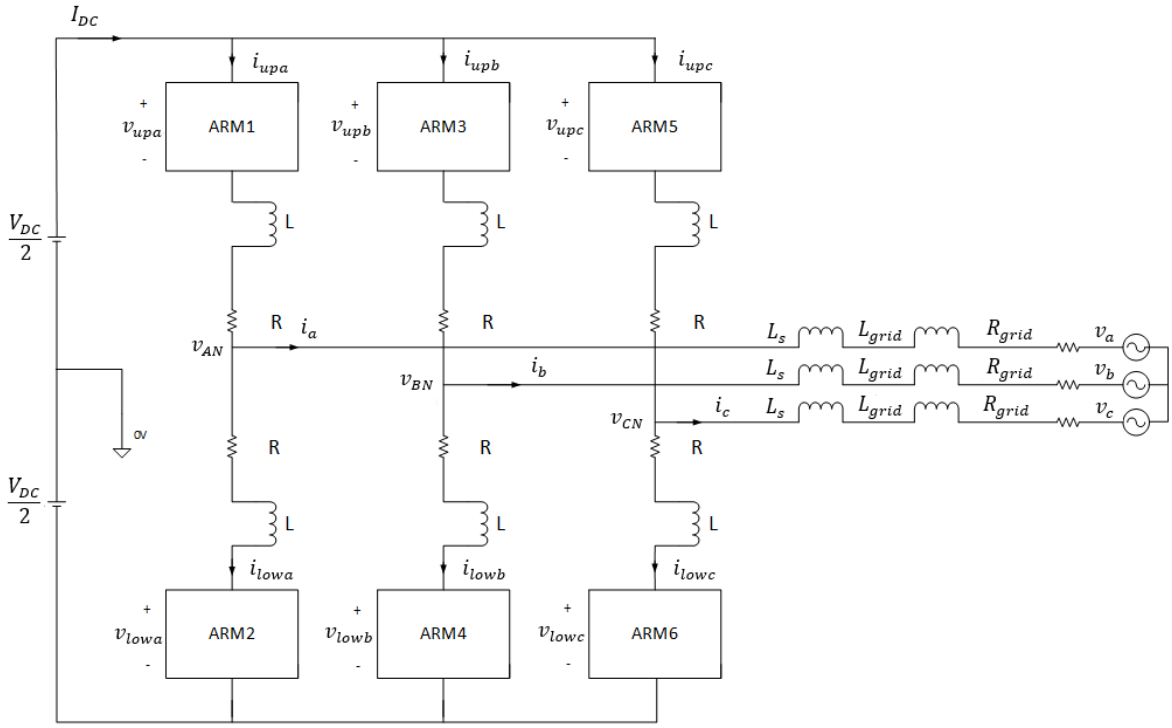

Figure 3.1: MMC scheme

Each leg has two arm converters (ARM) and each one of them has submodules connected in series. All the ARMs have the same number of submodules. In this dissertation the system has 12 submodules in each ARM as the one represented in figure 3.2.

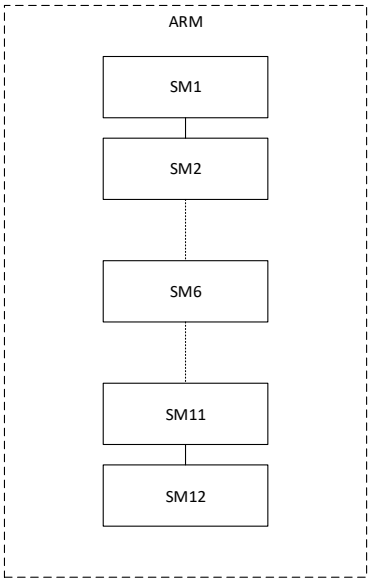

Figure 3.2: ARM scheme

In each phase next to each ARM there is an inductor to support the voltage difference that results from when the submodule is switching states [Angquist, 2009]. It can limit the circulating currents between the phases and reduces the effects of faults in the converter.

A higher inductor means that the circulating currents and the chances of an event of DC fault in the converter decreases [Beddard, et al, 2015]. But obviously a higher inductor means a higher cost.

According to [Beddard, et al, 2015] a minimum L_{arm} should be used to guarantee that the arm current does not exceed 20A/μs for the worst case. In this project, an arm inductor L_{arm}=46 μH was considered. Additionally, a parasitic resistance R=1 mΩ was considered.

The converter arm currents have 3 components, as described in equations (3.1) to (3.4) for phase a. The circulating current results from the DC voltages not being the same as the phase voltages [Beddard, et al, 2015].

$$i_{upa} = \frac{I_{DC}}{3} + \frac{i_a}{2} + i_{circ\_a} \tag{3.1}$$

$$i_{lowa} = \frac{I_{DC}}{3} - \frac{i_a}{2} + i_{circ\_a} \tag{3.2}$$

$$i_{circ\_a} = \frac{i_{upa} + i_{lowa}}{2} - \frac{I_{DC}}{3} \tag{3.3}$$

The sum of the circulating current in all three phases must be zero (3.4).

$$i_{circ\_a} + i_{circ\_b} + i_{circ\_c} = 0 \tag{3.4}$$

Using Kirchhoff's laws, the converter phase voltages can be obtained. For example, the voltage in phase "a" can be obtained from (3.5) and (3.6) through the voltage in DC link V_c, and the voltages and currents in the upper or lower arm.

$$v_{AN} = \frac{V_{DC}}{2} - v_{upa} - L\frac{di_{upa}}{dt} - Ri_{upa} \tag{3.5}$$

Or

$$v_{AN} = \frac{V_{DC}}{2} + v_{lowa} + L\frac{di_{lowa}}{dt} + Ri_{lowa} \quad (3.6)$$

The upper and lower arm voltages are the sum of the voltage of the submodules that are in the ON state, as represented in (3.7) and (3.8):

$$v_{upa} = \sum_{k=}^{N} S_{upk_a} v_{c_{upa}} \quad (3.7)$$

$$v_{lowa} = \sum_{k=}^{N} S_{lowk_a} v_{c_{lowa}} \quad (3.8)$$

$$S = \begin{cases} 1, & SM\ is\ ON \\ 0, & SM\ is\ OFF \end{cases} \quad (3.9)$$

3.2. Submodule

The topology that was chosen was the half bridge as it is more common, and it costs less than full bridge even though it doesn't have fault block capability. It consists of two IGBTs (T1 and T2), two diodes in antiparallel connection (D1 and D2) and a capacitor, as seen in figure 2.3.

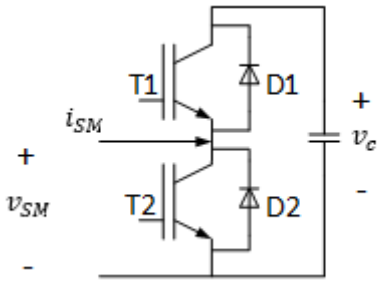

Figure 3.3: Half-Bridge Submodule scheme.

In each SM there is bypass switch in order to remove the submodule in case of a DC fault current, and a thyristor to protect the diode from overcurrent [Beddard, et al, 2015].

The current that flows in the SM, which depends on the arm current direction will affect the charging and discharging of the capacitor.

When the SM is turned ON then T1 is ON and T2 is OFF. In this case, and when the current in the SM i_{sm} is positive, the current flows through D1 which charges the capacitor C as it increases its voltage (V_c). If the current is negative with the SM turned ON, then the current flows through T1 and discharges the capacitor and its voltage decreases.

If the SM is OFF then T1 is OFF and T2 is ON. If the current i_{sm} is positive the current flows through T2 and the voltage of the capacitor remains equal. It also remains constant if the current i_{sm} is negative as it flows through D2.

The voltage of the SM is equal to the voltage in the capacitor when the state of the SM is ON. If it is OFF then the voltage of the SM is zero. Table 3.1 features all the possible combinations of the elements of the SM and in figure 3.4 is a representation of the current flow for all possible combinations.

Table 3.1 Possible states of the Submodule and the relationship between the variables.

Case	SM state	T1 state	T2 state	i_{SM}	Δv_c	v_{SM}
1	ON	ON	OFF	>0	+	v_c
2	ON	ON	OFF	<0	-	v_c
3	OFF	OFF	ON	>0	0	0
4	OFF	OFF	ON	<0	0	0

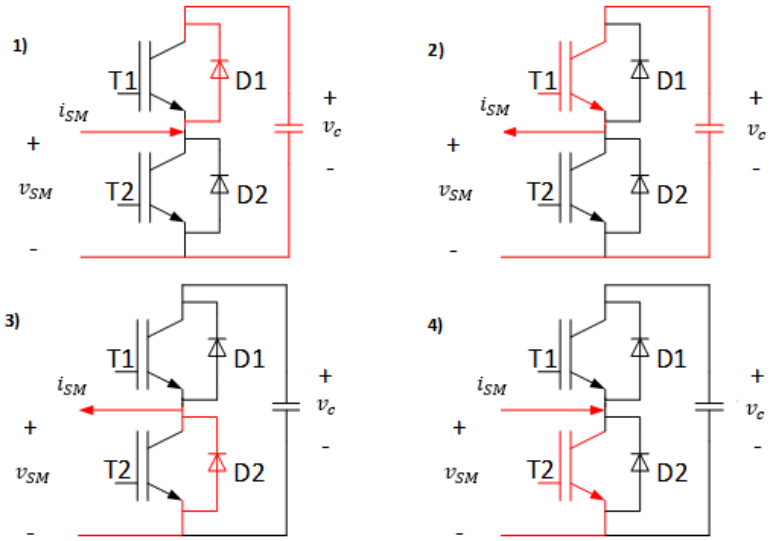

Figure 3.4: Current flow in the four cases in a Submodule

The voltages in the capacitors will be:

$$v_c = \frac{V_{DC}}{N} \tag{3.10}$$

where N is the number of submodules in each arm or in other way the number of submodules in ON state in the upper arm and the ones in the lower arm [Ramirez, et al, 2017] which can be expressed by:

$$N_{up} + N_{low} = N \tag{3.11}$$

3.2.1. Semiconductors sizing

For the number of submodules that has been used, the voltage in each submodule capacitor is:

$$v_c = \frac{V_{DC}}{N} = \frac{200 \times 10^3}{12} = 16.7\ kV \tag{3.12}$$

To guarantee 50% margin of security, the semiconductors should be able to block around 25kV.This value is not suitable for a real system because the voltage applied to each IGBT is too high. However,

this is a consequence of considering a reduced number of submodules to minimize the computational burden in the simulations.

In a real system the number of submodules would be around 200, and for that reason the voltages in the capacitors would be 1 kV, which is an acceptable value.

Knowing the power of the converter and AC voltage, the peak value of the phase currents, as well as the peak value of the semiconductors currents is (3.13).

$$i_{ACmax} = 8000\ A \tag{3.13}$$

For the purpose of simulation, the semiconductors conducting resistance (Ron) is 10mΩ, the snubber resistance (R_s) is 1MΩ and the snubber capacitance (C_s) is inf in Matlab simulation.

3.2.2. Capacitor

The value for the capacitor is a compromise between the size of the capacitor and the submodule capacitor voltage ripple. The following equation shows that the capacitor value depends on the current voltage ripple and frequency.

$$i_c = C\frac{dv_c}{dt} \Leftrightarrow i_c = C\frac{\Delta v_c}{\Delta t} \tag{3.14}$$

Usually if the voltage ripple is in the range of ±5% it is considered a good compromise. According to [Jacobson, et al, 2010], for this range of ripple is provided from a 30-40kJ of stored energy per MVA. With all these in mind a capacitor (C) of 90mF was chosen.

3.2.3. Number of SM

The number of the “output steps” depends straight on the number of modules available in each arm. As we seen previously it will affect the number of levels the voltage in the capacitors.

A higher number of submodules will produce better waveforms, that will result in lower Total Harmonic Distortion. The simulation will start with 6 SM and then 12 SM will be considered in order to evaluate the differences between the obtained results.

In figure 3.5 the waveform for an MMC with 6 submodules in each arm is illustrated.

3.1. Filters

For higher voltages, the number of SMs should increase and the filter requirements should be reduced. If the number of levels is high enough filters may even not be required. However, they should be used as they contribute to reduce the harmonic content of the currents.

The inductor is sized according to (3.15), where V_{DC} represents the DC voltage, Δi is the variation of the current in the coil and f_{PWM} is the switching frequency [Silva, et al, 2012].

$$L_s = \frac{V_{DC}}{4\Delta i f_{PWM}} \tag{3.15}$$

The computed value for the inductor was L_s=3mH with the parasitic resistance being equal to 1mΩ.

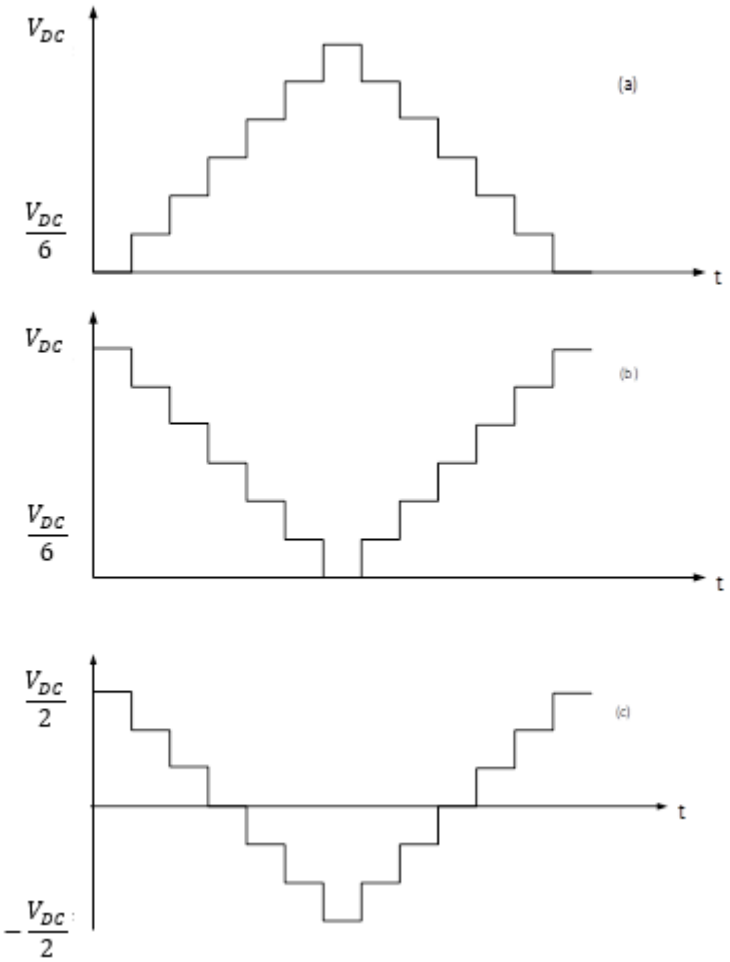

Figure 3.5: Waveforms of an MMC. (a) Output voltage of the upper arm (b) Output voltage of the lower arm (c) Phase voltage of the converter.

3.2. Modulation Strategy

There are many modulation techniques but the most used in these converters is the sinusoidal pulse width modulation (SPWM) and the phase shifted carrier sinusoidal pulse width modulation (PSC-SPWM). In this work the second method was chosen as it has higher flexibility, robustness, a lower total harmonic distortion (THD), a more equal power distribution and lower semiconductor stress due to the switching processes [Hasan, 2017]. In [Li, 2016] and [Bang, 2014] state that in cascaded H bridge converters, the PSC-PWM enables the reduction of common mode voltage, the decreasing in the number of commutations, lowering the switching losses and in the electromagnetic interference. The same results can be obtained in an MMC.

As to all modulation processes there is a reference waveform and several carriers. Each carrier is responsible for the gate signals for each submodule. In this process the carrier waves, usually triangular waves, differ from each other from a phase angle differing from SPWM modulation where the carriers have not different phase angles but different offset levels.

This phase difference is established using the frequency and the number of submodules and it is represented by the equation:

$$\varphi = n\frac{T_c}{N} \tag{3.16}$$

where *n* is the number that corresponds to the selected submodule.

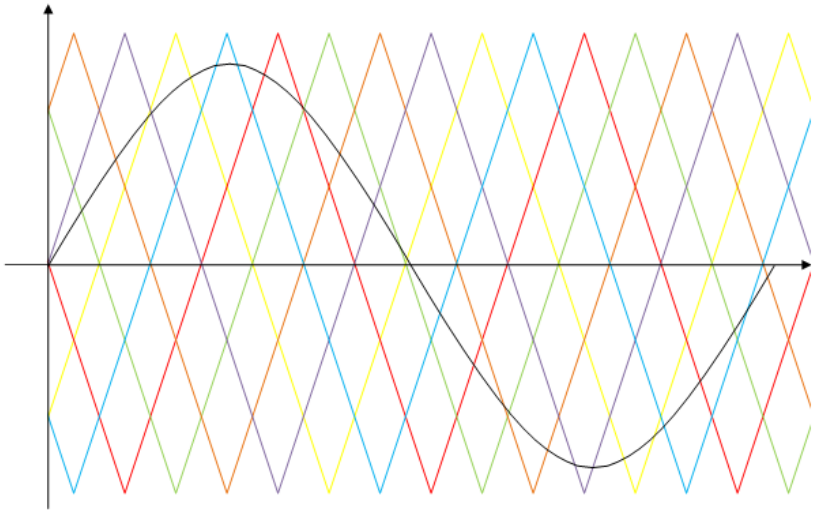

Figure 3.6: PSC-PWM modulation with a reference wave (black) and six carriers.

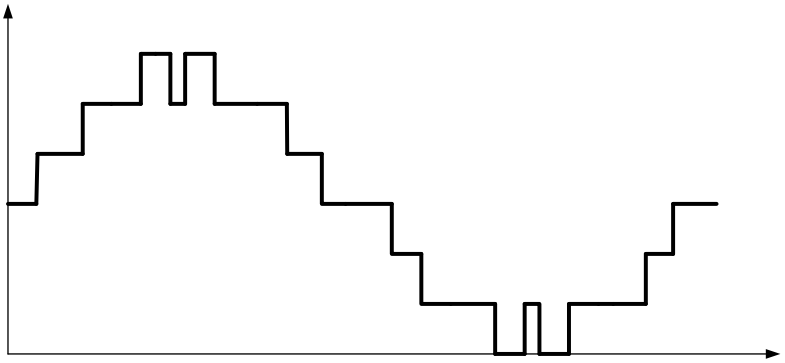

Figure 3.7: Result of the process modulation in an arm with 6 SM.

The PWM modulation principle maintains as there is a comparation between the reference and the carriers. If the modulator wave is higher than all carrier then all the modules are in ON state. In a more general way, the SMs at state ON are the ones where the carrier wave is below the reference.

As a result of this comparison, knowing the SMs that will be ON, the signals to turn ON and turn OFF the IGBTs will be generated.

Figure 3.6 represents the reference and six carriers for 6 submodules. It can be seen that the carriers have a phase shift of 60 degrees.

An example with 6 submodules is shown in figure 3.7, where there are 7 levels corresponding to 6 submodules and the zero level.

4. Controllers Design

A linear controller and a nonlinear controller are proposed for the currents. In the linear control approach Proportional-Integral (PI) controllers are used with an anti-windup system. The output will be the modulator waveform to be used in the PSC-PWM which triggers the IGBTs of the submodules. For the nonlinear approach, a nonlinear current control algorithm (NLCC) will be presented.

For both approaches it is implemented a balance control algorithm to control the voltages in the capacitors.

In order to mitigate voltage sags and overvoltage events, controllers are designed to introduce reactive current component to stabilize the voltage. Finally, it is designed a DC voltage control with PI controllers as well by using the direct part of the current and its reference.

4.1. State Space model

The dynamics of the grid side currents of the MMC in figure 3.1 can be expressed as:

$$\begin{cases} \frac{di_a}{dt} = \frac{v_{AN}}{L_s} - \frac{Ri_a}{L_s} - \frac{v_a}{L_s} \\ \frac{di_b}{dt} = \frac{v_{BN}}{L_s} - \frac{Ri_b}{L_s} - \frac{v_b}{L_s} \\ \frac{di_c}{dt} = \frac{v_{CN}}{L_s} - \frac{Ri_c}{L_s} - \frac{v_c}{L_s} \end{cases} \quad (4.1)$$

Where v_{ABCN} are the MMC three phase AC voltages, $v_{a,b,c}$ are the three phase grid voltages and $i_{a,b,c}$ are the three phase grid currents.

This MMC will be connected to a balance grid which is defined as (4.2).

$$\begin{cases} v_a = \sqrt{2}Vcos(\omega t) \\ v_b = \sqrt{2}Vcos(\omega t - \frac{2\pi}{3}) \\ v_c = \sqrt{2}Vcos(\omega t + \frac{2\pi}{3}) \end{cases}, \quad where\ \sqrt{2}V = 100\ kV \quad (4.2)$$

4.2. System coordinate transform

In three phase systems it is usually used the Concordia transformation (also known as Power invariant transformation) and Park transformation. Concordia transformation allows the representation of a three-phase system as a two-phase linearly independent equivalent, while with Park transformation the time invariance is guaranteed [Silva, et al, 2012].

The Concordia transformation matrix is expressed by:

$$[C]^T = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{4.3}$$

Then, the two-phase equivalent system voltages and currents can be obtained as in (4.4), where x represents the current or the voltage vector.

$$\left[x_{\alpha\beta 0}(t)\right]^T = [C]^T[x_{abc}(t)]^T \tag{4.4}$$

For the grid voltages established in equation (4.2), in αβ coordinates the grid voltage becomes:

$$\begin{cases} v_\alpha = \sqrt{3}Vcos(\omega t) \\ v_\beta = \sqrt{3}Vcos(\omega t) \end{cases} \tag{4.5}$$

The Park matrix that allows the conversion to dq coordinates is expressed as:

$$[D] = \begin{bmatrix} cos\ (\omega t) & -sin\ (\omega t) \\ sin\ (\omega t) & cos\ (\omega t) \end{bmatrix} \tag{4.6}$$

Then, the time invariant voltages and currents can be obtained as in:

$$\left[x_{dq}\right]^T = [D]\left[x_{\alpha\beta}\right]^T \tag{4.7}$$

An interesting characteristic of both transformation matrices is that their transpose is equal to the inverse of the matrix.

The dq axis is synchronous with the voltage source and rotates with an angular speed ω. There are many ways to perform the synchronization with the grid voltages, as phase-locked loop-based synchronization. One possible solution is using the grid voltages in αβ coordinates. Then, we reach the equations (4.8) and (4.9) to compute the cosine and sine for the park transformation [Silva, et al, 2012].

$$sin(\omega t) = \frac{x_\beta}{\sqrt{{x_\alpha}^2 + {x_\beta}^2}} \tag{4.8}$$

$$cos(\omega t) = \frac{x_\alpha}{\sqrt{{x_\alpha}^2 + {x_\beta}^2}} \tag{4.9}$$

With these transformations we can establish through the equation systems already presented above an equivalent system in dq coordinates, which facilitates the control system.

The dynamics of the grid side currents in abc coordinates can be rewritten as:

$$\begin{cases} v_a = v_{AN} - Ri_a - L_s\frac{di_a}{dt} \\ v_b = v_{BN} - Ri_b - L_s\frac{di_b}{dt} \\ v_c = v_{CN} - Ri_c - L_s\frac{di_c}{dt} \end{cases} \tag{4.10}$$

From (4.1), the dynamics of the grid side currents in dq coordinates is obtained (4.11), where v_d, v_q are the modulators, v_{od}, v_{oq} are the grid voltages and i_d, i_q are the currents in dq coordinates.

$$\begin{cases} v_d = Ri_d + L_s\dfrac{di_d}{dt} - \omega L_s i_q + v_{o_d} \\ v_q = Ri_q + L_s\dfrac{di_q}{dt} + \omega L_s i_d + v_{o_q} \end{cases} \quad (4.11)$$

For the design of the controllers it will help to establish the power equation in dq components as well. For three phase system the active and reactive power can be expressed as:

$$P = 3|V||I|\cos(\varphi) \quad (4.12)$$

$$Q = 3|V||I|\sin(\varphi) \quad (4.13)$$

The instantaneous active power can be obtained as

$$P = v_a i_a + v_b i_b + v_c i_c \quad (4.14)$$

Then in dq components and usually considering for the reference that is chosen $v_{oq} = 0$ and $v_{od} = \sqrt{3}V$, where V is the RMS value of the grid voltage the power equations are:

$$P = v_{od} i_d \quad (4.15)$$

$$Q = -v_{od} i_q \quad (4.16)$$

As can be seen from the last equation, for balanced conditions, the design of controllers in dq components is easier as the active and reactive current can be controlled independently with only i_d and i_q respectively [Silva, et al, 2011]. In these conditions the currents and voltages are constant in the chosen reference frame.

4.3. Linear Controllers Design

The variables to control are the phase currents which will be transformed in dq components. The output of the current control will be the modulation voltage (or reference) that will later be transformed to abc coordinates. After that it will be performed the process of modulation described in the previous chapter which results in turning ON and OFF the submodules.

The reference currents in dq components will be set by the voltage controllers. The i_q component will change only when in a presence of a voltage sag or overvoltage, and the i_d component will depend on the power flowing through the HVDC.

As it can be seen in equations (4.11), there are cross terms, i.e, the dynamics of i_q current component depends of i_d current component. Also, the dynamics of i_d current component depends of i_q current component. The equation (4.11) can be rewritten as:

$$\begin{cases} u_d = Ri_d + L\dfrac{di_d}{dt} - \omega L i_q + v_{o_d} \\ u_q = Ri_q + L\dfrac{di_q}{dt} + \omega L i_d + v_{o_q} \end{cases} \Leftrightarrow \begin{cases} \dfrac{di_d}{dt} = \dfrac{u_d}{L} - \dfrac{R}{L}i_d + \omega i_q - \dfrac{v_{o_d}}{L} \\ \dfrac{di_q}{dt} = \dfrac{u_q}{L} - \dfrac{R}{L}i_q - \omega i_d - \dfrac{v_{o_q}}{L} \end{cases} \Leftrightarrow \begin{cases} \dfrac{di_d}{dt} = -\dfrac{R}{L}i_d + \dfrac{H_{id}}{L} \\ \dfrac{di_q}{dt} = -\dfrac{R}{L}i_q + \dfrac{H_{iq}}{L} \end{cases} \quad (4.17)$$

Where,

$$\begin{cases} H_{id} = u_d + \omega L i_q - v_{o_d} \\ H_{iq} = u_q - \omega L i_d - v_{o_q} \end{cases} \quad (4.18)$$

Which results that the modulators u_d and u_q depend on H_{id}, H_{iq}, the cross terms and grid voltage in dq components. The output of the linear controllers are the H_{id}, H_{iq} components.

To reach the goal, Proportional-Integral (PI) controllers are used, as they produce good results, relatively fast response times, and zero steady state errors.

For the proportional component, the correction of the variable is proportional to the error. The integral term sums the error continuously in time meaning an integration of the error over time. For instance, if the error is positive it accumulates the error and when it is negative the error decreases correcting itself. This latter term has another advantage compared to the proportional as it eliminates the offset through the integral of it. It will act on it until the error is zero. Thus, this integral action eliminates the steady state error that would appear if only a proportional controller would be used.

4.3.1. PI Controllers

The transfer function of a PI controller can be expressed as

$$C(s) = K_P + \frac{K_I}{s} \quad (4.19)$$

where K_p and K_i are the proportional and integral gains. Through the block diagram of the figure 4.1 it can be established the output of the controller as

$$y = K_P e + K_I \int e dt \quad (4.20)$$

With *e* as the error of the variable to control.

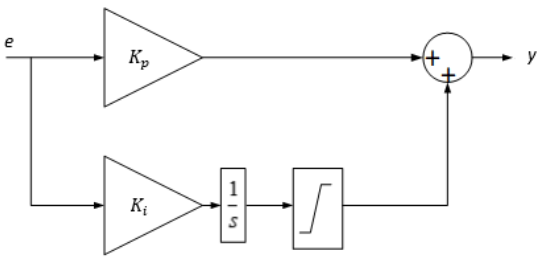

Figure 4.1: PI controller

To compute the gains it is helpful to look at the equation (4.21) and to the block diagram in figure 4.2.

$$\begin{cases} i_a = \dfrac{v_{AN} - v_a}{R + sL_s} \\ i_b = \dfrac{v_{BN} - v_b}{R + sL_s} \\ i_c = \dfrac{v_{CN} - v_c}{R + sL_s} \end{cases} \quad (4.21)$$

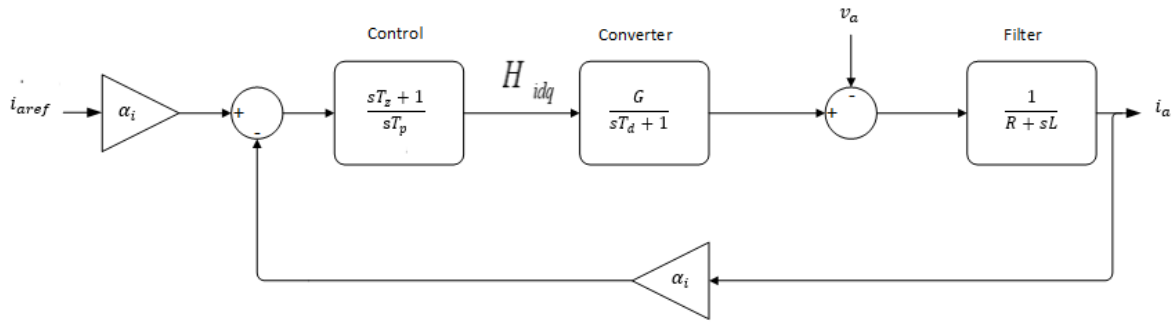

Figure 4.2: Linear Control representation.

The converter can be characterized as a first order transfer function, with a gain *G* and a delay T_d [Silva et al, 2012]:

$$G = \frac{u_d}{V_{DC}} \tag{4.22}$$

T_d is the delay time of the system to a response to an input and it is usually equal to one half the switching period (4.23).

$$T_d = \frac{T_c}{2}. \tag{4.23}$$

When designing these controllers, one possibility would be to consider the optimum symmetry method [Jelani, et al, 2011]. This method presents advantages, as maximizing the phase margin or optimizing the control system to any disturbance input.

Another option is to cancel the zero of the controller with the pole introduced by the filter.

$$T_z = \frac{L}{R} \tag{4.24}$$

Then, the closed loop transfer function, written in the canonical form of a 2nd order transfer function is obtained:

$$H(s) = \frac{i_{dq}}{i_{dqref}} = \frac{\frac{G}{T_d T_p R}}{s^2 + \frac{s}{T_d} + \frac{\mathrm{G}}{T_d T_p R}} = \frac{\omega_n^2}{s^2 + 2s\xi\omega_n + \omega_n^2} \tag{4.25}$$

From equation (4.25) it is reached:

$$T_p = \frac{2T_d G}{R} \tag{4.26}$$

From (4.24) and (4.26) the proportional and integral gains are obtained:

$$\begin{cases} K_P = \frac{T_z}{T_p} = \frac{L}{2T_d \mathrm{G}} = \frac{L}{T_c \frac{u_d}{V_{DC}}} \\ K_I = \frac{1}{T_p} = \frac{R}{2T_d G} = \frac{R}{T_c \frac{u_d}{V_{DC}}} \end{cases} \tag{4.27}$$

Any big change of the error will result in a peak of the output of the controller. If it is too large for a long time can bring problems as the integrator outputs accumulates the error. One simple way to solve this problem would be to add a limiter. It can solve some problems but if the error remains nonzero for a long time we have the same issue as before. An anti-windup method can solve this issue.

4.3.2. Anti-windup system

When using PI controllers, eventually saturation phenomena can appear. In order to minimize the decreasing of performance, an anti-windup method can be used [Ghoshal, et al, 2010]. During the simulation, problems due to saturation sometimes appeared, and this method was used to solve the issue.

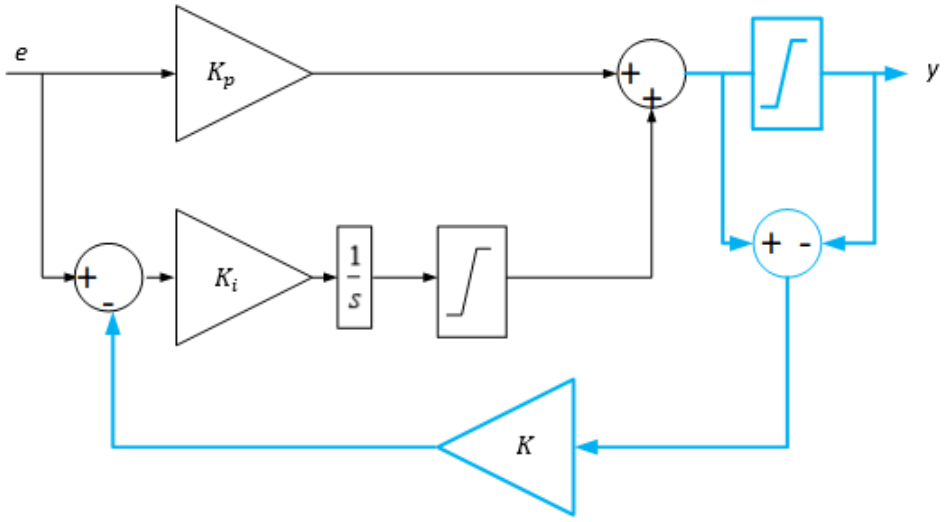

Figure 4.3: Anti-windup scheme (in blue).

Usually saturation issues appear when the error is too large or if the error is nonzero (and always positive or always negative) for a long time. This leads to an accumulation of errors and in delays in the response to any change of the reference. The higher the saturation the higher the delay and the system may lose controllability.

A way of controlling the saturation is using the tracking anti-windup [Ghoshal, et al, 2010]. This method includes a gain fed by the difference of the output of the converter and the saturated value after the limiter which then reduces the error to be integrated. With this, the output of the integrator will be reduced and removed from saturation.

This gain should be high enough to remove the integrator from saturation. However, it should not be too high, otherwise some problems may arise in the control of the desired variable because it can reduce the effect of the integral gain.

The final control scheme is shown in figure 4.4. For mitigation of voltage sags or overvoltages, the AC voltage controller sets the reference for i_{q_ref}. The DC voltage controller will set the reference for i_{d_ref}. Both control systems will be explained in sections 4.5 and 4.6.

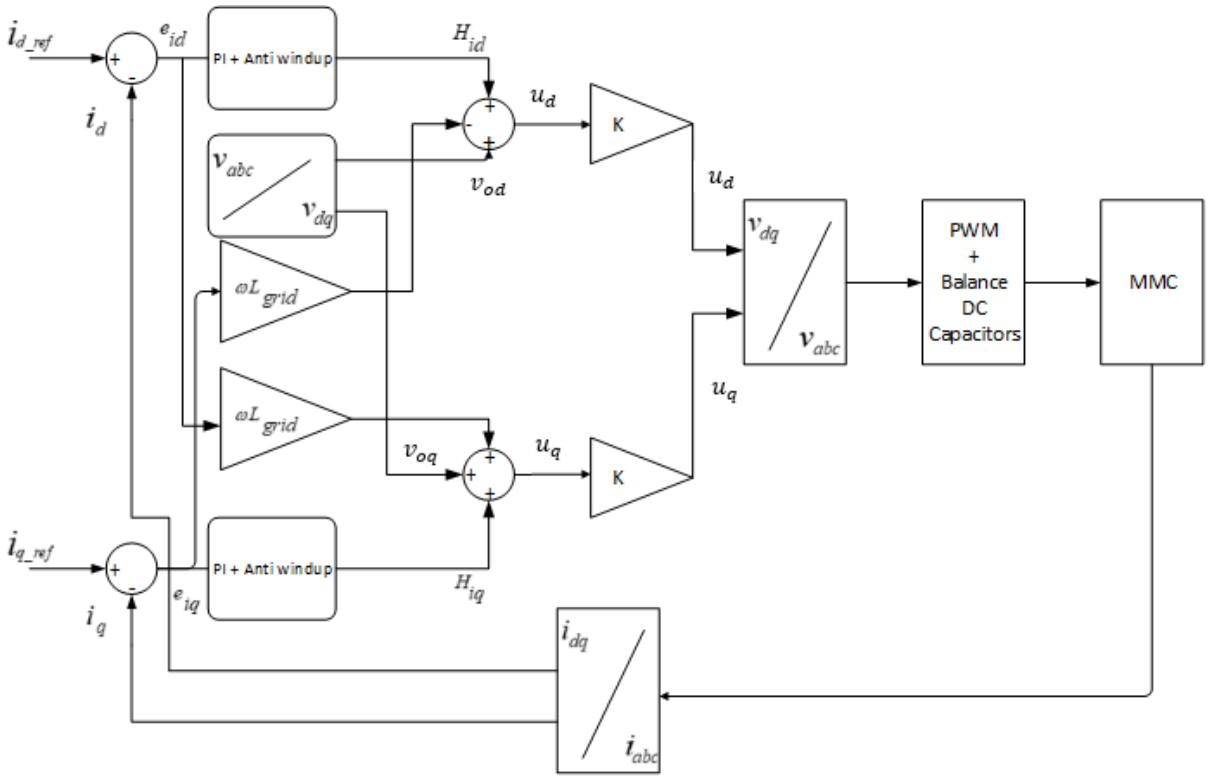

Figure 4.4: Linear control scheme

4.4. Nonlinear Controllers Design

Another way of controlling the phase currents is using a nonlinear approach: Nonlinear current control (NLCC). Compared to the linear approach it does not require PWM modulator, as the algorithm provides directly the number of submodules to be turned ON. Usually it may be not necessary the dq transformation but for comparison and simplicity it was chosen to use it. It has a faster response than the linear controller which will be shown in chapter 5.

The main idea is to establish a hysteresis band of value ε around the reference current. To guarantee that the current error is contained in that hysteresis, it is chosen the number of SM to be active or not which is equivalent to the level of the output voltage. If there are *n* SM then there will be *n*+1 levels.

There are many ways to implement this kind of thinking. The main difference between them is choosing whether the converter's output voltage has values regulated by the grid voltage or not [Martinez, et al, 2015].

It was chosen the first option on which the output voltage of the converter has values adjusted to the grid voltage. This means that the output voltage only has values near the grid voltage and depends on the number of SM in the ON state which will be determined by equation (4.28). The second is more useful when there is a bigger number of submodules because with a higher number of submodules the voltage in the inductor will be lower. This leads to increasing the converter phase voltage which may be necessary to use values that are not adjusted to the grid voltage and to increase the inductance voltage (and the speed of variation of the phase current). Another reason for the choice is that by having values

adjusted the grid voltage it is possible to reduce the inductance value and using the capabilities and advantages of a multilevel topology.

The NLCC algorithm can be seen in the flowchart in figure 3.5 by [Ramirez, et al, 2017]. With the voltage in the DC side (V_{DC}) and the voltage in the capacitor (v_c). the number of submodules in the ON state in the upper and lower arms can be calculated according to the equation (4.28).

$$k = floor\left(\frac{v_{abc} + \frac{V_{DC}}{2}}{v_c}\right) \tag{4.28}$$

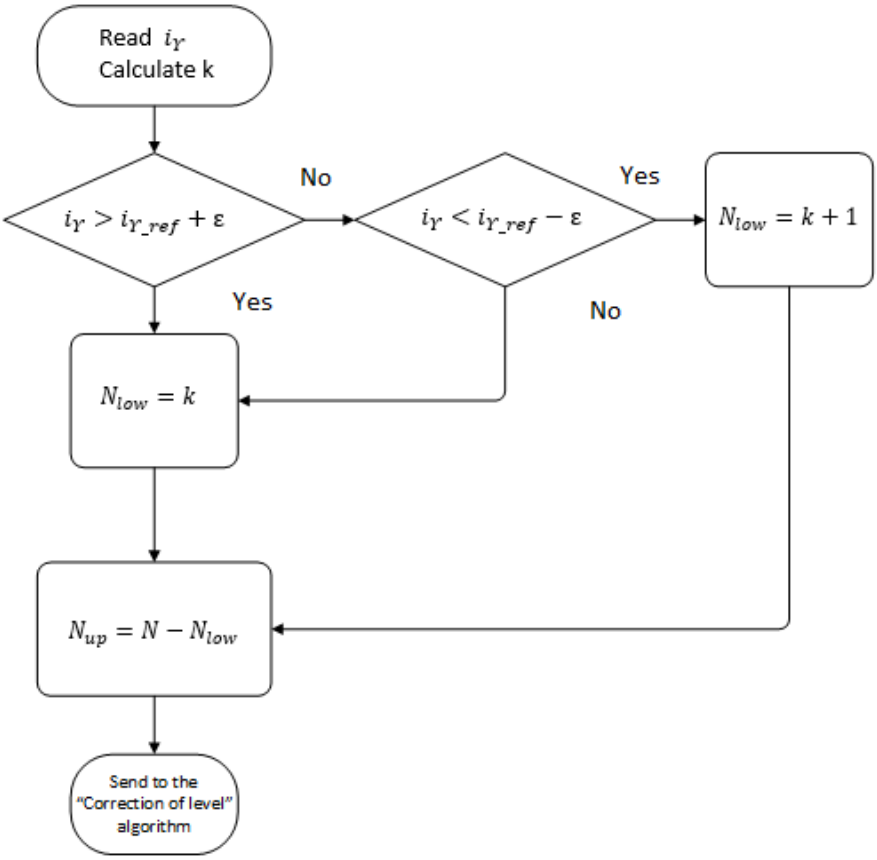

Figure 4.5: NLCC Algorithm

If the phase current i_Υ, where Υ can be phase a, b or c, is higher than the hysteresis band then the number of submodules in the lower arm is the one calculated by the equation above. If not and if the current isn't lower than the hysteresis band the number of SM in the ON state doesn't change. If it is then it is necessary to increase one SM to the one previous calculated. The number of SM in the ON state in the upper arm is selected to complete the number of total SM in an arm, as shown by equation (3.11).

Once again i_{d_ref} and i_{q_ref} will be important for controlling purposes.

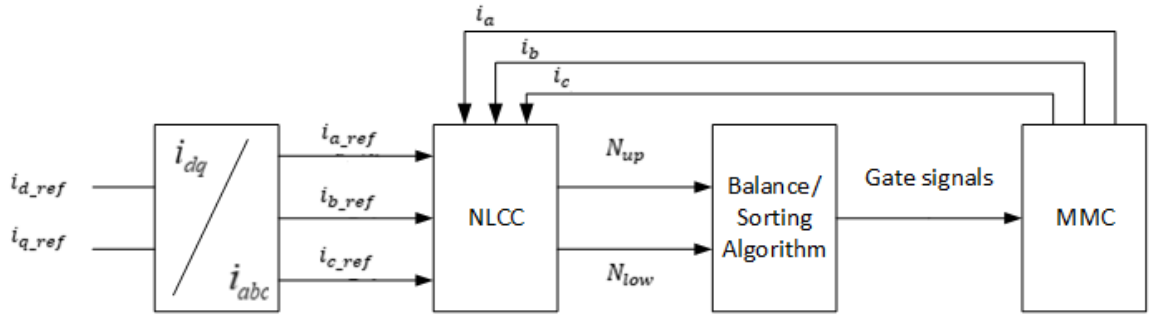

Figure 4.6: Nonlinear control block diagram

4.5. DC Voltage Control

In many papers to illustrate the operation of these systems, the DC side is represented by a DC voltage source to simplify the analysis. However, this is not realistic as the voltage in the DC link will not keep exactly constant, depending on the operation conditions. For that reason, capacitors should be used instead of these voltage sources.

The current control can be represented by a first order transfer function with gain G_i and delay T_{dv} [Alexandre, et al, 2016]. Knowing that the power in the DC link is the same as in the AC link it can be concluded that the gain can be represented as

$$P_d = v_d i_d = V_{DC} I_{DC} \Leftrightarrow I_{DC} = \frac{v_d}{V_{DC}} i_d \Leftrightarrow I_{DC} = G_i i_d \tag{4.29}$$

$$\frac{i_{dq}(s)}{i_{dqref}(s)} = \frac{G_i}{\alpha_i} \frac{1}{sT_{dv} + 1} \tag{4.30}$$

The block diagram of the DC voltage controller is represented in Fig. 4.7 where i_{cable} is the current that enters in the DC side of the converter

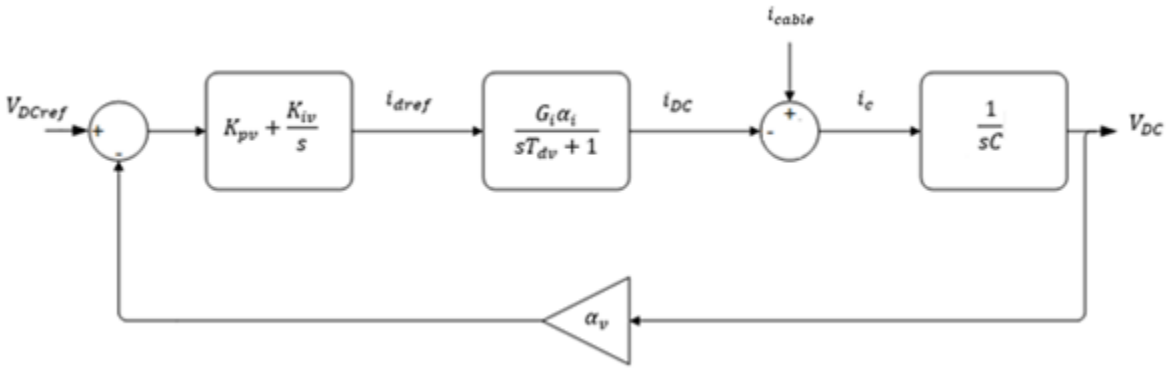

Figure 4.7: Block diagram of DC control voltage.

From the block diagram, the closed loop transfer function is obtained (4.31).

$$\frac{V_{DC}}{V_{DCref}} = \frac{\frac{\alpha_v G_i}{\alpha_i} \frac{K_{pv} + sK_{iv}}{T_{dv} C}}{s^3 + s^2 \frac{1}{T_{dv}} + s \frac{\alpha_v G_i K_{pv}}{\alpha_i T_{dv} C} + \frac{\alpha_v G_i K_{iv}}{\alpha_i T_{dv} C}} \tag{4.31}$$

Comparing the denominator of the transfer function with the third order polynomial (4.32) the values of the controllers gains can be obtained [Alexandre, et al, 2016].

$$p_3(s) = s^3 + 1.75\omega_o s^2 + 2.15{\omega_o}^2 s + {\omega_o}^3 \quad (4.32)$$

$$K_{pv} = -\frac{2.15C\alpha_i}{1.75^2\alpha_v G_i T_{dv}} \quad (4.33)$$

$$K_{iv} = -\frac{C\alpha_i}{1.75^3\alpha_v G_i {T_{dv}}^2} \quad (4.34)$$

4.6. Control during Voltage Sags

According to the standard EN 50160, the definition of a voltage sag or dip is when there is an unexpected decrease of the RMS value of the voltage between 90% to 5% of the nominal value during a short period of time. It can last between 10ms to 60s, and this range depends on the time that it takes for the system protections to act.

The most common origins of voltage sags are faults. The short circuits can have multiple origins as lightning or contamination in the insulators or during connection / disconnection of high consumption loads. Phase-earth faults are the most common type of faults (around 80%). The depth of the sag depends on the point of common coupling (PCC) and the impedance between this point and where the fault originally happened (where the depth of the sag is higher).

The main consequences of voltage sags to power supplies are the decrease of the DC bus as the capacitor may not be properly sized and if it reaches a certain DC voltage the converter may stop functioning. A way to overcome this issue is performing an AC voltage control in the PCC. This controller introduces reactive power in the connection to the grid, so the system keeps working in the conditions previously established.

For the converter to maintain the rated voltage in the load, even in case of occurrence of a voltage sag, then there must be a change in the current controller. This change is in the reference current i_{q_ref} that should no longer be zero, it should introduce reactive power to mitigate the problem. This new value will be calculated by a PI controller that will measure the voltage value in the PCC and calculate the error, based on the AC voltage reference value (the rated value). Then, the PI controller sets the reference current i_{q_ref}. for the current controller (linear or non-linear).

The differences in the voltage in the PCC and the current i_q can be detailed in a first order transfer function with a gain and delay [Sensarma, et al, 2001]. The gain can be expressed as in (4.35), where ω is the grid frequency and L_s is the inductance connected to the grid.

$$K_{AC} = \frac{\Delta v_d}{\Delta i_q} \approx \omega L_s \quad (4.35)$$

The Block diagram of the AC voltage controller is shown in figure 4.8.

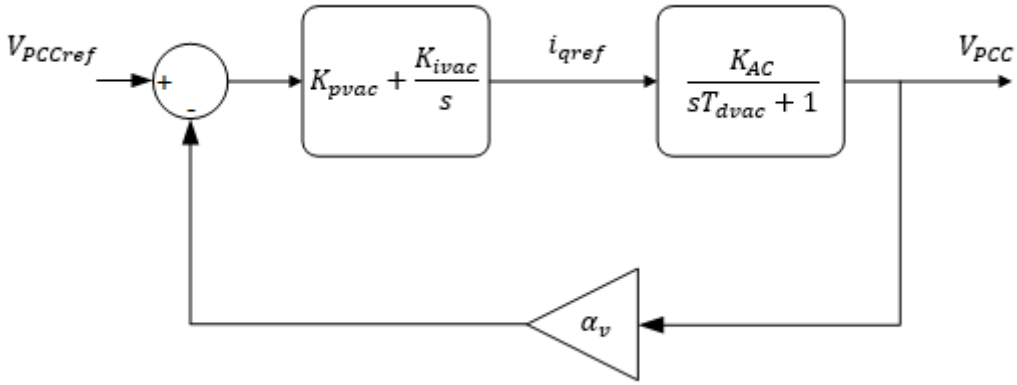

Figure 4.8: Block diagram of Vac voltage controller.

The closed loop transfer function is established in (4.36):

$$\frac{V_{PCCd}}{V_{PCCdref}} = \frac{\frac{sK_{AC}K_{pvAC} + K_{AC}K_{ivAC}}{T_{dvAC}}}{s^2 + s\frac{1 + \alpha_v K_{AC}K_{pvAC}}{T_{dvAC}} + \frac{\alpha_v K_{AC}K_{ivAC}}{T_{dvAC}}} \quad (4.36)$$

The expression for the proportional and integral gains can be obtained comparing the denominator of (4.36) with the second order transfer function written in the canonical form:

$$K_{pvAC} = \frac{2\xi\omega_n T_{dvAC} - 1}{\alpha_v K_{AC}} \quad (4.37)$$

$$K_{ivAC} = \frac{T_{dvAC}\omega_n{}^2}{\alpha_v K_{AC}} \quad (4.38)$$

According to the transfer function, for the system to be stable the gain must be positive and in order to have a finite bandwidth $K_{pvAC} < 1$ [Sensarma, et al, 2001], ω_n must be bounded as in (4.39) and (4.40):

$$\omega_n > \frac{1}{2\xi T_{dvAC}} \quad (4.39)$$

$$\omega_n < \frac{\alpha_v K_{AC} + 1}{2\xi T_{dvAC}} \quad (4.40)$$

4.7. Algorithm to Balance the Capacitors Voltage

One of the main challenges when using MMC is to balance the capacitor voltages. There is a capacitor in each SM and its charge and discharge depends on the current in the arms. This unbalance problem or the existence of circulating currents happens since the SMs differ from each: slightly different capacitance values, parasitic resistances, or different conduction times, resulting on different charge and discharge of the capacitors during the period that the system is active.

The modulation process used is, up to a certain point, a good method for balancing the capacitors. However, due to system unbalances, inequality of semiconductors and filters characteristics, among others, in the long term the capacitors voltage balancing is not guaranteed.

There are many solutions to a reduced switching frequency strategy. Chai [Chai, et al, 2013] uses the switching states of the SM to reduce the number of switching operations at every period of balancing. Kalle [Kalle, et al, 2013] main objective is to reduce the capacitor ripple even with a reduced switching frequency by predicting the capacitor voltage variation at every fundamental period. This leads to a more even charge distribution of all the capacitors. Zhao [Zhao, et al, 2014] uses a method of dividing the submodules into groups and then determining the switching states of the SM.

It is then important to have another balancing algorithm, operated at a lower frequency, in order to avoid the dependency on the PSC-PWM modulation. To explain the method used in this Thesis, inspired by [Ahmad, et al. 2018] the example that will be used will be a system with 6 SM per arm. For 6 SM there will be 7 levels in the output voltage of the ARM. According to (4.41) it is possible to establish the number of redundancies of each level, i.e, the number of switching combinations that the converter can use to have the same level, with *N* being the number of submodules and *l* the level.

$$N_{red} = \frac{N!}{(N-l)!\,l!} \tag{4.41}$$

According to (4.41) there are 64 combinations to have 7 levels. Each level of the AC voltages is obtained as a sum of SM voltages. For instance, if the level is 3 V_c, then three SMs must be in state ON.

The redundancies in each level will help balancing the capacitors as it can be chosen which SMs are ON to obtain a specific level, from all the possible combinations. With this it can be established the required voltage level and a good performance of the SM. These combinations will help choosing the best SM on their need of charging and discharging to reach the capacitors voltage reference value.

The charge/discharge of the SM capacitors results from the direction of the current. In order to work, the balancing algorithm will need to know the reference voltages in the capacitors (1.5), the actual capacitor voltage and the current in the arm (and more important if it is positive or negative). Then it is calculated the error, i.e, the difference between the capacitor reference voltage and the measured value. After, in the linear case through the PWM modulation and in the nonlinear one through NLCC receives the information on the voltage level level.

Then the sorting of the capacitors is made with the sign of current being the main player. If the current that enters in the arm ($i_{upa,b,c}$ or $i_{lowa,b,c}$) is positive, meaning the capacitors will charge, then the capacitor must be sorted from with the biggest difference of voltages to the smallest difference, i.e, form the one which is most discharged to the one which is most charged. If the current is negative, meaning the capacitors will discharge, then the sorting will be the opposite.

With the capacitors of the SMs sorted, each one of them will receive a weight value. The first one will receive the highest and the last one the lowest one. Through the redundancies it is chosen the combination of capacitors with the highest weight result.

After the last step is completed, the output of the algorithm will be the signal gates to the SMs with the indication of which semiconductors should be turned ON and the ones which should be turned OFF to guarantee the desired voltage level. Figure 4.9 shows a flowchart describing the steps mentioned

before for balancing the upper ARM converters. For the lower ARM, the current chosen must be $i_{lowa,b,c}$.

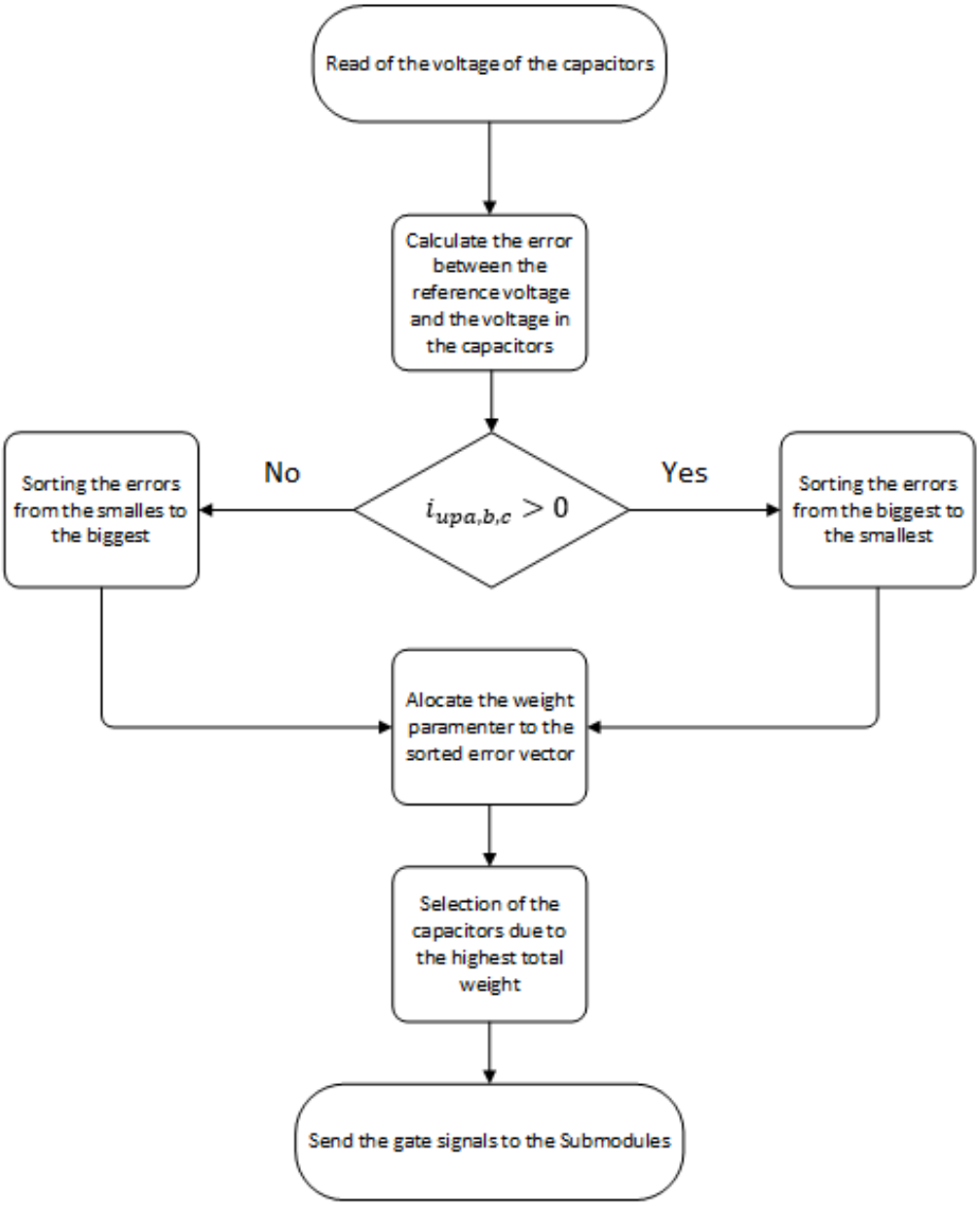

Figure 4.9: Balance of the capacitors algorithm

As an example, if the desired voltage level is $+2V_c$, then it means that there must be 2 SMs in the ON state. The reference voltage in the capacitors in this example is 1000V and the current is positive (case with Pos) and negative (case with Neg).

Table 4.1 shows the actual voltages in the capacitors, the difference and the weight parameter attributed from the smallest to the highest difference if the current is positive (Pos) and from the highest to the lowest if the current is negative (Neg).

Table 4.1: Capacitor voltages, error between it and the reference value and weight parameter.

	SM1	SM2	SM3	SM4	SM5	SM6
v_c	1005	1050	970	880	900	1150
Δv_c	-5	-50	30	120	100	-150
Weight (Pos)	3	2	4	6	5	1
Weight (Neg)	4	5	3	1	2	6

Table 4.2 shows the SM sorted from the smallest to the higher error with the weight parameter chosen, considering that the current is positive.

Table 4.2: Submodules sorted when the current is positive.

	SM4	SM5	SM3	SM1	SM2	SM6
Weight	6	5	4	3	2	1

Table 4.3 presents the SM sorted from the highest to the lowest error with the weight parameter chosen, considering that the current is negative.

Table 4.3: Submodules sorted when the current is negative.

	SM6	SM2	SM1	SM3	SM5	SM4
Weight	6	5	4	3	2	1

Table 4.4: Combination of submodules and weight.

Combination	Total Weight (Pos)	Total Weight (Neg)
SM1+SM2	5	9
SM1+SM3	7	7
SM1+SM4	9	5
SM1+SM5	8	6
SM1+SM6	4	10
SM2+SM3	6	8
SM2+SM4	8	6
SM2+SM5	7	7
SM2+SM6	3	11
SM3+SM4	10	4
SM3+SM5	9	5
SM3+SM6	5	9
SM4+SM5	11	3
SM4+SM6	7	7
SM5+SM6	6	8

In table 4.4 is the analysis for all the combinations that result in the desired voltage level and the weight that is computed with the sum of weight parameter of the modules that are in that combination.

According to this example the best combination where the current is positive would be SM4+SM5 as it has the highest weight parameter. If the current is negative, then the best combination would be SM+SM6. Then, this information is sent to the SM gate signals, as represented in the figure 4.9.

4.8. Correction of level

This is a simple correction algorithm applied to the linear and nonlinear controllers. To establish what is the number of submodules turned on, in other words, what is the level of the converter at the same time, it is used the PSC-SPWM modulation for the linear case and the NLCC for the nonlinear.

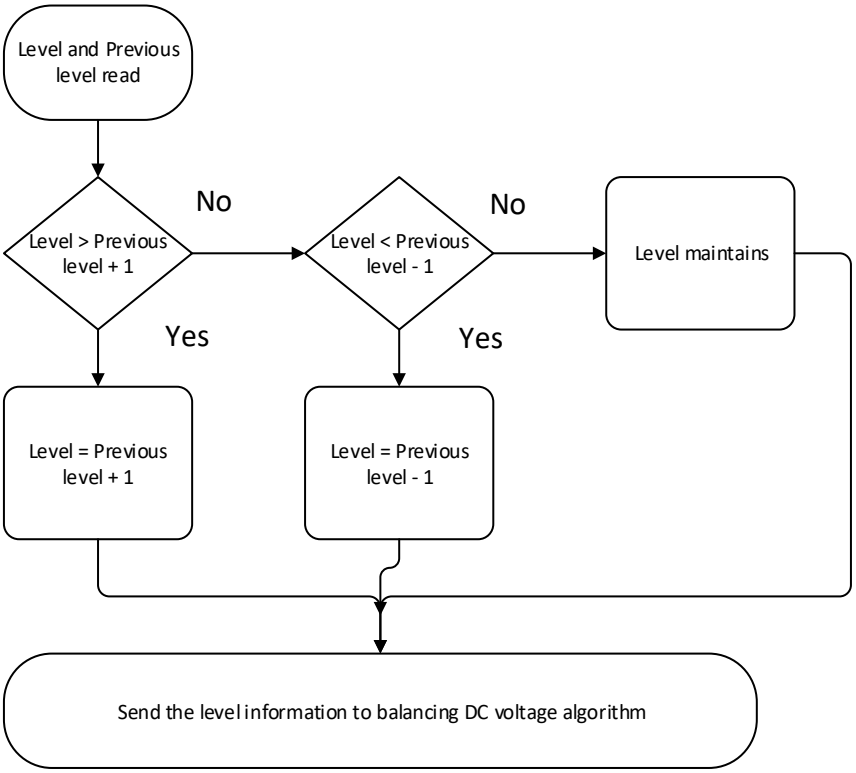

Figure 4.10: Correction of level Algorithm.

Usually the levels are continuously in order to obtain a waveform as similar as possible to a sinusoid. However, during this modulation process sometimes there can be a jump of two levels or more. This algorithm prevents this situation as it receives the number of the previous level and compares it to the following one. If the difference between the previous level and the calculated one is higher than one then the real level that will be sent to the system will be limited to one level above or below the previous one. With this approach it is possible to solve a problem that could bring bigger issues to the AC waveform as it would result in higher distortion.

5. Simulation Results

In this chapter the system is tested and the results are discussed. The simulated MMC-HVDC system is the one represented in figure 5.1 that connects two grids: one operated at 50 Hz and the other operated at 60 Hz. The length of the DC cable is 100km.

In the first sections, it will be analysed in detail the converter connected to the 50 Hz grid. The last one will show the results obtained with the converter connected to the 60 Hz grid. To assess the performance of both control strategies, in each section they will be compared. Also, it will be assessed the DC voltage control, as well as the control for voltage sags and overvoltage events.

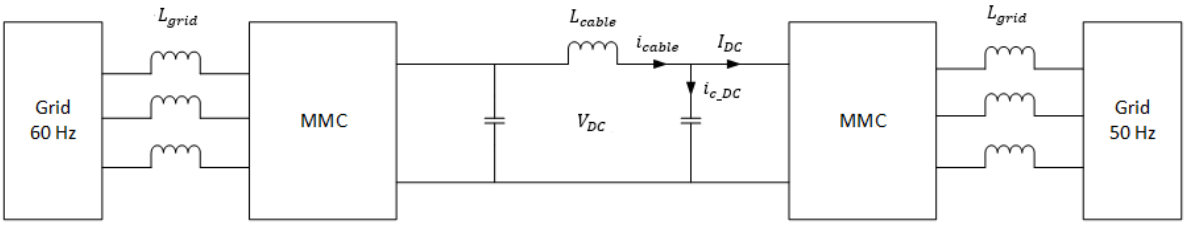

Figure 5.1: MMC-HVDC scheme under analysis.

The waveforms of currents and voltages in the submodules, in the arms, in the DC link and in the grid are obtained. These waveforms will be further used to evaluate the AC voltage controller and DC voltage controller response.

In each section, it is observed the effect of removing a significant number of submodules (6 which means half of the system proposed) in order to observe the importance of having a large number of submodules (even though in this dissertation the studied system has a much lower number of submodules when compared to a real HVDC system).

Table 5.1: System Parameters.

Parameter	Variable description	Value
N	Number of modules in each arm	12
$\boldsymbol{V_{dc}}$	DC voltage	200 kV
R	Resistance in each phase	1 mΩ
L	Coil in each phase	45 μH
C	Capacitor in each submodule	90 mF
U_{cref}	Reference value for the voltage in each capacitor for 12 sm in each arm	16.7 kV
R_{grid}	Resistance connected to the grid	1 mΩ
L_{grid}	Coil connected to the grid	3 mH
C_{dc}	Capacitor in the DC side	100 mF
R_{on}	Conductor resistance	0.1 mΩ
L_{cable}	Coil in the DC cable	10 mH
L_s	Series inductance connected to the grid	1.5 mH

5.1. Simulation parameters

Table 5.1 and 5.2 show the parameter values used in the simulation. Table 5.1 presents the number of modules, as well as the filter values, according to the representation of Fig. 3.1.

Table 5.2 presents the controller parameters obtained from equations (4.1), (4.2), (4.4), (4.7) and (4.8).

Table 5.2: Control Parameters

Parameter	Variable description	Value
K_p	Proportional gain for the linear current control	2640
K_i	Integral gain for the linear current control	929280
ε	Error for the NLCC	5 A
i_{dref}	Reference for the direct current	10000
i_{qref}	Reference for the quadratic current	0
K_{pv}	Proportional gain for the DC voltage control	-11464
K_{iv}	Integral gain for the DC voltage control	-30470959
K_{pvac}	Proportional gain for control during voltage sag or overvoltage event	0.0106
K_{ivac}	Integral gain for control during voltage sag or overvoltage event	541
$f_{carrier}$	Switching frequency	2000 Hz
$f_{modulator}$	Frequency of the modulator	50 Hz

These values will be further used in the simulations.

5.2. Waveforms in the Submodules and in the Arms

In chapter 2 an HVDC system with 12 submodules in each arm was proposed. In figure 3.5 an example with 6 modules is shown where if an ARM has 6 submodules then its waveform will have 7 levels. If the proposed HVDC systems has 12 submodules in each arm then the waveform will have 13 levels.

According to equation (3.12) the voltage in each capacitor will be 16.7 kV and the voltage in the submodule can be the voltage in the capacitor or zero according to table 2.1. Then the voltage in each level will be according to 4.1, where n is the number of submodules in the ON state.

$$u_{level} = n \times u_c \tag{5.1}$$

In table 5.3 it is shown the voltage in each level for a system with 12 submodules in each arm

Table 5.3: Levels of voltage in an ARM with 12 SM.

12 SM in each ARM			
Level	v_{up} **[V]**	**Level**	v_{up} **[V]**
13	$12\frac{V_{DC}}{12} = 2 \times 10^5$	**7**	$6\frac{V_{DC}}{12} = 1 \times 10^5$
12	$11\frac{V_{DC}}{12} = 1.83 \times 10^5$	**6**	$5\frac{V_{DC}}{12} = 8.33 \times 10^4$
11	$10\frac{V_{DC}}{12} = 1.67 \times 10^5$	**5**	$4\frac{V_{DC}}{12} = 6.67 \times 10^4$
10	$9\frac{V_{DC}}{12} = 1.5 \times 10^5$	**4**	$3\frac{V_{DC}}{12} = 5 \times 10^4$
9	$8\frac{V_{DC}}{12} = 1.33 \times 10^5$	**3**	$2\frac{V_{DC}}{12} = 3.33 \times 10^4$
8	$7\frac{V_{DC}}{12} = 1.17 \times 10^5$	**2**	$\frac{V_{DC}}{12} = 1.67 \times 10^4$
7	$6\frac{V_{DC}}{12} = 1 \times 10^5$	**1**	0

In table 5.4 it is shown the voltage in each level for a system with 6 submodules in each arm.

Table 5.4: Levels of voltage in an ARM with 6 SM.

6 SM in each ARM	
Level	v_{up} **[V]**
7	$6\frac{V_{DC}}{6} = 1 \times 10^5$
6	$5\frac{V_{DC}}{6} = 1.67 \times 10^5$
5	$4\frac{V_{DC}}{6} = 1.33 \times 10^5$
4	$3\frac{V_{DC}}{6} = 1 \times 10^5$
3	$2\frac{V_{DC}}{6} = 6.67 \times 10^4$
2	$\frac{V_{DC}}{6} = 3.33 \times 10^4$
1	0

In figure 5.2 it is shown the arm voltage for the system with only 6 submodules in each arm and in figure 5.3 with 12 submodules. On the left the results were obtained using the linear control strategy and on the right were obtained using the nonlinear control approach. In figure 5.4 it is shown the lower arm for the 12-submodule system to show the principle stated in chapter 3. In other words, the upper and lower arm voltages must be out of phase as, in total, the number of SM in the ON state is N (in this case 12 submodules). It can be easily observed that when the upper arm reaches the highest level (level $+13\mathrm{u_c}$) the lower arm has a voltage equal to zero.

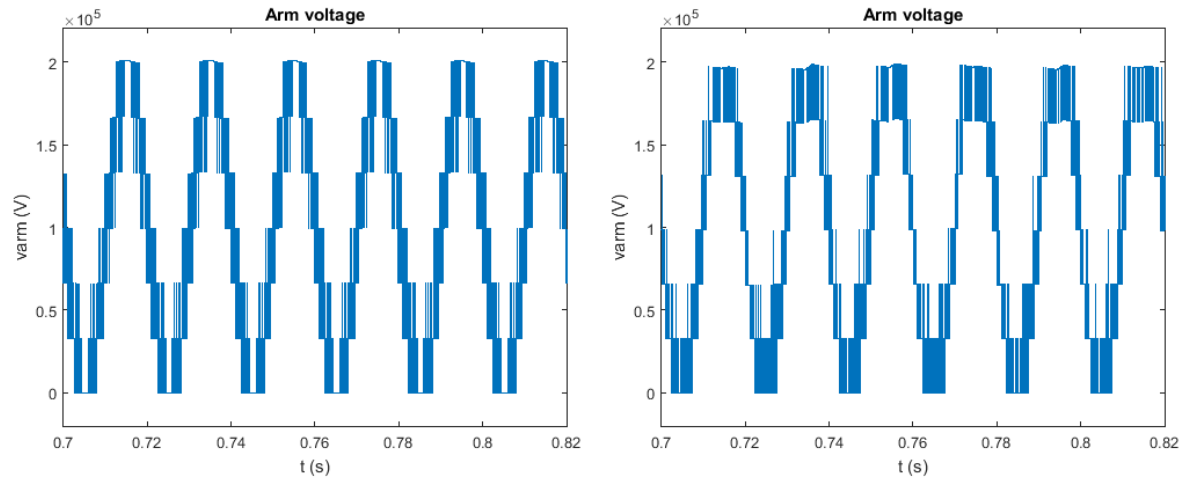

Figure 5.2: Arm voltage for an arm with 6 SM using linear control (a) and nonlinear control (b).

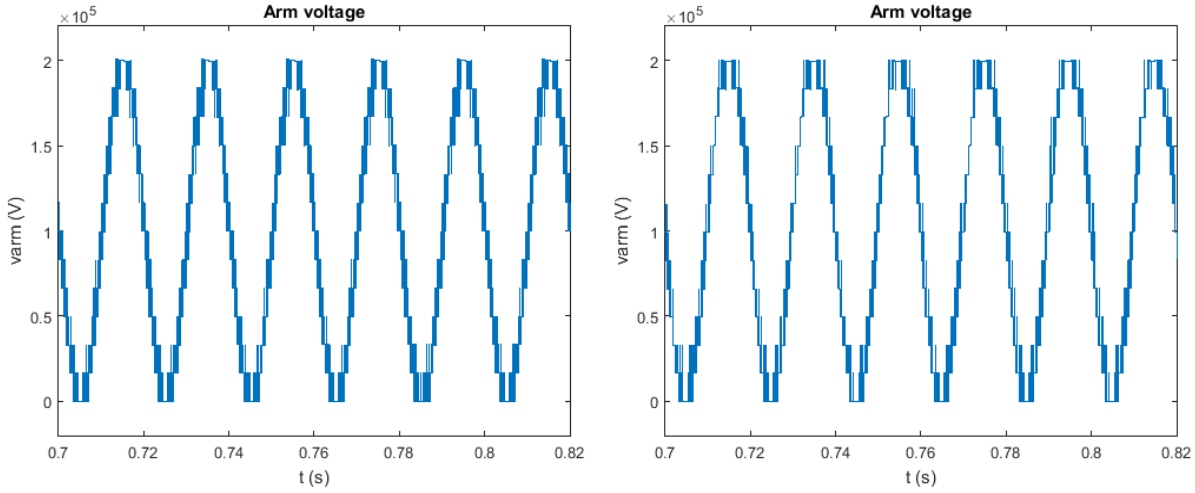

Figure 5.3: Arm voltages for an arm with 12 SM using linear control (a) and nonlinear control (b).

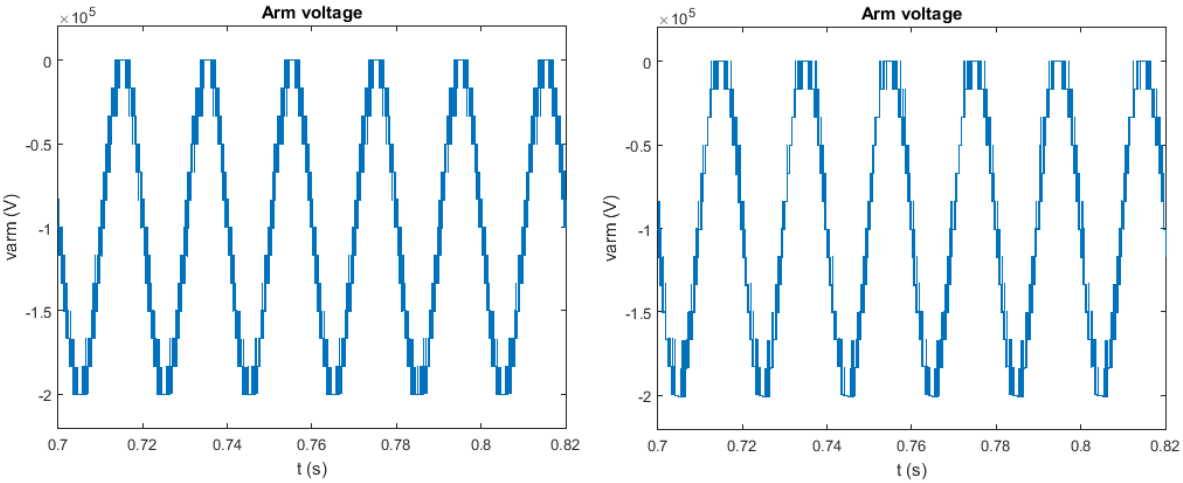

Figure 5.4: Lower Arm voltages for an arm with 12 SM using linear control (a) and nonlinear control (b).

Comparing both control approaches it can be observed that both perform good results. This latter observation can be confirmed in figures 5.5 and 5.6 where the voltages of the capacitor of the first submodule of the upper arm in the first leg of the converter are compared. Figure 5.5 represents the system with 6 submodules and figure 5.6 represents the system with 12 submodules.

For the 6 submodule system, in the nonlinear control approach it can be noticed that the balance of the capacitor reaches the desired value faster than the linear. Also the variation around the target value is lower than in the linear approach.

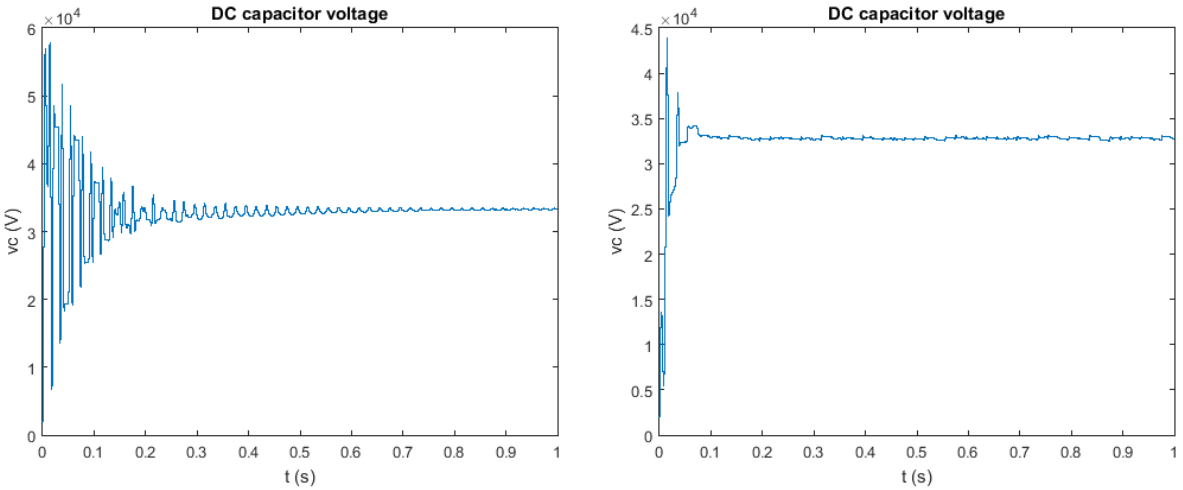

Figure 5.5: Capacitor voltage in one SM with an arm with 6 SM using linear control (a) and nonlinear control (b).

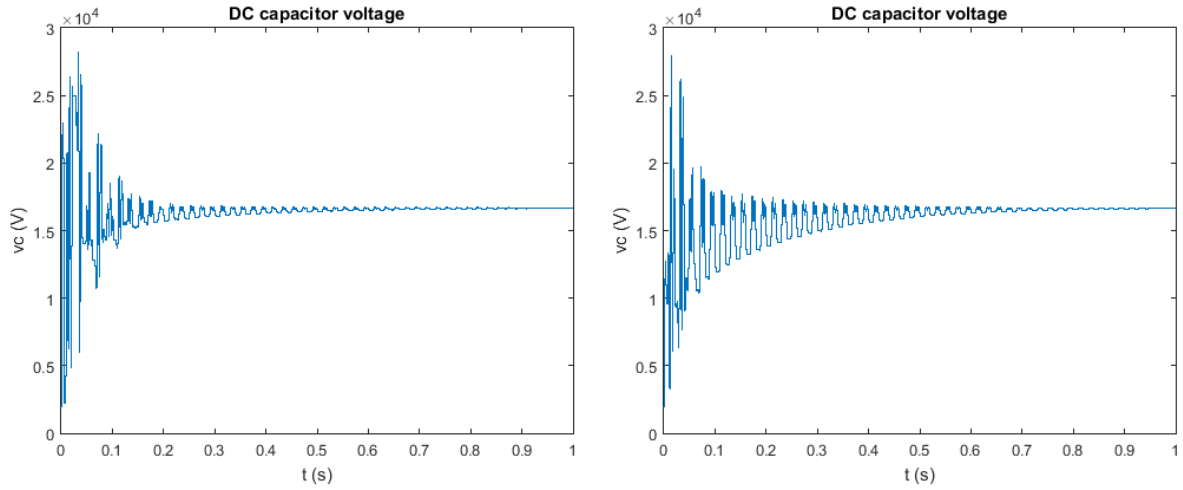

Figure 5.6: Capacitor voltage in one SM with an arm with 12 SM using linear control (a) and nonlinear control (b).

For the 12 SM system, the results appear to be different. The linear approach reaches the desired value faster with less fluctuation than the nonlinear controllers in the beginning of simulation. Even though the linear controller is faster, both approaches present similar results in steady state. The capacitors balance algorithm produces good results for both control methods.

5.3. Waveform of the Phase Voltage

Figures 5.7 and 5.8 show the waveforms of voltage in phase a. According to chapter 2 this waveform results of summing the voltages in the upper and lower arm of the phase converter and it should have the same number of positive and negative levels.

As it can be seen in the next two figures the linear and nonlinear control shows exactly that. However, for the system with 6 submodules with the nonlinear approach there were problems with the middle levels although they were corrected in the 12 submodules system.

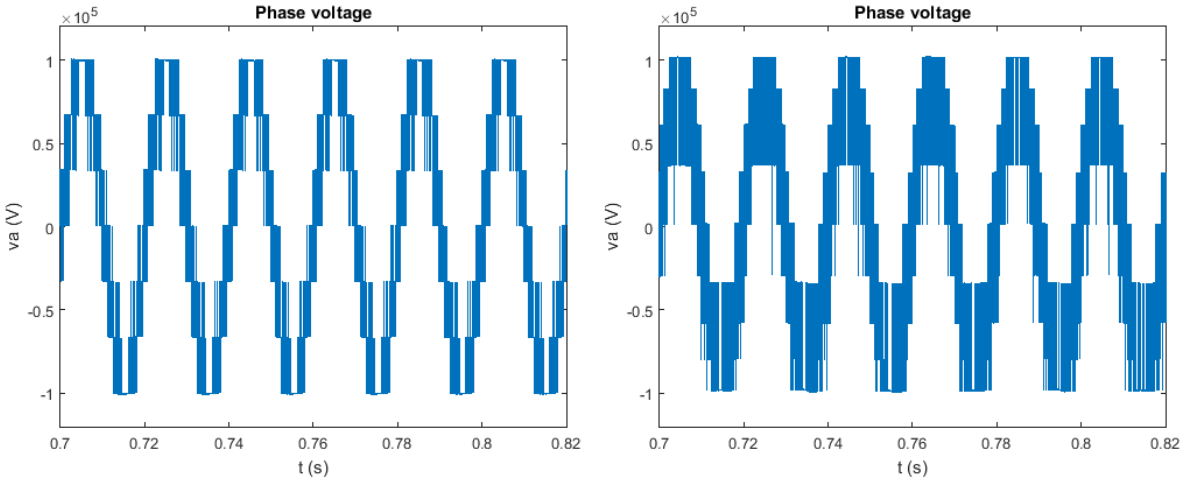

Figure 5.7: Phase voltage in a system on which arm has 6 SM using linear control (a) and nonlinear control (b).

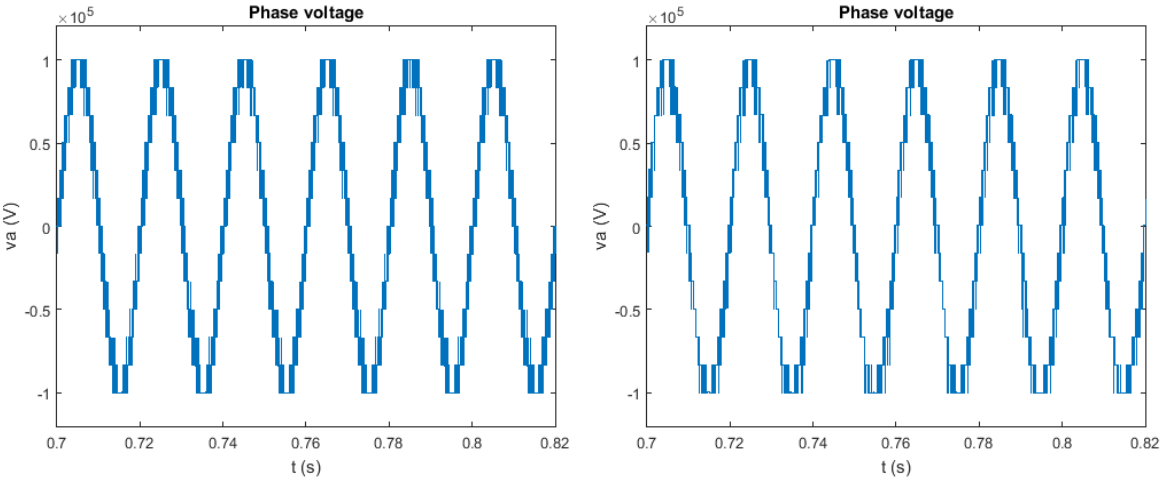

Figure 5.8: Phase voltage in a system on which arm has 12 SM using linear control (a) and nonlinear control (b).

5.4. Responsiveness of the controllers

As it was explained in chapter 4, to facilitate the design of the linear controllers it was used the Park and Concordia transformation in order to transform this three-phase system in an equivalent two-phase system. In the nonlinear approach there is no need for this transformation as the control system can be easily implemented. However, in order to establish the reference currents, it is useful to use dq coordinates.

Although the reference may be the same in dq components the results will be presented in dq components in the linear approach and abc for the nonlinear. Even though they are different they are equivalent.

In figure 5.9 it is presented the error of i_{dq} currents (being the error the difference between the reference values and the measured values $i_{dq\_ref} - i_{dq}$) in the 6 submodules system and 12 submodules for the linear control.

Figure 5.10 shows the error of the three phase currents for the nonlinear approach. In figure 5.11 it is visible the same base of thinking but only one phase being shown.

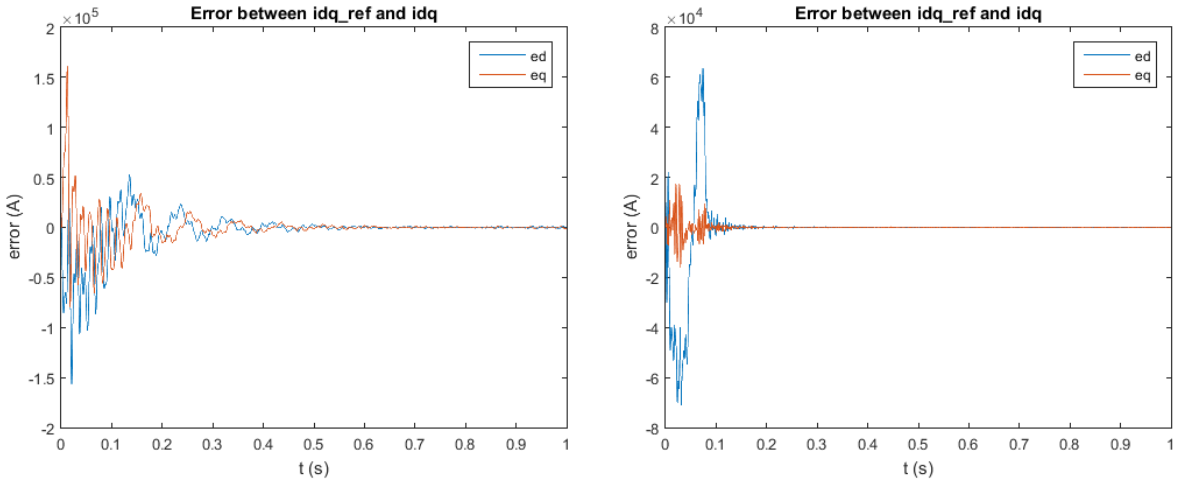

Figure 5.9: Error between direct and quadratic current and their reference using linear control for a system with 6 SM (a) and for 12 SM (b).

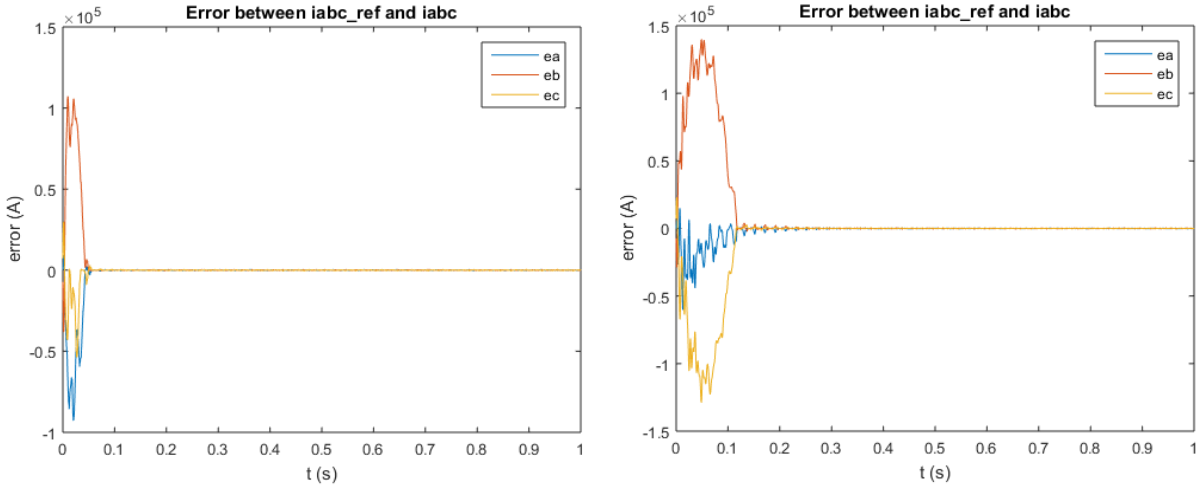

Figure 5.10:Error between three-phase currents and their reference using nonlinear control for a system with 6 SM (a) and for 12 SM (b).

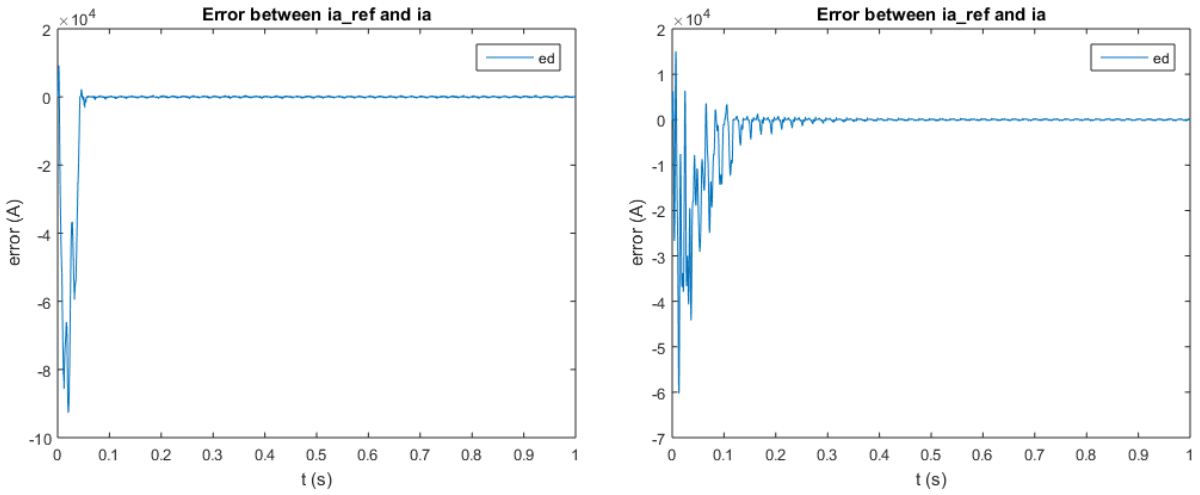

Figure 5.11:Error between current of one phase and their reference using linear control for a system with 6 SM (a) and for 12 SM (b).

In these results, three things can be noticed: when comparing the control approaches for the same number of submodules system, the nonlinear control is faster. For the 12-submodule system the difference is not as big as it was for the 6 submodule system. The other conclusion is that if more submodules are added to the system the control system is slower.

So in order to have the same level of responsiveness of the controllers with fewer submodules the controllers must be designed to be more robust.

5.5. Waveforms of the output current of the converter

Figures 5.12 and 5.13 show the AC currents waveforms. It can be seen that when the number of submodules increases, the waveforms will have a more sinusoidal shape. As predicted, when the submodules increase, the THD is lower and the waveforms resemble perfect sinusoids.

The other point of interest results from comparing the control approaches. The nonlinear control presents better results than the linear counterpart. That was expected as it is faster when adjusting to errors.

In figure 5.12 it is shown the output currents for the 6 SM system with the results obtained with the linear control being on the left and the results obtained with the nonlinear approach on the right. Figure 5.13 presents similar results for a 12-submodule system.

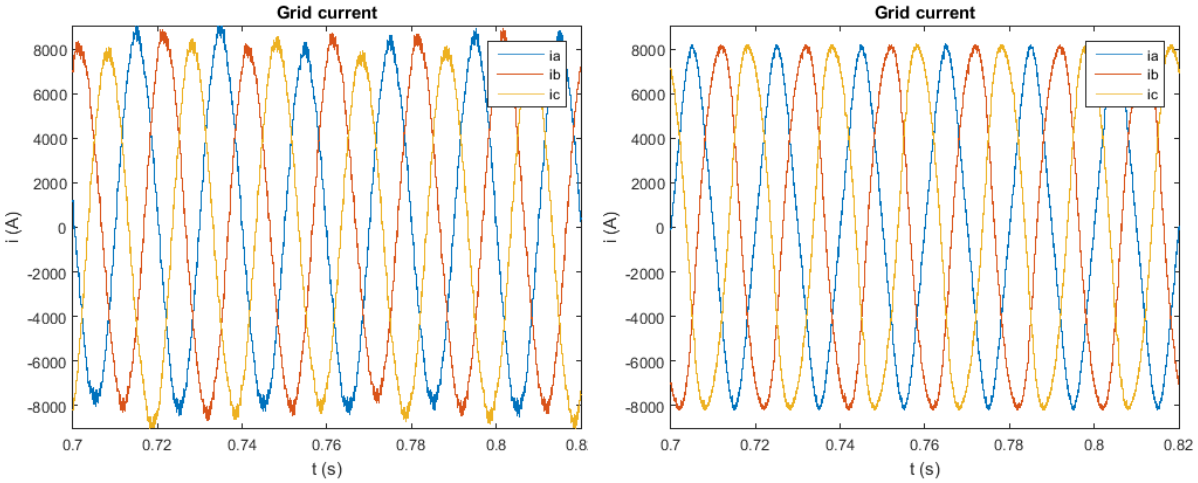

Figure 5.12: Output current for a system with 6 SM using (a) linear control and (b) nonlinear control.

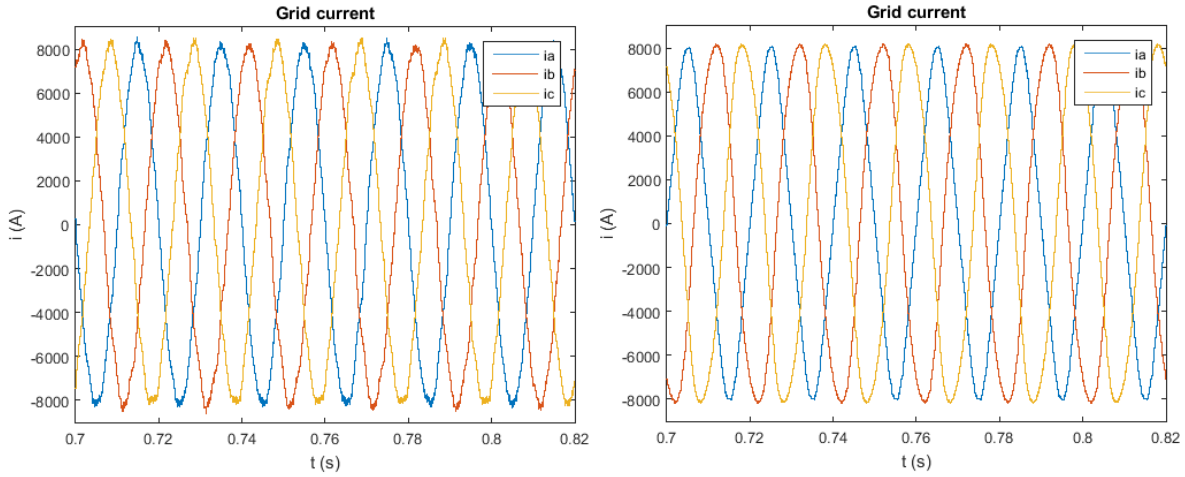

Figure 5.13: Output current for a system with 12 SM using (a) linear control and (b) nonlinear control.

5.6. Waveforms of the output voltage of the converter

In both systems the converter is connected to a balanced grid which voltage waveform is represented in figure 5.14.

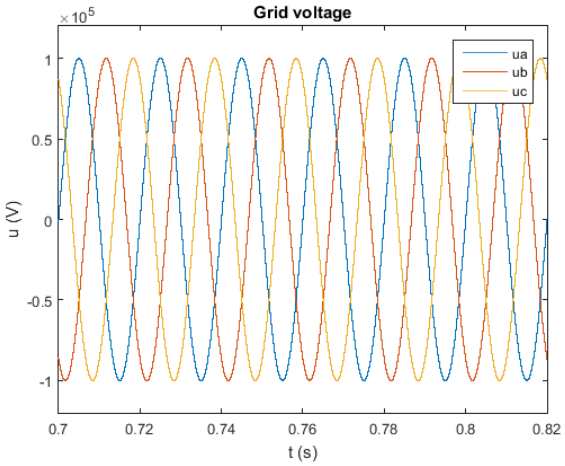

Figure 5.14: Grid voltage.

In the linear control there is a reference wave for modulation purposes. Fig. 5.15 represents that waveform for both examples.

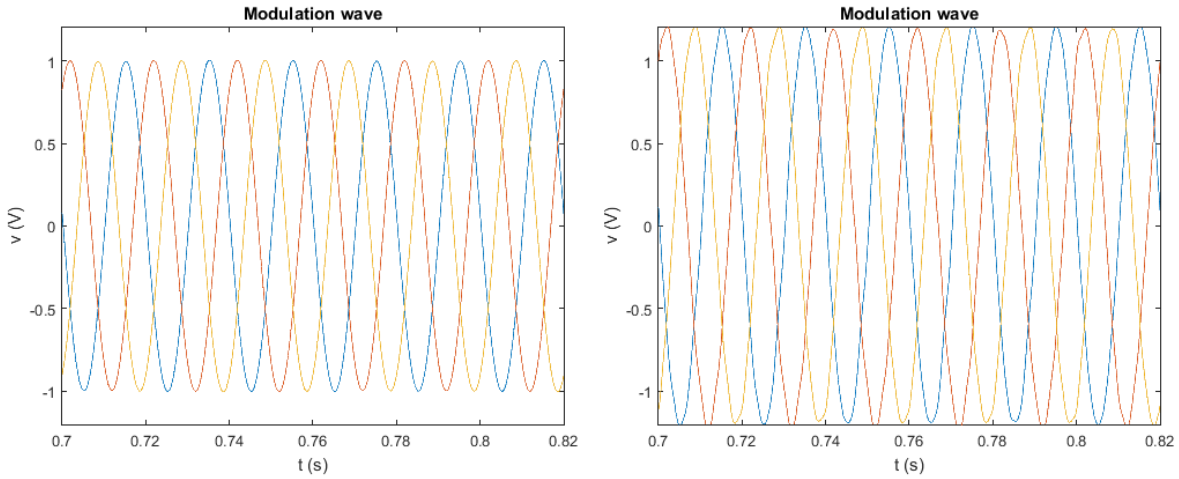

Figure 5.15: Reference wave for modulation purposes in the linear control for a system with 6 SM (a) and for 12 SM (b).

When analysing the waveforms of the output voltage of the converter the differences in both approaches can be noticed.

For the same system, i.e, systems that have the same number of submodules in each leg, it can be observed that the linear control presents better results in face of the nonlinear approach. That difference is lower when adding more submodules as it was the same when comparing the current waveforms. For the 12 SM system the difference is not as big.

Figures 5.16 and 5.17 show the three phase output voltages of the converter and only in one phase to facilitate the observation.

Increasing the number of SMs (Figures 5.18 and 5.19) has an immediate result, improving the waveforms. This was and expected result because if there are more submodules then there are more voltage levels in the arms, resulting in better output voltages in the converter.

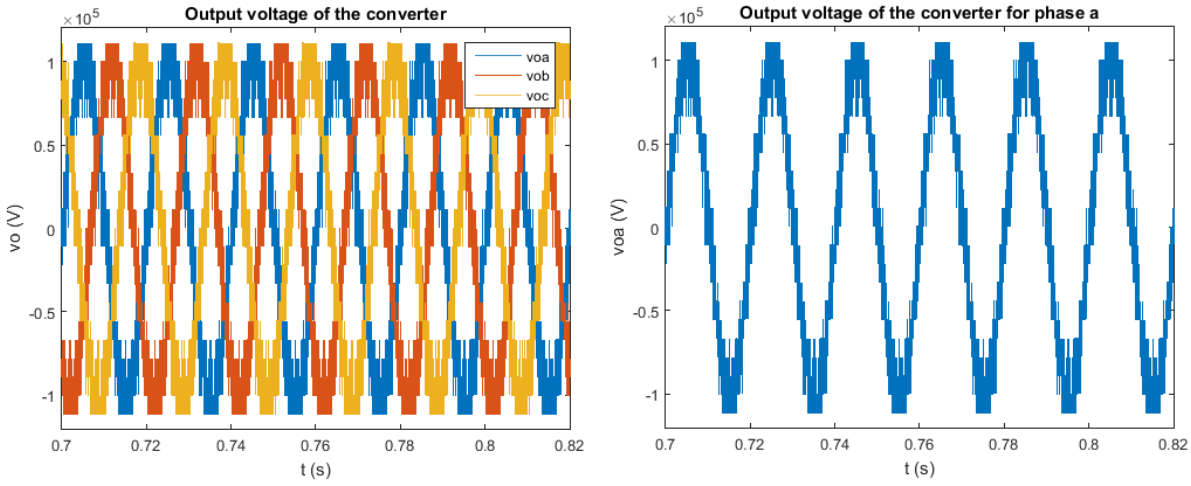

Figure 5.16: Three phase (a) and one phase output voltage (b) of the converter for a system with 6 SM with linear control.

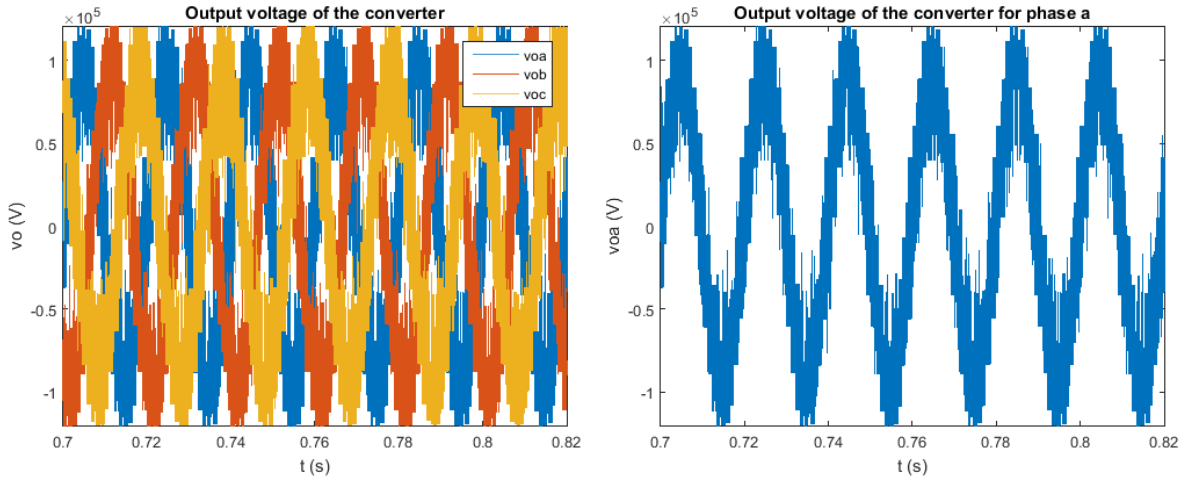

Figure 5.17: Three phase (a) and one phase output voltage (b) of the converter for a system with 6 SM with nonlinear control.

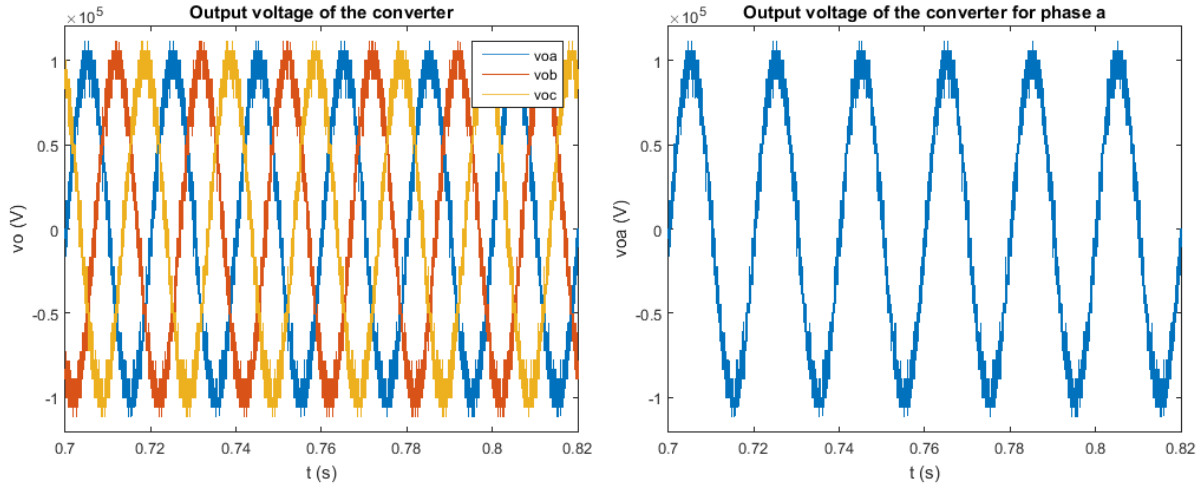

Figure 5.18:Three phase (a) and one phase output voltage (b) of the converter for a system with 12 SM with linear control.

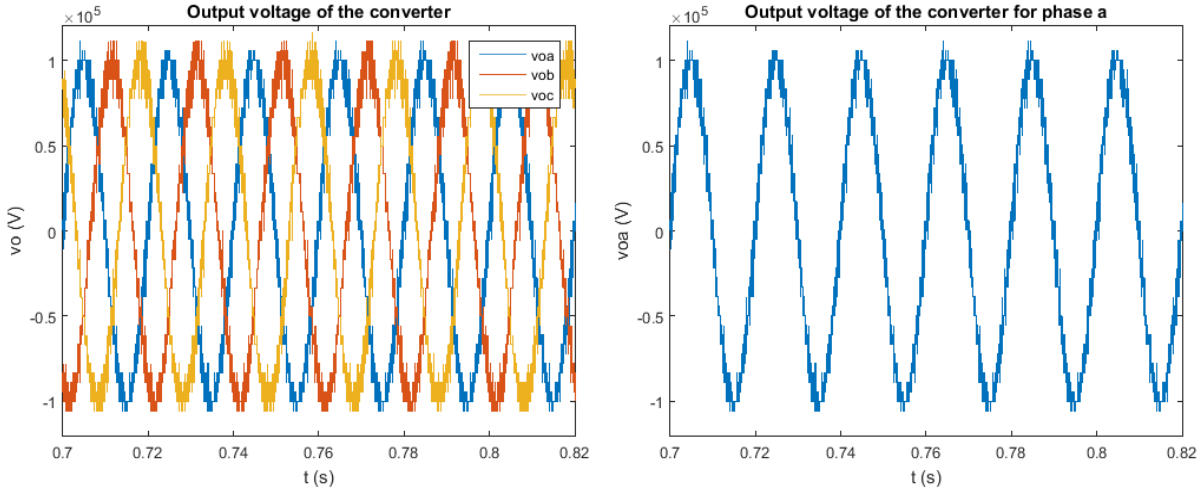

Figure 5.19: Three phase (a) and one phase output voltage (b) of the converter for a system with 12 SM with nonlinear control.

5.7. Voltage Sag and Overvoltage

The evaluation of the dynamic performance was made creating a voltage sag from *t*=0.3s to *t*=0.4s and an overvoltage from *t*=0.6s to *t*=0.7s. These power quality issues may appear in the grid and must be solved, since they can destroy or result in serious equipment damage. For the voltage sag it was considered a 10% decrease from the maximum voltage, and for the overvoltage, it was considered a 10% increase of the voltage.

In figure 5.20 it is shown the voltage sag and overvoltage, with the representation of the *d* component of the grid voltage.

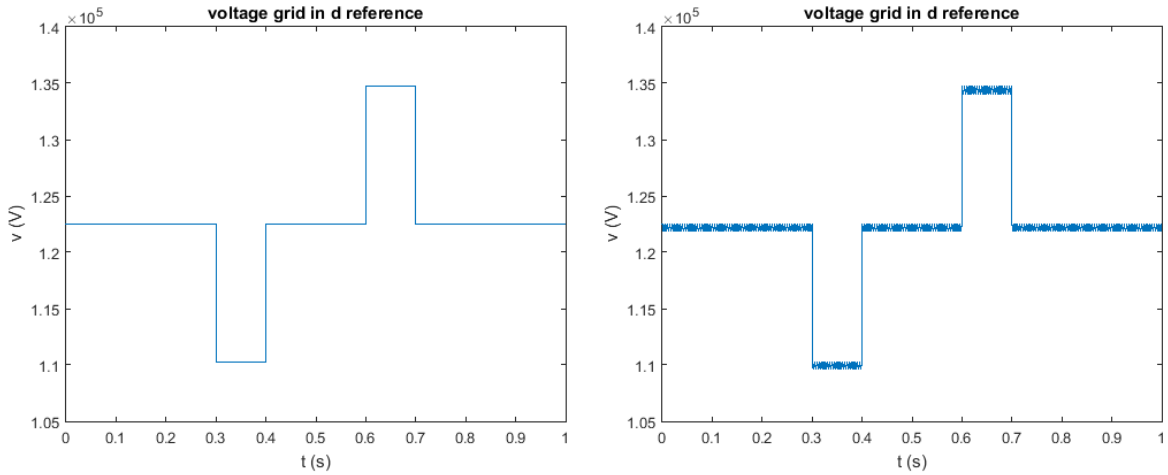

Figure 5.20: Voltage sag and overvoltage in d components and in the gird voltage with linear control (a) and nonlinear (b).

As stated in chapter 4, in the presence of a voltage sag there must be a reactive compensation, in this case, injection of reactive current. In other words, the reference of i_q must no longer be zero. In figure 5.21 and 5.22 there is a change in the reference current: for positive values in the presence of a voltage dip (a) and for negative values in an overvoltage situation (b). In the same figures it can be concluded that the i_q component of the current follows the reference with better results in the linear control (figure 5.21) than in the nonlinear control (figure 5.22).

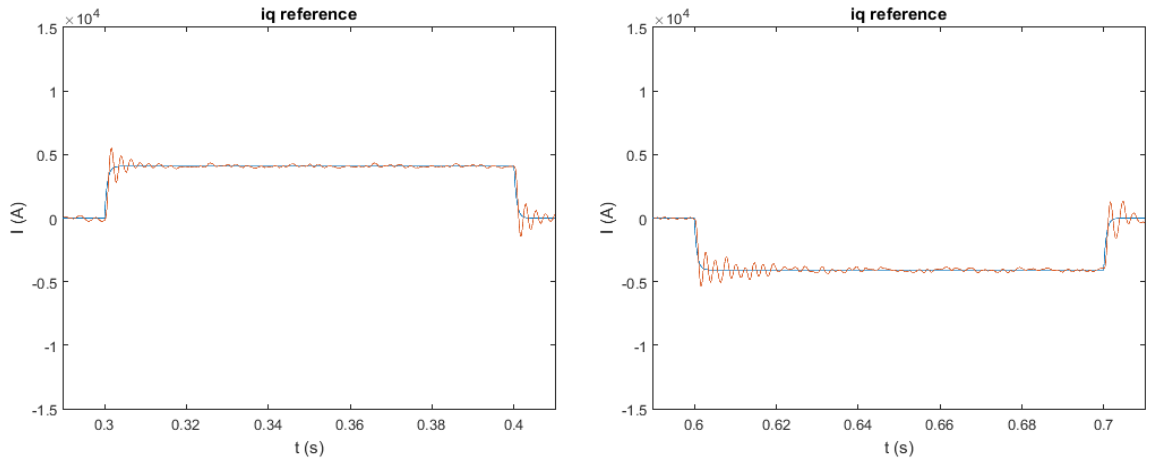

Figure 5.21: Current iq reference and iq in a voltage sag (a) and in a overvoltage (b) for the system with linear control.

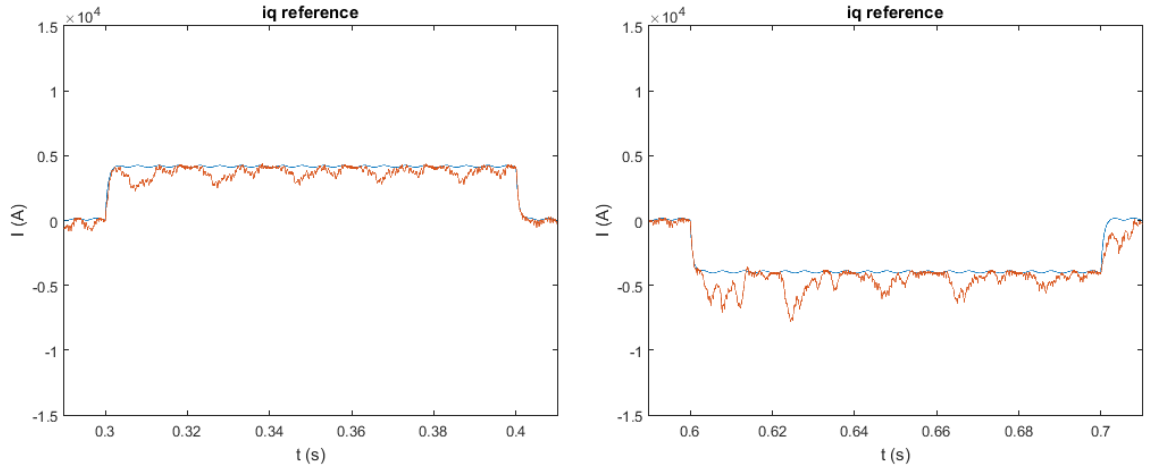

Figure 5.22: Current iq reference and iq in a voltage sag (a) and in a overvoltage (b) for the system with nonlinear control.

As mentioned in chapter 4, the voltage in PCC needs to be controlled. The objective is that even though there is a dip or overvoltage the voltage in the PCC does not change much from the nominal values. Figure 5.23 shows that for both controllers there is a small difference in the PCC voltage. However, this difference could be worse there was not any control system. Although both of them perform well, the linear control has better performance.

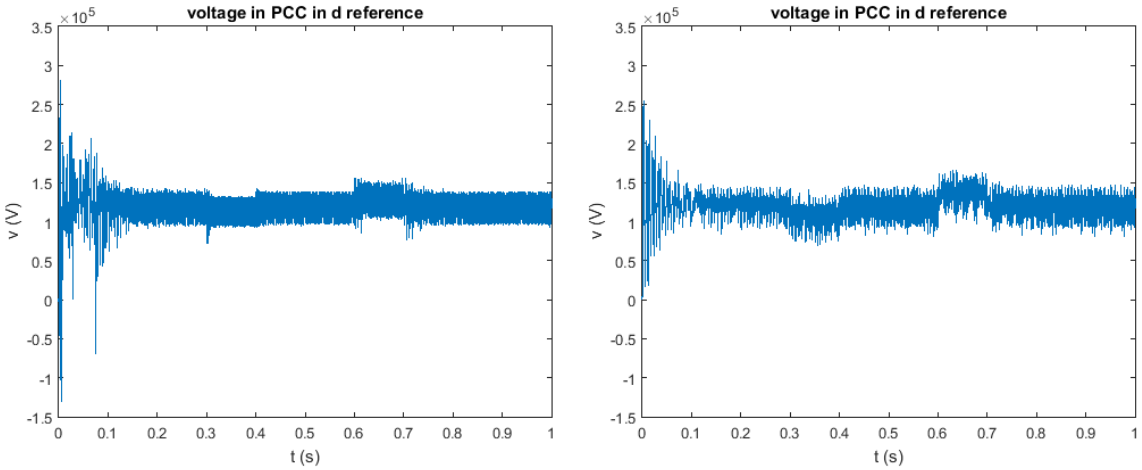

Figure 5.23: Voltage in the PCC in d reference with linear control (a) and nonlinear (b).

Figure 5.24 presents the voltage profile in the output of the converter (on the left for the system with linear control and on the right with nonlinear one) where it can be observed the voltage sag and the overvoltage.

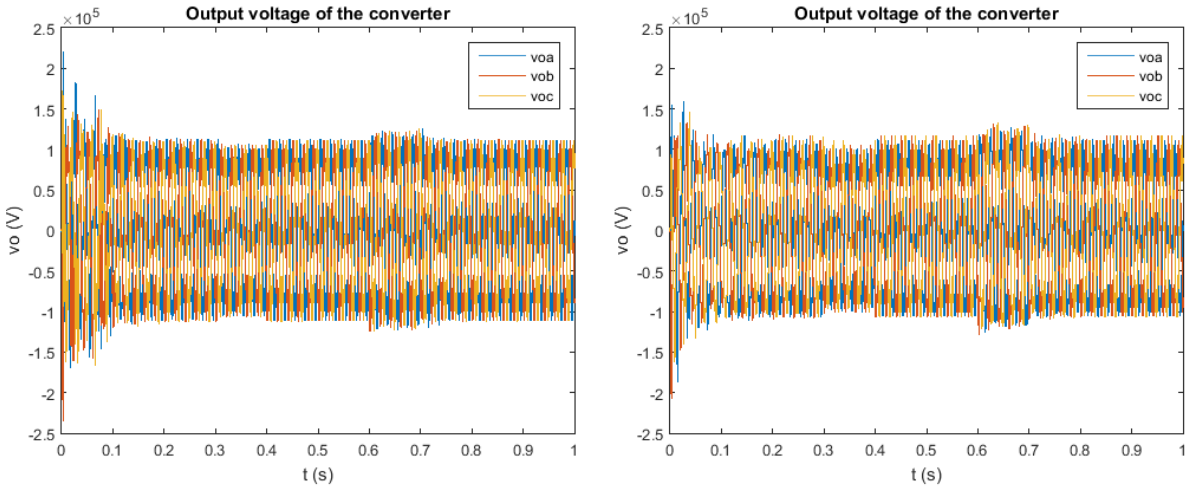

Figure 5.24: Output voltage of the converter during a voltage sag and overvoltage with linear control (a) and nonlinear (b).

In figures 5.25 to 5.27 it is observed the error, and both controllers perform better during voltage sag than in overvoltage. This can be explained by the lack or poor performance in controlling the DC voltage. However, it can be understood that when there is an increase of the error when an event happens followed by a decreasing of the error meaning the controller is functioning.

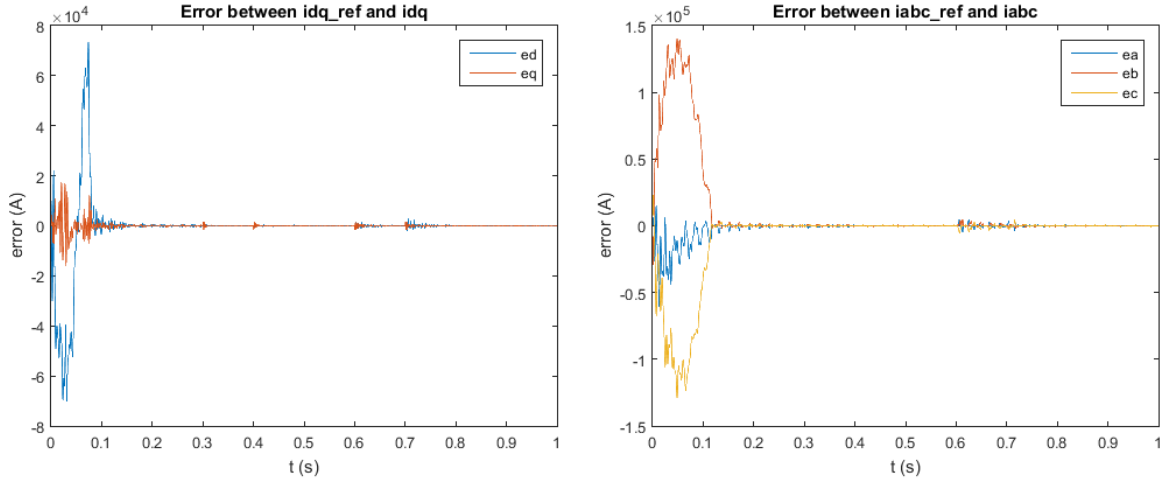

Figure 5.25: Error for the linear control (a) and nonlinear control (b) during a voltage sag and overvoltage.

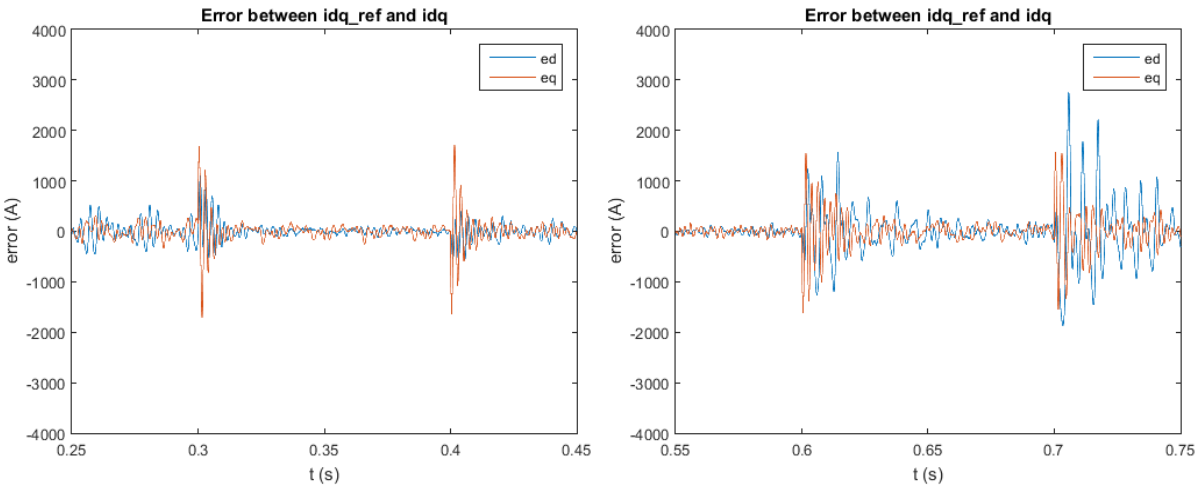

Figure 5.26: Error for the linear control system during voltage sag (a) and overvoltage (b).

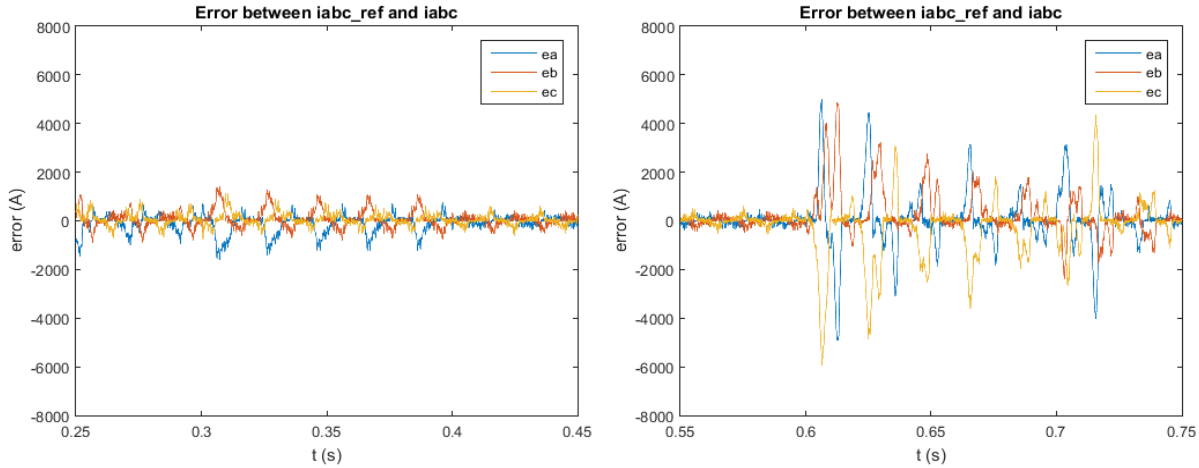

Figure 5.27: : Error for the nonlinear control system during voltage sag (a) and overvoltage (b).

5.8. Connection to a 60 Hz grid

One of the advantages of using these systems is allowing the connection of two AC grids operated at different frequencies (asynchronous connection). Until now the results were obtained for a converter connected to a 50 Hz grid. The following results are from the other terminal of the HVDC system connected to a 60 Hz grid. The results are presented in a similar way: on the left are the results obtained with the linear approach and on the right are the results obtained with the nonlinear approach.

In analysing the results it can be seen that the controllers for a 60 Hz grid, work with the same level of performance as the ones designed to the 50 Hz grid.

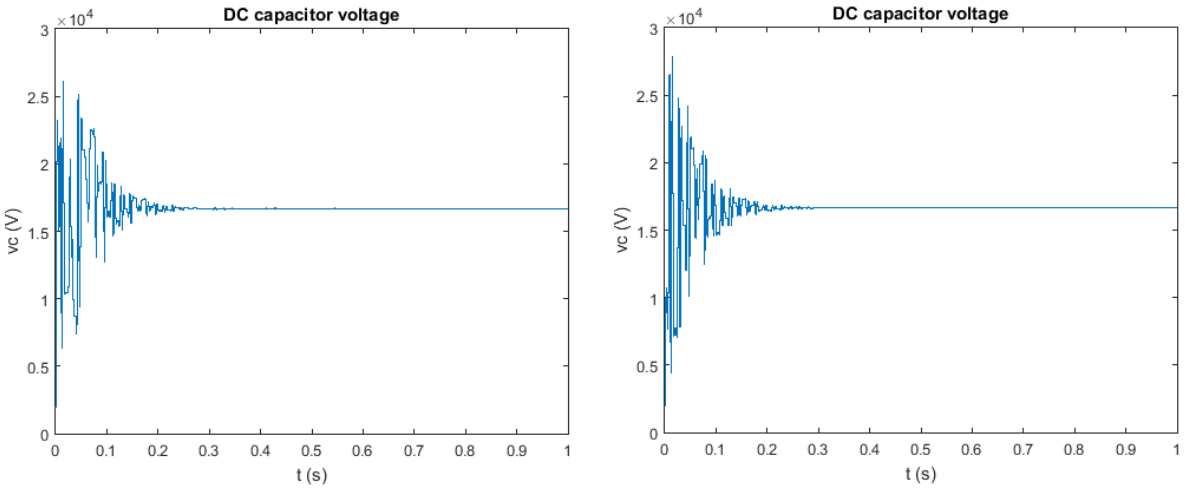

Figure 5.28: DC capacitor voltage in the linear control system (a) and nonlinear (b) for the connection to the 60 Hz grid.

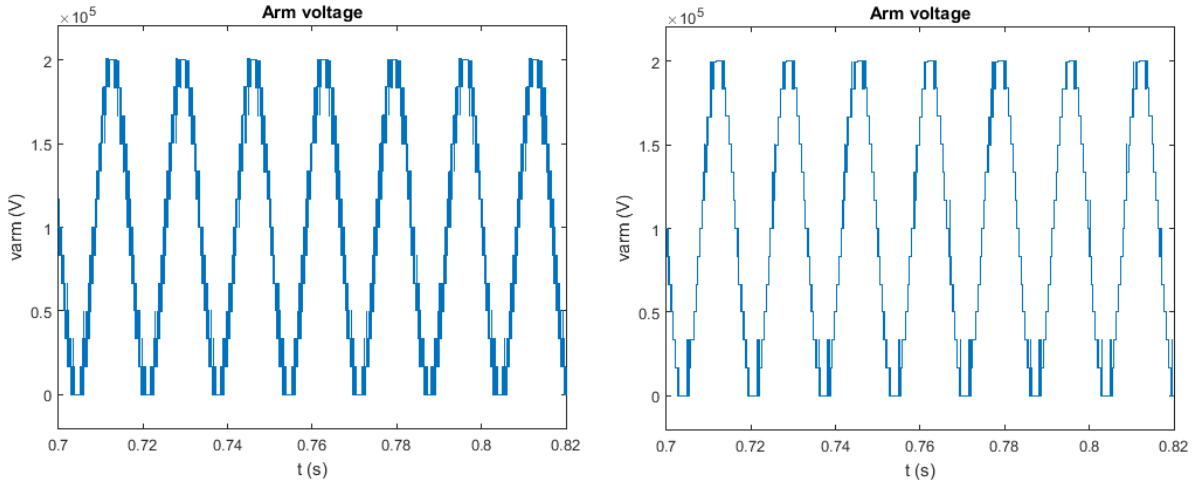

Figure 5.29: Arm voltage in the linear control system (a) and nonlinear (b) for the connection to the 60 Hz grid.

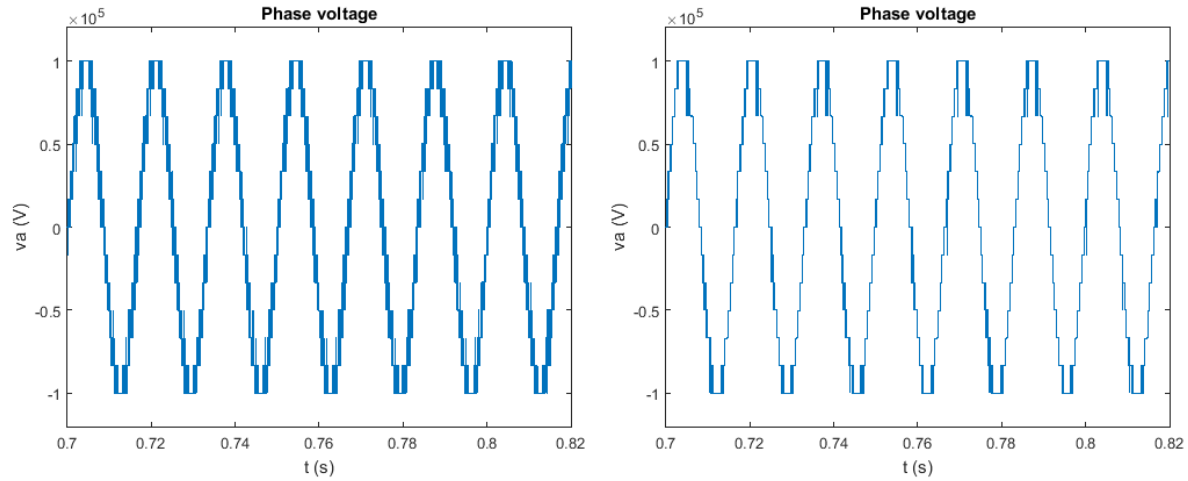

Figure 5.30: Phase voltage in the linear control system (a) and nonlinear (b) for the connection to the 60 Hz grid.

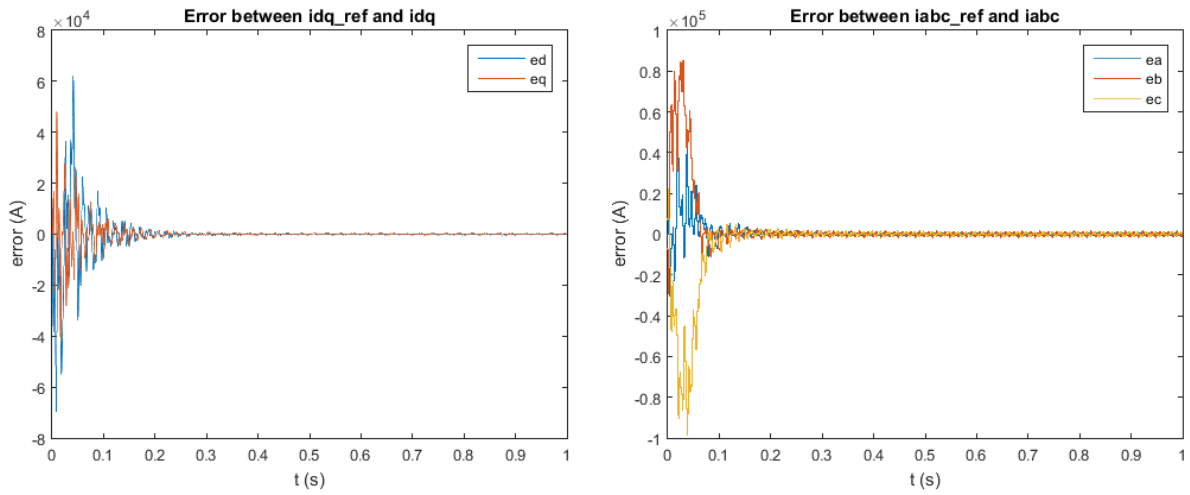

Figure 5.31: Error for the currents in the linear control system (a) and nonlinear (b) for the connection to the 60 Hz grid.

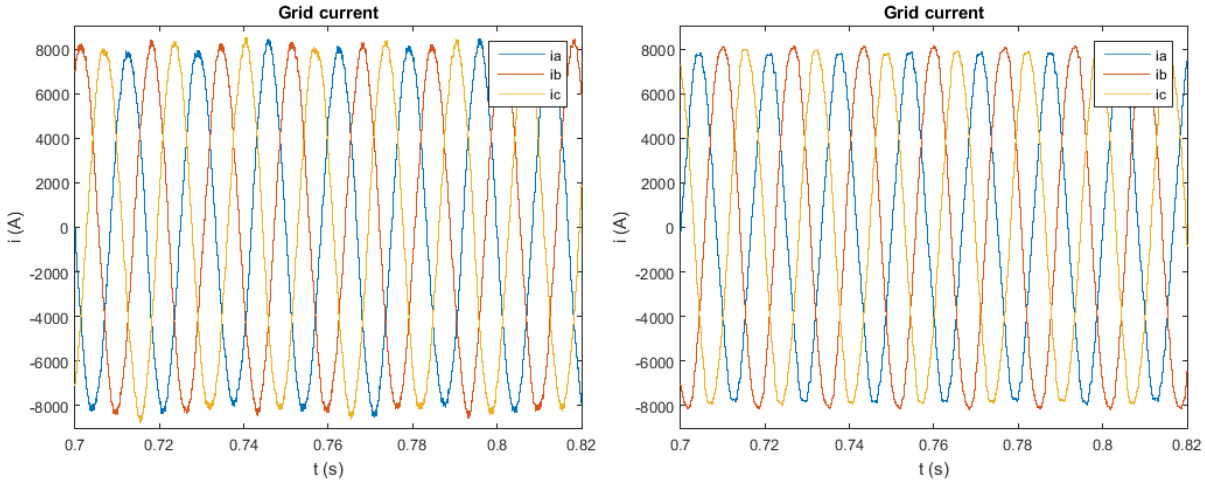

Figure 5.32: Grid currents in the linear control system (a) and nonlinear (b) for the connection to the 60 Hz grid.

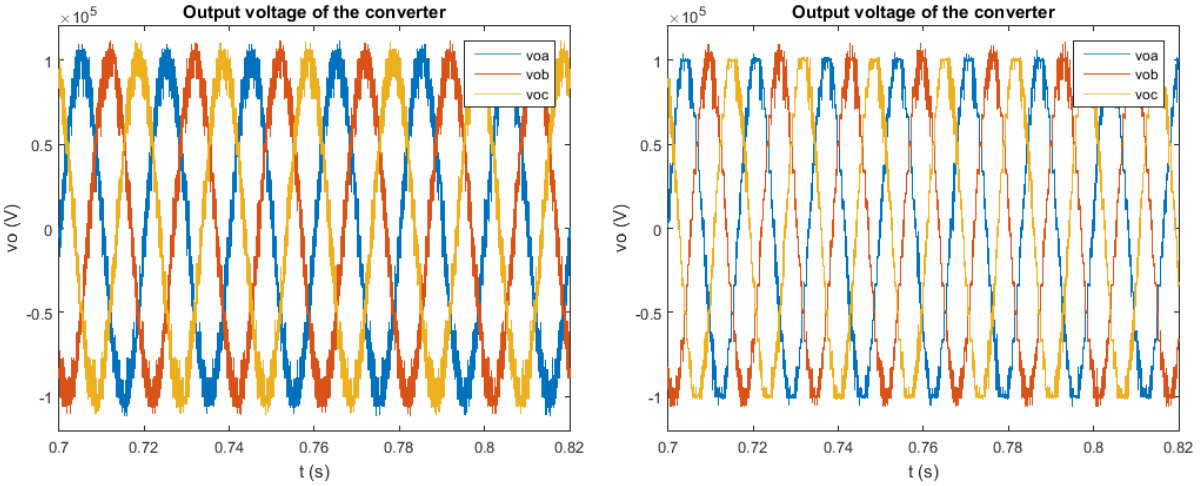

Figure 5.33: Output voltage of the converter in the linear control system (a) and nonlinear (b) for the connection to the 60 Hz grid.

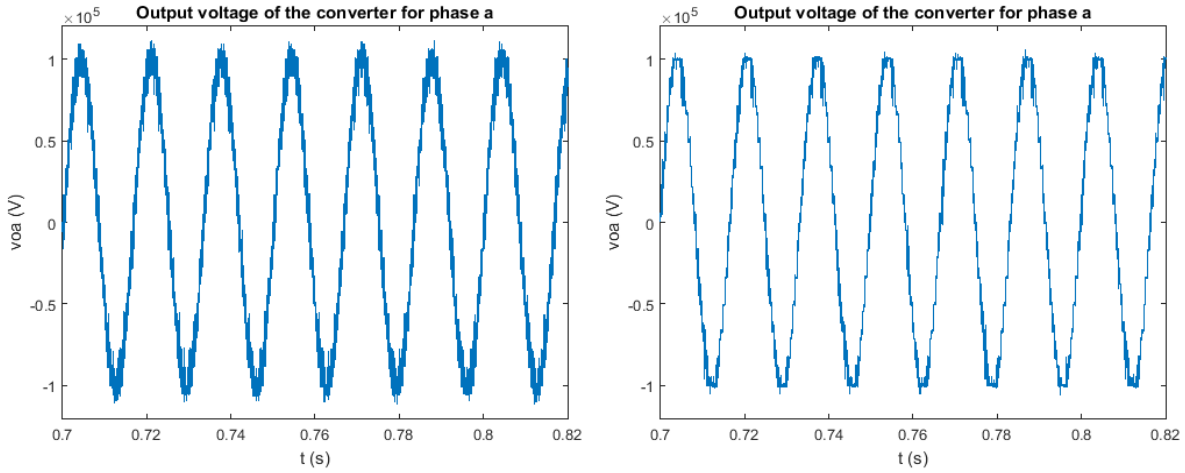

Figure 5.34: Output voltage of the converter in phase a for the linear control system (a) and for the nonlinear (b) for the connection to the 60 Hz grid.

5.9. Results with DC voltage control

In a real system it is necessary to control the DC voltage, as the limits of the system may be reached and it is necessary to increase the DC voltage, or during other power disturbances.

One example is when an overvoltage event happens. If the overvoltage reaches values that surpass the limits, it becomes necessary that the difference of the nominal voltage to the overvoltage in percentage must be the same in the DC voltage.

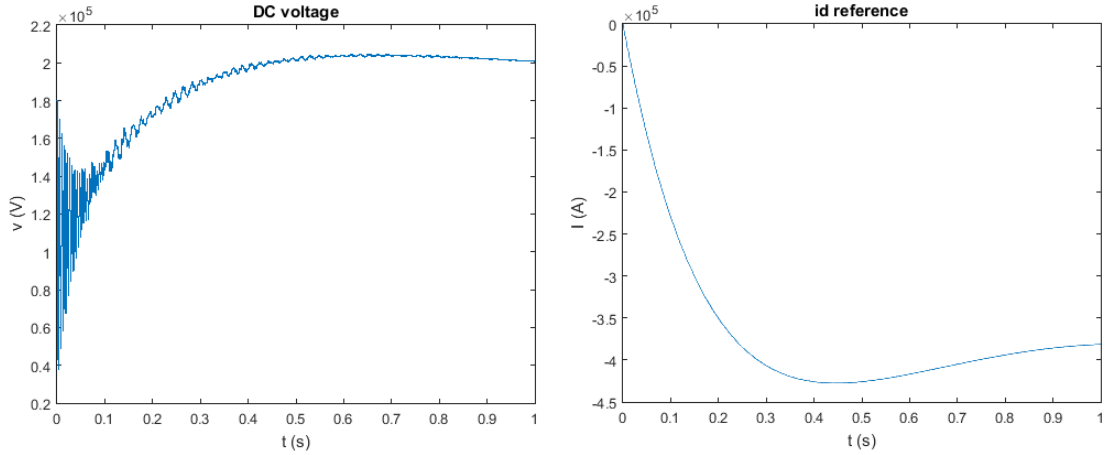

Figure 5.35: DC voltage (a) and id reference (b).

In this system the objective is for the DC voltage to have 200 kV. As it can be seen in figure 5.35 the DC voltage reaches the desired value. In the same figure on the right side it can be observed that i_{dref} changes through the time. As explained in section 4.5, in order to control the DC voltage, i_{dref} must be continuously adjusted.

The DC capacitors voltage changes naturally with the DC voltage reaching the result obtained previously in section 5.2. In the waveforms of the arm voltage, it can be seen the same number of levels but during the process there is a saturation in the waveform which indicates that the system reached its limits.

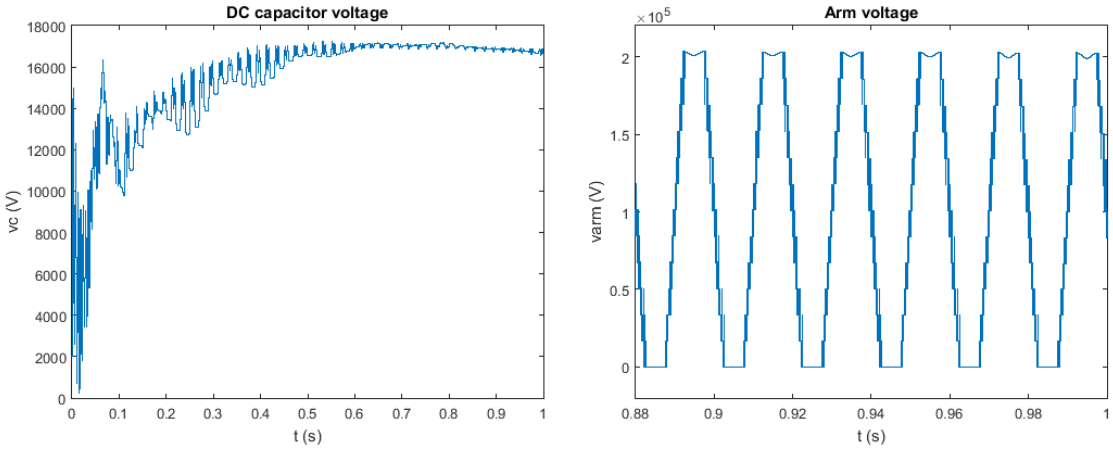

Figure 5.36: DC capacitor voltage (a) and arm voltage (b) during the DC voltage control process.

The output voltage of the converter presents similar results as the previously discussed. This analysis leads to the conclusion that the control presents good results during the process.

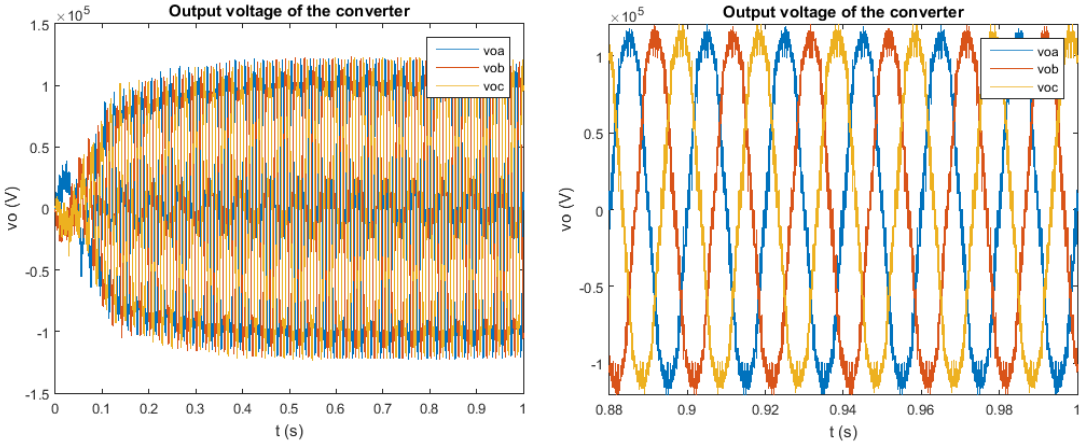

Figure 5.37: Output voltage of the converter during DC voltage control.

6. Conclusions

In this thesis a linear and nonlinear controller for an HVDC system were designed and evaluated. It was assessed the performance of both control approaches taking into consideration the evaluation of the error of the currents and the waveforms of the voltages.

In the beginning of this work, all the possible HVDC topologies that exist and that were implemented throughout the years were analysed, as well as their advantages and disadvantages. Also, all the possible configurations of HVDC systems and the technologies that they required were presented.

Considering all the advantages/disadvantages of the HVDC topologies, in this work it was adopted a modular multilevel converter.

Our case study was an MMC-HVDC system connected to two grids, one operated at 50 Hz and other operated at 60Hz. This converter has 24 submodules in each leg: 12 in the upper and down arm. Even though the real systems have more than 200 submodules, due to computation restrictions, only 12 submodules were chosen in each arm. The voltage in the DC link is 200kV and peak value in the AC side is 100kV.

All the filtering components as the ones connected to the grid and the capacitors in the submodules, as well as the semiconductors were sized.

Two control methods for the current were used: a linear control approach and a nonlinear control.

For the linear control, the gains for the PI controller were sized and the modulation process chosen was the Phase Shift Carrier Pulse Width Modulation (PSC-PWM), in order to obtain the desired output voltage. The nonlinear current control algorithm was implemented and the goal was to compare the performance with the linear controller.

A balance algorithm for the capacitors was implemented in both control methods, because in these converters it is necessary to balance the voltage of these capacitors due to the existence of circulating currents.

A controller to mitigate voltage sags and overvoltages was also developed as required in systems connected to grids. It was also implemented a control for the DC voltage, as there is always fluctuation on it.

After the design, simulation results for both methods were obtained and compared. Additionally an evaluation of the effect of having more/less submodules was performed as well.

It was observed that the nonlinear control has a faster response to a disturbance than the linear one. Both methods present good results in the control of the current with better results in the nonlinear control. In the voltages analysis it could be observed that both performed well with the linear control having better results when there are fewer SMs.

It was possible to corroborate that the method implemented for balancing the capacitors was very satisfactory in both control methods.

It was observed that the more submodules the system has the better results in the AC waveforms, however the response of the control being slower with the increase of submodules. So, for different systems with different submodules the design of controllers should be different as well.

The results when having voltage sags or overvoltage events were also positive, even though in the overvoltage case, the results were not as good when comparing to the voltage sag. This was result of poor performance of the DC control that even though reached the objective, it was a slow controller.

Finally the same analysis was made to the connection to the 60 Hz grid which showed that the design of the controllers works for both grids.

The results of the simulation in Matlab/Simulink environment show that this converter and the designed controllers can be a good solution for HVDC systems.

Final Remarks

There are subjects that would be interesting to investigate, simulate or implement.

One of the main topics that would be interesting and to implement as well would be the control of circulating currents that exist in this converter. It is one of the challenges of these converters and it would be interesting to design and implement strategies in the converters.

It would be interesting to compare other techniques for balancing the capacitors, other topologies and to add even more submodules for this converter.

Finally, in some cases, our grid can be unbalanced opposing to the one in this dissertation. How would the system and control react to disturbances to unbalanced grid and what changes it would be needed to implement can be an interesting work to investigate in future works.

References

[ABB, 2014] ABB, Brochure: Introduction HVDC, 2014.

[Ackermann, 2005] T. Ackermann, “Wind power in power systems”, pp 287-290, 2005. John Wiley & Sons, Ltd.

[Ahmad, 2014] Y. Ahmad, “STATCOM as a Solution to Improve the Voltage Profile of a Power Grid”, MSc Thesis, IST, 2014.

[Ahmad, et al, 2018] Y. Ahmad, S. Pinto, “Cascade Multilevel STATCOM as a solution to improve the voltage profile of a power grid”, IEEE International Young Engineers Forum (YEF-ECE), 2018.

[Alexandre, et al, 2016] R. Alexandre, S. Pinto, J. Santana, “Energy storage system for grid connection and Island operation”, IEEE Inter. Smart Cities Conf. (ISC2), Trento, Italy, September 2016.

[Angquist, 2009] A. Antonopoulos, L. Angquist, H. Nee, “On Dynamics and Voltage Control of the Modular Multilevel Converter”, 13th European Conference on Power Electronics and Applications, 2009.

[Bahrman, 2008] M. Bahrman, “HVDC Transmission Overview”, 2008 IEEE/PES Transmission and Distribution Conference and Exposition

[Bang, 2014] Bang NLH, Nho NV, Tam NKT, Dung NM, “A phase shifted PWM technique for common-mode voltage reduction in five level H-bridge cascaded inverter”, International conference and utility exhibition on green energy for sustainable development (ICUE), 2014.

[Black, 1983] R. Black, “The History of Electric Wires and Cables”, Peter Perigrinus, London, ISBN 0-86341-001-4 pages 94–96, 1983

[Beddard, et al, 2015] A. Beddard and M. Barnes, “Modelling of MMC-HVDC Systems – An Overview“, 12th Deep Sea Offshore Wind R&D Conference, EERA DeepWind, 2015.

[Bo, 2014] H. Bo, K. Kurachi, S. Gaosheng, “A suitable 4.5kV HVIGBT for VSC-HVDC”, PCIM Europe 2014, 20-22 May 2014, Nuremberg, Germany.

[Chai, et al, 2013] R. Chai, B. Zhang, Z. Hao, T. Zheng, S. Ma, D. Chen. “A Low Switching Frequency Voltage Balancing Strategy of Modular Multilevel Converter”, IEEE International Conference of IEEE Region 10 (TENCON 2013), 2013.

[Cory, et al, 1965] B. Cory, C. Adamson, J. Ainsworth, L. Freris, B. Funke, L. Harris, J. Sykes, “High voltage direct current converters and systems”, Macdonald & Co. (publishers) Ltd, 1965, chapter 3.

[Czisch, 2009] G. Czisch, “Low Cost but Totally Renewable Electricity Supply for a Huge Supply Area – a European/Trans-European Example”, 2009.

[Davies et al, 2008] M. Davies, M. Dommaschk, J. Dorn, J. Lang, D. Retzmann, D. Soerangr, “HVDC PLUS-Basics and principle of operation”, SIEMENS 2008.

[Dekka, et al, 2017] A. Dekka, B. Wu, R. Fuentes, M. Perez, N. Zargari, “Evolution of Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters”, IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 4, December 2017.

[EU, 2017] “Towards a sustainable and integrated Europe. Report of the Commission Expert Group on electricity interconnection targets.”, November 2017.

[Ghoshal, et al, 2010] A. Ghoshal, V. John, “Anti-windup Schemes for Proportional Integral and Proportional Resonant Controller”, National power electronic conference, 2010.

[Gonzalez, et al, 2012] F. Gonzalez-Longatt, J. Roldan, C. A. Charalambous, “Power Flow Solution on Multi-Terminal HVDC Systems: Supergrid Case”, European Association for the Development of Renewable Energies, Environment and Power Quality (EA4EPQ), International Conference on Renewable Energies and Power Quality (ICREPQ’12), March 2012.

[Hasan, 2017] N. Hasana, N. Rosmina, D. Osmana, A. Musta’amal, “Reviews on multilevel converter and modulation techniques“, Renewable and Sustainable Energy Reviews, vol. 80, pp. 163-174, Dec. 2017.

[Jacobson, et al, 2010] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, and T. Jonsson, "VSC-HVDC Transmission with Cascaded Two-Level Converters," Cigre Paris Conference, 2010.

[Jelani, et al, 2011] N. Jelani, M. Molinas, “Stability investigation of control system for power electronic converter acting as load interface in AC distribution system”, IEEE International Symposium on Industrial Electronics 2011.

[Jovcic, et al, 2017] D. Jovcic, W. Lin, S. Nguefeu, H. Saad, “Full Bridge MMC Converter Controller for HVDC Operation in Normal and DC Fault Conditions”, 19th International Symposium on power electronics, October 19-21, 2017, Novi Sad, Serbia.

[Lesnicar, et al, 2003] A. Lesnicar, R. Marquardt, “An innovative modular multilevel converter topology suitable for a wide power range”, Proceeding of Power Tech Conference, 2003.

[Long, 2019] W. Long, “Evolution of HVDC links mercury-arc valves, thyristors, and more”, IEEE power & energy magazine may/June 2019.

[Kalle, et al, 2015] K. Ilves, L. Harnefors, St. Norrga, H. Neec, “Predictive Sorting Algorithm for Modular Multilevel Converters Minimizing the Spread in the Submodule Capacitor Voltages”, IEEE Transactions on Power Electronics, vol. 30, Issue: 1, Jan. 2015.

[Kharade, et al, 2017] J. Kharade N. Savagave, “A Review of HVDC Converter Topologies“, International Journal of Innovative Research in Science, Engineering and Technology, Vol. 6, Issue 2, February 2017.

[Li, 2016] Y. Li, Y. Wang, B. Li, “Generalized Theory of Phase-Shifted Carrier PWM for Cascaded H-Bridge Converters and Modular Multilevel Converters”, IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, Issue: 2, June 2016.

[Manohart, et al, 2011] P. Manohart, V. Kelamane, D. Kaushik, W. Ahmed, “Improved Controls for LCC-VSC Hybrid HVDC System”, International conference on Circuits, Controls and Communications (CCUBE), 2013.

[Martinez, et al, 2015] F. Martinez-Rodrigo, S. Pablo, L. Lucas, “Current control of a modular multilevel converter for HVDC applications”, Renew. Energy, Elsevier, vol. 83, pp. 318 to 331, 2015.

[Merlin, et al, 2017] M. Merlin, T. Green, P. Mitcheson, D. Trainer, R. Critchley, W. Crookes, F. Hassan, “The Alternate Arm Converter: A New Hybrid Multilevel Converter With DC-Fault Blocking Capability”, IEEE Trans. Power Del., vol. 29, no. 1, pp. 310-317, Feb. 2014.

[Okba, et al, 2012] M. Okba, M. Saied, M. Mostafa, T. Abdel-Moneim, “High Voltage Direct Current Transmission: A Review, Part I”, 2012 IEEE Energytech, 2012.

[Oni, 2016] O. Oni,I. Davidson, K. Mbangula, ”A Review of LCC-HVDC and VSC-HVDC Technologies and Applications”, 2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC).

[Ramirez, et al, 2017] D. Ramirez, F. Martinez-Rodrigo, S. Pablo, L. Lucas, “Assessment of a nonlinear current control technique applied to MMC-HVDC during grid disturbances”, Renewable Energy, vol. 101, pp. 945-963, 2017.

[Sapkota, 2017] R. Sapkota, S. Kolluri, J. Adhikari, S. Panda, “MMC based Multi-terminal HVDC Subsea Power Transmission System with the Integration of Offshore Renewable Energy”, 2017 IEEE Innovative Smart Grid Technologies - Asia (ISGT-Asia).

[Sensarma, et al, 2001] P. Sensarma, K. Padiyar, V. Ramanarayanan, “Analysis and performance evaluation of a distribution STATCOM for compensating voltage fluctuations”, IEEE Trans. Power Deliv., vol. 16, no. 2, pp. 259-264, April 2001.

[Siemens AG, 2016] Siemens AG, “HVDC PLUS – the decisive step ahead Stabilized power flows improve transmission grid performance”, 2016.

[Silva, 2013] J. Silva, “Electrónica Industrial”, Fundação Calouste Gulbenkian (2nd ed), 2013.

[Silva, et al, 2011] J. F. Silva; S. F. Pinto, “Advanced Control of Switching Power Converters,” Cap. 36, pp 1037-1113, Power Electronics Handbook 3rd edition, Editor M. H. Rashid, Burlington: Butterworth-Heinemann, ELSEVIER, ISBN: 978-0-12-382036-5, 2011.

[Silva, et al, 2012] J. Silva, S. Pinto, J. Santana, “Conversores Comutados para Energias Renováveis”, Instituto Superior Técnico, Folhas da Disciplina, 2013.

[Song, et al, 2013] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, L. Li, “Protection of nonpermanent faults on DC overhead lines in MMC-based HVDC systems”, IEEE Transactions on Power Delivery, vol. 28, pp. 483-90, 2013.

[Teodorescu, et al, 2011] R. Teodorescu, M. Liserre, P. Rodriguez, “Grid Converters for Photovoltaic and Wind Power Systems”, Wiley 2011.

[Tiku, 2014] D. Tiku,” DC power transmission mercury-arc to thyristor HVDC valves”, IEEE power & energy magazine, March/April 2014.

[Zhang, 2002] L. Zhang, L. Dofnas, “A novel method to mitigate commutation failures in HVDC systems”, IEEE International Conference in Power System Technology, PowerCon 2002, vol. 1, pp. 51–56, 2002.

[Zhang, et al, 2017] L. Zhang, Y. Zou, J. Yu, J. Qin, V. Vittal, G. Karady, D. Shi, Z. Wang, “Modelling, Control, and Protection of Modular Multilevel Converter-based Multi-terminal HVDC Systems: A Review”, IEEE, CSEE journal of power and energy systems, vol. 3, no. 4, December 2017.

[Zhang, et al, 2017a] L. Zhang, J. Qin, D. Shi, Z. Wang, “Efficient Modelling of Hybrid MMCs for HVDC Systems”, 2017 IEEE Energy Conversion Congress and Exposition (ECCE).

[Zhao, et al, 2014] C. Zhao, M. Lu, X. Huang, P. Qiu, “A Novel Reduced Switching-Frequency Voltage-Balancing Strategy for Modular Multilevel Converters”, 2014 IEEE PES General Meeting, Conference & Exposition, 2014.