MMC-HVDC System: Design and Assessment

Miguel Saldanha

DEEC, Instituto Superior Técnico,
Universidade de Lisboa,
Lisboa, Portugal,
miguel.saldanha@tecnico.ulisboa.pt

Sónia Ferreira Pinto
INESC-ID Lisboa
DEEC, Instituto Superior Técnico,
Universidade de Lisboa,
Lisboa, Portugal,
soniafp@tecnico.ulisboa.pt

***Abstract*— The main aim of this paper is to design controllers and assess the response of a High Voltage Direct Current (HVDC) system. The focus of this work is to design linear and nonlinear controllers for the AC currents and to compare the obtained results. An HVDC system is constituted by two AC/DC power electronic conversion systems connected by a DC cable. In this work, each converter is connected to an AC grid, one being operated at 50 Hz and the other at 60 Hz. Modular multilevel converters (MMC) with 24 submodules (SM) in each leg of the converter (12 in the upper arm and 12 in the lower arm) were used for each terminal of the HVDC system. The voltage in the DC link is 200kV and the line to line voltages in the AC side are 100kV.For the linear control approach, it is used a Phase Shift Carrier Pulse Width Modulation (PSC-PWM) and Proportional-Integral (PI) controllers. For the nonlinear controllers, a sliding mode control approach is used. In both cases a balancing control algorithm for the capacitors voltages in the submodules is developed. The system is simulated in Matlab/Simulink and the obtained results show that nonlinear current controllers present better results than the linear controllers. Both present good performance in the output voltage control of the converters. The DC voltage control and the DC capacitors voltage balancing is successfully guaranteed as well as the mitigation of voltage sag or overvoltage events in the grid.**

Keywords*— *High Voltage Direct Current (HVDC), Modular Multilevel Converter (MMC), Submodule (SM), Phase Shifter Carrier Pulse Width Modulation (PSC-PWM), Nonlinear current control (NLCC).

I. INTRODUCTION

One of the greatest challenges of the 21st century is to prevent climate change and its devastating effects. This awareness made governments to act and start creating incentives to promote the production of electricity through renewable energies. In the last few years the grid integration of renewable energies as wind, solar, or hydro has been steadily growing. However, these sources of energy bring challenges to fulfil the demands of the consumers. This problem results in the requirement for additional energy storage capabilities, either as hydro pump, when possible, or using large capacity flywheel energy systems or battery-based energy storage systems. These technologies have significantly evolved in the last few years but there is still a long way to go.

High Voltage Direct Current (HVDC) transmission systems can be a good solution for this latter problem. In comparison with typical alternate current (AC) transmission systems, HVDC can transport more power over longer distances because only two cables are required, thus reducing the losses and the cost. However, the biggest advantage is the absence of reactive power absorption in the lines, and the minimization of losses in the cable capacitances [1], [2].

The European Union (EU) wants to improve the interconnection between the countries to upgrade the security of electricity supply, to integrate more renewable energy sources and to have a more integrated energy market. Reliable connection with the EU countries reduces the risk of blackouts and reduces the need to build more power plants [3], allowing the decommissioning of nuclear power plants. HVDC systems helped and will help to reach current and more ambitious goals. like the Baixas-Santa Llogaia interconnection HVDC transmission link between France and Spain (2015) which doubled the interconnection capacity between the two countries [2].

II. MMC-HVDC SYSTEM

The MMC-HVDC system proposed is a system like the one in figure 1 that connects two grids: one at 50 Hz and one at 60 Hz by a cable of 100km.

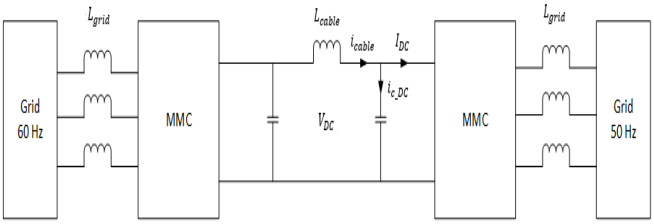

Fig. 1. MMC-HVDC scheme under analysis

III. MMC

The structure of a MMC is shown in figure 2. As we seen before it consists in three legs which one of them represents one phase of the system.

Each leg has two arm converters (ARM) which one of them have submodules connecting in series with the same number in each ARM. In this work the system has 12 submodules in each ARM like in figure 3. In each phase next to each ARM there is a inductor to support the voltage difference that results from when the submodule is switching states [4]. It can limit the circulating currents between the phases and reduces the effects of faults in the converter.

A higher inductor means that the circulating currents and the chances of an event of DC fault in the converter

decreases [5]. But obviously a higher inductor means a higher cost. According to [5] a minimum Larm should be able to guarantee that the arm current does not exceed 20A/us for the worst case.

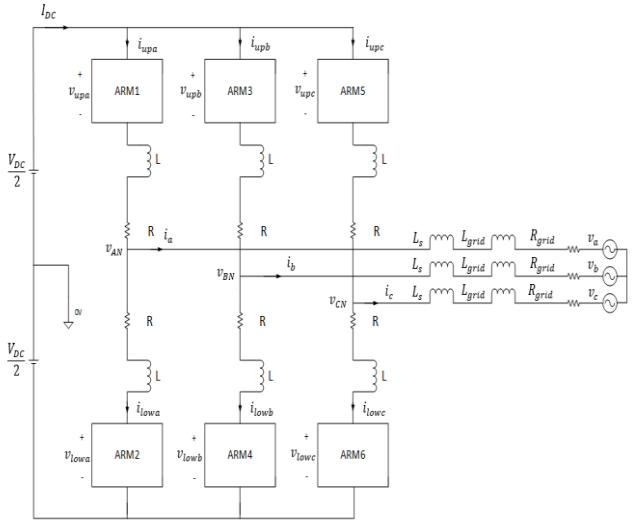

Fig. 2. MMC scheme

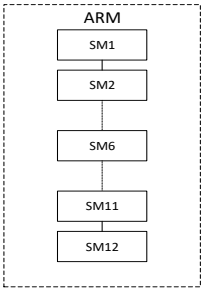

Fig. 3. ARM scheme.

The converter arm currents have 3 components as described in the equations (1) to (4) for phase a. The circulating current results from the DC voltages from the three phases not being the same [5]. The sum of the circulating current in all three phases must be zero (4).

$$i_{upa} = \frac{I_{DC}}{3} + \frac{i_a}{2} + i_{circ\_a} \quad (1)$$

$$i_{lowa} = \frac{I_{DC}}{3} - \frac{i_a}{2} + i_{circ\_a} \quad (2)$$

$$i_{circ\_a} = \frac{i_{upa} + i_{lowa}}{2} - \frac{I_{DC}}{3} \quad (3)$$

$$i_{circ\ a} + i_{circ\ b} + i_{circ\ c} = 0 \quad (4)$$

Using Kirchhoff's laws, the converter phase voltages can be obtained. The first phase converter voltage can be expressed in (5) and (6) through the voltage in DC link Vc, and the voltages and currents in the upper or lower arm.

$$v_{AN} = \frac{V_{DC}}{2} - v_{upa} - L\frac{di_{upa}}{dt} - Ri_{upa} \quad (5)$$

$$v_{AN} = \frac{V_{DC}}{2} + v_{lowa} + L\frac{di_{lowa}}{dt} + Ri_{lowa} \quad (6)$$

The upper and lower arm voltages are the sum of the voltage of the submodules that are in the ON state, as represented in (7) and (8):

$$v_{lowa} = \sum_{k=1}^{N} S_{lowk_a} v_{c_{lowa}} \quad v_{upa} = \sum_{k=1}^{N} S_{upk_a} v_{c_{upa}} \quad (7)$$

$$S = \begin{cases} 1, & SM\ is\ ON \\ 0, & SM\ is\ OFF \end{cases} \quad (8)$$

A. Submodule

The topology that was chosen was the half bridge as it is more common, and it costs less than full bridge even though it doesn't have fault block capability. It consists of two IGBTs (T1 and T2), two diodes in antiparallel connection (D1 and D2) and a capacitor, as seen in figure 4.

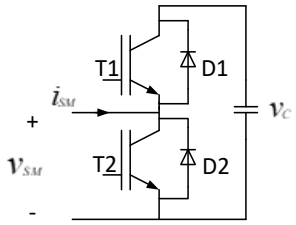

Fig. 4. Half-Bridge Submodule scheme.

The current that flows in the SM that comes from the arm current direction will affect the charging and discharging of the capacitor.

When the SM is turned ON then T1 is ON and T2 is OFF. In this case, and when the current in the SM ism is positive, the current flows through D1 which charges the capacitor C as it increases its voltage (Vc). If the current is negative with the SM turned ON, then the current flows through T1 and discharges the capacitor and its voltage decreases. If the SM is OFF then T1 is OFF and T2 is ON. If the current ism is positive the current flows through T2 and the voltage of the capacitor remains equal. It also remains constant if the current ism is negative as it flows through D2.

The voltage of the SM is equal to the voltage in the capacitor when the state of the SM is ON. If it is OFF then the voltage of the SM is zero. Table 3.1 features all the possible combinations of the elements. The voltage in the capacitor will be like (9) the number of submodules in each arm or in other way the number of submodules in ON state in the upper arm and the ones in the lower arm [6] which can be expressed by:

$$v_c = \frac{V_{DC}}{N} \qquad N_{up} + N_{low} = N \quad (9)$$

TABLE I. POSSIBLE STATES OF THE SUBMODULE AND THE RELATIONSHIP BETWEEN THE VARIABLES.

Case	*SM state*	*T1 state*	*T2 state*	i_{SM}	Δv_c	v_{SM}
1	*ON*	*ON*	*OFF*	*>0*	+	v_c
2	*ON*	*ON*	*OFF*	*<0*	-	v_c
3	*OFF*	*OFF*	*ON*	*>0*	*0*	*0*
4	*OFF*	*OFF*	*ON*	*<0*	*0*	*0*

B. Semiconductors sizing

In this work, it was chosen the IGBT as it is the preferable semiconductors for high voltage application and low frequency. For the number of submodules that has been used, the voltage in each submodule capacitor is:

$$v_c = \frac{V_{DC}}{N} = \frac{200000}{12} = 16.6\,kV \quad (10)$$

To guarantee 50% margin of security, the semiconductors should be able to block around 25kV.This value is not suitable for a real system because the voltage applied to each IGBT is too high. However, this is a consequence of considering a reduced number of submodules to minimize the computational burden in the simulations.

C. Capacitor

The value for the capacitor is a compromise between the size of the capacitor and the submodule capacitor voltage ripple. The following equation shows that the capacitor value depends on the current voltage ripple and frequency.

$$i_c = C\frac{dv_c}{dt} \Leftrightarrow i_c = C\frac{\Delta v_c}{\Delta t} \quad (11)$$

D. Filters

For higher voltages, the number of SMs should increase and the filter requirements should be reduced. If the number of levels is high enough filters may even not be required. However, they should be used as they contribute to reduce the harmonic content of the currents. The inductor is sized according to (12), where VC represents the DC voltage, Δi is the variation of the current in the coil and f_{PWM} is the commutation frequency [19].

$$L_s = \frac{V_{DC}}{4\Delta i f_{PWM}} \quad (12)$$

E. Modulation Strategy

In this work the PSC-PWM was chosen as it has higher flexibility, robustness, a lower total harmonic distortion (THD), a more equal power distribution and lower semiconductor stress due to the switching processes [18].

In [7] and [8] state that in cascaded H bridge converters, the PSC-PWM enables the reduction of common mode voltage, the decreasing in the number of commutations, lowering the switching losses and in the electromagnetic interference.The same results can be obtained to a MMC.

As to all modulation processes there is a reference waveform and several carriers. Each carrier is responsible for the gate signals for each submodule. In this process the carrier waves, usually triangular waves, differ from each other from a phase angle differing from SPWM modulation where the carriers have not different phase angles but different offset levels.

This phase difference is established using the frequency and the number of submodules and it is represented by the equation:

$$\varphi = n\frac{T_c}{N} \quad (13)$$

The PWM modulation principle maintains as there is a comparation between the reference and the carriers. If the modulator wave is higher than all carrier then all the modules are in ON state. In a more general way, the SMs at state ON are the ones where the carrier wave is below the reference. There are 7 levels corresponding to 6 submodules and the zero level which can be seen in figure 5 a).

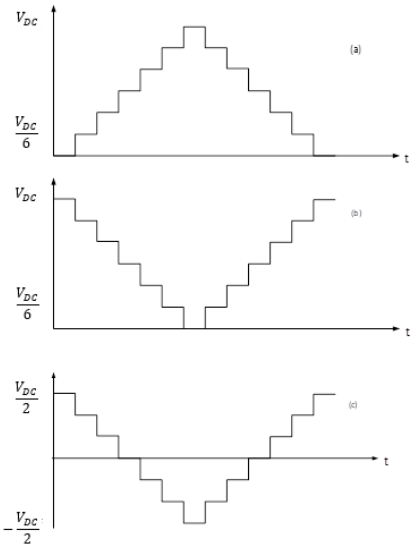

Fig. 5. Waveforms of a MMC. (a) Output voltage of the upper arm (b) Output voltage of the lower arm (c) Phase voltage of the converter.

IV. Design of the Controllers

In this paper it is established differences in the control approaches for the current using linear and nonlinear current controllers. Then it is designed control for the DC voltage, control for voltage sags and overvoltage events and a balance method for the DC capacitors.

A. Linear Controllers Design

For this kind of control it is used PI controllers. It was introduced as well an anti-windup method which helps the PI controllers in saturation event when the error is too large for a long period of time. It is represented in figure 6.

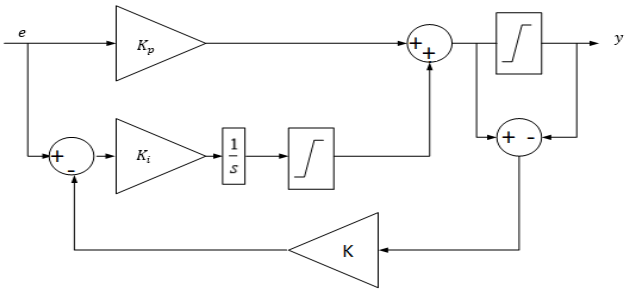

Fig. 6. PI controllers and Anti-windup scheme

For the proportional component, the correction of the variable is proportional to the error. The integral term sums the error continuously in time meaning an integration of the error over time. For instance, if the error is positive it accumulates the error and when it is negative the error decreases correcting itself. This latter term has another advantage compared to the proportional as it eliminates the offset through the integral of it. It will act on it until the error is zero. Thus, this integral action eliminates the steady state error that would appear if only a proportional controller

would be used. As it is known the transfer function of a PI controller can be expressed as (14), where Kp and Ki are the proportional and integral gains.

$$C(s) = K_P + \frac{K_I}{s} \tag{14}$$

The converter can be characterized as a first order transfer function, with a gain G and a delay Td [19].

$$G = \frac{u_d}{V_{DC}} \tag{15}$$

T_d is the delay time of the system to a response to an input and it is usually equal to one half the switching period.

When designing these controllers, one possibility would be to consider the optimum symmetry method [9]. This method presents advantages, as maximizing the phase margin or optimizing the control system to any disturbance input. Another option is to cancel the zero of the controller with the pole introduced by the filter.

$$T_d = \frac{T_c}{2} \qquad T_z = \frac{L}{R} \tag{16}$$

Then, the closed loop transfer function, written in the canonical form of a 2nd order transfer function is obtained

$$H(s) = \frac{i_{dq}}{i_{dqref}} = \frac{\frac{G}{T_d T_p R}}{s^2 + \frac{s}{T_d} + \frac{G}{T_d T_p R}} = \frac{\omega_n^2}{s^2 + 2s\xi\omega_n + \omega_n^2} \tag{17}$$

Through the equation (18) it is reached and the gains obtained by comparison

$$\begin{cases} K_P = \dfrac{T_z}{T_p} = \dfrac{L}{2T_d G} = \dfrac{L}{T_c \frac{u_d}{V_{DC}}} \\ K_I = \dfrac{1}{T_p} = \dfrac{R}{2T_d G} = \dfrac{R}{T_c \frac{u_d}{V_{DC}}} \end{cases} \quad T_p = \frac{2T_d G}{R} \tag{18}$$

Any big change of the error will result in a peak of the output of the controller. If it is too large for a long time can bring problems as the integrator outputs accumulates the error. One simple way to solve this problem would be to add a limiter. It can solve some problems but if the error remains nonzero for a long time we have the same issue as before. An anti-windup method can solve this issue.

When using PI controllers, eventually saturation phenomena can appear. In order to minimize the decreasing of performance, an anti-windup method can be used [10]. Usually saturation issues appear when the error is too large or if the error is nonzero (and always positive or always negative) for a long time. This leads to an accumulation of errors and in delays in the response to any change of the reference. The higher the saturation the higher the delay and the system may lose controllability.

A way of controlling the saturation is using the tracking anti-windup [10]. This method includes a gain fed by the difference of the output of the converter and the saturated value after the limiter which then reduces the error to be integrated. With this, the output of the integrator will be reduced and removed from saturation.

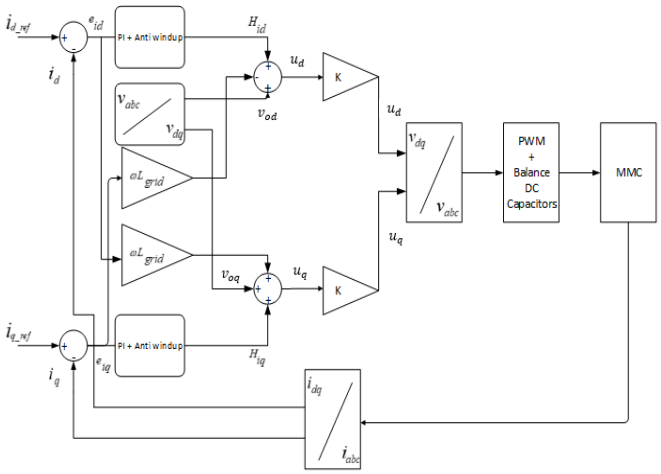

Fig. 7. Linear control block diagram.

B. *Nonlinear Controllers Design*

Another way of controlling the phase currents is using a nonlinear approach: Nonlinear current control (NLCC).

Compared to a linear approach it does not require PWM control, as the algorithm provides directly the number of submodules to be turned ON. Usually it may be not necessary the dq transformation but for comparison and simplicity it was chosen to use it. It has a faster response than the linear controller which will be shown in section V.

The main idea is to establish a hysteresis band of value ε around the reference current. To guarantee that the current error is contained in that hysteresis, it is chosen the number of submodules to be active or not which is equivalent to the level of the output voltage. If there are n submodules then there are n+1 levels.

There are many ways to implement this kind of thinking. The main difference between them is choosing whether the converter's output voltage has values regulated by the grid voltage or not [11].

It was chosen the first option on which the output voltage of the converter has values adjusted to the grid voltage. This means that the output voltage only has values near the grid voltage and depends on the number of SM in the ON state which will be determined by equation (19). The second is more useful when there is a bigger number of submodules because with a higher number of submodules the voltage in the inductor will be lower. This leads to increasing the converter phase voltage which may be necessary to use values that are not adjusted to the grid voltage and to increase the inductance voltage (and the speed of variation of the phase current). Another reason for the choice is that by having values adjusted the grid voltage it is possible to reduce the inductance value and using the capabilities and advantages of a multilevel topology.

With the voltage in the DC side (V_{DC}) and the voltage in the capacitor (v_c). the number of submodules in the ON state in the upper and lower arms can be calculated according to the equation (19) [6].

$$k = floor\left(\frac{v_{abc} + \frac{V_{DC}}{2}}{v_c}\right) \tag{19}$$

If the phase current is higher than the hysteresis band then the number of submodules in the lower arm is the one calculated by the equation above. If not and if the current isn't lower than the hysteresis band the number of SM in the ON state, the number of SM doesn't change. If it is then it is necessary to increase one SM to the one previous calculated [6]. The number of SM in the ON state in the upper arm is selected to complete the number of total SM in an arm, as shown by equation (9).

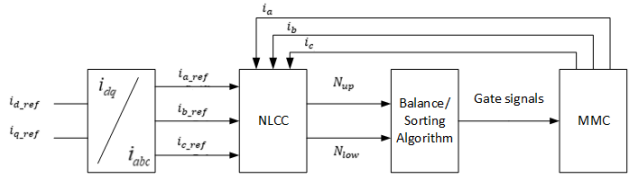

Fig. 8. Nonlinear control block diagram.

C. DC voltage controller

In many papers to illustrate the operation of these systems, the DC side is represented by a DC voltage source to simplify the analysis. However, this is not realistic as the voltage in the DC link will not keep exactly constant, depending on the operation conditions. For that reason, capacitors should be used instead of these voltage sources.

The current control can be represented by a first order transfer function with gain G_i and delay T_{dv} (pole) [12]. Knowing that the power in the DC link is the same as in the AC link it can be concluded that the gain can be represented as

$$P_d = v_d i_d = V_{DC} I_{DC} \Leftrightarrow I_{DC} = \frac{v_d}{V_{DC}} i_d \Leftrightarrow I_{DC} = G_i i_d \quad (20)$$

$$\frac{i_{dq}(s)}{i_{dqref}(s)} = \frac{G_i}{\alpha_i} \frac{1}{sT_{dv}+1} \quad (21)$$

From the block diagram in figure 9, the closed loop transfer function is obtained (22). Comparing the denominator of the transfer function with the third degree polynomial shown in (23) it can be obtained the values of the gains of controllers in (24) [12].

$$\frac{V_{DC}}{V_{DCref}} = \frac{\frac{\alpha_v G_i}{\alpha_i}\frac{K_{pv}+sK_{iv}}{T_{dv}C}}{s^3 + s^2\frac{1}{T_{dv}} + s\frac{\alpha_v G_i K_{pv}}{\alpha_i T_{dv} C} + \frac{\alpha_v G_i K_{iv}}{\alpha_i T_{dv} C}} \quad (22)$$

$$p_3(s) = s^3 + 1.75\omega_o s^2 + 2.15{\omega_o}^2 s + {\omega_o}^3 \quad (23)$$

$$K_{pv} = -\frac{2.15C\alpha_i}{1.75^2 \alpha_v G_i T_{dv}} \quad K_{iv} = -\frac{C\alpha_i}{1.75^3 \alpha_v G_i {T_{dv}}^2} \quad (24)$$

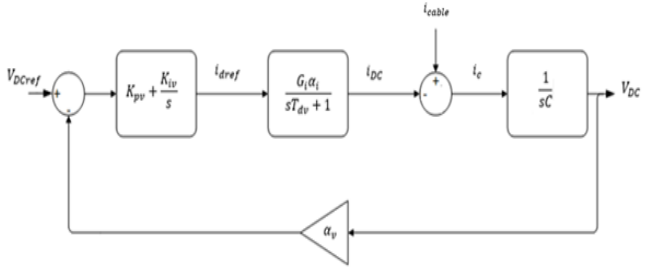

Fig. 9. Block diagram of DC control voltage.

D. Control during Voltage Sags

For the converter to maintain the rated voltage in the load even in case of occurrence of a voltage sag, then there must be a change in the current controller. This change is in the reference current i_{q_ref} that should no longer be zero, it should introduce reactive power to mitigate the problem.

This new value will be calculated by a PI controller that will measure the voltage value in the PCC and calculate the error, based on the AC voltage reference value (the rated value). Then, the PI controller sets the reference current i_{q_ref}. for the current controller (linear or non-linear).

The differences in the voltage in the PCC and the current iq can be detailed in a first order transfer function with a gain and delay [13]. The gain can be expressed as (25) where ω is the grid frequency and L_s is the inductance connected to the grid. The Block diagram of the AC voltage controller is shown in figure 10.

$$K_{AC} = \frac{\Delta v_d}{\Delta i_q} \approx \omega L_s \quad (25)$$

The closed loop transfer function is established in (26).The expression for the proportional and integral gains (27) can be obtained comparing the denominator of (26) with the second order transfer function written in the canonical form.

$$\frac{V_{PCCd}}{V_{PCCdref}} = \frac{\frac{sK_{AC}K_{pvAC} + K_{AC}K_{ivAC}}{T_{dvAC}}}{s^2 + s\frac{1+\alpha_v K_{AC}K_{pvAC}}{T_{dvAC}} + \frac{\alpha_v K_{AC}K_{ivAC}}{T_{dvAC}}} \quad (26)$$

$$K_{pvAC} = \frac{2\xi\omega_n T_{dvAC} - 1}{\alpha_v K_{AC}} \quad K_{ivAC} = \frac{T_{dvAC}\omega_n^2}{\alpha_v K_{AC}} \quad (27)$$

According to the transfer function, for the system to be stable the gain must be positive and in order to have a finite bandwidth $K_{pvAC} < 1$ [13], ω_n must be bounded as in (28)

$$\omega_n > \frac{1}{2\xi T_{dvAC}} \quad \omega_n < \frac{\alpha_v K_{AC} + 1}{2\xi T_{dvAC}} \quad (28)$$

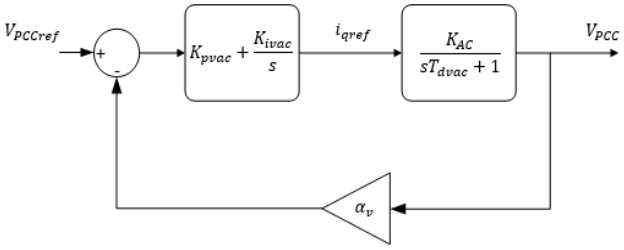

Fig. 10. Block diagram of AC voltage controller.

E. Algorithm to Balance of the Capacitors voltages

The modulation process used is, up to a certain point, a good method for balancing the capacitors. However, due to system unbalances, inequality of semiconductors and filters characteristics, among others, in the long term the capacitors voltage balancing is not guaranteed.

There are many solutions to a reduced switching frequency strategy.

Chai [14] uses the switching states of the SM to reduce the number of switching operations at every period of balancing. Kalle [15] main objective is to reduce the capacitor ripple even with a reduced switching frequency by predicting the capacitor voltage variation at every fundamental period. This leads to a more even charge distribution of all the capacitors. Zhao [16] uses a method of dividing the submodules into groups and then determining the switching states of the SM.

It is important to have another balancing algorithm, operated at a lower frequency, in order to avoid the dependency on the PSC-PWM modulation.

According to (29) it is possible to establish the number of redundancies of each level, i.e, the number of switching combinations that the converter can use to have the same level, with N being the number of submodules and l the level

$$Nred = \frac{N!}{(N-l)!\,l!} \tag{29}$$

According to (29) there are in total 64 combinations to have 7 levels. Each level of the AC voltages is obtained as a sum of SM voltages. For instance, if the level is 3Vc, then three SMs must be in state ON. The redundancies in each level will help balancing the capacitors as it can be chosen which SMs are ON to obtain a specific level, from all the possible combinations. With this it can be established the required voltage level and a good performance of the SMs. These combinations will help choosing the best SM on their need of charging and discharging to reach the capacitors voltage reference value.

The charge/discharge of the SM capacitors results from the direction of the current. In order to work, the balancing algorithm will need to know the reference voltages in the capacitors (1.5), the actual capacitor voltage and the current in the arm (and more important if it is positive or negative). Then it is calculated the error, i.e, the difference between the capacitor reference voltage and the measured value. After, in the linear case through the PWM modulation and in the nonlinear one through NLCC receives the information on the voltage level.

Then the sorting of the capacitors is made with the sign of current being the main player. If the current is positive, meaning the capacitors will charge, then the capacitor must be sorted from with the biggest difference of voltages to the smallest difference, i.e, form the one with less charge to the one which is most charged. If the current is negative, meaning the capacitors will discharge, then the sorting will be the opposite [17].

With the capacitors of the SMs sorted, each one of them will receive a weight value. The first one will receive the highest and the last one the lowest one. Through the redundancies it is chosen the combination of capacitors with the highest weight result.

After the last step is completed, the output of the algorithm will be the signal gates to the SMs with the indication of which semiconductors should be turned ON and the ones which should be turned OFF to guarantee the desired voltage level. Figure 4.9 shows a flowchart describing the steps mentioned before [17].

F. Correction of level

This is a simple correction algorithm applied to the linear and nonlinear controllers. To establish what is the number of submodules turned on, in other words, what is the level of the converter at the same time, it is used the PSC-SPWM modulation for the linear case and the NLCC for the nonlinear.

Usually the levels are continuously in order to obtain a waveform as similar as possible to a sinusoid. However, during this modulation process sometimes there can be a jump of two levels or more. This algorithm prevents this situation as it receives the number of the previous level and compares it to the following one. If the difference between the previous level and the calculated one is higher than one then the real level that will be sent to the system will be limited to one level above or below the previous one. With this approach it is possible to solve a problem that could bring bigger issues to the AC waveform as it would result in higher distortion.

V. Simulation Results

The simulated MMC-HVDC system is the one represented in figure 5.1 that connects two grids: one operated at 50 Hz and the other operated at 60 Hz. The length of the DC cable is 100km. The number of submodules is 12.

TABLE II. Simulation parameters

Parameter	***Variable description***	***Value***
N	Number of modules in each arm	12
Vdc	DC voltage	200 kV
R	Resistance in each phase	1 mΩ
L	Coil in each phase	45 μH
C	Capacitor in each submodule	90 mF
Ron	Reference value for the voltage in each capacitor for 12 sm in each arm	0.1 mΩ
Rgrid	Resistance connected to the grid	1 mΩ
Lgrid	Coil connected to the grid	3 mH
Ucref	Capacitor in the DC side	16.7 kV
Cdc	Conductor resistance	100 mF
Lcable	Coil of the cable	10 mH
idref	Reference for the direct current	10000 A
iqref	Reference for the quadratic current	0 A
Kp	Proportional gain for the linear current control	2640
Ki	Integral gain for the linear current control	929280
Kpv	Proportional gain for the DC voltage control	-11464
Kiv	Integral gain for the DC voltage control	-30470959
Kpvac	Proportional gain for control during voltage sag or overvoltage event	0.0106
Kivac	Integral gain for control during voltage sag or overvoltage event	541
fcarrier	Switching frequency	2000 Hz
fmodulator	Frequency of the modulator	50 Hz
ε	Error for the NLCC	5 A

In figure 11 and 12 it is represented the arm voltages (a), phase voltages (b) and DC capacitor voltage for the linear and nonlinear approach (c). For the first two images of each figure shows the principle stated in section III. As for the for the DC capacitor voltage the results appear to be different. The linear approach reaches the desired value faster with less fluctuation than the nonlinear controllers in the beginning of

simulation. Even though the linear controller is faster, both approaches present similar results in steady state. The capacitors balance algorithm produces good results for both control methods.

When comparing the error of the currents in both control approaches (figure 13(a) and 14 (a)), it can be concluded that the nonlinear control is faster.

In figure 13, 14 (b) and (c) it can be seen as well that comparing the current waveforms, it is easier to see that the nonlinear control presents better results than the linear counterpart as it was expected as it is faster to adjust to errors. Analysing the output voltage of the converter, it can be observed that both controllers present good results with the linear being better.

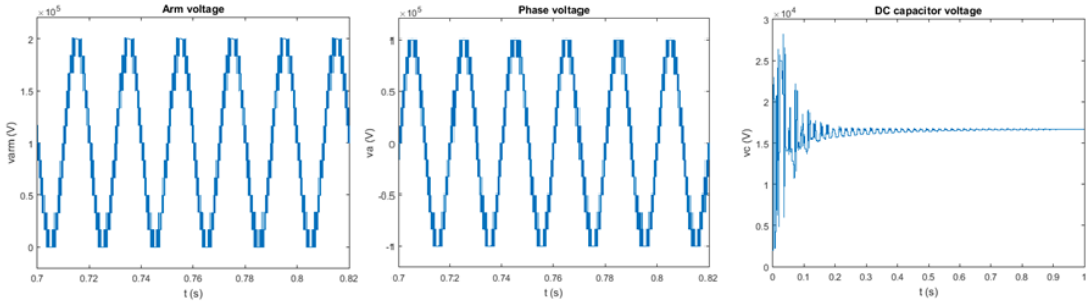

Fig. 11 From linear control system a)upper arm voltage, b) phase voltage, c) DC capacitor voltage.

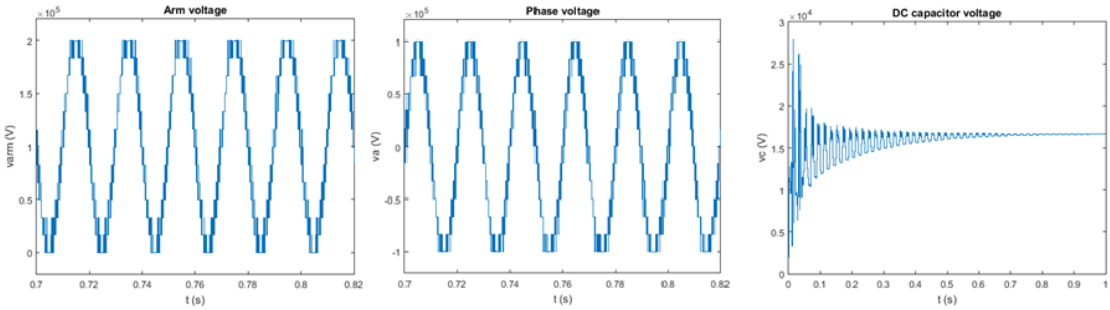

Fig. 12 From nonlinear control system a)upper arm voltage, b) phase voltage, c) DC capacitor voltage.

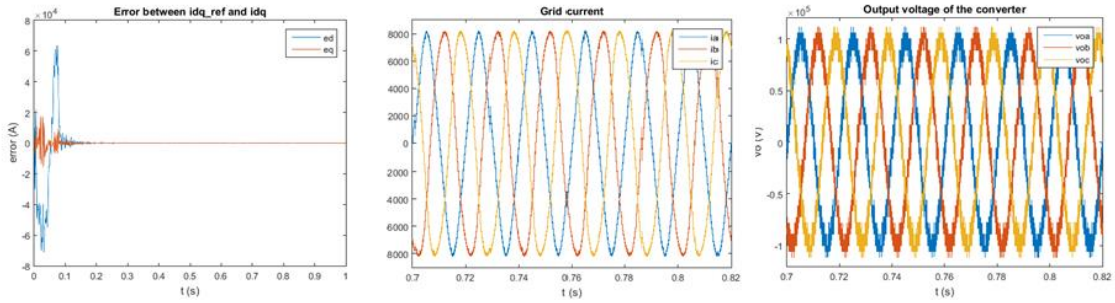

Fig. 13 From linear control system a) error of idq currents b) grid current c) output voltage of the converter.

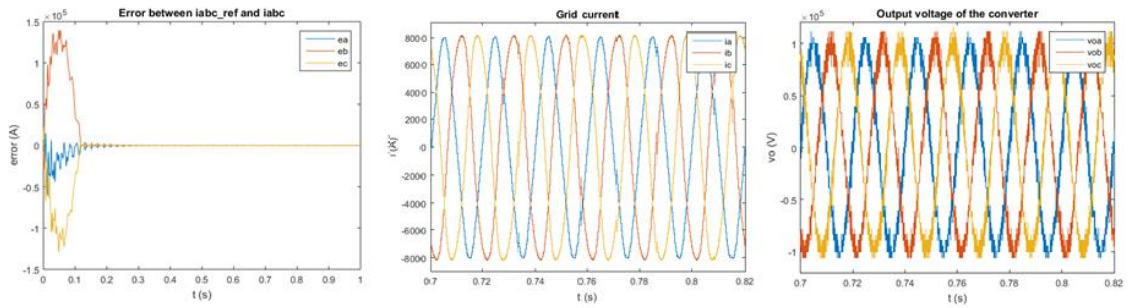

Fig. 14 From nonlinear control system a) error of idq currents b) grid current c) output voltage of the converter.

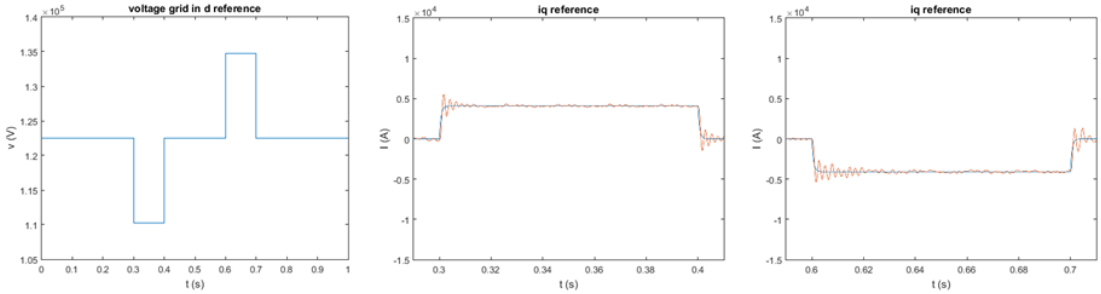

Fig. 15 From linear control system a) voltage grid in d reference b) iq and iqreference during voltage sag c) during overvoltage.

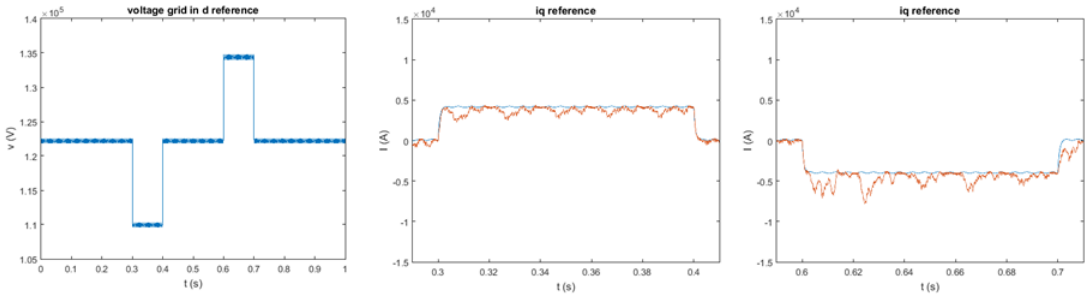

Fig. 16 From nonlinear control system a) voltage grid in d reference b) iq and iqreference during voltage sag c) during overvoltage.

The evaluation of the dynamic performance was made creating a voltage sag from t=0.3s to t=0.4s and an overvoltage from t=0.6s to t=0.7s. These power quality issues may appear in the grid and must be solved, since they can destroy or result in serious equipment damage. For the voltage sag it was considered a 10% decrease from the maximum voltage, and for the overvoltage, it was considered a 10% increase of the voltage. It can be seen in d refence in figure 15 (a) and 16 (a).

As stated previously, when in the presence of a voltage sag there must be a reactive compensation, in this case, injection of reactive current. In other words, the reference of iq must no longer be zero. In figure 15 and 16 there is a change in the reference current for positive values in the presence of a voltage dip (b) and for negative values in an overvoltage situation (c). In the same figures it can be concluded that the quadratic component of the current follows the reference with better results in the linear control (figure 15) than in the nonlinear control (figure 16).

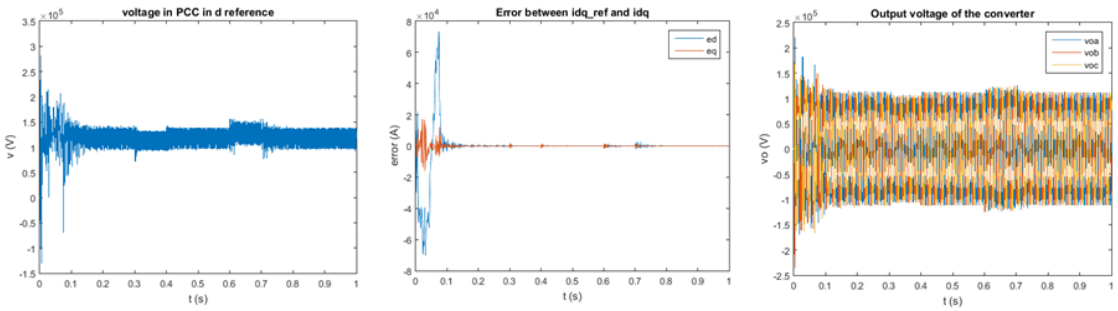

Fig. 17 From linear control system a) voltage in PCC in d reference b) error of the currents c) output voltage of the converter.

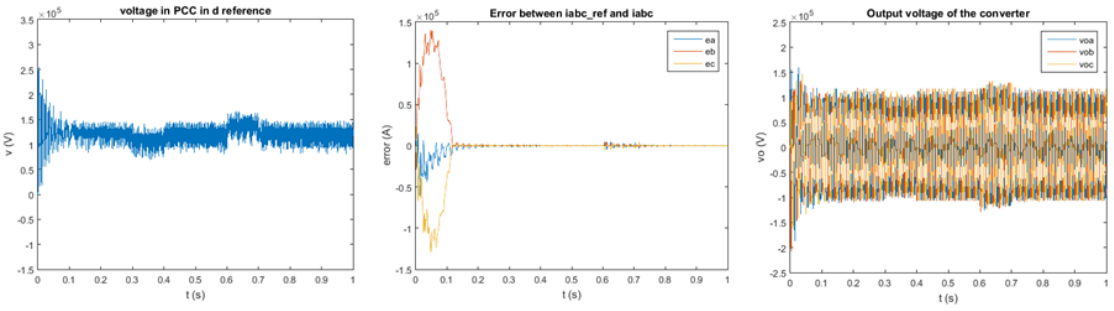

Fig. 18 From nonlinear control system a) voltage in PCC in d reference b) error of the currents c) output voltage of the converter.

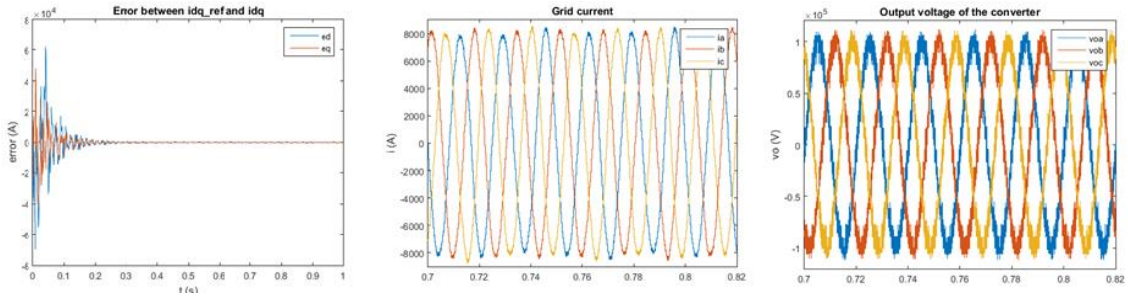

Fig. 19 Connection to a 60 Hz grid: from linear control system a) error of the currents b) grid current c) output voltage of the converter.

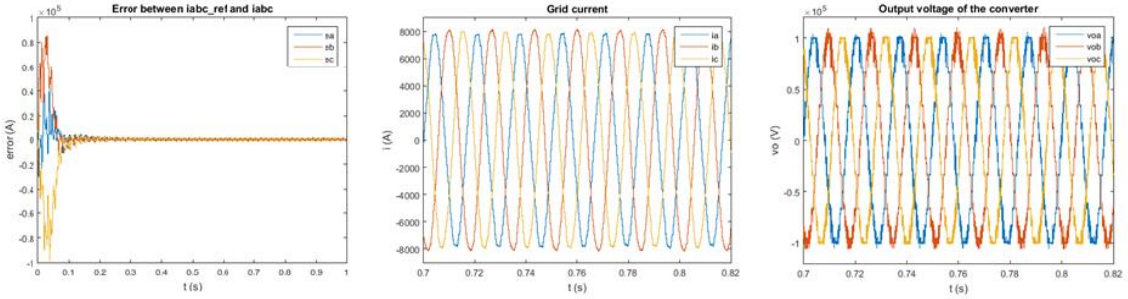

Fig. 20 Connection to a 60 Hz grid: from nonlinear control system a) error of the currents b) grid current c) output voltage of the converter.

As mentioned in section IV-D, the voltage in PCC needs to be controlled. The objective is that even though there is a dip or overvoltage the voltage in the PCC does not change much from the nominal values. Figures 17 (a) and 18 (a) shows that for both controllers there is a small difference in the PCC voltage. However, this difference could be worse there was not any control system. Although both perform well there is a slightly better performance in the linear case.

In figures 17(b) and 18 (b), it is observed the error, and both controllers perform better during voltage sag than in overvoltage. This can be explained by the lack or poor performance in controlling the DC voltage. However, it can be understood that when there is an increase of the error when an event happens followed by a decreasing of the error meaning the controller is functioning.

In the same figures in (c) it is presented the voltage profile in the output of the converter (in the 17 for the system with linear control and in the 18 with nonlinear one) where it can be observed the voltage sag and the overvoltage.

One of the advantages of using these systems is being able to connect two grid with different frequencies

Until now the results were from a converter connected to a 50 Hz grid. The following results are from the other side of the system connected to a 60 Hz grid. The same principle is followed as before as in the left are the results from the linear approach and on the right from the nonlinear approach. In analysing the results in figure 19 and 20 it can be stated that the controllers for a 60 Hz grid works with the same level of performance when it is connected to a 50 Hz grid

For the DC control as it can be seen by figure 21 (a), the control reach the desired value (200 kV) even though it is a little bit slow. The DC capacitors voltage changes naturally with the DC voltage reaching the result obtained previously

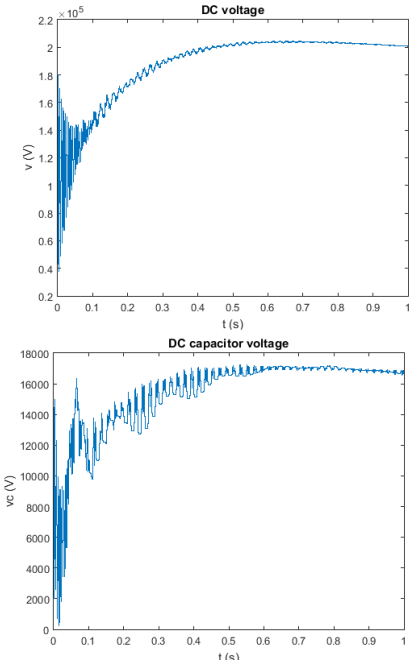

Fig. 21 DC voltage of the MMC and the DC voltage of the capacitor.

VI. Conclusions

Two control methods for the current were used: a linear control approach and a nonlinear control. For the linear control, the gains for the PI controller were sized and the modulation process chosen was the Phase Shift Carrier Pulse Width Modulation (PSC-PWM), in order to obtain the desired output voltage. The nonlinear current control algorithm was implemented and the goal was to compare the performance with the linear controller.

A balance algorithm for the capacitors was implemented in both control methods, because in these converters it is necessary to balance the voltage of these capacitors due to the existence of circulating currents. A controller to mitigate voltage sags and overvoltages was also developed as required in systems connected to grids. It was also implemented a control for the DC voltage, as there is always fluctuation on it.

It was observed that the nonlinear control has a faster response to a disturbance than the linear one. Both methods present good results in the control of the current with better results in the nonlinear control. In the voltages analysis it could be observed that both performed well.

It was possible to corroborate that the method for balancing the capacitors was implemented with success in both control methods. The results when having voltage sags or overvoltage events were also positive, even though in the overvoltage case, the results were not as good when comparing to the voltage sag control. This was result of poor performance of the DC control that even though reached the objective, it was a slow controller.

Finally the same analysis was made to the connection to the 60 Hz grid which showed that the design of the controllers works for both grids. The results of the simulation in Matlab/Simulink environment show that this converter and the designed controllers can be a good solution for HVDC systems.

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