TÉCNICO LISBOA

SAR ADC for Stochastic Self-Calibration Algorithms

A 12-bit, 35 MS/s, 0.38 mW SAR ADC with Digital Calibration

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Thesis to obtain the Master of Science Degree in

Electrical and Computer Engineering

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June 2019

I declare that this document is an original work of my own authorship and that it fulfils all the requirements of the Code of Conduct and Good Practices of the *Universidade de Lisboa*.

In memory of Jim Williams, “a poet who wrote in electronics”.

“At about this stage I sat back and stared at the wall. There comes a time in every project where you have to gamble. At some point the analytics and theorizing must stop and you have to commit to an approach and start actually doing something. This is often painful, because you never really have enough information and preparation to be confidently decisive. There are never any answers, only choices. But there comes a time when your gut tells you to put down the pencil and pick up the soldering iron.” — Jim Williams

Agradecimentos

Ainda me lembro como fiquei maravilhado quando comecei a interessar-me por eletrónica. Desenhar um circuito para desempenhar determinada tarefa era desafiante e divertido. Vou levar para a vida as palavras de Harold Kroto, uma pessoa marcante com quem tive a oportunidade de conversar: "Tenta encontrar algo em que sintas que estás a brincar. Acontece que essa é a forma de ser criativo. Eu ainda estou a brincar".

Sou extremamente grato ao meu pai por plantar a curiosidade em mim desde pequeno. Sou igualmente grato à minha mãe por sempre ter dado a mim e à minha irmã o melhor que ela podia. Quero também agradecer a toda a minha família por todo o apoio durante o meu percurso académico.

Tive imensa sorte em ter sido aluno das professoras Fátima Pataco, Paulete Estima e Ana Ferrão. O entusiasmo com que ensinam e a dedicação aos alunos servir-me-ão como exemplo para o resto da minha vida profissional. Quero também agradecer ao Diogo Albuquerque, ao Vitaliy Davydovych e ao Samuel Santos, três fantásticos estudantes de quem tive o prazer de ser mentor durante o desenvolvimento de um projeto de eletrónica para uma feira de ciências. O encanto deles por engenharia foi revitalizante para mim.

O desenvolvimento deste trabalho não teria sido possível sem o conhecimento que adquiri nas aulas do Prof. Jorge Fernandes. Para além do rigor científico, o Prof. Jorge Fernandes sempre tentava incutir nos alunos a intuição, uma ferramenta que considero muito importante e que raramente é desenvolvida nas aulas. Quero também agradecer ao Taimur Rabuske pelos conselhos e pela supervisão durante o desenvolvimento do trabalho.

Finalmente, quero agradecer à Luciana Mendonça pelo amor, carinho e companheirismo. Nunca teria conseguido terminar este trabalho sem a tua preciosa ajuda.

Abstract

An Analog-to-Digital Converter (ADC) is a device whose function is to convert an analog signal (continuous in time and amplitude) into a digital signal (discrete in time and amplitude). In the past, the signal path in most systems was implemented in the analog domain. Nowadays more of the signal path is implemented in the digital domain, creating a demand for data converters, which bridge the analog and digital domains.

The Successive-Approximation-Register (SAR) ADC is becoming a popular architecture for high-accuracy and high-speed applications. Being a switching intensive and free of precision amplification architecture allows it to benefit greatly from faster transistor speed of scaled CMOS technologies. The key linearity limiting factor in SAR ADCs is capacitor mismatch of the DAC caused by production process non-idealities. Laser trimming and precision layout techniques can be used to reduce these mismatches. In this thesis, a sub-radix-2 SAR ADC was implemented that tackles this problem using redundancy and digital calibration. Furthermore, the usage of multiple comparators instead of only one comparator as in a typical SAR ADC was studied. Since the differential voltage at the comparator input (residue voltage) is reduced from the most significant bit (MSB) to the least significant bit (LSB), a higher noise can be tolerated when resolving the MSB while a lower noise is desired when resolving the LSB. As the comparator input-referred noise variance is inversely proportional to its power consumption, using different comparator noise specifications in resolving each bit improves the overall power consumption of the ADC. In a typical implementation, the comparator offset only introduces an offset in the transfer function of the converter. However, when multiple comparators are used, their different offset values generate non-linearity, reducing the dynamic performance of the ADC. To solve this problem, the offset of each comparator is calibrated.

The ADC was implemented in a 130 nm process, fitting in an area of 260 × 155 μm^2. Simulation results show that the ADC consumes 380 µW while sampling at 17.5 MS/s, having an estimated SNDR of 71.5 dB, which corresponds to an ENOB of 11.6 bit.

Keywords

SAR ADC, redundancy, digital calibration, multiple comparators.

Resumo

Um Conversor Analógico-Digital (ADC) é um dispositivo que converte um sinal analógico (contínuo no tempo e em amplitude) num sinal digital (discreto no tempo e em amplitude). No passado, os sinais eram processados no domínio analógico. Atualmente, grande parte desse processamento é feito no domínio digital, criando um aumento na procura de ADCs e DACs, que estabelecem a ligação entre os dois mundos.

O Conversor por Aproximações Sucessivas (SAR ADC) é uma arquitetura popular para aplicações que requerem resolução e velocidade elevadas. O facto desta arquitetura assentar bastante em comutação e não precisar de amplificação precisa faz com que ela beneficie bastante com o aumento da velocidade dos transístores que acontece com a evolução das tecnologias CMOS. O grande fator que limita a linearidade dos ADCs SAR são os erros introduzidos pelas não-idealidades do processo de produção nos condensadores do DAC. O corte a laser e técnicas de layout de precisão podem ser usadas para reduzir esses erros. Nesta tese, foi implementado um ADC SAR sub-radix-2 que aborda o problema utilizando redundância e calibração digital. Para além disso, estudou-se a utilização de múltiplos comparadores em vez de um como numa implementação típica. Como a tensão diferencial à entrada do comparador diminui desde o bit mais significativo (MSB) até ao bit menos significativo (LSB), um ruído maior pode ser tolerado ao determinar o MSB enquanto que um ruído menor é desejado ao determinar o LSB. Dado que a variância do ruído do comparador é inversamente proporcional ao seu consumo de energia, utilizar diferentes especificações de ruído na determinação de cada bit melhora o consumo total de potência do ADC. Numa implementação típica, a tensão de offset do comparador apenas introduz um desvio na função de transferência do conversor. No entanto, as diferentes tensões de offset quando múltiplos comparadores são utilizados geram não-linearidade e reduzem o desempenho dinâmico do ADC. Para resolver este problema, a tensão de offset de cada comparador é calibrada.

O ADC foi implementado numa tecnologia CMOS de 130 nm, ocupando uma área de 260 × 155 μm^2. Os resultados de simulações mostram que o ADC consome 380 µW com uma frequência de amostragem de 17.5 MS/s e atinge um SNDR estimado de 71.5 dB, que corresponde a um ENOB de 11.6 bit.

Palavras-chave

ADC SAR, redundância, calibração digital, múltiplos comparadores.

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List of Acronyms

ADC	Analog-to-Digital Converter
BWC	Bitwise Correlation
CDF	Cumulative Distribution Function
CMOS	Complementary Metal-Oxide Semiconductor
CR	Charge Redistribution
CS	Charge Sharing
DAC	Digital-to-Analog Converter
DNL	Differential Non-Linearity
DSP	Digital Signal Processing
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
IMCS	Inverted Merged Capacitor Switching Scheme
INL	Integral Non-Linearity
LMS	Least-Mean-Square
LSB	Least Significant Bit
MCS	Merged Capacitor Switching Scheme
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
MOSCAP	Metal-Oxide Semiconductor Capacitor
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
NMOS	N-channel Metal-Oxide Semiconductor
ODC	Offset Double Conversion
PMOS	P-channel Metal-Oxide Semiconductor
PN	Pseudorandom Noise
S/H	Sample and Hold
SAR	Successive Approximation Register
SFDR	Spurious Free Dynamic Range
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal-to-noise ratio
THD	Total Harmonic Distortion

Chapter 1

Introduction

1.1 Motivation

Electronic systems nowadays use some sort of digital data storage and processing. Digital systems are becoming faster and smaller as science and technology progress and this has led to a shift in the way signals are handled and processed. Although analog circuits continue to be used, much of the signal path in many systems is now implemented in the digital domain. Digital Signal Processing (DSP) provides storage capability, does not add noise to the signals, can carry out complex algorithms without adding significant hardware complexity and in many cases the firmware can be updated and improved without having to replace any component or change the circuit.

To take advantage of all the DSP features in real world systems, conversions between analog and digital domains are needed. As a result, the Analog-to-Digital Converter (ADC) became a key component in the signal chain. Given the trade-offs between speed, resolution and power consumption, several ADC topologies were developed, being Flash, Delta Sigma, Successive Approximation Register (SAR) and Pipeline the most known. Figure 1.1 highlights the differences of achievable signal to noise and distortion ratios (SNDR), power consumption and sampling frequencies among these architectures.

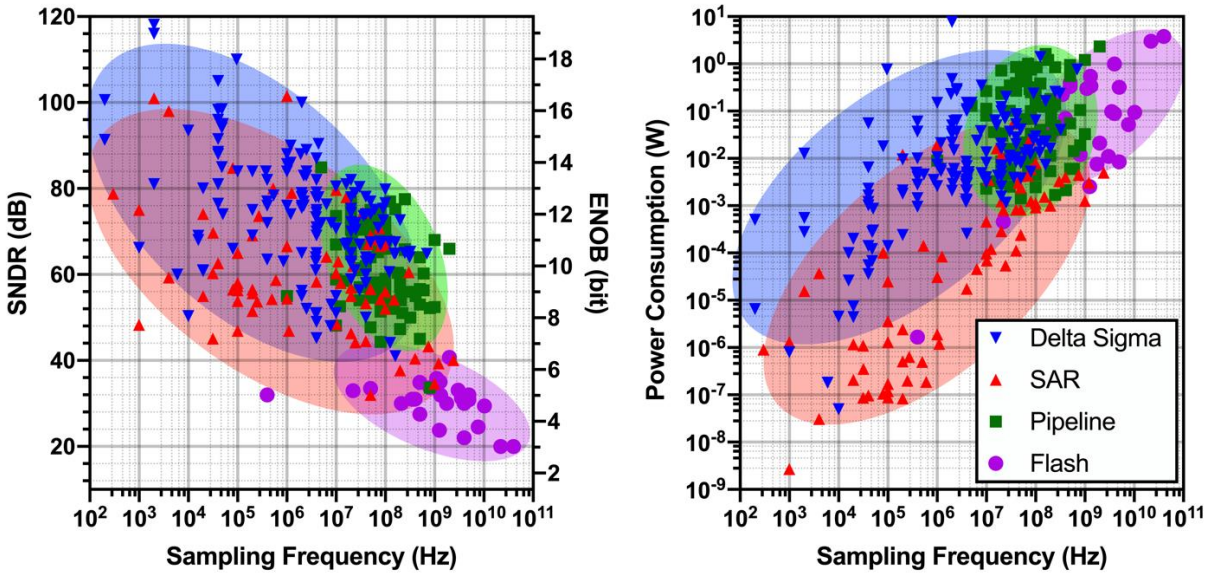

Figure 1.1 – SNDR and power consumption vs. sampling rate of ADCs from the ISSCC and the VLSI Symposium from 1997 to 2019 for each of the main ADC architectures [1].

Flash and Pipeline ADCs are commonly used in applications requiring high sampling rates, having therefore lower resolution. On the other hand, applications which require very high resolutions at low sampling rates commonly use Delta Sigma ADCs. SAR ADCs are usually the choice for data-acquisition applications requiring medium to high resolutions at medium sampling rates with low power consumption.

This work is going to be focused on SAR ADCs. Since SAR ADCs have a highly digital composition, they greatly benefit from new technological advances in CMOS technologies, which usually improve the performance of digital circuits but degrade the performance of analog circuits. For this reason, the popularity of this architecture has been increasing significantly since 2006, as shown in Figure 1.2.

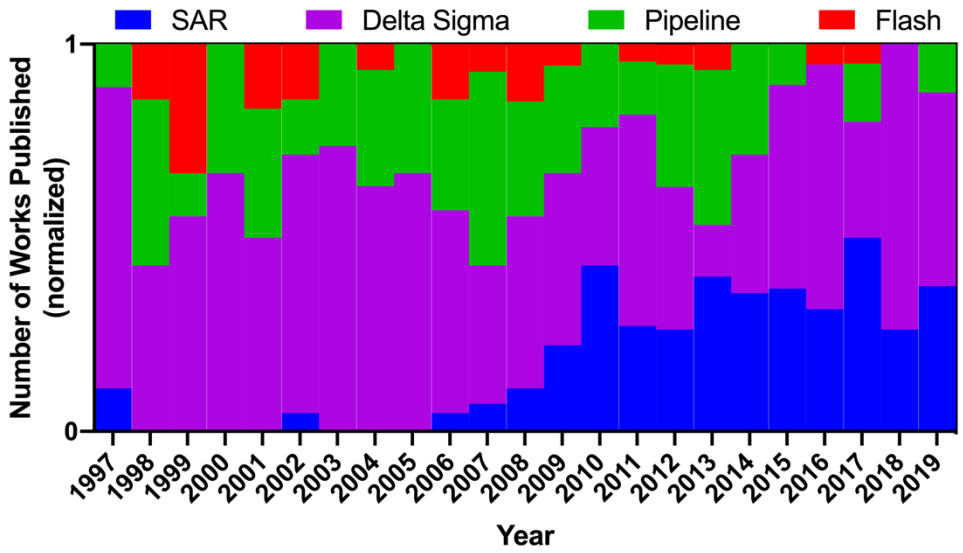

Figure 1.2 – Number of works published at the ISSCC and the VLSI Symposium from 1997 to 2019 for each of the main ADC architectures [1].

Even though ADCs have been improving in terms of speed, power consumption and resolution, the SAR architecture is still the only one able to achieve figures of merit (FoM) [2], below 10 fJ/step, as shown in Figure 1.3. In fact, some works started to report FoM below 1 fJ/step since 2014.

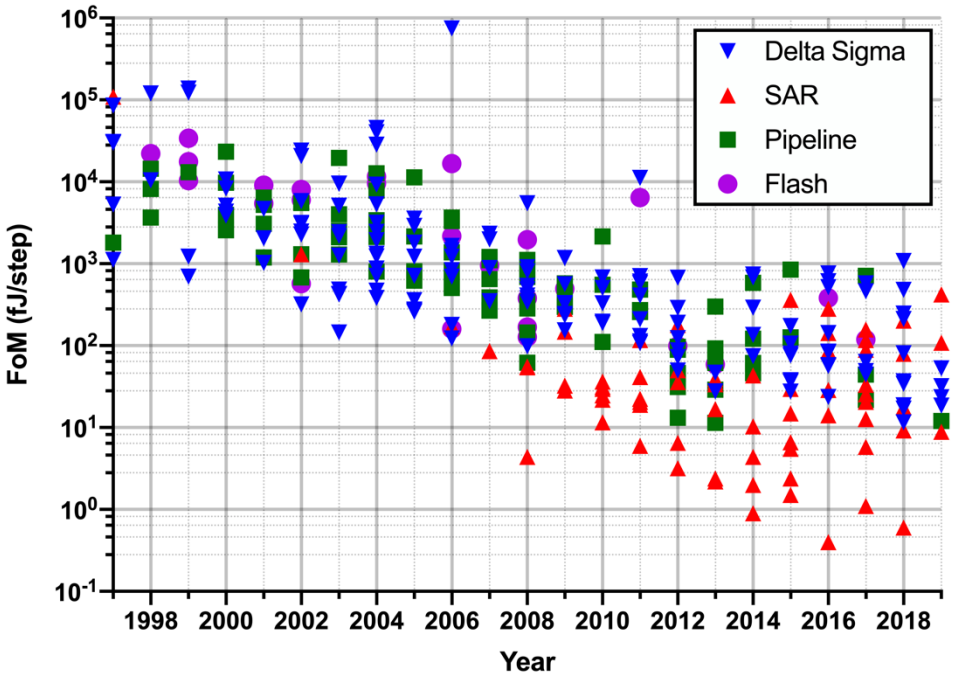

Figure 1.3 – Evolution of the FoM of ADCs from the ISSCC and the VLSI Symposium from 1997 to 2019 for each of the main ADC architectures [1].

This thesis describes the study and design of a SAR ADC featuring multiple comparators for power consumption optimization, a split-capacitor DAC for area reduction and redundancy for dynamic error correction. The ADC was designed such that DAC mismatches can be calibrated digitally using the Offset Double Conversion (ODC) technique [3].

1.2 Goals

The main goal of this work is to develop a SAR ADC with 14 raw bit output using redundancy for dynamic errors correction and digital calibration to correct for manufacturing mismatches. The usage of multiple comparators to optimize power consumption is going to be studied. The ADC is going to be implemented in a 130 nm CMOS technology. To build the ADC it is necessary to design all the blocks that constitute the converter, namely the capacitive DAC array, the dynamic comparators, the delay cells, the switches and the logic. These blocks should be implemented first in terms of transistor level schematic and finally as a physical layout. Each of the blocks should be validated during the design process. Finally, the entire ADC should be validated and characterized.

1.3 Document Structure Overview

The organization of this thesis as follows. Chapter 2 reviews the fundamentals of ADCs and the parameters used to characterize them. Chapter 3 presents important concepts of SAR ADCs and an overview of techniques, technologies and methods used in state-of-art SAR ADCs. The design of the SAR ADC is described in detail in Chapter 4, covering all its blocks: DAC, switches, delay cell, comparators and logic. In Chapter 5, the results of the simulation of the entire SAR ADC design are presented and discussed. Finally, Chapter 6 presents conclusions, summarizes the achievements of this work and suggests future work to further improve the ADC.

Chapter 2

Fundamentals of ADCs

2.1 Overview

The Analog-to-Digital Converter (ADC) is a device whose function is to convert an analog signal (continuous in time and amplitude) into a digital signal (discrete in time and amplitude). One conversion can be divided in 3 steps: sampling, quantization and encoding.

First, the analog input signal is converted to a time discrete signal by sampling it at a certain sampling rate (f_s). Then, the signal is quantized, becoming discrete both in amplitude and time. Finally, encoding is performed such that in the end we can represent the digital signal with a certain number of bits (resolution), being the LSB the least significant bit and the MSB the most significant bit.

When the signal is sampled, some noise is added due to the thermal noise inherent to the transistors. Also, when the signal is quantized, some more noise is added since there is a limited number of discrete values that the output can have. All of this will limit the signal-to-noise ratio (SNR) of the ADC and, therefore, the effective number of bits (ENOB).

This chapter introduces some concepts needed to characterize ADCs and understand their specifications. Then, we will discuss the difference between Nyquist Rate ADCs and Oversampling ADCs. Finally, a quick overview of the most common ADC architectures is presented.

2.2 Characterization of ADCs

2.2.1 Static specifications

The characterization of an ADC regarding its static performance is given by the parameters that characterize the deviation of the actual transfer function from the ideal one. Some of them are listed and described below:

- **Monotonicity** – An ADC is monotonic if, for an increasing input analog voltage, the digital output code also increases. Monotonicity is especially important if the ADC is used in feedback control loops since a non-monotonic response can make a system unstable.

- **Offset Error** – Defined as the constant offset of the transfer function of the ADC relative to the ideal transfer function.

- **Gain Error** – Defined as the deviation of the slope of the transfer function of the ADC relative to the ideal transfer function.

- **Absolute Error** – Defined as the maximum deviation between the transfer function of the ADC and the ideal transfer function. It includes quantization error, offset error, gain error and non-linearity. An ideal ADC would have 0.5 LSB of absolute error due to the quantization error.

- **Differential Non-Linearity Error (DNL)** – Measures the deviation between the actual and the ideal step width for every output code (Figure 2.1). Non-linearity produces quantization steps with varying widths, some narrower and some wider.

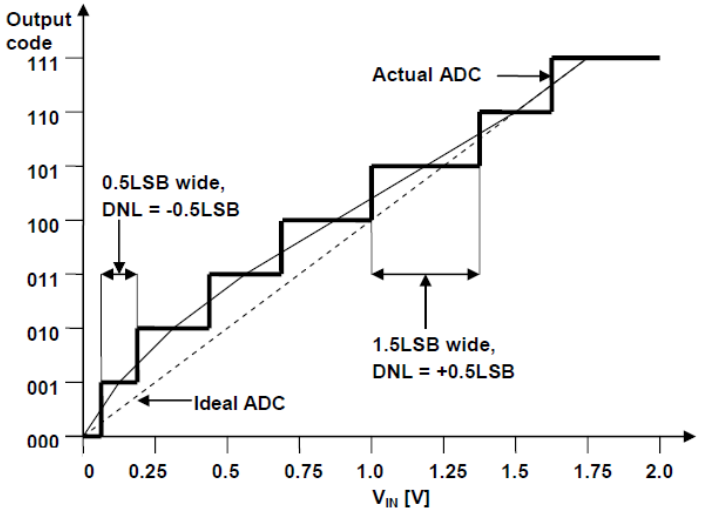

Figure 2.1 – DNL example [4].

- **Integral Non-Linearity Error (INL)** – Measures the deviation of the transfer function of the ADC from the ideal transfer function (Figure 2.2). It is possible to prove that INL can be determined by computing the cumulative sum of DNL.

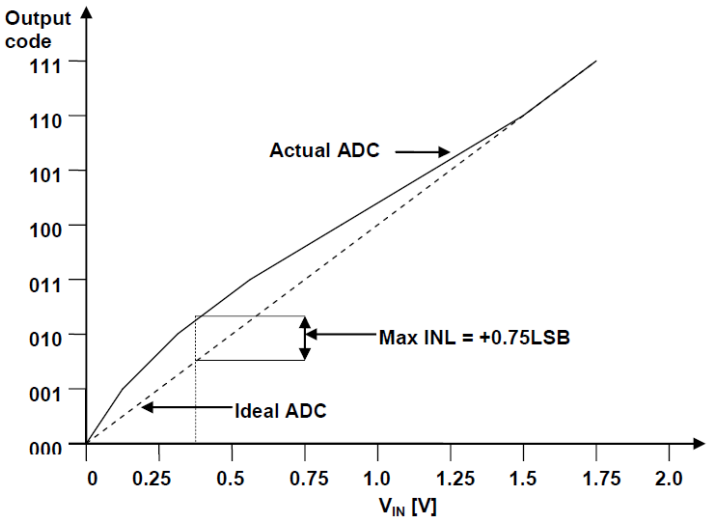

Figure 2.2 – INL example [5].

2.2.2 Dynamic specifications

For applications where the input signal is steady-state or has a very low frequency compared to the sampling frequency of the ADC, the static specifications are the most important. However, when the signal frequency is increased, other specifications should be used to determine the performance of the ADC in the frequency domain. Some of these specifications are listed and described below:

- **Signal to Noise Ratio (SNR)** – Ratio between the power of the signal and the noise power, excluding harmonic distortion. SNR is usually expressed in dB as in Equation 2.1.

$$SNR\left[dB\right] = 10\log_{10}\frac{P_{signal}}{P_{noise}} \tag{2.1}$$

  For a given resolution N, the best achievable SNR for a Nyquist Rate ADC is expressed in Equation 2.2.

$$SNR\left[dB\right] \approx 6.02N + 1.76 \tag{2.2}$$

- **Signal to Noise and Distortion Ratio (SNDR)** – Ratio between the power of the signal and the noise power, including harmonic distortion. SNDR can be expressed in dB as in Equation 2.3.

$$SNDR\left[dB\right] = 10\log_{10}\frac{P_{signal}}{P_{noise} + \sum_{i=2}^{\infty} P_i} \tag{2.3}$$

- **Effective Number of Bits (ENOB)** – Is computed by substituting the measured SNDR value into the equation that describes the SNR for an ideal ADC and solving for N, the number of bits. Equation 2.4 shows the calculation of the ENOB.

$$ENOB\left[bit\right] \approx \frac{SNDR\left[dB\right] - 1.76}{6.02} \tag{2.4}$$

- **Total Harmonic Distortion (THD)** – Ratio between the power of the harmonics at the output of the converter and the power of the fundamental. Equation 2.5 shows the calculation of the THD.

$$THD\left[dB\right] = 10\log_{10}\frac{\sum_{i=2}^{\infty} P_i}{P_1} \tag{2.5}$$

- **Spurious Free Dynamic Range (SFDR)** – Ratio of the level of the signal to the level of the highest distortion component in the FFT spectrum.

2.3 Nyquist Rate vs Oversampling Converters

The ADCs can be divided in two categories depending on their sampling rate: Oversampling ADCs and Nyquist Rate ADCs. A Nyquist Rate ADC samples the input signal at the minimum possible frequency to avoid aliasing, which is twice the signal bandwidth. Most of the ADC architectures fit in this category, like Flash, SAR and Pipeline.

An Oversampling ADC samples the input signal at a frequency higher than twice the signal bandwidth. These ADCs spread the quantization noise across a bigger range of frequencies, allowing them to have smaller integrated quantization noise in the range of frequencies of interest. The quantization noise that lays outside of the band of interest can be filtered. The most common ADC architecture in this category is the Delta Sigma. The Delta Sigma uses not only oversampling but also noise shaping to further reduce the quantization noise.

2.4 Nyquist Rate Architectures

2.4.1 Flash

A circuit diagram of a Flash ADC is presented in Figure 2.3. An N-bit flash ADC is composed by 2^N-1 comparators. The reference voltages are provided to the comparators by a resistive divider of 2^N resistors. The reference voltage for each comparator is one LSB greater than the reference voltage for the comparator immediately below it. The output of the comparators is thermometer code encoded. This name is used because similarly to a mercury thermometer in which the mercury column always rises to the appropriate temperature and no mercury is present above that temperature, in this ADC the output of the comparators with reference voltages bellow the input signal voltage are high and the output of the comparators above those are low. A priority encoder, finally, converts the thermometer code to the appropriate digital code.

These ADCs are usually the fastest and that is the reason why they are used in applications requiring very large bandwidths and very large sampling rates. However, these converters consume considerable power and have low resolution (usually not more than 8 bit).

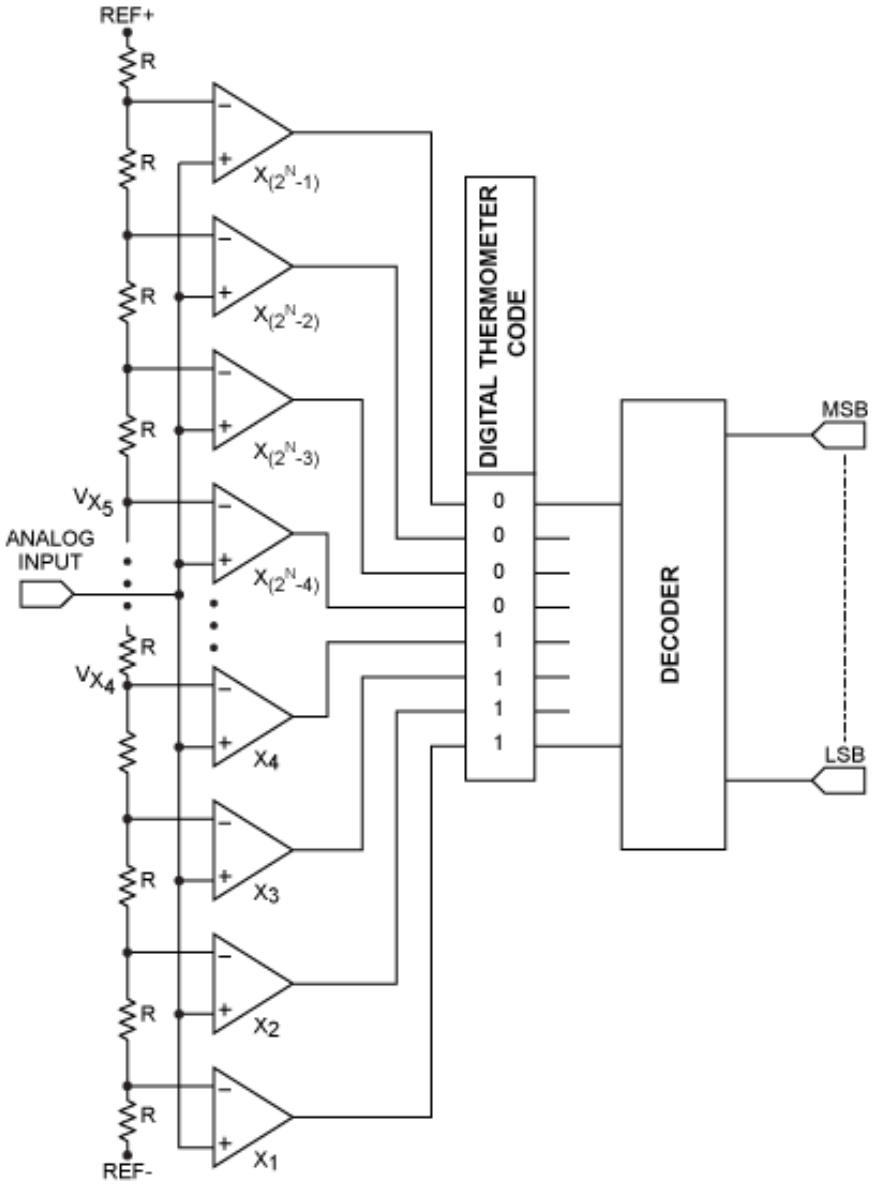

Figure 2.3 – Flash ADC block diagram [6].

2.4.2 Successive Approximation Register

The Successive Approximation Register (SAR) ADC is frequently the architecture of choice for medium to high resolution applications. Although there are many variations regarding the implementation, the basic block diagram is presented in Figure 2.4.

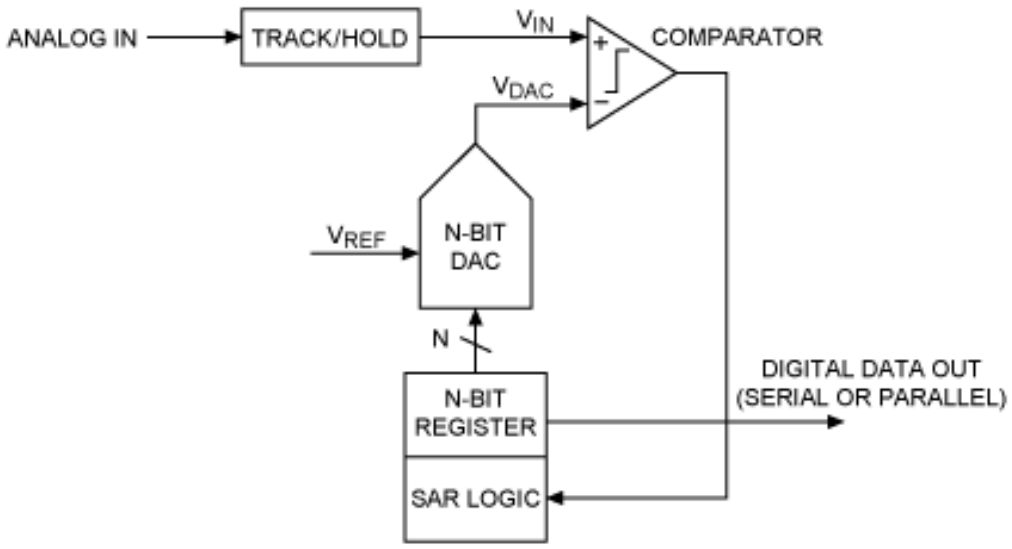

Figure 2.4 – SAR ADC block diagram [7].

The SAR ADC uses a binary search algorithm. The analog input signal is first sampled at the sample and hold (S/H). Then, the MSB bit of the register is set high. This sets the DAC output voltage to half the reference voltage, allowing the comparator to find out if the sampled signal's voltage is higher or lower than this threshold. If the voltage of the sampled signal is higher than half the reference voltage, the output of the comparator goes high and the MSB remains at '1'. However, if the output of the comparator is low, the MSB is cleared to '0'. The controller then moves to the next bit, forces that bit high and does another comparison. This process is repeated for all bits until the result of the conversion is present at the register.

The speed of the SAR ADC is limited by the required sampling time, the settling time of the DAC, the comparator's speed and the logic's speed.

2.5 Oversampling Architectures

2.5.1 Delta Sigma

The Delta Sigma ADC is an oversampling ADC because the sampling frequency is much higher than twice the signal's bandwidth. A block diagram of a Delta Sigma modulator is represented in Figure 2.5. The input signal is sampled at the 1-bit ADC (which is nothing more than a comparator) at a frequency much higher than the required bandwidth such that the quantization noise gets spread through a broader range of frequencies. Posterior filtering allows to remove the quantization noise that lies outside the frequencies of interest. The oversampling alone, however, is not enough to provide the high resolutions that Delta Sigma ADCs are known for. The SNR of a 1-bit Nyquist Rate ADC is 7.78 dB (Equation 2.2). It can be shown that each factor-of-4 oversampling increases the SNR by 6 dB and each 6 dB increase is equivalent to gaining one bit of ENOB. Having this in consideration, to achieve an effective resolution of 12-bit with a bandwidth of 20 kHz which would be adequate for audio applications, one would need an oversampling factor of 4^{11}. The sampling frequency would need to be at least 168 GHz, which is not feasible. Fortunately, Delta Sigma ADCs overcome this limitation using the technique of noise shaping.

Noise shaping is the technique of passing the quantization noise through a different transfer function than the signal in a way that the high-pass nature of the noise transfer function shapes the quantization noise to further reduce it in the frequencies of interest. Digital filtering and decimation are then able to filter the unwanted quantization noise and reduce the data rate frequency.

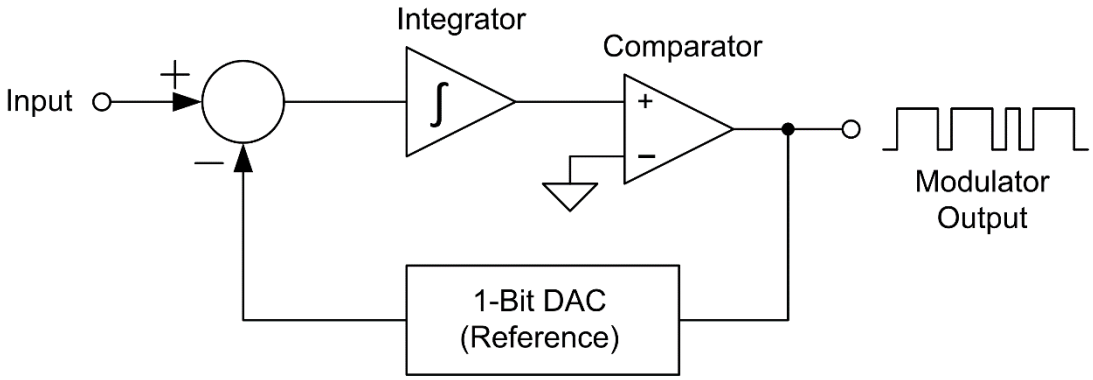

Figure 2.5 – Delta Sigma modulator block diagram [8].

Chapter 3

SAR ADC Concepts

3.1 Binary Search Algorithm

As mentioned in the last chapter, a conversion starts with the sampling of the analog input signal. Then, the sampled signal is quantized. Quantization is the search for the closest decision level and the corresponding digital code to the analog sampled input signal (V_{in}). Since the quantization takes considerably more time in a SAR ADC than the sampling, it is target of more research. An ideal N-bit quantizer has 2^N-1 decision levels over its full-scale range. Since there is a difference between the closest decision level and V_{in}, noise is introduced in the quantization process, referred as quantization noise.

Flash ADCs employ an exhaustive search algorithm, since the sampled signal is compared with all the 2^N-1 decision levels at the same time. Although it is time efficient to directly compare the sampled signal with all the decision levels at the same time, the required number of comparators grows exponentially with N. Thus, the power consumption and the circuit complexity increase exponentially. The offset of the comparators and other mismatches end up limiting the ENOB of these converters to about 8-bit. SAR ADCs, on the other hand, use a binary search algorithm, allowing them to consume very low power and to achieve larger resolutions. The binary search algorithm works iteratively: the search range is divided in two halves and a decision is made about whether the sampled analog signal is in the top or bottom half of the search range. Then, this process is repeated and the updated search range (the chosen half in the last iteration) is divided in half again (hence the name of the algorithm) and a decision is made. This iterative process continues until a certain resolution (number of bits) is achieved.

It is obvious that the binary search is usually slower than the exhaustive search, since it works iteratively. However, in the binary search only one comparator is needed because only one decision is made in each iteration. Thus, the complexity of the circuit doesn't grow exponentially as before, at least with respect to the number of comparators. The power consumption is also lower, since one conversion needs N decisions (comparisons), while the exhaustive search algorithm requires 2^N-1 decisions.

Figure 3.1 shows an example of a conversion using binary search. The input signal V_{in} is compared with half of the full-scale range, 0 in this example. Since the input signal is higher than 0, the comparator outputs '1' and now the search range is confined to the upper half of the full-scale range (0 to 1). Similarly, if the input signal was lower than 0, the comparator would output '0' and the search range would be confined to the lower half of the full-scale range (-1 to 0). This process is repeated 4 more times until the result of the conversion ('10101') is achieved.

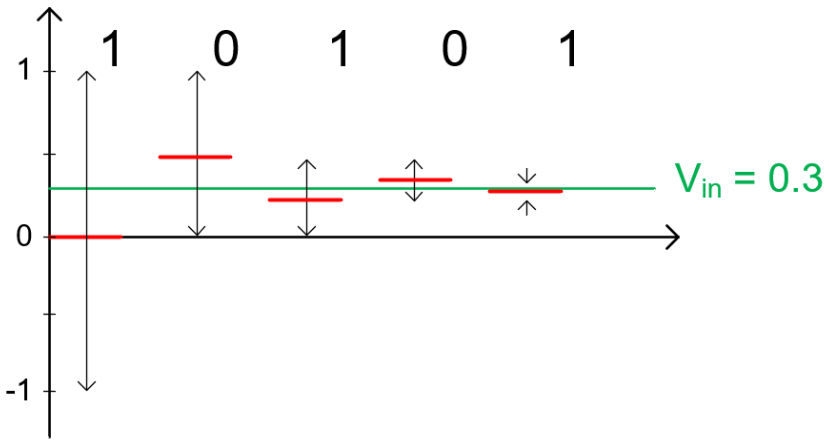

Figure 3.1 – Example of a conversion using binary search algorithm.

3.2 Charge Redistribution SAR ADC Architecture

The block diagram of a typical N-bit Charge Redistribution (CR) SAR ADC single-ended implementation is represented in Figure 3.2. The first SAR ADC based on CR principle was proposed in 1975 by McCreary *et al.* [9]. This SAR ADC implementation combines the S/H with the capacitive DAC. In a typical implementation the capacitors are sized with a radix of 2 ($C_i = 2C_{i-1}$).

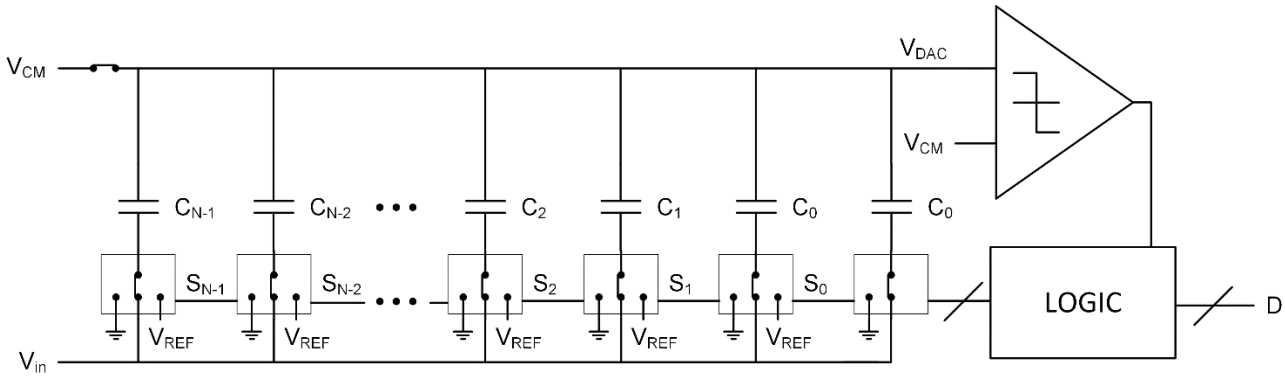

Figure 3.2 – Charge Redistribution SAR ADC circuit diagram.

All the DAC capacitors have the top plates connected. The bottom plates can be connected to GND, V_{REF} or V_{IN}, while the top plates can be connected to V_{CM} or left floating. The logic block controls these switches and determines D, the N-bit conversion result.

The circuit working principle is illustrated in Figure 3.3 (a)-(d). In Figure 3.3 (a), the input is being sampled. The top plates of the capacitors are connected to V_{CM} and the bottom plates of the capacitors are connected to the input signal V_{in}. At the sampling instant, the switch that connects the top plates to V_{CM} opens, and the charge stored on the top plates of the capacitors is:

$$Q_x = (V_{CM} - V_{IN})C_{tot}, \tag{3.1}$$

where $C_{tot} = \sum_{i=0}^{N-1} C_i + C_0$.

Figure 3.3 (b) illustrates the first conversion step. The bottom plate of the capacitor C_{N-1} is connected to V_{REF} and the bottom plates of all the other capacitors are connected to ground. One can recalculate the charge Q_x stored in the top plates:

$$Q_x = (V_{DAC} - V_{REF})C_{N-1} + V_{DAC}(C_{tot} - C_{N-1}) \tag{3.2}$$

Since the top plates of the capacitors are floating, the total stored charge is conserved. The voltage V_{DAC} at the input of the comparator can be calculated with Equations 3.1 and 3.2, as shown in Equation 3.3.

$$V_{DAC} = V_{CM} - V_{in} + V_{REF}\frac{C_{N-1}}{C_{tot}} \tag{3.3}$$

The comparator checks whether V_{DAC} is above or below V_{CM}. If the capacitors are binary weighted, then $C_{tot} = 2C_{N-1}$ and the current decision level is set to half of V_{REF}, which is half the search range. If V_{DAC} is above V_{CM}, then the MSB b_{N-1} is '1'. In this situation, the capacitor C_{N-1} remains connected to V_{REF} and the bottom plate of capacitor C_{N-2} is now also connected to V_{REF}, as illustrated in Figure 3.3 (c). Now we are ready to determine the bit b_{N-2} by performing one more comparison.

Figure 3.3 (d) illustrates the behaviour in case b_{N-1} is '0'. In this situation, the bottom plate of capacitor C_{N-1} is connected to ground and the search continues through the lower half of the search range. Capacitor C_{N-2} is connected to V_{REF} to determine the next bit. The process is then repeated and after N iterations, N bits are resolved. After all bits are resolved, V_{DAC}-V_{CM} becomes the quantization error (the difference between the sampled input signal and the output of the ADC), as expressed by Equation 3.4.

$$V_{DAC} - V_{CM} = -V_{in} + V_{REF}\sum_{i=0}^{N-1}\frac{b_i C_i}{C_{tot}} \tag{3.4}$$

The group of bits that minimize the quantization error is D = [b_{N-1}, b_{N-2}, …, b_1, b_0]. The dummy capacitor C_0 is in the DAC to define the highest decision level at a voltage of V_{REF} - V_{LSB}. The bottom plate of this dummy capacitor should be connected to the input signal V_{IN} during sampling and should remain connected to ground during the rest of the conversion.

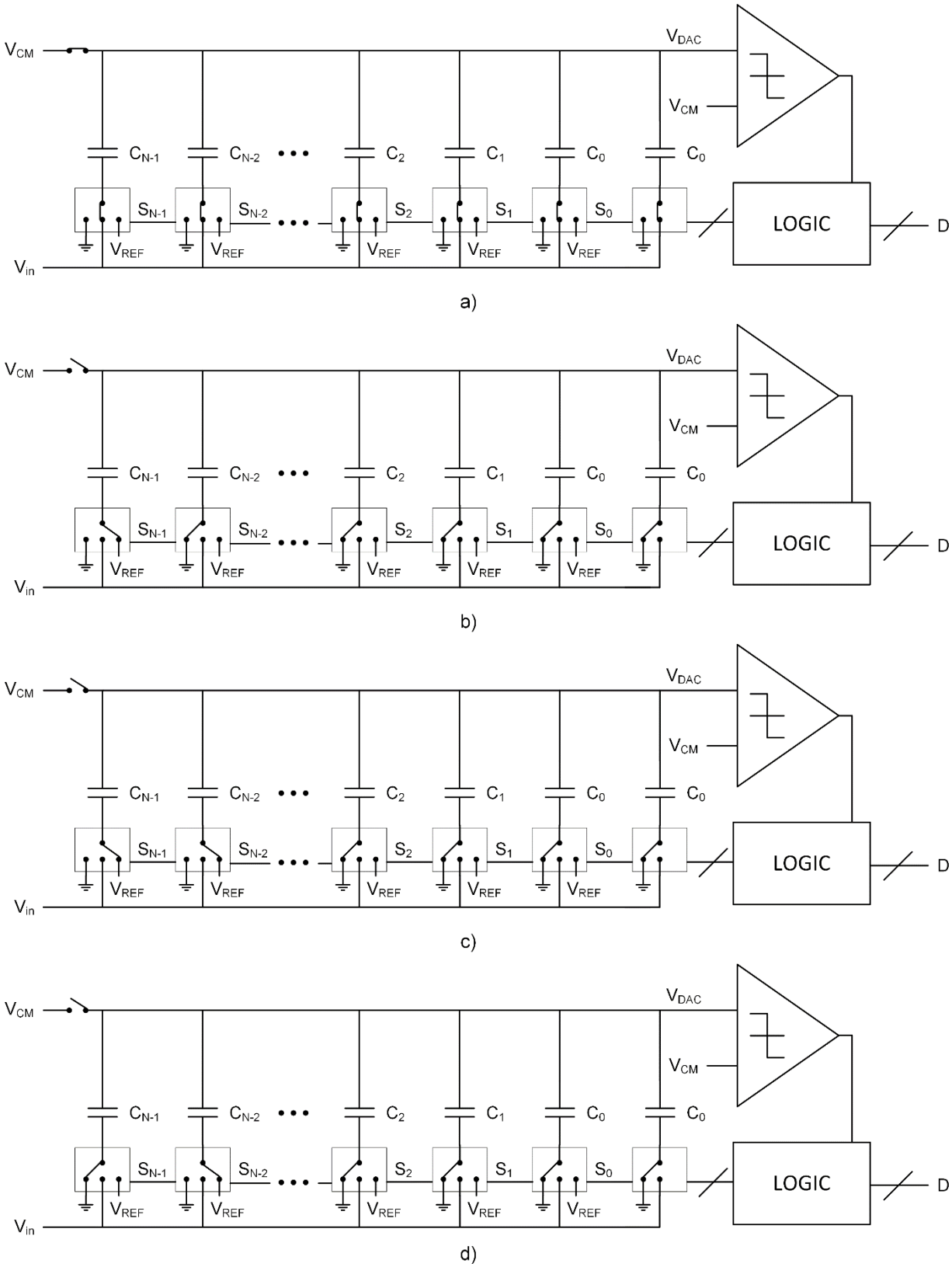

Figure 3.3 – CR SAR ADC operation example.

3.3 Bootstrapped Switch

Transistors have been used as switches since 1950s [10]. A MOSFET in the triode region ($V_{DS} < V_{GS} - V_{Th}$) behaves as a resistor whose resistance is controlled by its gate-to-source voltage, as shown in Equation 3.5.

$$R_{DS} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{Th})} \tag{3.5}$$

Using a simple MOSFET as a switch, as depicted in Figure 3.4, has several issues. As the input voltage rises, the resistance of the NMOS increases until it completely stops conducting when the gate-to-source voltage drops below the threshold voltage. Therefore, the input range is quite limited.

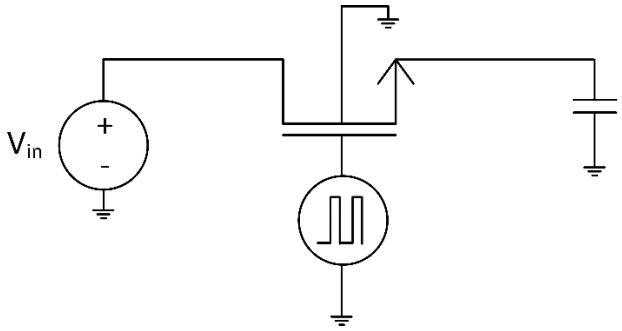

Figure 3.4 – NMOS transistor as a switch.

This problem is easily solved using the complementary topology shown in Figure 3.5. When the NMOS transistor is not conducting, the PMOS transistor takes over and keeps the switch resistance low. Similarly, when the input voltage drops below the threshold voltage of the PMOS transistor and it turns off, the NMOS transistor takes over and keeps the switch conducting. Although this switch has solved the limited input range of the single transistor switch, its on-resistance is still a heavy function of the input voltage. The on-resistance of the complementary switch is the on-resistance of the PMOS and NMOS transistors in parallel. At around half the input voltage range (depending on the sizing of the transistors and the technology parameters) the switch has its maximum on-resistance, achieving the minimum on-resistance at the extremes of the input voltage range. Although it might not be a problem in some applications, the variation of the on-resistance with the input voltage modulates the phase shift of the sampling circuit [10], generating distortion. Both the limited input range and the on-resistance modulation by the input signal can be solved resorting to the bootstrapping technique. The bootstrapping technique, as exemplified in Figure 3.6, forces a constant V_{GS} across the transistor. The on-resistance of the transistor is kept constant by fixing V_{GS} to a constant value instead of the gate voltage (with respect to ground). The input range problem is also fixed, since the gate voltage can rise above the supply voltage.

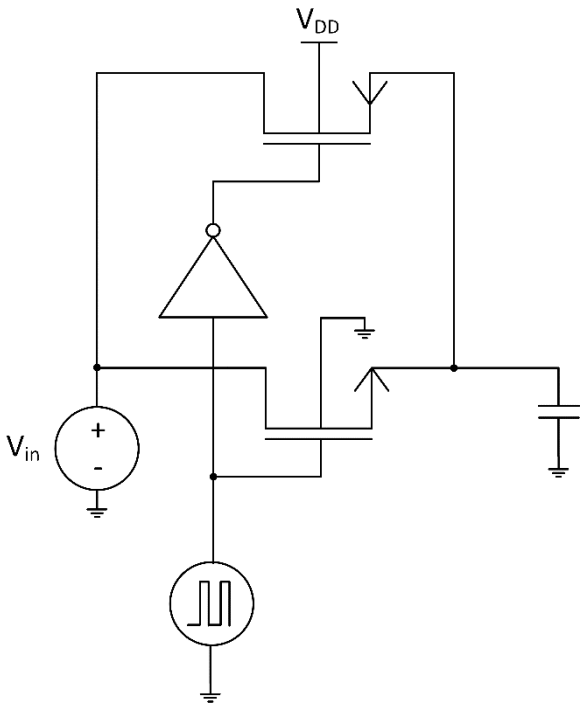

Figure 3.5 – The complementary switch solves the limited input range of the single transistor switch.

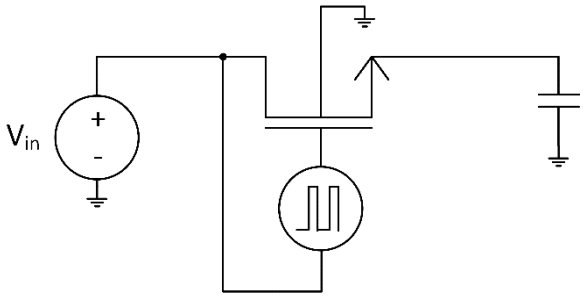

Figure 3.6 – The bootstrapped switch to the rescue.

These three switch topologies were simulated and their on-resistances were measured using *Cadence Virtuoso*. The PMOS transistor was set larger than the NMOS to compensate for the lower mobility. The results obtained are summarized in Figure 3.7. Notice that even though V_{GS} is kept constant in the bootstrapped switch, its on-resistance still increases slightly with the input voltage. This happens because the body of the transistor is not tied to the source. Therefore, its threshold voltage varies with the input voltage. This is usually called “body effect”.

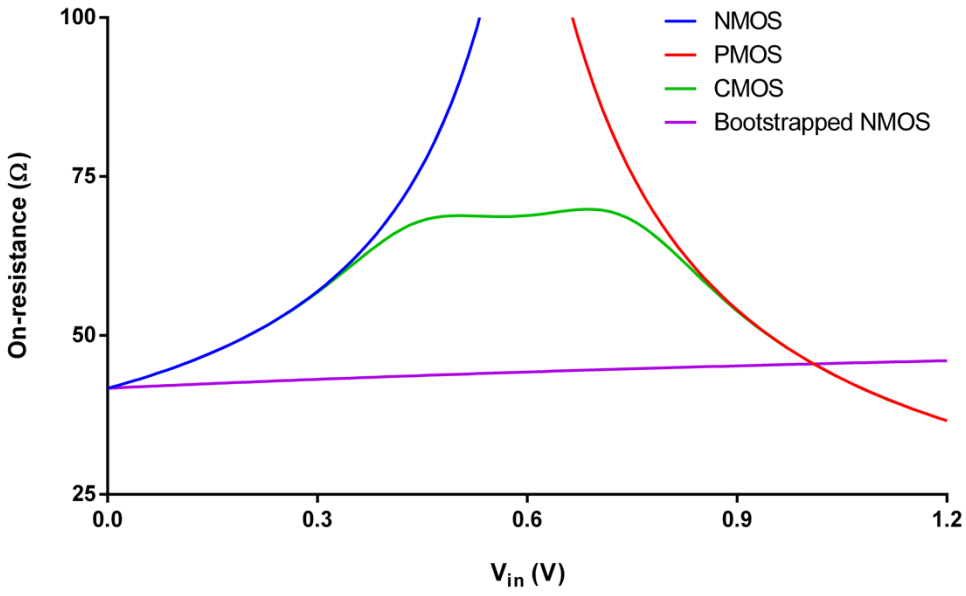

Figure 3.7 – Comparison of the on-resistance of several switch topologies.

3.4 Bottom-plate Sampling Technique

As depicted in Figure 3.8, a charge Q_{ch} is formed at the channel surface when a transistor is conducting, which is described in Equation 3.6. When the transistor is switched off, this charge is released to the source and to the drain. This injection of charge into the DAC and sampling capacitors can degrade the dynamic performance of the ADC if it has a non-linear signal dependency.

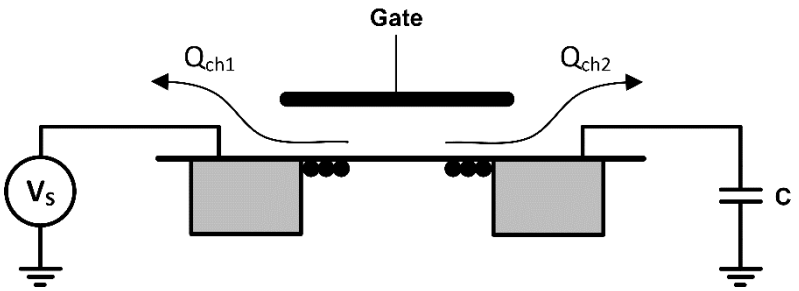

Figure 3.8 – Charge formed at the channel surface.

$$Q_{ch} = WLC_{ox}(V_{GS} - V_{Th}) \tag{3.6}$$

As shown in Equation 3.6, the charge formed at the channel surface is dependent on V_{GS}, but also on the threshold voltage. The threshold voltage V_{Th} varies non-linearly with the source-to-body voltage V_{SB}, as seen in Equation 3.7.

$$V_{Th} = V_{T0} + \gamma\left(\sqrt{\left|2\Phi_F + V_{SB}\right|} - \sqrt{\left|2\Phi_F\right|}\right) \quad (3.7)$$

To make sure that the charge injected into the DAC at the end of the sampling process does not degrade the performance of the ADC, this charge should be kept constant and should not be signal dependent. The V_{GS} of all switches is kept always constant if bootstrapping is used. Therefore, our attention should be focused on the V_{Th}. The switch that connects the top plates of the DAC capacitors to V_{CM} has a constant and signal independent (at least to first order) threshold voltage, since its V_{SB} is constant. However, the switches that connect the bottom plates of the DAC to the analog input signal have a signal dependent V_{SB}. Thus, their threshold voltage is not constant and the charge stored in the channel is also not constant. It becomes clear by now that the V_{CM} switch should be open first to inject a constant and signal independent charge into the DAC capacitors. After opening this switch, the top plates of the DAC are floating and no further charge can be injected into the DAC capacitors. This means that if the V_{IN} switches are open after the V_{CM} switch, their stored charge is not injected into the DAC. This technique is called “bottom-plate sampling”. In a single-ended ADC implementation, this constant charge injected in the DAC would translate into a constant offset error in the ADC transfer function, not introducing non-linearity errors. In a differential ADC implementation, the offset error is eliminated due to its differential nature.

3.5 Switching Schemes Comparison

Since the sampling switches are open during the conversion phase, the total charge in the top plates of the capacitors is kept constant. However, as the voltages of the bottom plates change, the charge of each capacitor also changes. So, some charge flows into and out of the bottom plates and, therefore, energy is spent to change the charge of each capacitor. The amount of energy that is spent depends on the switching scheme that is used during the conversion. Some of the most relevant switching schemes are presented here.

3.5.1 Conventional Switching Scheme

Figure 3.9 shows the conventional switching scheme for a 3-bit ADC in a differential implementation. During the sampling phase, the differential input signal is connected to the bottom plates and the top plates are connected to V_{CM}. After sampling, the input signal is disconnected from the bottom plates and V_{CM} is disconnected from the top plates. The bottom plate of the MSB capacitor is connected to V_{REF} and the remaining bottom plates are connected to ground for the top array. The opposite is done for the bottom array. This operation has an energy consumption of $4CV_{REF}^2$. The comparator then determines the first bit. If the determined bit is ‘0’, then the switching scheme takes the down transition and if the determined bit is ‘1’, then the switching scheme takes the up transition. This switching scheme is clearly

not optimized for energy consumption, since it takes more than 75% of the total energy consumption just to determine the sign bit. This bit can be determined by directly comparing V_{IN+} and V_{IN-} without consuming any energy. We can also see that the energy consumption is much lower in the up transitions than in the down transitions. This happens because in the up transitions only two bottom plate connections are changed while in the down transitions four bottom plate connections must be changed. The average switching energy for an N-bit ADC using conventional switching scheme is:

$$E_{conv} = \sum_{i=1}^{N} 2^{N+1-2i}\left(2^{i}-1\right)CV_{REF}^{2} \tag{3.8}$$

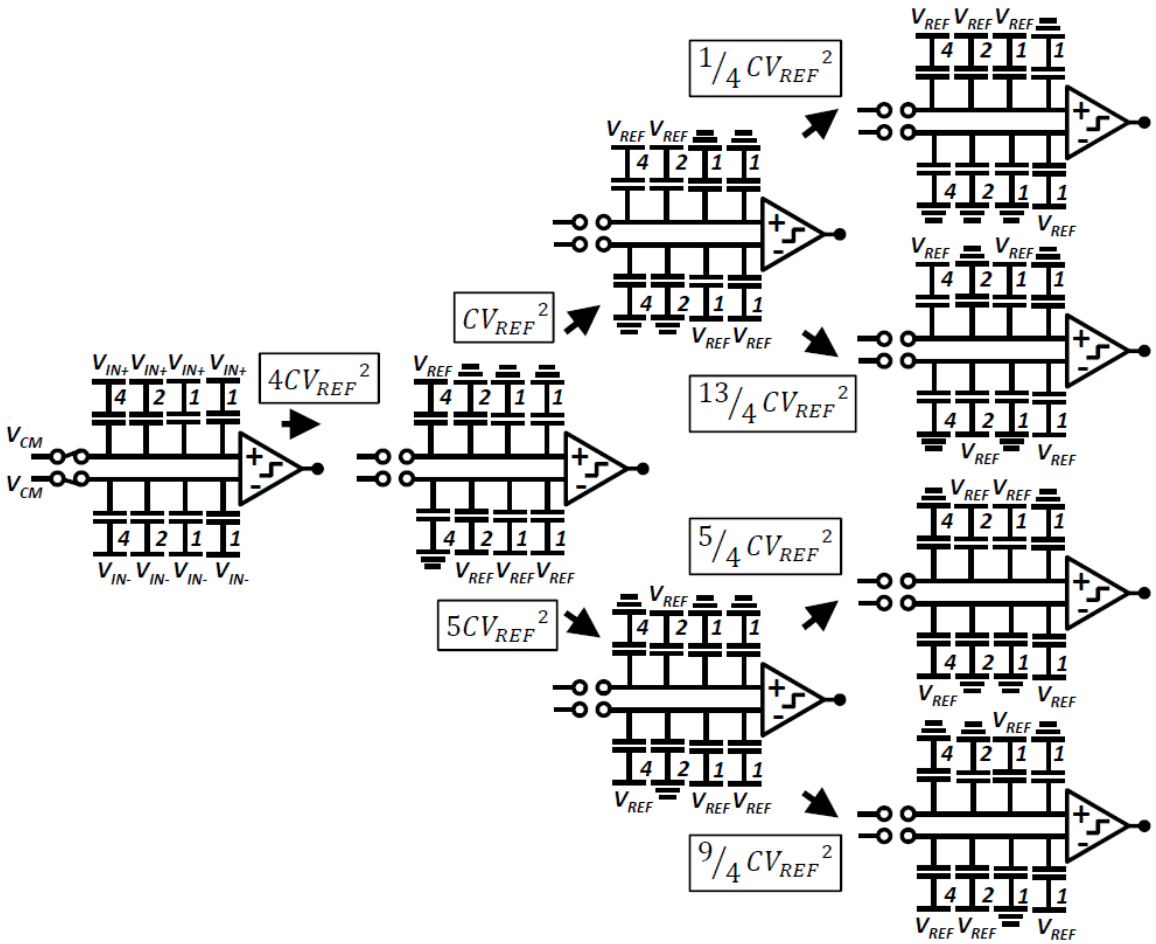

Figure 3.9 – Conventional switching scheme with energy consumption of every conversion step [11].

3.5.2 Monotonic Switching Scheme

This switching scheme was proposed by Liu *et al.* [12] and is depicted in Figure 3.10. This switching scheme is an improvement compared to the conventional switching scheme: there is no energy spent in determining the sign bit since the sampling is done by connecting the input signal to the top plates and there are no operations that require changing a previously set bottom plate voltage. The sign bit is determined just by comparing V_{IN+} and V_{IN-}, allowing the MSB capacitor to be removed. As a result, this

switching scheme consumes 81% less energy compared to the conventional switching scheme. However, this switching scheme is not insensitive to parasitic capacitances between top plates and ground, because the input signal is also sampled into the parasitic capacitances. Thus, a gain error is introduced. The average switching energy for an N-bit ADC using monotonic switching scheme is:

$$E_{conv} = \sum_{i=1}^{N-1} 2^{N-2-i} C V_{REF}^2 \tag{3.9}$$

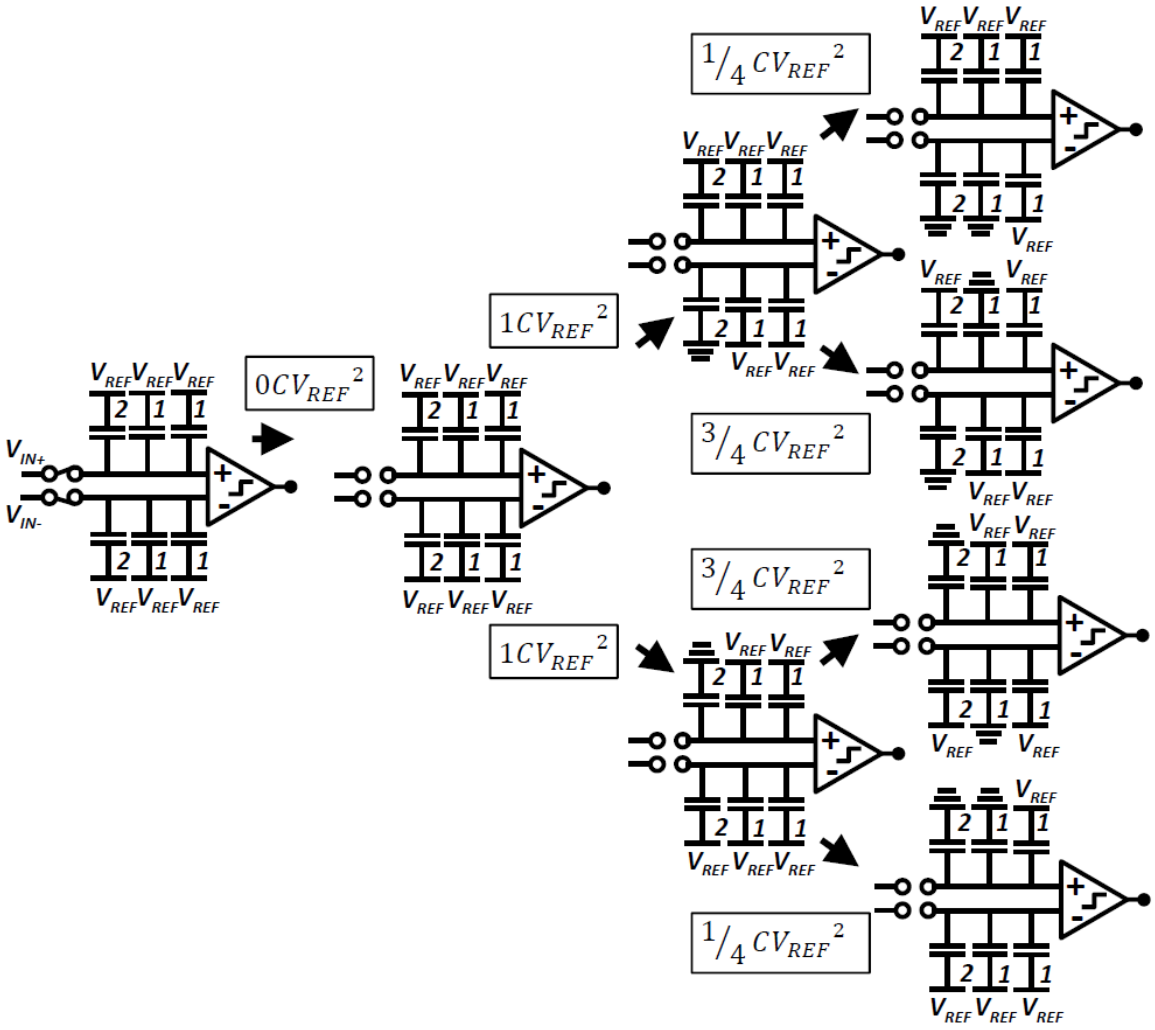

Figure 3.10 – Monotonic switching scheme with energy consumption of every conversion step [11].

3.5.3 Merged Capacitor Switching Scheme

This switching scheme was proposed by Hariprasath *et al.* [13] and is depicted in Figure 3.11. Just like the previous switching scheme, top plate sampling is used and, therefore, this switching scheme is not insensitive to parasitic capacitances. Every transition involves changing just two bottom plate connections. This switching scheme consumes 94% less energy compared to the conventional one. The average switching energy for an N-bit ADC using merged capacitor switching scheme (MCS) is:

$$E_{conv} = \sum_{i=1}^{N} 2^{N-3-2i}\left(2^{i}-1\right)CV_{REF}^{2} \tag{3.10}$$

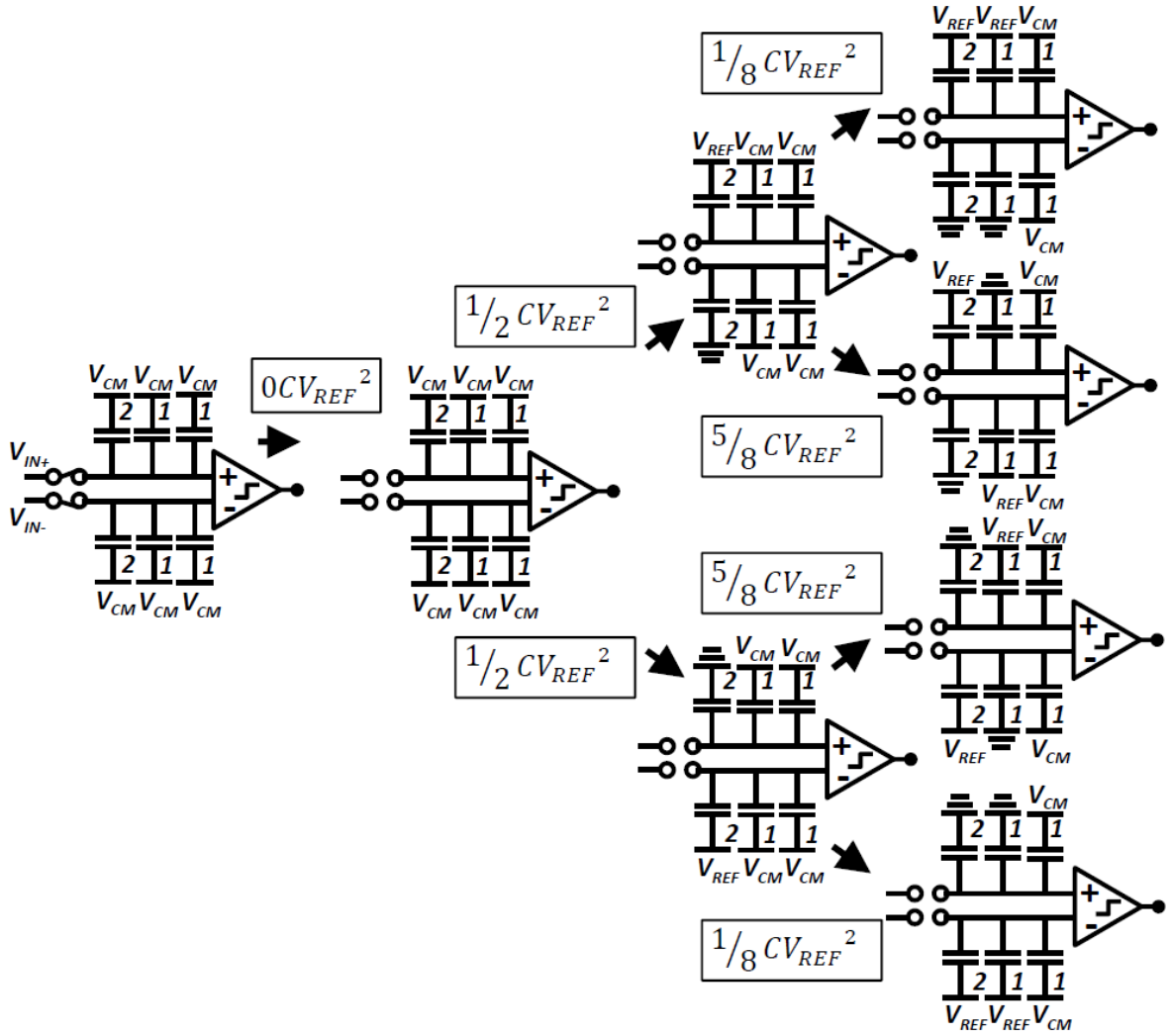

Figure 3.11 – MCS switching scheme with energy consumption of every conversion step [11].

3.5.4 Inverted Merged Capacitor Switching Scheme

This switching scheme was proposed by Chang [11]. The key idea is to bring the insensitivity to parasitic capacitances to the MCS switching scheme by sampling the input signal into the bottom plates instead of into the top plates. The signal is sampled by connecting the top plates to V_{CM} and the bottom plates to the input signal. After sampling, the sampling switches that connect the input signal to the bottom plates and V_{CM} to the top plates are open and the bottom plates are connected to V_{CM}. The remaining operations are the same as in the MCS switching scheme. The inverted merged capacitor switching scheme (IMCS) ensures that the input signal is not sampled into the parasitic capacitances of the top plates to ground. With the correct switching sequence, it is also possible to make the charge injection from the switches constant, making the result insensitive also to charge injection. Regarding the energy

consumption, the average energy consumption of the IMCS algorithm is the same as the average energy consumption of the MCS algorithm, as given by Equation 3.10. The working principle of this switching scheme is depicted in Figure 3.12.

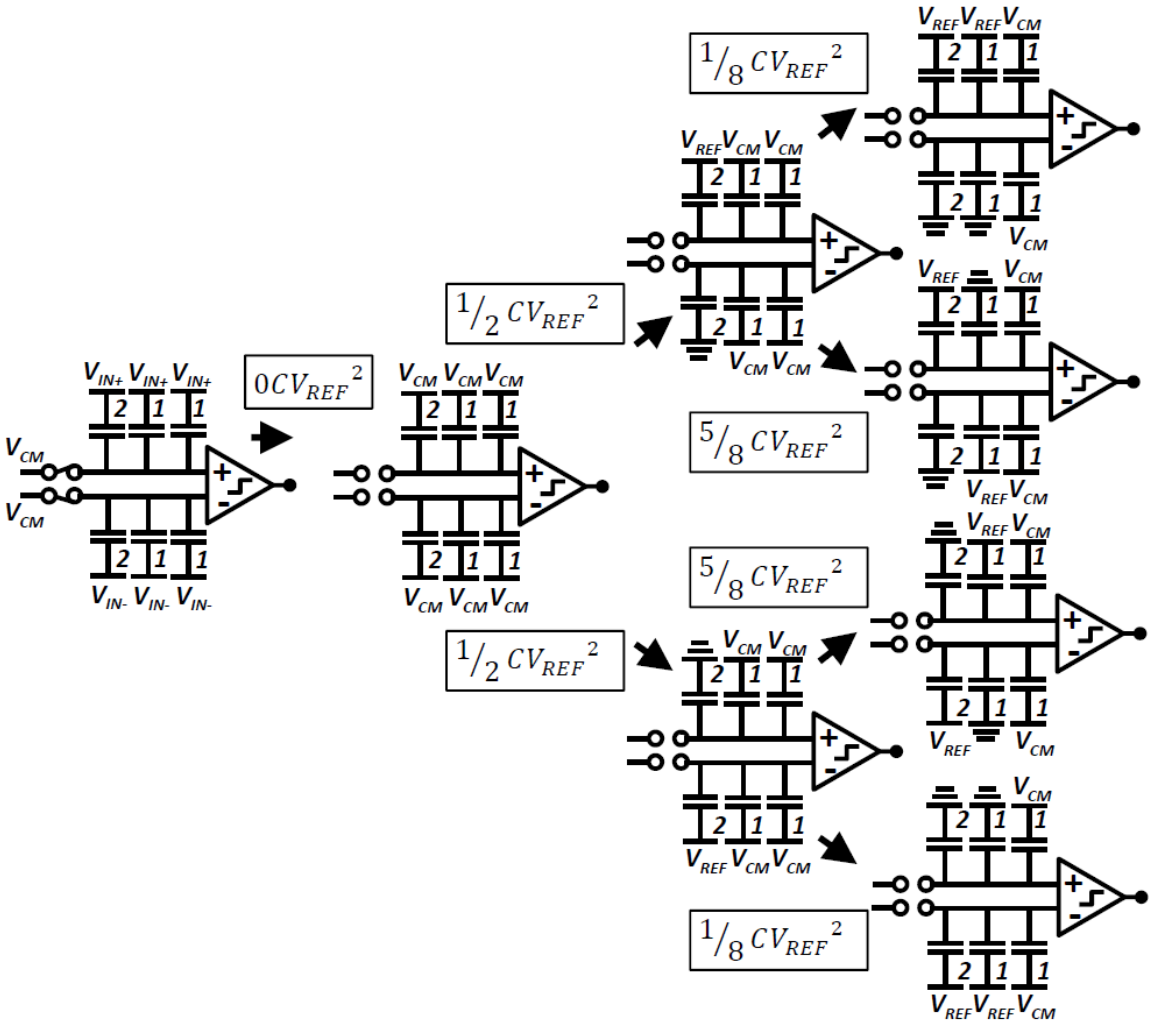

Figure 3.12 – IMCS with energy consumption of every conversion step [11].

3.5.5 Overview of the Switching Schemes

The highest energy efficiency is achieved by the MCS and IMCS switching schemes. In terms of area, the MCS and IMCS are also superior, since they only require half the DAC capacitance of the conventional and monotonic switching schemes. In the IMCS switching scheme the input signal is sampled into the bottom plates of the DAC capacitors. For this reason, the IMCS switching scheme also presents insensitivity to parasitic capacitances of the DAC. These characteristics are compared in Table 3.1. The average energy consumption (normalized to CV_{REF}^2) of the four discussed switching schemes for different resolutions is plotted in Figure 3.13.

Table 3.1 – Comparison of the four switching schemes regarding total DAC capacitance, sensitivity to parasitic capacitances and average energy consumption.

Switching Scheme	Total Capacitance (normalized)	Sensitive to Parasitic Capacitances	Energy Consumption
Conventional	1	No	100%
Monotonic	1	Yes	18%
MCS	½	Yes	6%
IMCS	½	No	6%

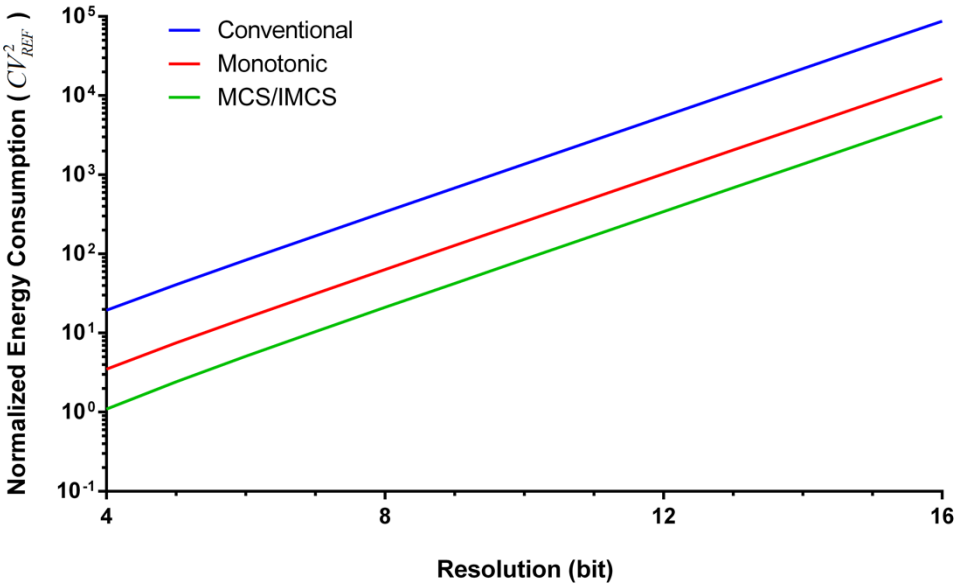

Figure 3.13 – Comparison of the energy consumption of the four switching schemes.

3.6 Sampling Noise

Quantization noise was already referred in Chapter 2. While quantization noise is related to the limited number of values the output of the ADC can have, sampling noise is related to thermal noise inherent to the transistors used in the sampling circuit. Let's use the sampling circuit of Figure 3.6 with the bootstrapped switch as an example to analyze the sampling noise. Since the transistor will be operating mainly in the triode region, it behaves as a resistor. Thus, the noise generated by the transistor is equivalent to the noise generated by a resistor. An equivalent sampling circuit is depicted in Figure 3.14, where the resistor is replaced by a noiseless resistor in series with a voltage source representing the resistor noise.

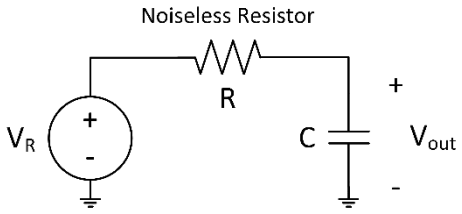

Figure 3.14 – Equivalent sampling circuit.

The thermal noise generated by the resistor is white, meaning that its power spectral density is constant over the entire frequency spectrum, as expressed in Equation 3.11.

$$S_v(f) = 4kTR\,, \tag{3.11}$$

where k is the Boltzmann constant (1.38×10^{-23} J/K) and T is the temperature expressed in Kelvin.

In this example circuit, the resistor noise is filtered by a first order RC low pass filter. The transfer function of the filter is:

$$\frac{V_{out}}{V_R}(s) = \frac{1}{RCs+1} \tag{3.12}$$

The output noise spectral density can be calculated by multiplying the input power spectral density by the power transfer function, which is the square magnitude of the transfer function given in Equation 3.12. The resulting output power spectral density is:

$$S_{out}(f) = 4kTR\frac{1}{(2\pi fRC)^2+1} \tag{3.13}$$

The average noise power can be calculated by integrating the output noise power spectral density over the entire frequency range, yielding the following result:

$$P_{n,out} = \int_0^\infty 4kTR\frac{1}{(2\pi fRC)^2+1}df = \frac{kT}{C} \tag{3.14}$$

It is interesting to note that although the noise is being generated by the resistor, the average noise power is independent from the resistor value. This happens because the noise power spectral density of the resistor is proportional to the resistance value and the circuit bandwidth is inversely proportional. The sampling noise is, therefore, only a function of the total DAC capacitance and will limit the SNR of the ADC. The SNR of the ADC having into account the quantization noise and sampling noise is expressed in Equation 3.15.

$$SNR[dB] = 10\log_{10}\frac{P_{signal}}{P_{n,quant}+P_{n,samp}} = 10\log_{10}\frac{\left(\frac{2^N}{2}\Delta\right)^2 \Big/ 2}{\frac{\Delta^2}{12}+K^2\Delta^2} \tag{3.15}$$

$$\approx 1.76 + 6.02N - 10\log_{10}\left(1+12K^2\right),$$

where N is the resolution of the ADC, Δ is the LSB voltage and K is the ratio between the sampling noise RMS voltage and the LSB voltage.

The ENOB loss due to the sampling noise is expressed in Equation 3.16 and depicted in Figure 3.15.

$$ENOB_{loss} \approx \frac{10\log_{10}(1+12K^2)}{6.02} \tag{3.16}$$

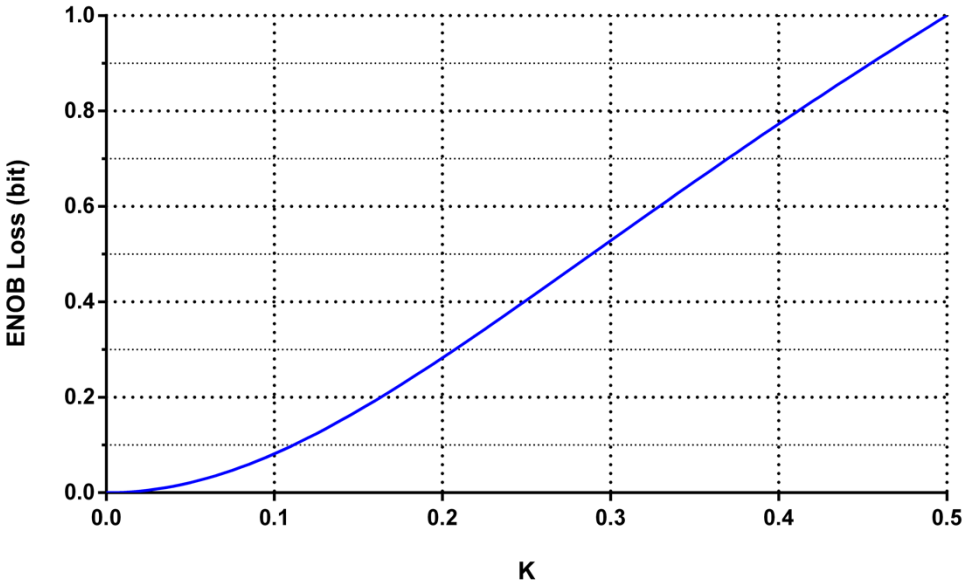

Figure 3.15 – ENOB loss due to sampling noise as a function of K.

3.7 Redundancy

With limited on-chip bypass capacitance, reference voltage bouncing increases the DAC settling time in conventional binary search SAR ADCs. This happens especially when large DAC capacitors are used, either for good matching or to have low kT/C noise. An approach to alleviate this issue is to use

redundancy in the conversion steps [3]. A redundant ADC is one in which several output codes have an overlap with respect to the analog range of the input signal that they cover. This means that errors early in the conversion process can be absorbed in the redundant ranges of the later steps, as demonstrated in Figure 3.16 Thus, the DAC settling accuracy of the most MSB conversion steps can be relaxed. Redundancy also allows the usage of digital calibration to calibrate for DAC mismatches due to the overlap in parts of the ADC transfer function. There are several ways of implementing redundancy in the ADC. The simplest one is to build it in the DAC by sizing the capacitors in a sub-binary way, leading to a sub-radix-2 approach. In a sub-radix-2 ADC more conversion steps are required to achieve a certain SNR due to the smaller sub-binary step sizes.

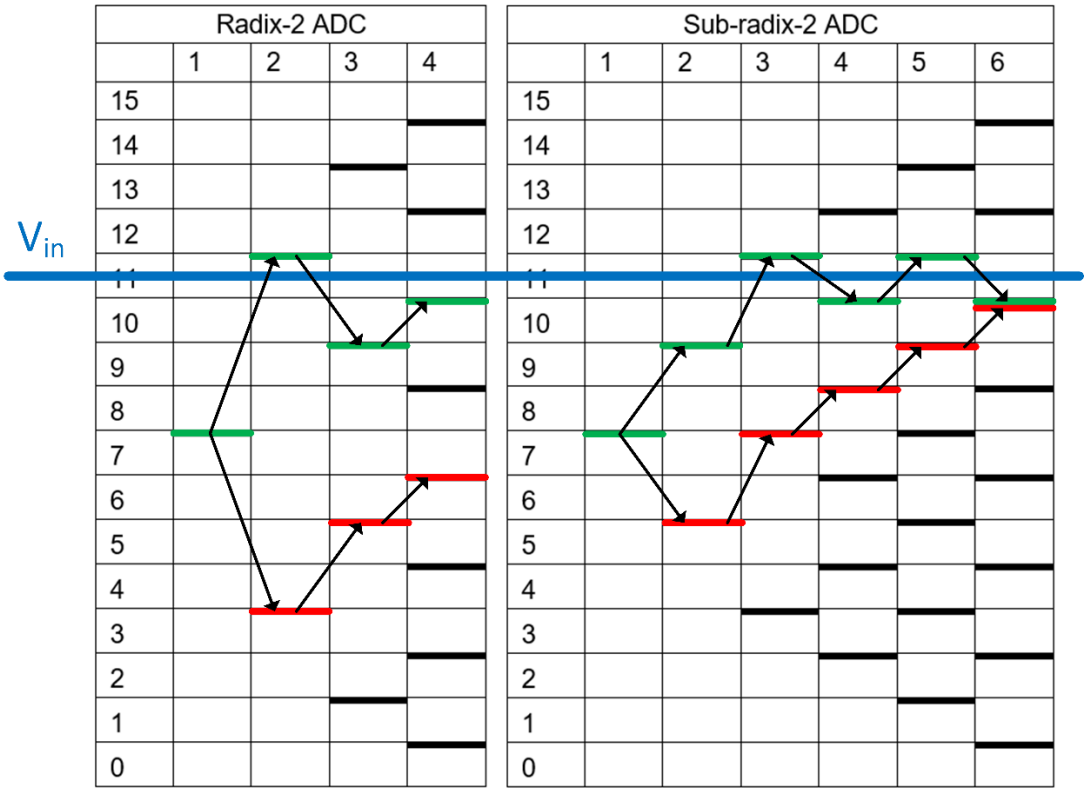

Figure 3.16 – Comparison of error resilience in a 4-bit radix-2 ADC and a 6 raw bit sub-radix-2 ADC. The thicker lines represent the decision levels. The green decision levels are the ones used in an errorless conversion and the red ones are used when an error is introduced in the determination of the first bit. In this case, the redundant ADC still has a correct output, while the radix-2 ADC is not able to recover.

3.8 Summary of Techniques

In this section, a comparison between different SAR ADC designs is made. This comparison is important, since it will be used as a reference for this project, illustrating what technologies, topologies or methods could be employed and what results could be expected. For this analysis, four papers with

different SAR ADC designs were chosen, as indicated in Table 3.2.

Table 3.2 – Comparison of different SAR ADC designs.

Reference	[3]	[14]	[15]		[11]	
Method	Digital calibration based on offset double conversion	Digital calibration based on pseudorandom noise injection	Comparator Offset Calibration		IMCS switching scheme and split-capacitor DAC	
Technology	130 nm	90 nm	130 nm		65 nm	
Area	0.06 mm^2	0.046 mm^2	0.038 mm^2		0.083 mm^2	
Supply Voltage	1.2 V	1.2 V	0.35 V	0.6 V	1.2 V	
Sampling Freq.	22.5 MS/s	50 MS/s	0.2 MS/s	3 MS/s	10 MS/s	50 MS/s
Power	1.58 mW	3.3 mW	84.7 nW	3.44 µW	400 µW	2.09 mW
ENOB	11.5 bit	10.5 bit	6.4 bit	6.53 bit	11.0 bit	10.9 bit
FOM	51.3 fJ/step	44.9 fJ/step	5.04 fJ/step	12.5 fJ/step	19.5 fJ/step	21.9 fJ/step
Date	2011	2012	2015		2013	

Most of the ADCs described in the analyzed papers have an asynchronous operation, meaning that the resolution of one bit starts automatically as soon as the resolution of the last bit ends, and have a differential input. Papers [3], [14] and [11] describe CR SAR ADCs, while [15] describes a Charge Sharing (CS) SAR ADC. A CS ADC only draws current from the reference supply during sampling to charge the DAC capacitors and uses that charge for the rest of the conversion, while in a CR implementation current is drawn from the reference supply at every bit resolving cycle. This characteristic of the CS implementation reduces the requirements for the reference supply circuit.

The work in [3] uses digital calibration to calibrate for mismatches in the DAC capacitors, which are the dominant static linearity-limiting factor in SAR ADCs. To ensure that no codes are missing and that it is possible to calibrate digitally the DAC mismatches it is imperative to use redundancy. The output codes of a redundant ADC have an overlap with respect to the analog range of the input signal that they cover. This overlap allows some amount of mismatch in the DAC capacitors. If the amount of redundancy is correctly chosen the linearity of the transfer function of the ADC can be recovered by learning the true bit weights built into the DAC. In this paper, a sub-radix-2 approach is used and the redundancy is built directly into the DAC. The digital calibration is accomplished using the Offset Double Conversion technique (ODC). Two conversions are made for each sampled analog signal, one conversion with a small negative perturbation and one conversion with an equal but positive perturbation applied to the

sampled signal. The working principle of the ODC technique is illustrated in Figure 3.17.

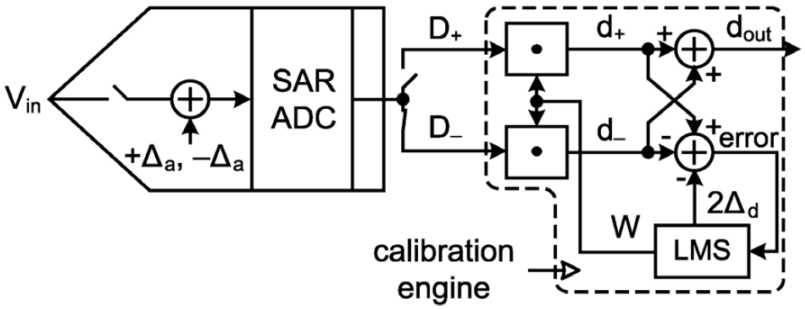

Figure 3.17 – Block diagram of the digital calibration using Offset Double Conversion (ODC) [3].

First, the input signal is sampled. Then, two conversions are performed with the sampled input signal. The first conversion is made after adding a perturbation with amplitude +Δa to the sampled signal. This perturbation can be easily applied to the sampled signal if an extra capacitor is used in the DAC. Another conversion starts after obtaining the raw bits D_+ (result of the first conversion), but now a perturbation with amplitude -Δa is used. The dot product of the raw bits from each conversion (D_+ and D_-) and the weights W is computed and d_+ and d_- are obtained. The result of the conversion d_{out} is obtained by averaging d_+ and d_-. If there are mismatches in the DAC capacitors, the weights W used in the conversion do not correspond to the true weights. Therefore, the true weights must be learned. In this paper, the Least-Mean-Square (LMS) algorithm is used for this task. With correct weights, d_{out} could be computed by simply subtracting the digital converted version of the perturbation Δd to d_+ or by adding it to d_-. Since the correct weights are not known, the two results are not equal. The difference between these two results is the error and the goal of the LMS algorithm is to minimize the square of this error. This is described by Equations 3.17 and 3.18.

$$d_{out} = \frac{d_+ + d_-}{2} = \left(D_+ + D_-\right)\cdot\frac{W}{2} = \sum_{i=0}^{N-1}\left(b_+^i + b_-^i\right)\frac{w^i}{2} \tag{3.17}$$

$$error = d_+ + d_- - 2\Delta_d = \left(D_+ + D_-\right)\cdot W - 2\Delta_d = \sum_{i=0}^{N-1}\left(b_+^i + b_-^i\right)w^i - 2\Delta_d \tag{3.18}$$

The LMS update equations can be calculated from Equations 3.17 and 3.18 and can be written as:

$$w^i[n+1] = w^i[n] - \mu_w error[n]\left(b_+^i[n] - b_-^i[n]\right) \tag{3.19}$$

$$\Delta_d[n+1] = \Delta_d[n] + \mu_\Delta error[n] \tag{3.20}$$

In this paper, the 14 DAC capacitors are scaled with a radix of 1.86, which is adequate for a target ENOB of 12 bit with a mismatch standard deviation of 5 % [16]. A dynamic latch comparator is used together with a two-stage preamplifier. The preamplifier relaxes the dynamic latch comparator offset and noise

requirements. After learning the weights, ODC can be disabled and the ADC can operate at twice the sampling frequency. The averaging of the two conversions when ODC is enabled halves the quantization noise power and the comparator noise power. Thus, when the ODC is disabled a decrease of the SNDR up to 3 dB is expectable.

The ADC described in paper [14] has similarities to the one of paper [3]. It also uses digital calibration to calibrate for DAC mismatches and the principle of perturbation injection is also employed. However, the sampling frequency does not need to be halved since a technique based on bitwise correlation (BWC) is used. The working principle of the digital calibration used in this ADC is illustrated in Figure 3.18.

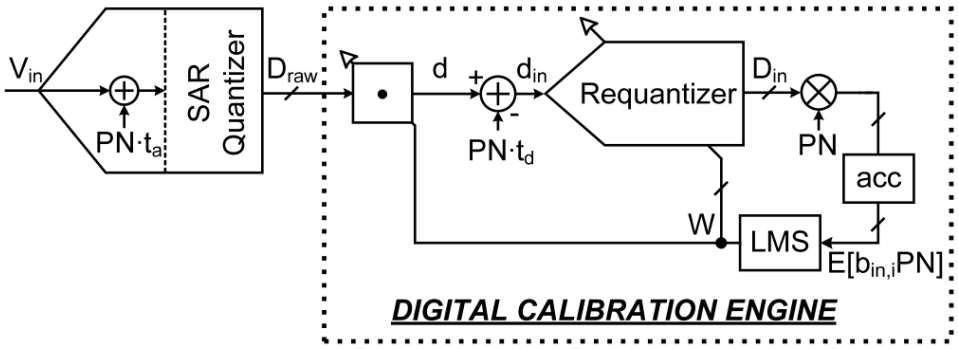

Figure 3.18 – Block diagram of the digital calibration using Bitwise Correlation (BWC) [14].

A discrete time single-bit pseudorandom noise (PN) signal with amplitude t_a is injected into the sampled signal. The conversion result d is calculated from a weighted sum of the raw bits D_{raw} using the weights W. In an ideal scenario, the injected PN can be removed from d and d_{in} is obtained, which is a representation of V_{in} totally independent of the PN. However, if the optimum weights are not known a residual information of the PN will be contained in d_{in}. Thus, a non-zero correlation between d_{in} and the PN can be used to estimate the optimum bit weights. However, a single correlation cannot be used to determine all the bit weights and, for this reason, a requantizer block is used to decompose d_{in} back to its sub-radix-2 format D_{in}. This digital signal is correlated at the bit level with the PN. The LMS algorithm is used to update the weights, according to Equations 3.21 and 3.22.

$$w^i[n+1] = w^i[n] - \mu E[PN \cdot b_{in}^i] \tag{3.21}$$

$$t_d[n+1] = t_d[n] - \mu E[PN \cdot d_{in}] \tag{3.22}$$

The paper [15] uses CS technique instead of the CR technique. In a SAR ADC using CR technique the comparator offset translates into an offset in the ADC transfer curve. However, in a SAR ADC using CS technique as in the paper [15], the comparator offset creates non-linearity and degrades the SNDR of the ADC. To overcome this limitation, the ADC described in [15] uses a background calibration technique to cancel the comparator mismatch. The offset calibration is achieved by shorting the inverting and non-inverting inputs of the comparator in the end of a conversion and performing a comparison. The

comparator has an extra differential pair and depending on the comparison result its differential input voltage is increased or decreased, effectively cancelling the comparator offset.

The dissertation [11] describes the design of a SAR ADC that uses the IMCS switching scheme. As described earlier in this chapter, the IMCS switching scheme has the lowest energy consumption among the ones studied in this thesis, utilizes half the DAC capacitance when built with a radix of 2 and is insensitive to parasitic capacitances of the DAC. This ADC also uses redundancy and background digital calibration. To increase the resolution of the ADC, the number of DAC capacitors must increase. Since the capacitance value increases exponentially, this becomes unfeasible at some point. The occupied area increases, leading to higher costs, and the performance decreases due to the switching of larger capacitors and to the increased sampling time. Consequently, a solution would be to reduce all the capacitance values in the DAC array, but then the parasitic capacitances would create a barrier to further lowering the capacitance values, not to mention the loss of SNR due to sampling noise or the increased mismatch. By inserting a split-capacitor (or bridge capacitor, C_B) in the middle of the DAC array (effectively splitting it in two, hence the name of the capacitor), as shown in Figure 3.19, it is possible to reduce the total DAC size. This ADC uses this technique to reduce the DAC area.

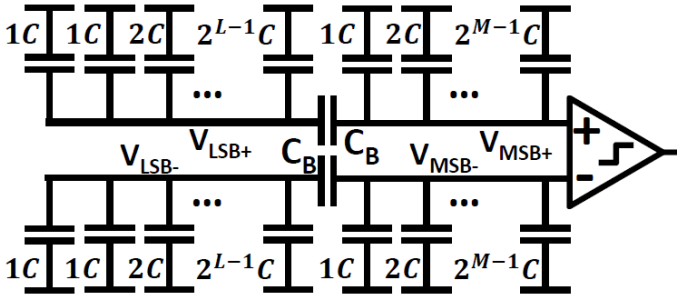

Figure 3.19 – Split-capacitor DAC [11].

The paper [17] suggests that one could optimize the power consumption of a SAR ADC by using multiple comparators with different noises and energy consumptions. During a conversion, the differential voltage at the output of the DAC gets smaller as the bits are resolved, tending to zero. Thus, when resolving the least significant bits a very small differential voltage is present at the input of the comparator while a large differential voltage is present when resolving the most significant bits. This suggests, intuitively, that the noise specification of the comparator can be relaxed when resolving the most significant bits. As the input-referred noise of a dynamic latch comparator is inversely proportional to its power consumption, the overall power consumption of the ADC is reduced when several comparators with different noise specifications are used. The authors of the paper [17] found that the power consumption of a 10-bit SAR ADC can be reduced by 50% if one comparator is used for each bit with optimum power/noise specification. The usage of multiple comparators to optimize power consumption is not new and has been used in the past. The papers [18] and [19] describe two SAR ADC designs that employ multiple comparators, but they lack a rigorous theoretical justification. The paper [20] corroborates the technique by reporting the first single channel SAR ADC to achieve an ENOB higher than 10 bit at 100 MS/s with a FoM of 10.1 fJ/step.

The comparator offset only generates an offset in the transfer function of a typical SAR ADC with a single comparator. However, non-linearity is introduced when multiple comparators are used due to their different offset values. The paper [21] presents a statistical analysis of the effect of comparator mismatch in the ENOB of a SAR ADC. To limit the ENOB loss to 0.5 bit in an 8-bit SAR ADC with a yield target of 99%, the comparator offset cannot be higher than 0.15 LSB. To meet this requirement in a 130 nm CMOS process, the transistors would occupy an area of around 87 μm^2, which would introduce large parasitic capacitances. For this reason, the ADC described in [21] uses offset self-calibrated comparators, as in [15].

3.9 Proposed Architecture

The 14 raw bit SAR ADC developed in this thesis will use ODC to digitally calibrate for DAC mismatches. The capacitive DAC will have additional capacitors to introduce a positive or negative offset into the sampled signal, as it is required for digital calibration. Redundancy is also required for digital calibration. A radix of 1.86 was chosen for this ADC, as used in [3] and [14], which is adequate for a target ENOB of 12 bit with a 5 % DAC capacitors mismatch standard deviation [16]. To reduce the DAC size, a split-capacitor is used. The split-capacitor divides the DAC in two sub-DACs, the MSB and LSB. To optimize power consumption, the IMCS switching scheme is used. This switching scheme is insensitive to parasitic capacitances in the DAC, requires half the DAC capacitance compared to conventional and monotonic switching schemes and consumes the least energy [11]. Multiple comparators are going to be used in this ADC. For a 10-bit ADC, two different comparator designs achieves close to optimal performance regarding overall power consumption [17]. Since this ADC has 14 raw bits and targets an ENOB of 12 bit, a total of four different comparator designs is going to be used. The optimal input-referred noise values for each comparator design will be computed according to [17]. Additional circuitry is going to be added to each comparator to calibrate its offset voltage and avoid degrading the dynamic performance of the ADC.

Chapter 4

SAR ADC Design

4.1 SAR ADC Block Diagram

A representation of the inputs and outputs of the SAR ADC described in this work is depicted in Figure 4.1. This SAR ADC is composed by several instances of four main building blocks: dynamic latch comparator, switch, delay cell, logic and finally, the capacitive DAC. This ADC does not have a dedicated S/H. Its differential input signal is instead sampled into the capacitive DAC, as in [3], [11], [14]. The sampling starts at the rising edge of the CLK signal. At this instant, the input signal is connected to the bottom plates of the DAC capacitors through bootstrapped switches and the top plates are connected to V_{CM}. At the falling edge of the *CLK* signal, the sampling ends and the DAC is reconfigured to start resolving the bits. Instead of using one comparator, this SAR ADC uses 14 comparators with 4 different designs to optimize power consumption. After each comparator decision, a *ready* signal is generated. There is logic replicated for each bit that generates the required signals to reconfigure the DAC after each bit is resolved. The *ready* signal triggers the next comparison after going through a delay cell to allow the DAC output to settle. Thus, the conversion itself is asynchronous. The *ready* signal of the last comparator is used as an output to inform that a conversion has finished, called *EOC*. The ADC uses ODC to digitally calibrate for DAC mismatches, as in [3]. For that reason, the DAC contains one more capacitor responsible for introducing an offset in the sampled signal. An output called *PERT* is used to inform if a positive or negative offset was applied to the sampled signal when the ODC is enabled. The ODC can be disabled by setting *ODC_EN* input low. When ODC is disabled, the sampling frequency is equal to the external *CLK* frequency. If the ODC functionality is enabled, then two conversions for the same sampled input signal are performed and the sampling frequency is halved. Finally, the DAC features a split-capacitor as explained in Chapter 3. The IMCS switching scheme was chosen due to its low energy consumption and allows a reduction of one capacitor in the DAC. To enable the offset calibration of the comparators, the input *CAL_EN* should be set high. To trigger an offset calibration cycle, a pulse should be applied to the *CAL* input. A simplified block diagram of the SAR ADC is depicted in Figure 4.2.

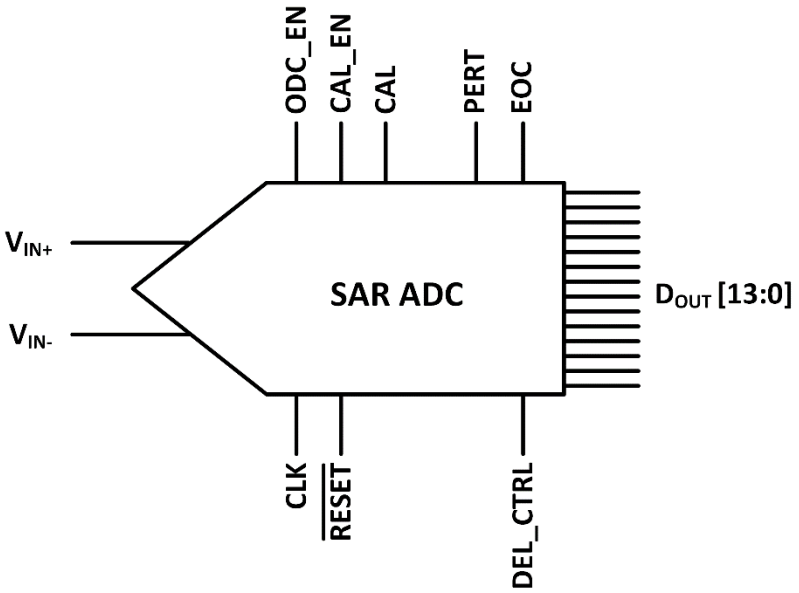

Figure 4.1 – Representation of the input and output signals of the ADC.

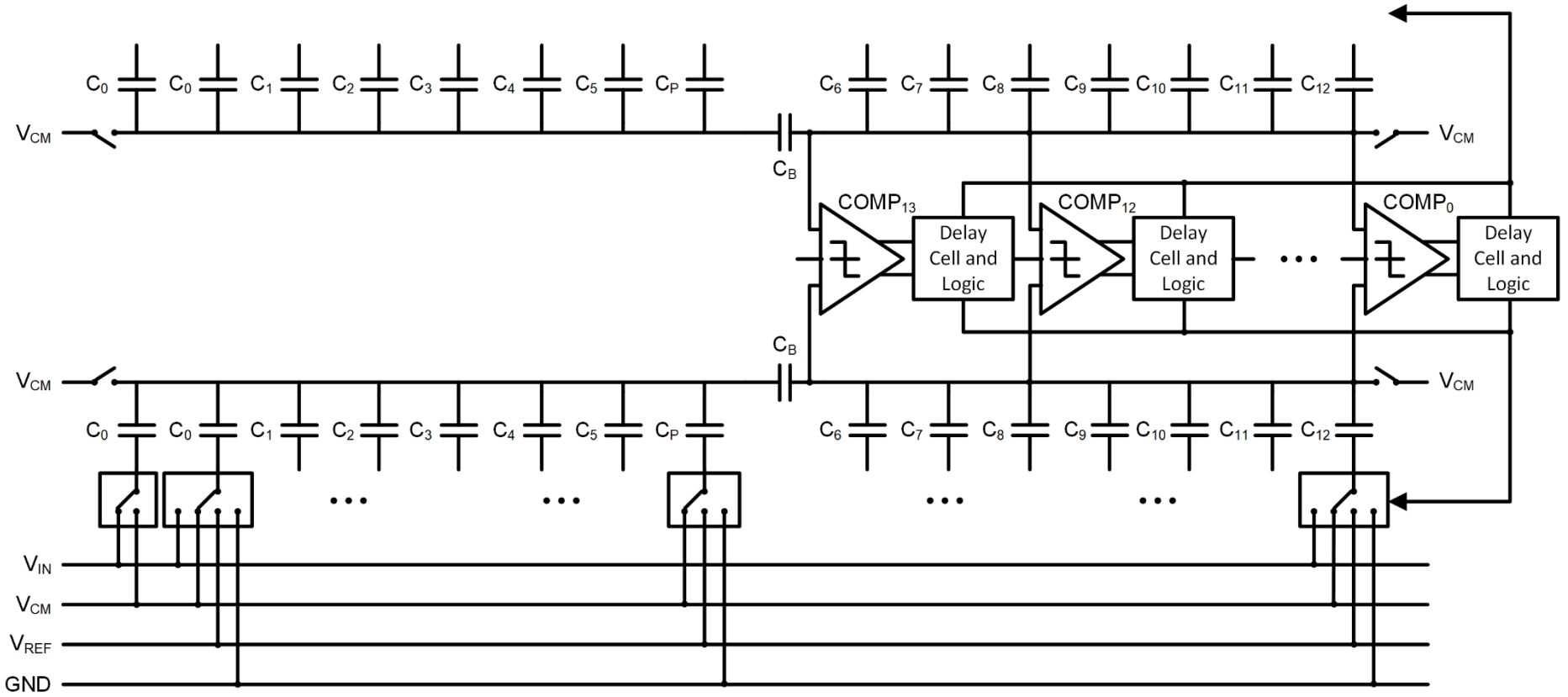

Figure 4.2 – Block diagram of the SAR ADC developed in this thesis.

4.2 DAC

One can calculate the decision levels using the charge conservation principle. This is a straightforward exercise in the case of a typical DAC implementation, but a bit more complicated for a split-capacitor DAC. Let's use as example the DAC depicted in Figure 4.3.

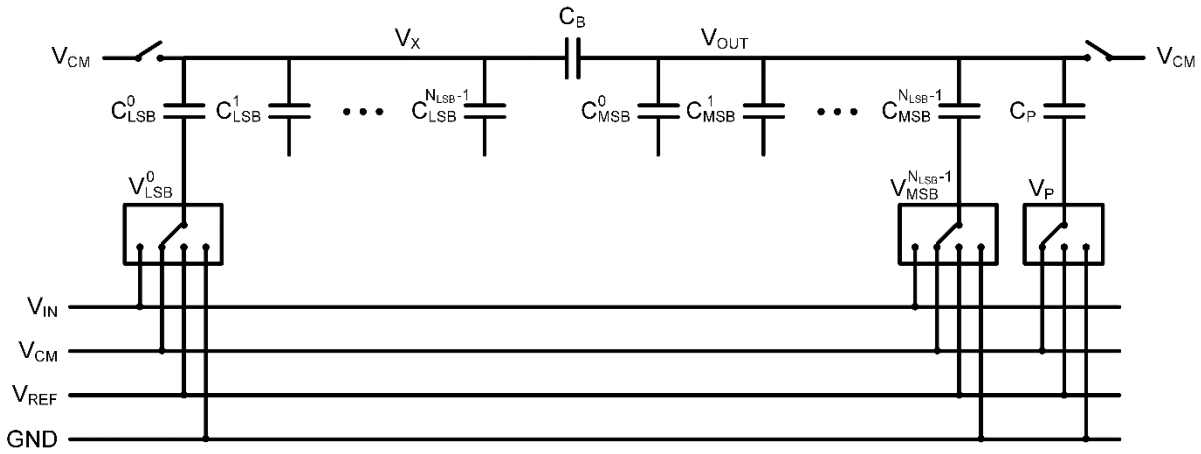

Figure 4.3 – Single-ended split-capacitor DAC with perturbation capacitor C_P in the MSB array.

Right after sampling, the stored charges in the LSB, MSB, bridge and perturbation capacitances are expressed by Equations 4.1 to 4.4.

$$Q_{LSB}^{samp} = \sum_{i=0}^{N_{LSB}-1} C_{LSB}^{i}\left(V_{in} - V_{CM}\right) \tag{4.1}$$

$$Q_{MSB}^{samp} = \sum_{i=0}^{N_{MSB}-1} C_{MSB}^{i}\left(V_{in} - V_{CM}\right) \tag{4.2}$$

$$Q_{P}^{samp} = 0 \tag{4.3}$$

$$Q_{B}^{samp} = 0 \tag{4.4}$$

During the bit resolving phase, the voltages of the bottom plates of the DAC capacitors are either V_{REF}, V_{CM} or GND. The total charge stored in the DAC remains constant because the top plates are floating. However, the individual charge of each capacitor depends on its bottom plate voltage. These charges during the bit resolving phase are expressed by Equations 4.5 to 4.8.

$$Q_{LSB}^{res} = \sum_{i=0}^{N_{LSB}-1} C_{LSB}^{i}\left(V_{LSB}^{i} - V_{X}\right), \tag{4.5}$$

$$Q_{MSB}^{res} = \sum_{i=0}^{N_{MSB}-1} C_{MSB}^{i}\left(V_{MSB}^{i} - V_{OUT}\right) \tag{4.6}$$

$$Q_{P}^{res} = C_{P}^{i}\left(V_{P}^{i} - V_{OUT}\right) \tag{4.7}$$

$$Q_{B}^{res} = C_{B}\left(V_{X} - V_{OUT}\right) \tag{4.8}$$

The charges in the top plates of the LSB DAC and the MSB DAC are kept constant. Using the charge conservation principle, one can write:

$$\begin{aligned} -Q_{LSB}^{samp} + Q_{B}^{samp} &= -Q_{LSB}^{res} + Q_{B}^{res} \\ Q_{MSB}^{samp} + Q_{B}^{samp} + Q_{P}^{samp} &= Q_{MSB}^{res} + Q_{B}^{res} + Q_{P}^{res} \end{aligned} \tag{4.9}$$

It is possible to calculate the values of V_{OUT} and V_X by solving Equation 4.9, yielding the following results:

$$\begin{aligned} V_{OUT} = {} & \frac{C_B}{A}\sum_{i=0}^{N_{LSB}-1} C_{LSB}^{i}V_{LSB}^{i} + \frac{C_B + C_{LSB}}{A}\sum_{i=0}^{N_{MSB}-1} C_{MSB}^{i}V_{MSB}^{i} + \frac{C_B + C_{LSB}}{A}C_P V_P \\ & + \frac{C_B C_{LSB} + C_B C_{MSB} + C_{LSB}C_{MSB}}{A}V_{CM} - \frac{C_B C_{LSB} + C_B C_{MSB} + C_{LSB}C_{MSB}}{A}V_{in} \end{aligned} \tag{4.10}$$

$$\begin{aligned} V_X = {} & \frac{C_B + C_{MSB} + C_P}{A}\sum_{i=0}^{N_{LSB}-1} C_{LSB}^{i}V_{LSB}^{i} + \frac{C_B}{A}\sum_{i=0}^{N_{MSB}-1} C_{MSB}^{i}V_{MSB}^{i} + \frac{C_B}{A}C_P V_P \\ & + \frac{C_B C_{LSB} + C_B C_{MSB} + C_{LSB}C_{MSB} + C_{LSB}C_P}{A}V_{CM} - \frac{C_B C_{LSB} + C_B C_{MSB} + C_{LSB}C_{MSB} + C_{LSB}C_P}{A}V_{in}, \end{aligned} \tag{4.11}$$

where $A = C_B C_{LSB} + C_B C_{MSB} + C_B C_P + C_{LSB}C_{MSB} + C_{LSB}C_P$, $C_{LSB} = \sum_{i=0}^{N_{LSB}-1} C_{LSB}^{i}$, $C_{MSB} = \sum_{i=0}^{N_{MSB}-1} C_{MSB}^{i}$.

The previous analysis was done for a single-ended DAC. Since the designed ADC is differential, the focus should be in the difference between the output of the two DACs. Furthermore, it is enough to know if this difference is positive or negative. This helps to simplify the problem to get a simpler result, as expressed in Equation 4.12.

$$\begin{aligned} V_{OUT+} - V_{OUT-} > 0 \Leftrightarrow {} & \frac{C_B}{B}\sum_{i=0}^{N_{LSB}-1} C_{LSB}^{i}\left(V_{LSB+}^{i} - V_{LSB-}^{i}\right) + \frac{C_B + C_{LSB}}{B}\sum_{i=0}^{N_{MSB}-1} C_{MSB}^{i}\left(V_{MSB+}^{i} - V_{MSB-}^{i}\right) \\ & + \frac{C_B + C_{LSB}}{B}C_P\left(V_{P+} - V_{P-}\right) > V_{in+} - V_{in-} \end{aligned} \tag{4.12}$$

where $B = C_B C_{LSB} + C_B C_{MSB} + C_{LSB}C_{MSB}$.

From Equation 4.12 it becomes evident that the decision levels are generated by the several combinations of voltages of the bottom plates. The weight of a DAC capacitor (w^i) is related to the size of its contribution to the decision level value. Therefore, Equation 4.12 can be rewritten:

$$\sum_{i=0}^{N_{LSB}-1} w_{LSB}^{i}\left(V_{LSB+}^{i}-V_{LSB-}^{i}\right)+\sum_{i=0}^{N_{MSB}-1} w_{MSB}^{i}\left(V_{MSB+}^{i}-V_{MSB-}^{i}\right)+w_P\left(V_{P+}-V_{P-}\right)>V_{in+}-V_{in-} \qquad (4.13)$$

There are two possible configurations regarding the perturbation capacitor C_P: either it is placed in the MSB array or in the LSB array. For the same capacitance value, the perturbation weight is larger in the MSB array than in the LSB array. The two configurations are depicted in Figure 4.4.

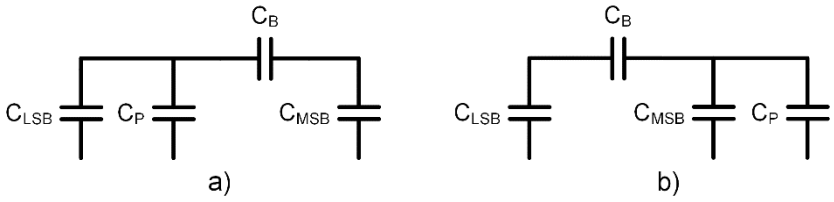

Figure 4.4 – Perturbation capacitor C_P in the LSB array (a) and in the MSB array (b).

The weights for the situation where the perturbation capacitors are placed in the MSB array are:

$$w_{LSB}^{i}=\frac{C_{LSB}^{i}C_B}{C_BC_{LSB}+C_BC_{MSB}+C_{LSB}C_{MSB}} \qquad (4.14)$$

$$w_{MSB}^{i}=\frac{C_{MSB}^{i}\left(C_B+C_{LSB}\right)}{C_BC_{LSB}+C_BC_{MSB}+C_{LSB}C_{MSB}} \qquad (4.15)$$

$$w_P=\frac{C_P\left(C_B+C_{LSB}\right)}{C_BC_{LSB}+C_BC_{MSB}+C_{LSB}C_{MSB}} \qquad (4.16)$$

The weights when the perturbation capacitors are placed in the LSB array are:

$$w_{LSB}^{i}=\frac{C_{LSB}^{i}C_B}{C_BC_{LSB}+C_BC_{MSB}+C_{LSB}C_{MSB}+C_{MSB}C_P} \qquad (4.17)$$

$$w_{MSB}^{i}=\frac{C_{MSB}^{i}\left(C_B+C_{LSB}+C_P\right)}{C_BC_{LSB}+C_BC_{MSB}+C_{LSB}C_{MSB}+C_{MSB}C_P} \qquad (4.18)$$

$$w_P=\frac{C_PC_B}{C_BC_{LSB}+C_BC_{MSB}+C_{LSB}C_{MSB}+C_{MSB}C_P} \qquad (4.19)$$

To minimize effort in the design of the switches, the same unitary capacitance value was considered for

the LSB and MSB DACs ($C_{LSB}^{0} = C_{MSB}^{0}$). A radix of 1.86 was used, as in [3], [14]. The perturbation capacitor C_P was placed in the LSB array because it would be the smallest capacitor if placed in the MSB array. Its weight was chosen to be 16 times the weight of the LSB capacitor. Table 4.1 summarizes the DAC capacitor values resulting from these constrains normalized to the unitary capacitance value.

Table 4.1 – Normalized DAC capacitor values.

i	C_{LSB}^{i}	C_{MSB}^{i}	C_B	C_P
0	1	1	1.58	16
1	1	1.86		
2	1.86	3.46		
3	3.46	6.43		
4	6.43	11.97		
5	11.97	22.26		
6	22.26	41.41		

The sampling noise can be easily calculated for a conventional (not split) DAC, as expressed in Equation 4.20. The result is very well known amongst ADC designers and was obtained in Chapter 3.6.

$$P_{n,samp} = \frac{kT}{C_{tot}} \tag{4.20}$$

Interestingly, this result also follows from statistical thermodynamics [22]. Every state variable in a system that is not constrained to have a fixed value is free to fluctuate. If the energy stored in a system relative to state variable x is proportional to x^2, then we say that x is a degree of freedom of the system. Therefore, the voltage of a capacitor is a degree of freedom, since the energy stored in the capacitor is proportional to its voltage squared. From statistical mechanics we know that a system in thermal equilibrium at a temperature T has a fluctuation energy of $kT/2$ per degree of freedom. Therefore, the previous result can also be calculated as:

$$\frac{1}{2}C\overline{V_{noise}^2} = \frac{kT}{2} \Leftrightarrow \overline{V_{noise}^2} = \frac{kT}{C} \tag{4.21}$$

This is a much more general result than the result of Chapter 3.6 since it was not derived for one specific circuit configuration. Quite the opposite, this result can be applied to any capacitor in any circuit configuration. Using the previous result, we can say that a capacitor has a charge noise with standard deviation of:

$$\sigma\left(Q_{noise}\right) = C\sqrt{\frac{kT}{C}} = \sqrt{kTC} \tag{4.22}$$

We can introduce a charge error ΔQ_i in each capacitor after the sampling phase to evaluate its effect in the conversion, simulating the charge noise of the capacitor. For a conventional DAC, the following result is obtained:

$$V_{OUT} = \frac{1}{C_{tot}}\sum_{i=0}^{N-1} C_i V_i - \left(V_{in} + \frac{1}{C_{tot}}\sum_{i=0}^{N-1}\Delta Q_i\right) \tag{4.23}$$

We can clearly see from Equation 4.23 that a charge error in each capacitor translates to an error in the sampled signal. The standard deviation of this error can be calculated resorting to Equation 4.22:

$$\sigma\left(\varepsilon\right) = \sigma\left(\frac{1}{C_{tot}}\sum_{i=0}^{N-1}\Delta Q_i\right) = \frac{1}{C_{tot}}\sqrt{\sum_{i=0}^{N-1}\sigma^2\left(\Delta Q_i\right)} = \frac{1}{C_{tot}}\sqrt{kTC_{tot}} = \sqrt{\frac{kT}{C_{tot}}} \tag{4.24}$$

The same procedure can be applied to determine the sampling noise of a split-capacitor DAC, yielding the following result:

$$\sigma\left(\varepsilon\right) = \sqrt{\frac{kT\left(C_B + C_{LSB}\right)}{C_B C_{LSB} + C_B C_{MSB} + C_{LSB} C_{MSB}}} \tag{4.25}$$

The perturbation capacitor was not included in the calculations. Its charge noise is small and can be neglected since its capacitance is small compared to the LSB and MSB DAC capacitances. Equation 4.25 can be rewritten for a differential ADC as a function of the unit capacitance value C_u:

$$\sigma\left(\varepsilon\right) = \sqrt{\frac{2kT\left(C_B + C_{LSB}\right)}{C_B C_{LSB} + C_B C_{MSB} + C_{LSB} C_{MSB}}}\sqrt{\frac{1}{C_u}} \approx 303.5\mu V\sqrt{fF} \tag{4.26}$$

A unit capacitance of 60 fF was chosen, which gives a total sampling noise of 39.2 μV_{RMS} – around 0.13 V_{LSB} for a 13-bit radix-2 ADC – which corresponds to an ENOB loss (see Figure 3.15) of less than 0.2 bit. The final values for the DAC capacitors are summarized in Table 4.2.

Table 4.2 – Final DAC capacitor values.

i	$C_{LSB}^{i}(fF)$	$C_{MSB}^{i}(fF)$	$C_B(fF)$	$C_P(fF)$
0	60	60	94.8	960
1	60	111.6		
2	111.6	207.6		
3	207.6	385.8		
4	385.8	718.2		
5	718.2	1335.6		
6	1335.6	2484.6		

4.3 Bottom-plate Switches

4.3.1 V_{IN} Switches

The bottom plate of each DAC capacitor needs to be connected to V_{IN} during the sampling phase. To ensure a constant on-resistance independently of the input voltage, the bootstrapped switch is used (as described in Chapter 3.3). The implemented circuit is depicted in Figure 4.5 [10].

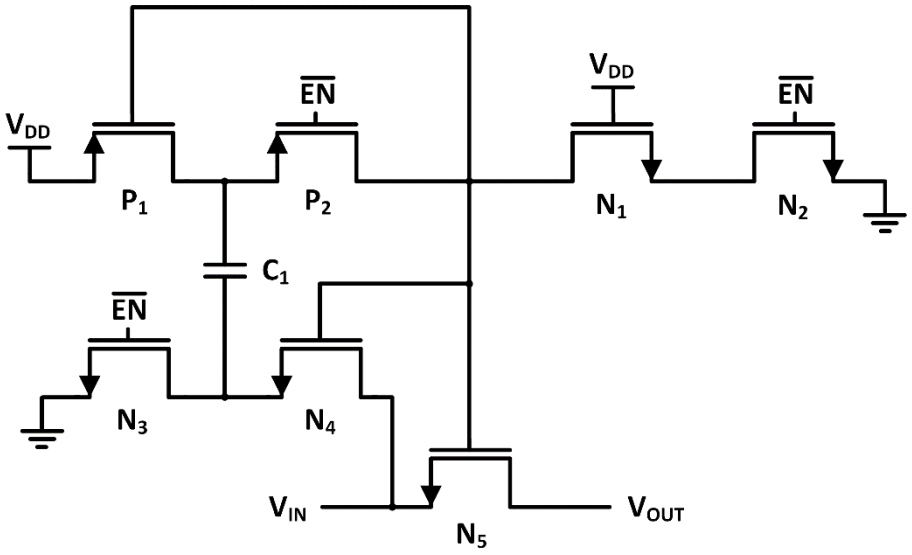

Figure 4.5 – Implemented circuit for bootstrapped switch.

This circuit places a capacitor C_1 previously charged to V_{DD} between the gate and the source of N_5, turning it on. All transistors were designed with minimum size. Only two instances of the circuit were implemented, one for V_{IN+} and one for V_{IN-}, instead of replicating it for every bottom-plate switch. The capacitor C_1 was implemented with a PMOS transistor with the source, drain and bulk tied together, also called MOSCAP. Since the bulk of a PMOS transistor is an N-well built in the P-substrate, it can be

connected to a voltage other than V_{DD}. The high capacity density of the MOSCAP in the triode region allows the bootstrapping circuit to be smaller without degrading the switch linearity. The capacitance of a MOSCAP in the triode region is expressed by Equation 4.27.

$$C_{GS} = WLC_{ox} = WL\frac{\varepsilon_{ox}}{t_{ox}}, \tag{4.27}$$

where ε_{ox} is the dielectric constant of the oxide and t_{ox} the thickness.

When C_1 is connected between the gate and source of N_5, some of its charge is shared with the gate-to-source capacitance of N_5. Consequently, the capacitor voltage drops. The capacitor was sized by simulation such that no more than 10% of its charge is lost. The NMOS for the LSB switch was designed with minimum size and the rest of the switches were scaled proportionally to the capacitors they are connected to in order to have an equal time constant for every bottom-plate switch. The circuit was simulated with all the V_{in} switches of the DAC. A turn-on delay of about 1.2 ns and a turn-off delay of about 0.5 ns were measured. The resulting waveforms are plotted in Figure 4.6.

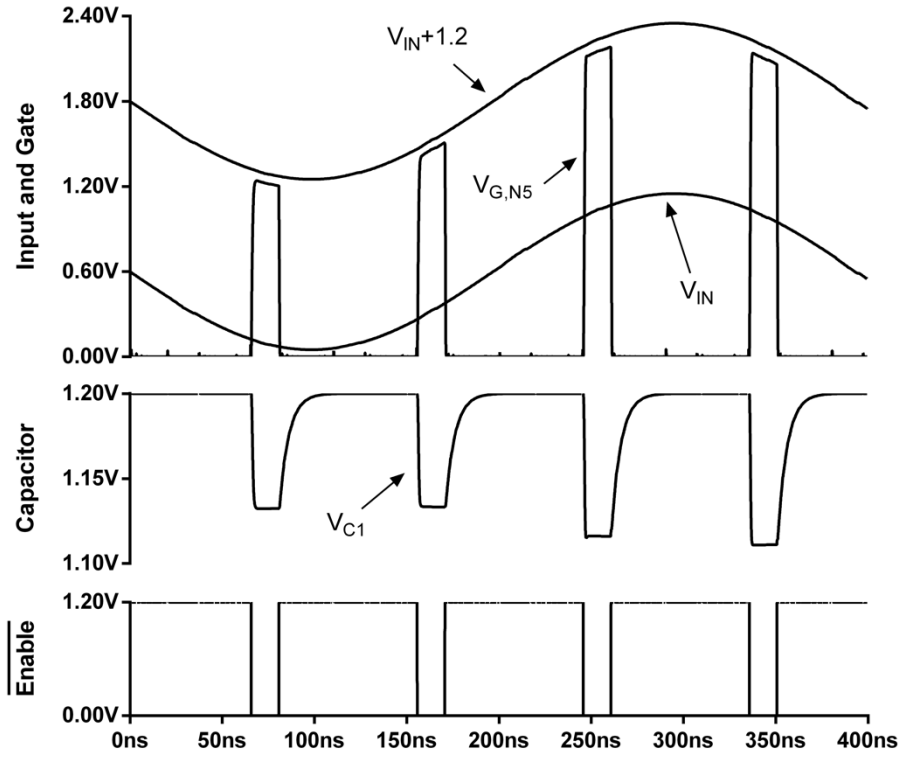

Figure 4.6 – V_{IN} bootstrapped switch waveforms.

4.3.2 V_{CM} Switches

The V_{CM} switches are responsible for connecting the bottom plates of the DAC to V_{CM} during the bit resolving phase. To maximize the V_{GS} and minimize the on-resistance, the same bootstrapping circuit

of Figure 4.5 was used. The LSB switch was designed with minimum size and the rest of the switches were scaled proportionally to the capacitors they are connected to. This way, the DAC settling time is kept consistent. The behaviour of the LSB switch was simulated and an on-resistance of 2.4 kΩ was measured. Since the bottom plate of the perturbation capacitor might need to be connected to V_{CM} throughout the entire conversion if the ODC is disabled, two transistors are used as switches and the bootstrapping circuit is doubled. This way the bootstrapping capacitor has time to charge.

4.3.3 V_{DD} and GND Switches

Simple NMOS transistors were used for the GND switches and PMOS transistors were used for the V_{DD} switches. As for the V_{CM} switches, the transistors were also scaled proportionally to the capacitors they are connected to. The NMOS LSB switch was designed with minimum size, presenting an on-resistance of 2.4 kΩ. Since the PMOS transistors have lower mobility values, they were designed 3 times larger than the NMOS ones. An on-resistance of 4.1 kΩ was measured for the PMOS LSB switch. Although the on-resistance of the PMOS LSB switch is considerably higher than the one of the corresponding NMOS switch, the switching behaviour when driving a capacitive load is similar, since the transistor is not always operating in the triode region.

4.4 Top-plate V_{CM} Switches

The top plates of the DAC capacitors need to be connected to V_{CM} during the sampling phase. To have the lowest possible on-resistance the higher possible V_{GS} should be used. For this reason, the circuit of Figure 4.5 was used. The switch that connects to the MSB DAC was designed with an on-resistance of 189 Ω and the one that connects to the LSB DAC with an on-resistance of 345 Ω, such that the time constant resulting from each sub-DAC capacitance and corresponding switch on-resistance is kept constant.

4.5 Delay Cell

The delay cell is responsible for delaying the *ready* signal to trigger the next comparison until the DAC is reconfigured and settled. Since redundancy is being used, the ADC has some resilience to incomplete settling. The required settling time was obtained empirically through simulation. Figure 4.7 shows the positive and negative DAC output voltages right after the sampling phase, capturing the bottom-plate V_{IN} switches turning off and the bottom-plate V_{CM} switches turning on. Similarly, Figure 4.8 shows the settling of the DAC after the first bit is resolved and the bottom-plates of the MSB capacitors of the positive and negative DACs are disconnected from V_{CM} and connected to V_{DD} and GND. The target

delay for the delay cell is in the order of 250 ps to 300 ps, since this was the measured settling time for the DAC. The delay is tuneable through an input voltage. The circuit implemented for the delay cell is depicted in Figure 4.9.

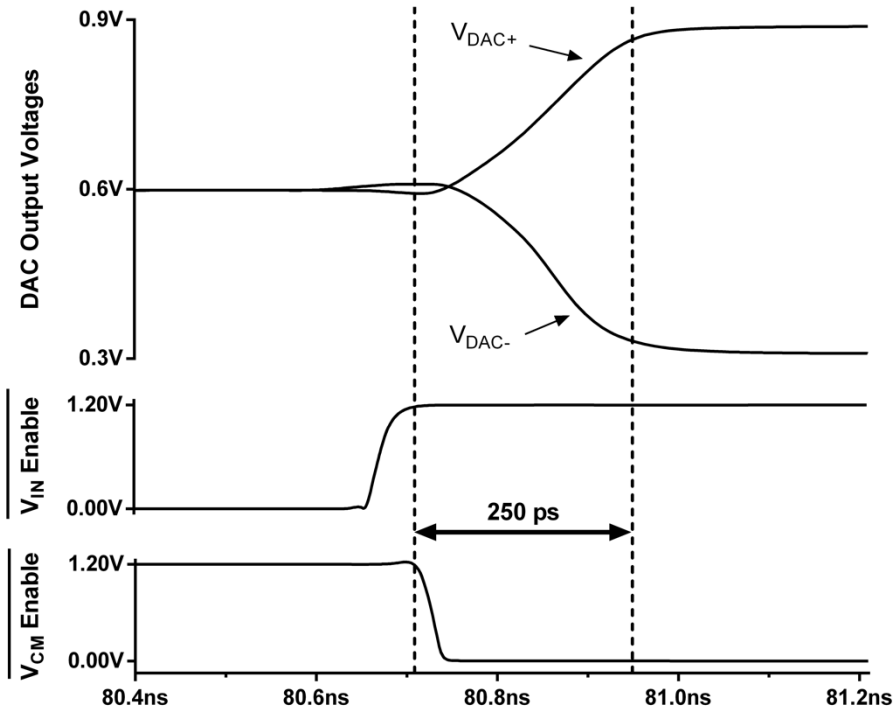

Figure 4.7 – A settling time of 250 ps was measured after the sampling phase when the V_{in} switches turn off and the bottom-plate V_{CM} switches turn on.

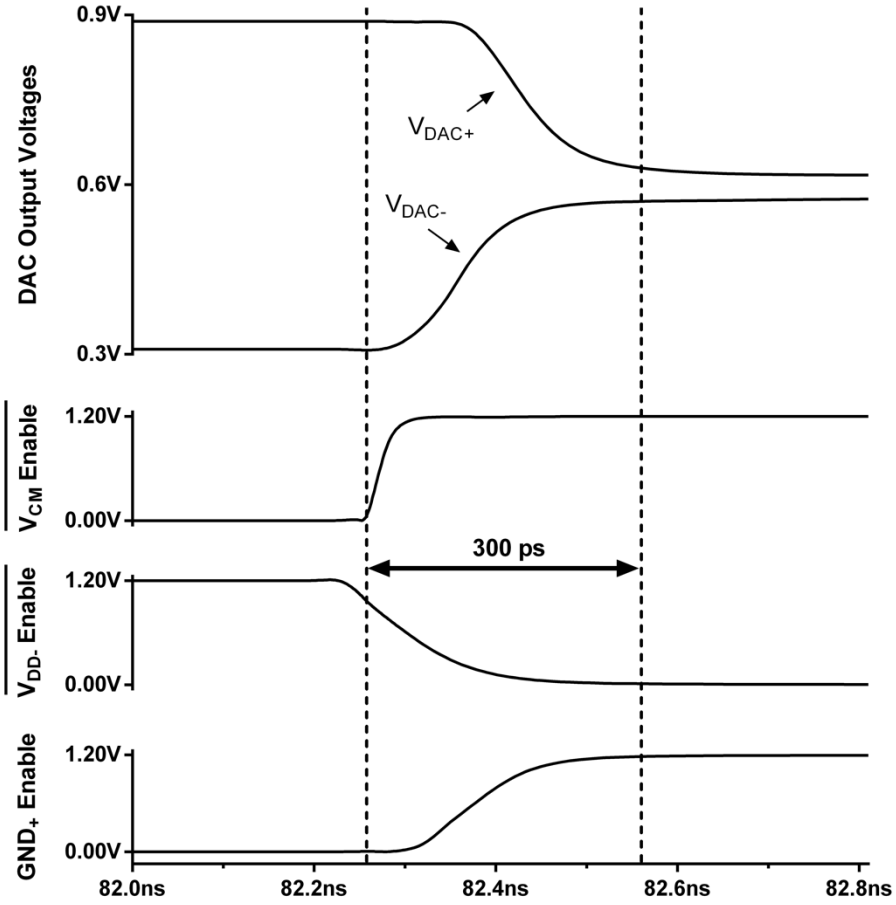

Figure 4.8 – A DAC settling time of 300 ps was measured after the first bit is resolved and the DAC is reconfigured.

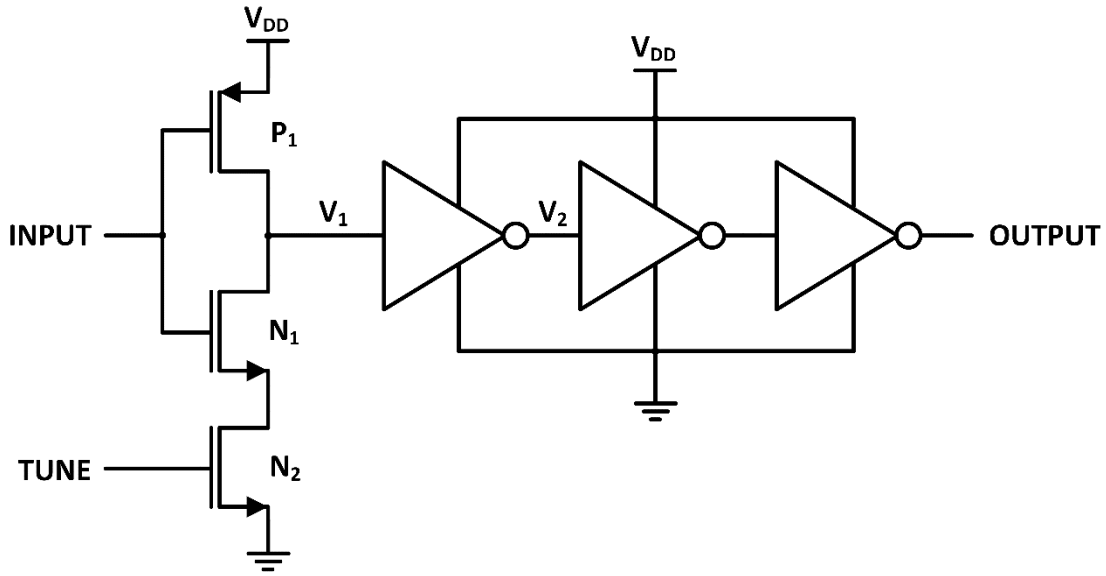

Figure 4.9 – Circuit of the delay cell.

Transistors P_1 and N_1 form an inverter. Another transistor N_2 is in series with N_1 to limit the discharge current of the node V_1 and increase its fall time. The three cascaded inverters serve two purposes: to invert the signal at V_1 such that the input and output of the delay cell are in phase and to speed up the

edges of V_1, mainly the falling edge. Three cascaded inverters were found to be adequate for the task through simulation. Transistors P_1 and N_1 were designed with minimum size. The size of N_2 was determined through simulation to achieve an adequate delay range. The circuit was simulated and the waveforms are depicted in Figure 4.10.

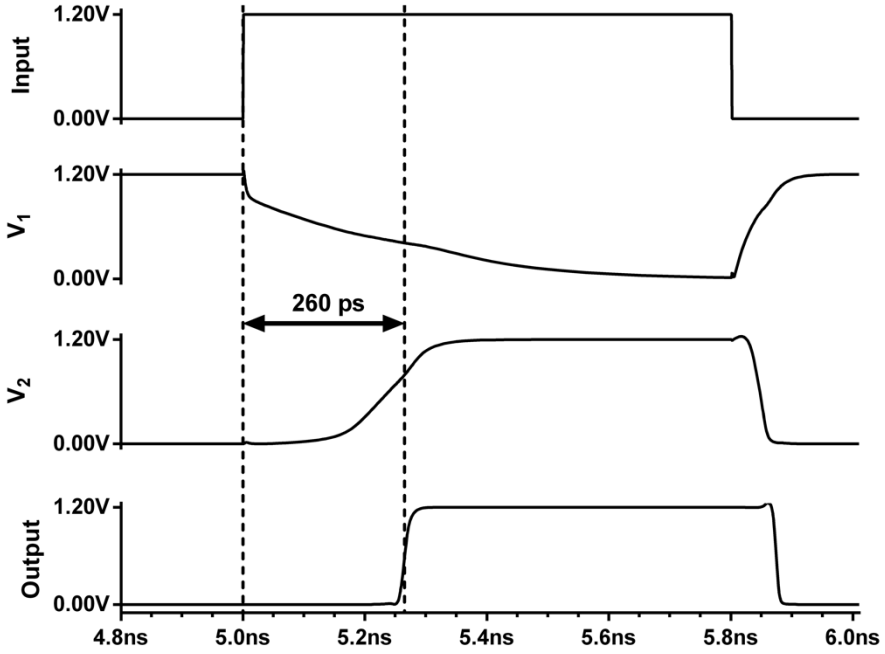

Figure 4.10 – The delay cell shows a rising edge delay of 260 ps for 600 mV of control voltage.

The layout tends to slow down circuits due to the added parasitic capacitances. Simulations were performed before and after layout parasitic extraction to avoid having an excessive delay and slowing down the ADC. The results from these simulations are plotted in Figure 4.11 and show a tuneable delay of 140 ps to 400 ps, which is adequate for this ADC.

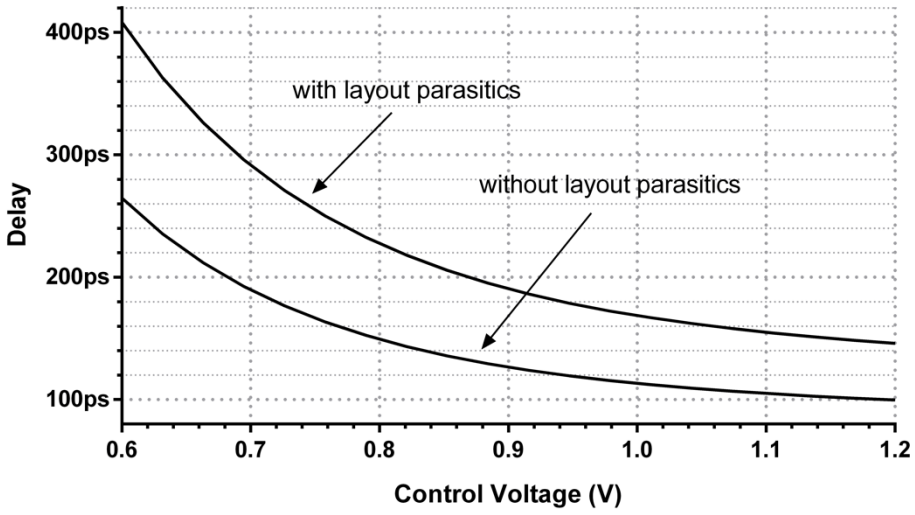

Figure 4.11 – Delay as a function of control voltage with and without layout parasitics.

4.6 Latched Comparators

A conventional SAR ADC only has one comparator that is used to resolve all bits. However, the input-referred RMS noise of the comparator should be at least 4 to 6 times lower than one LSB voltage to ensure that the ADC performance will not be limited by the noise of the comparator [23]. Since the differential voltage at the input of the comparator goes down from the MSB to the LSB, a higher noise can easily be tolerated when resolving the most significant bits and a lower noise is desirable when resolving the least significant bits. As the comparator input-referred noise variance is inversely proportional to the comparator power consumption [17], it becomes obvious that using the same comparator noise for each bit cycle is not optimal. In this work, one comparator per bit is used with four different input-referred noise values. Since noisier comparators consume less power, the optimization of the noise of each comparator will improve the overall power consumption of the ADC. The optimal noise for each of the four different comparator designs and their distribution along the 14 bits of the ADC were determined according to [17].

The StrongARM latch was the chosen topology. It has no static power consumption [24] and its latching nature allows the ADC to operate without flip-flops, increasing its speed. The offset calibration circuit of [15] was used with slight modifications due to the non-linearity generated by the different offset values of each comparator. The schematic of the StrongARM latch is depicted in Figure 4.12 and schematic of the offset calibration circuit used in this work is depicted in Figure 4.13.

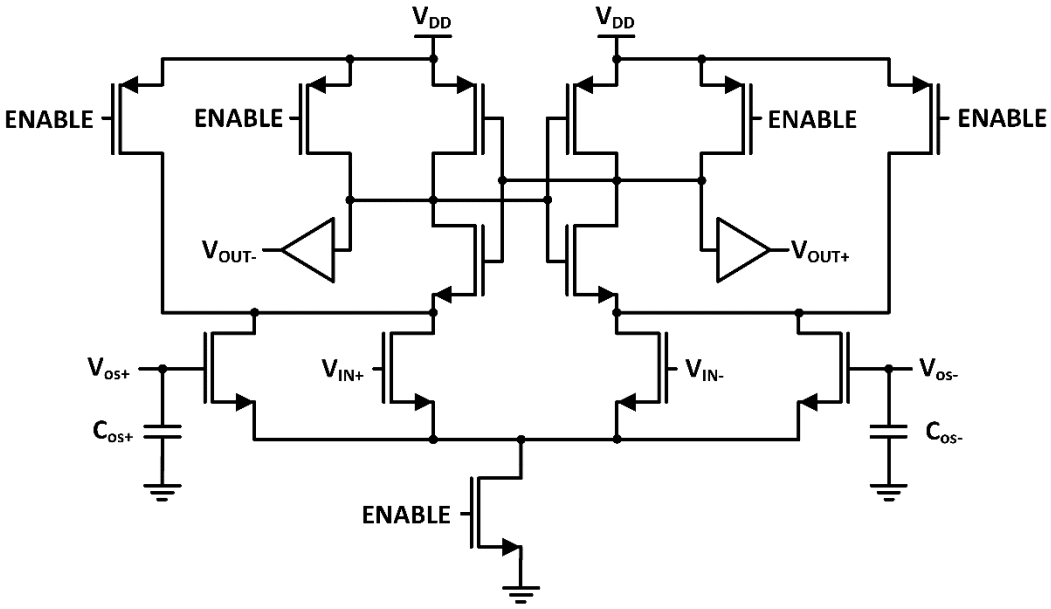

Figure 4.12 – StrongARM latch schematic.

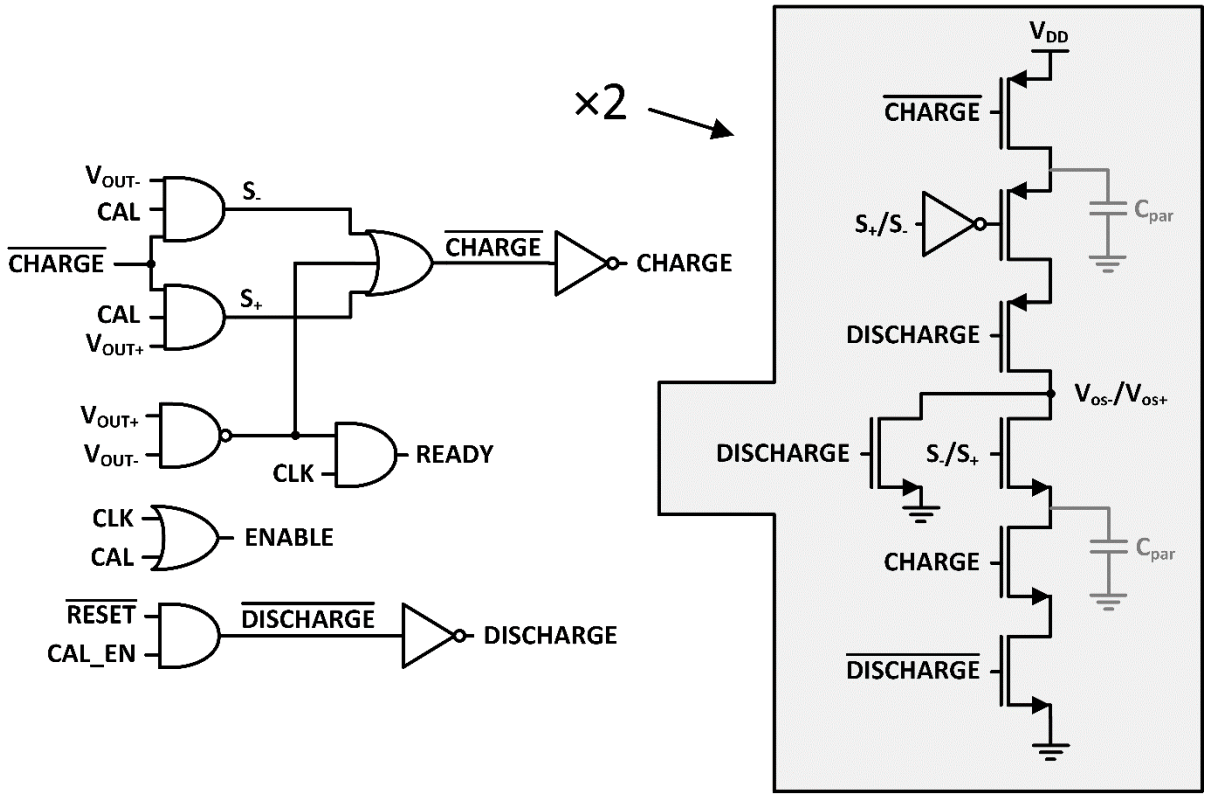

Figure 4.13 – Offset calibration circuit used in this ADC.

A comparison is triggered when the *CLK* or *CAL* signals go high. If the *CLK* signal triggers a comparison, the *READY* signal goes high as soon as an output is available. The *CAL* signal is used to calibrate the offset of the comparator and should not change the state of the DAC switches. For this reason, the *READY* signal remains low if the comparison is triggered by the *CAL* signal. The capacitors C_{os+} and C_{os-} are discharged if the $\overline{RESET}$ or *CAL_EN* signals are asserted. To calibrate the offset of the comparator, a comparison is triggered through the *CAL* signal when an equal input voltage is present at V_{IN+} and V_{IN-}. When the *CAL* signal is low, charge is stored in the parasitic capacitances C_{par}. After *CAL* goes high and an output is available, the *CHARGE* signal goes low and one of the signals S_+ or S_- goes high, sharing charge between C_{par} and C_{os+}/C_{os-} and changing V_{os+}/V_{os-} to counteract the comparison result caused by the offset voltage. After a maximum of 1000 calibration cycles, the offset voltage of the comparator is calibrated. The behavior of the circuit can be better understood with the simulation results of Figure 4.14.

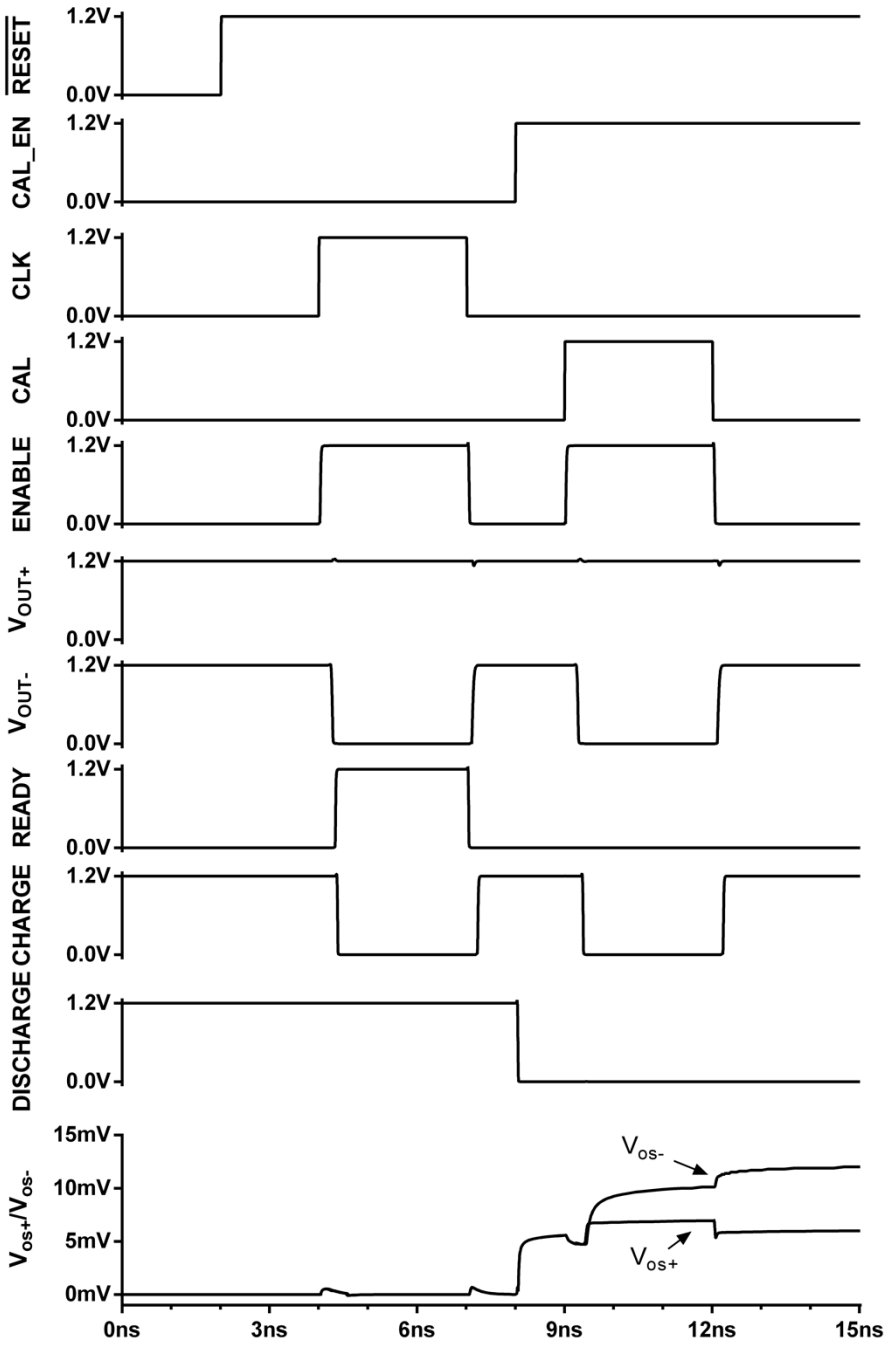

Figure 4.14 – Waveforms of the StrongARM latch with offset calibration circuit.

The comparators 1 and 2 have the lowest input-referred noise value. The sizing of those comparators was done according to [25]. Comparators 3 and 4 have higher input-referred noise values and cannot be designed according to [25]. Since the input differential pair is a dominant contributor to the comparator overall input-referred noise, the width of the transistors of the input pair was swept from minimum width to 20 times the minimum width in a comparator with minimum size transistors. The results which are available in Figure 4.15 were used to design the comparators 3 and 4. The noise of each comparator was obtained with a transient simulation with noise (constrained to 10 GHz) by calculating the probability of '1's for different differential input voltages and fitting these values to a cumulative distribution function (CDF) of a normal distribution. An example with the comparator 1 is

depicted in Figure 4.16.

The standard deviation of the input offset of each comparator was estimated through a 200 runs Monte Carlo simulation. The offset calibration circuit was designed such that an offset of at least 5 standard deviations can be calibrated. The characterization results for each comparator design is summarized in Table 4.3.

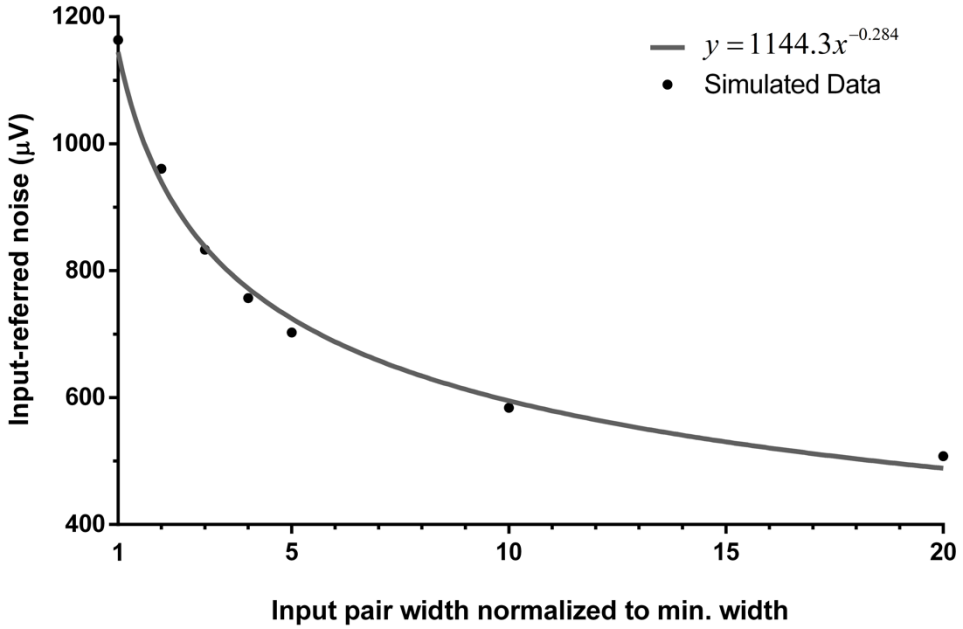

Figure 4.15 – Input-referred noise as a function of the width of the input pair transistors normalized to minimum width for a comparator using minimum width transistors.

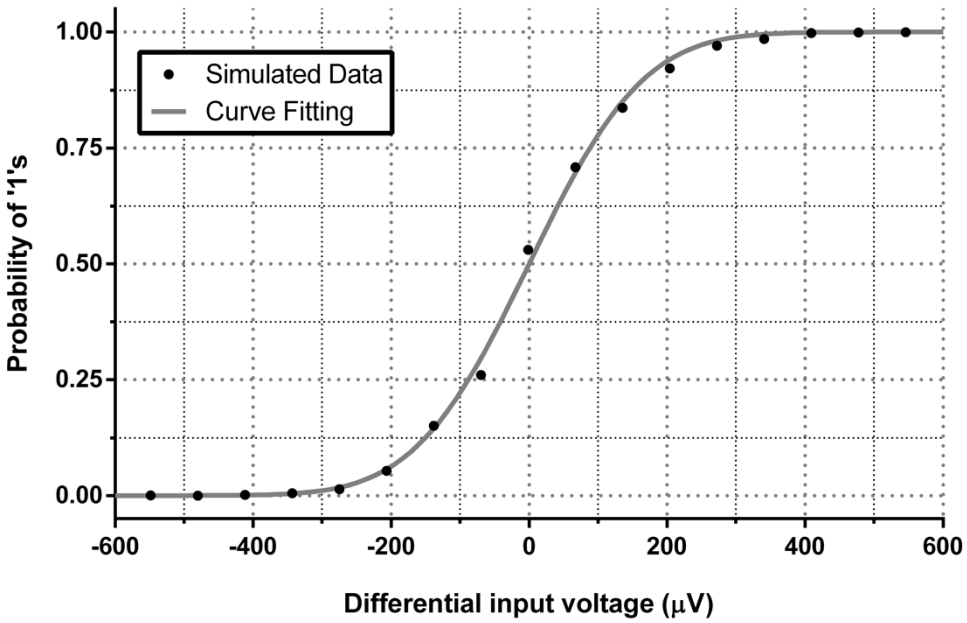

Figure 4.16 – Probability of ‘1’s simulated at different differential input voltages for comparator 1 with fitted CDF.

Table 4.3 – Parameters simulated from the designed comparators.

Parameter	Comparator 1	Comparator 2	Comparator 3	Comparator 4
Noise [μV]	126	243	368	971
Energy [fJ]	496.7	118.9	70.3	60.7
Offset [mV]	4.5	7.2	12.0	46.1
Used in bits	0-1	2-4	5-7	8-13

4.7 Control Logic

The ADC needs some logic to control the DAC switches. A part of the control logic is replicated for each bit. This logic is responsible for generating the control signals that reconfigure the DAC to resolve the next bit and for triggering the next comparator as soon as the DAC is reconfigured. The schematic of this logic is depicted in Figure 4.17. The logic that is instantiated only once is responsible for generating the control signals for the top plate V_{CM} switches, bottom plate V_{IN} switches and bottom plate switches for the perturbation capacitor, for toggling the perturbation sign at the rising edge of the clock signal and for triggering the first comparison. The schematic of this logic is depicted in Figure 4.18. Some of the waveforms are depicted in Figure 4.19.

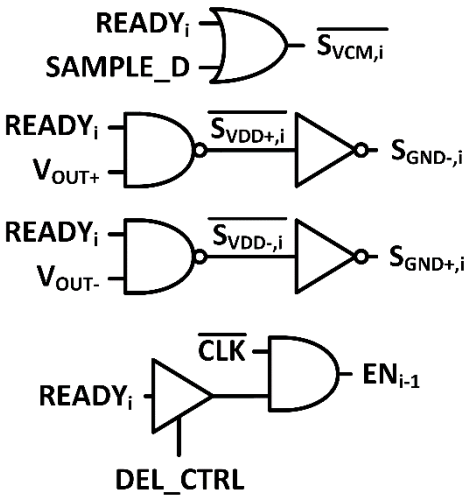

Figure 4.17 – Logic to control the bottom plate switches of the DAC and to trigger the next comparison.

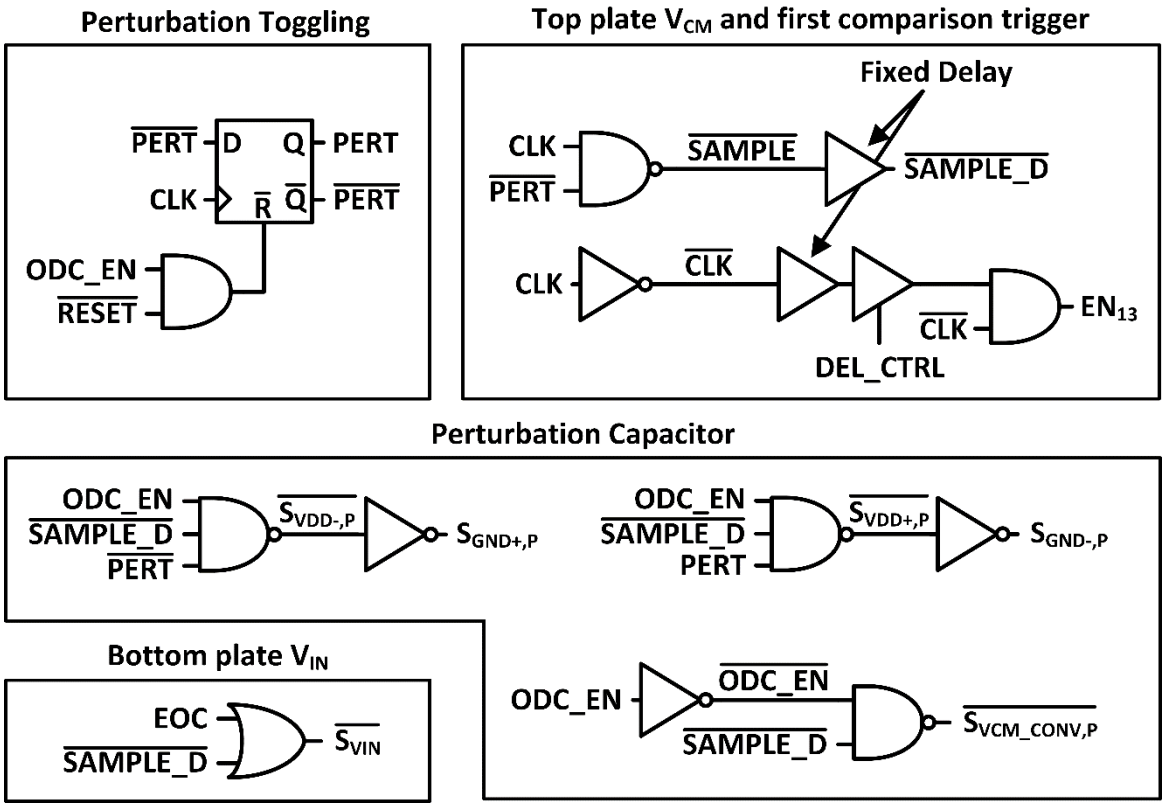

Figure 4.18 – Logic to control top plate V_{CM} switches, bottom plate V_{IN} switches and bottom plate switches for perturbation capacitor, to toggle the perturbation sign and to trigger the first comparison.

A type D Flip-Flop with the inverted output connected to the input is used to generate the *PERT* signal. The *PERT* signal indicates the sign of the perturbation to be applied to the sampled signal during the conversion. The *SAMPLE* signal is used to control the top plate V_{CM} switches. A delayed version of this signal *SAMPLE_D* is needed to control the V_{IN} switches to implement the bottom-plate sampling technique. A standard fixed delay cell from the digital library was used to create this delay. When the ODC is enabled, the sampling only happens when *PERT* is '0' and *CLK* is '1'. When ODC is disabled, the sampling happens at every clock cycle. The *CLK* signal is inverted, goes through a fixed delay cell and through a voltage-controlled delay cell and triggers the first comparator. An AND gate is used to ensure that the first comparator is reset as soon as the *CLK* signal goes low. The perturbation capacitors are always connected to V_{CM} if *ODC_EN* is low. In this case, the $S_{VCM\_CONV,P}$ signal is used to control the V_{CM} switches used during the conversion phase, while the *SAMPLE* signal is used to control the V_{CM} switches used during the sampling phase. When *ODC_EN* is high, the perturbation capacitors are connected to V_{DD} and GND depending on the *PERT* signal to add the perturbation to the sampled signal.

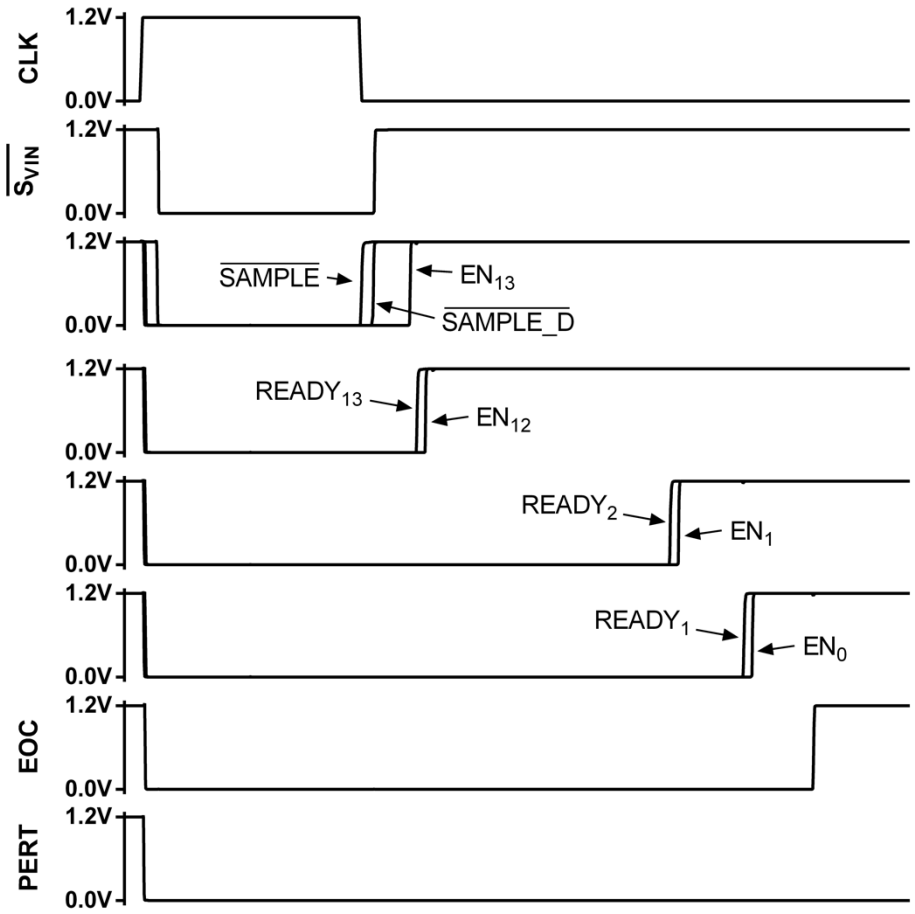

Figure 4.19 – Some of the waveforms generated by the logic when ODC_EN is high.

4.8 Layout

The complete layout of the SAR ADC is depicted in Figure 4.20. Since digital calibration is used to correct mismatch errors of the DAC capacitors, the layout is very straightforward and matching improvement techniques like “common centroid” were not used. The DAC is designed with MOM (Metal-Oxide-Metal) capacitors. Although they have worse matching compared to MIM (Metal-Insulator-Metal) capacitors, they do not require any special process option. The ADC occupies an area of 260 × 155 μm^2.

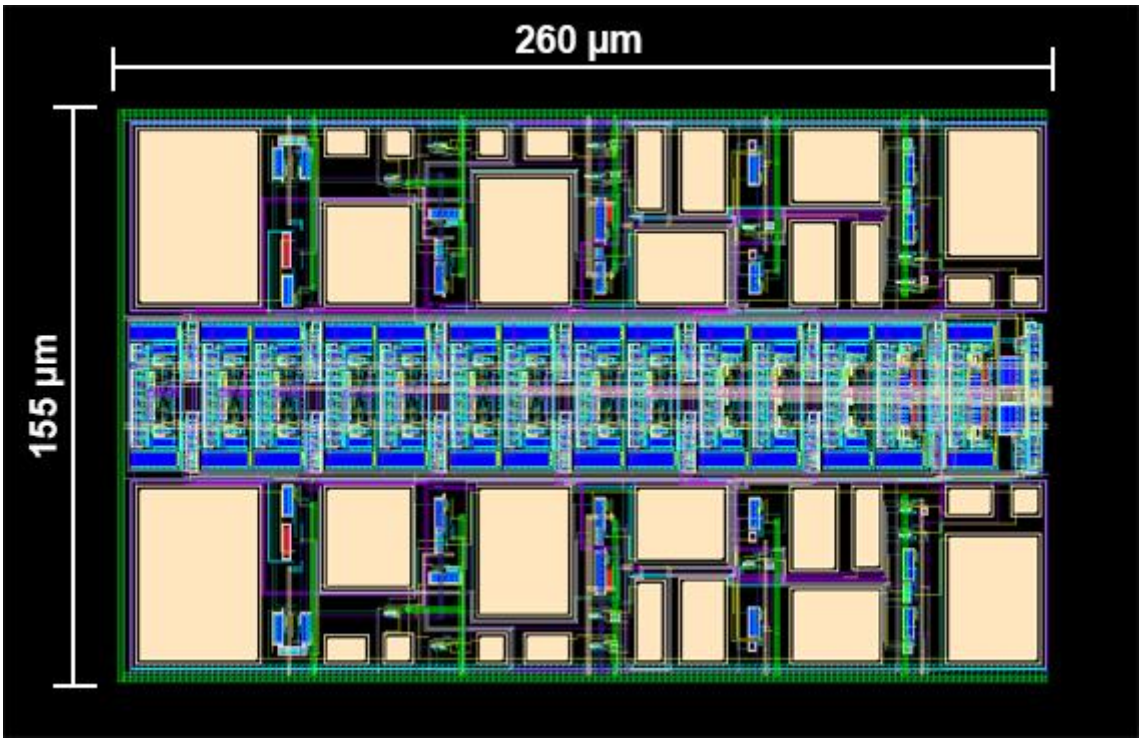

Figure 4.20 – SAR ADC Layout.

Chapter 5

Results and Discussion

5.1 Sampling Time

The on-resistance of the top plate V_{CM} switches and bottom plate V_{IN} switches together with the DAC capacitance will put a limit on the minimum sampling time needed and, consequently, on the maximum achievable sampling frequency. An excessive sampling time ensures correct settling of the sampling circuit and adequate sampling of the input signal at the expense of a lower sampling frequency, while a short sampling time introduces non-linearity due to the incomplete settling of the sampling circuit. A simulation with the DAC and the switches was performed to find the required sampling time. The switches were configured to sample the input signal into the bottom plates. After the sampling phase, the top plate V_{CM} switches and the bottom plate V_{IN} switches are disabled and the bottom plate V_{CM} switches are enabled. An FFT with 512 points is computed with the differential output voltage of the DAC and the ENOB is calculated. To avoid spectral leakage, the sampling frequency and the input frequency were chosen to have coherent sampling. This way a simple rectangular window can be used in the FFT. This was repeated for 6 different sampling times, from 4 to 14 ns. The results are depicted in Figure 5.1.

At sampling times higher than 8 ns the linearity of the sampling circuit limits the ENOB to about 16 bit. The ENOB drops quickly when a sampling time smaller than 8 ns is used, reaching 12 bit at 4 ns. This is due to the incomplete settling of the sampling circuit. We can see from these results that a sampling time lower than 6 to 8 ns should be avoided and no gain in performance is obtained for higher sampling times.

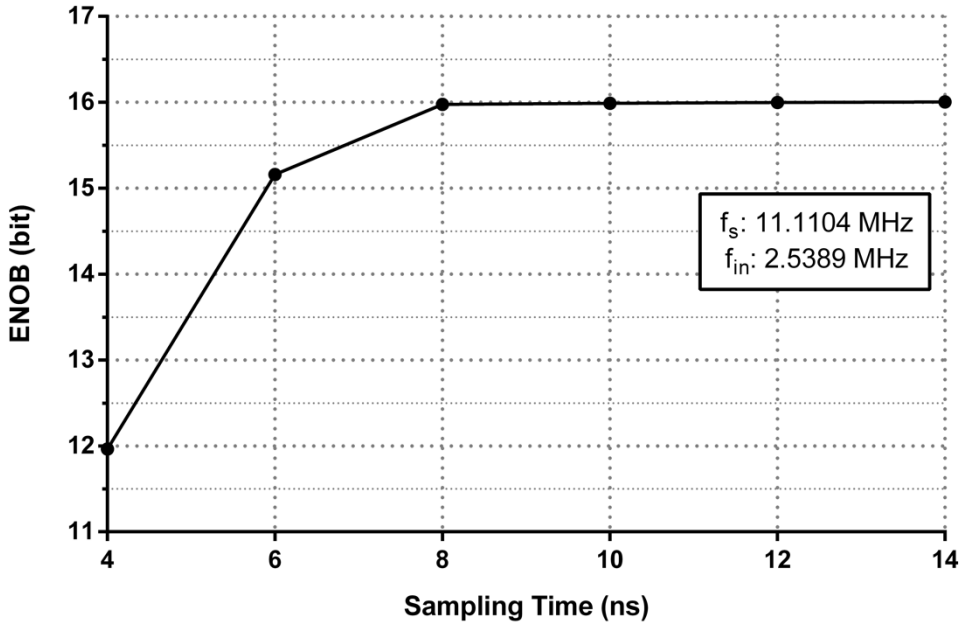

Figure 5.1 – Simulated ENOB of the sampling circuit as a function of the sampling time.

5.2 Sampling Bandwidth

By fixing the sampling time at 8 ns (minimum sampling time before incomplete settling of the sampling circuit starts introducing distortion), sweeping the frequency of the input signal and measuring the amplitude of the sampled signal, it is possible to determine the -3 dB bandwidth of the sampling circuit. The results obtained are depicted in Figure 5.2. A -3 dB bandwidth of around 280 MHz was measured.

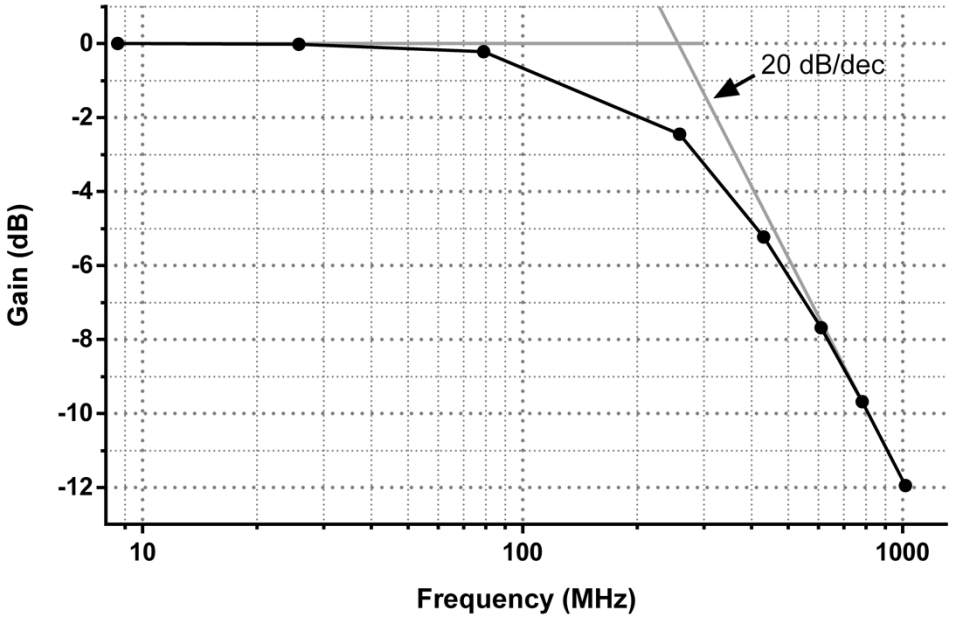

Figure 5.2 – Gain of the sampling circuit as a function of frequency.

5.3 Bottom-plate Sampling

To evaluate the benefit of using bottom-plate sampling in eliminating distortion caused by signal dependent charge injection as discussed in Chapter 3.4, a simulation of the sampling circuit was performed. The input signal was sampled into the DAC capacitors at a 25 MHz rate. To have coherent sampling while capturing 512 samples, the frequency of the input signal was set to 341.796875 kHz. The input signal was sampled for 8 ns. In the first simulation the top plate V_{CM} switches open and only 1 ns later the bottom plate V_{IN} switches open. The opening of the V_{CM} switches injects a constant charge into the DAC capacitors and should not introduce non-linearity into the sampled signal. After sampling, the bottom-plate V_{CM} switches are closed, placing the sampled signal at the output of the DAC. The spectrum of the sampled signal when bottom-plate sampling is used is depicted in Figure 5.3. The third harmonic is the most prominent and is around 100 dB below the fundamental tone. A THD of -100.8 dB was obtained.

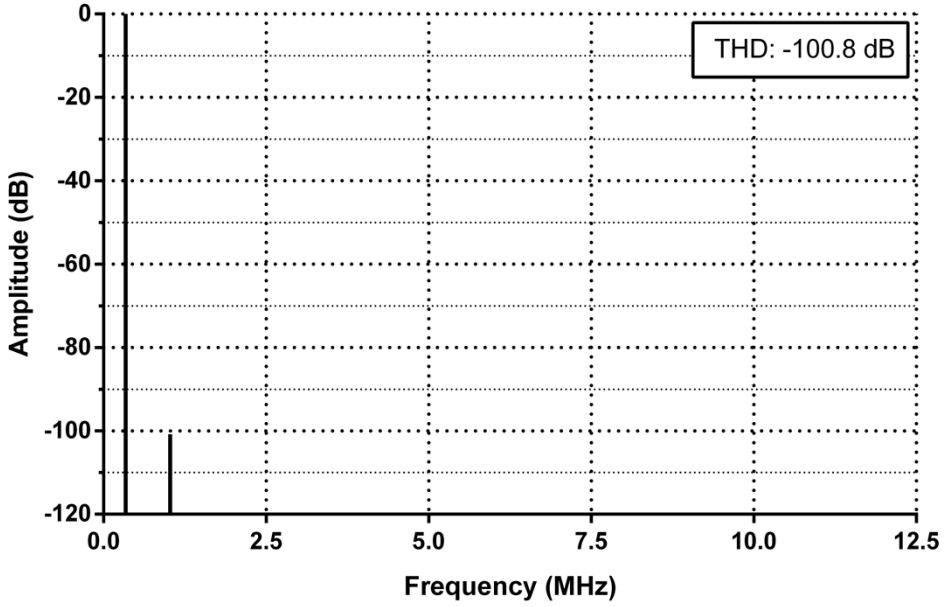

Figure 5.3 – FFT of the sampled signal using bottom-plate sampling.

The same simulation was repeated, but now the bottom plate V_{IN} switches were open first and only 1 ns later the top plate V_{CM} switches open. Although the V_{GS} of the V_{IN} transistors is kept constant with the bootstrapping circuit, the threshold voltage will vary with the input signal in a non-linear way due to the body effect. Therefore, the charge injected into the DAC capacitors is signal-dependent and adds a lot of distortion to the sampled signal as it is possible to see in Figure 5.4. A THD of -61.6 dB was measured, almost 40 dB higher than when bottom-plate sampling is used.

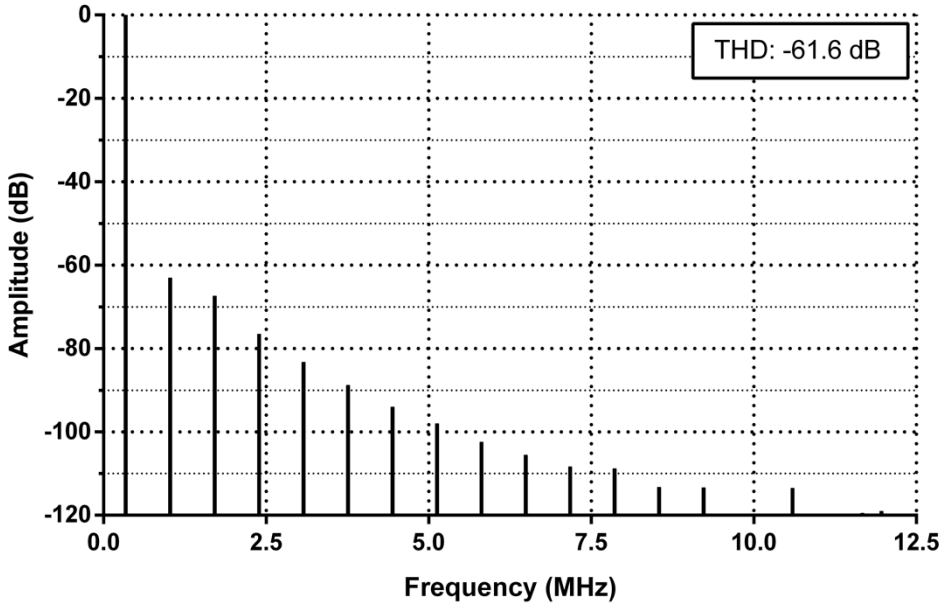

Figure 5.4 – FFT of the sampled signal when bottom-plate sampling is not used.

5.4 Total Output Noise

The paper [17] presents an in-depth analysis of the effect of comparator noise in the ENOB of a radix-2 ADC. Therefore, a 14-bit radix-2 ADC was considered for the noise allocation of each comparator. Unfortunately, their analysis is focused only on radix-2 ADCs and this ADC is out of the scope of the paper. For that reason, a different method was used to estimate the contribution of the noise of the comparators to the total output noise of the ADC. Since circuit simulations with noise take too long and were not possible to do, the contribution of the noise of the comparators to the total output noise power of the ADC was estimated using a model of the ADC that was developed in *MATLAB* because of the difficulty of estimating it analytically. First, the quantization noise was estimated by assuming zero comparator noise and zero sampling noise. An ENOB of 13.3 bit was obtained, which corresponds to a quantization noise of 63.5 µV. Then, another simulation was performed considering the noise of each comparator and zero sampling noise. In this experiment, an ENOB of 12.2 bit was obtained. Considering the quantization noise obtained previously, it is possible to estimate a contribution of 108.9 µV from the comparators to the total output noise of the ADC. All these results are summarized in Table 5.1. Furthermore, using only one comparator as in a typical SAR ADC with 126 µV of input-referred noise (comparator 1), would only reduce the contribution of the comparators on the total noise of the ADC by 16.0 µV, while increasing 3.6 times the comparators total power consumption.

The noise values were obtained with ODC enabled. In this case, two conversions are done for the same sampled signal. The averaging of the two conversions halves both the quantization noise power and the contribution of the comparators to the output noise power. However, the sampling noise is the same, since the two conversions are done with the same sampled signal. For this reason, when ODC is disabled the quantization noise power and the comparators equivalent output noise power doubles.

Table 5.1 – ADC Noise Budget.

	Noise [µV]
Comparators	108.9
Quantization	63.5
Sampling	39.2

5.5 SAR ADC Results

In order to measure the performance of the designed ADC, a differential input voltage of 2.2 V_{pp} with frequency of 1.0595703125 MHz and a clock frequency of 35 MHz were used. Due to the ODC which adds a positive and negative offset to the sampled signal the input full-scale range of the ADC is slightly reduced, hence the lower differential input voltage used. This clock frequency results in a sampling

frequency of 17.5 MHz with ODC enabled. The input signal frequency and clock frequency were chosen to have coherent sampling with a 512 samples FFT. Due to the large computational resources and time needed to simulate the entire ADC, all the digital circuitry was replaced by Verilog models. This greatly accelerates the simulations. A sampling time of 8 ns was used. During the sampling phase, the top plate V_{CM} switches are closed. Thus, the inputs of the comparators have a voltage equal to V_{CM} and their offset can be calibrated. Consequently, an offset calibration cycle is triggered 4 ns after the rising edge of the clock signal. The simulation was performed in *Cadence Virtuoso*. A logger was designed to save the 14 raw bit output data from the ADC. This data was then processed in *MATLAB* to execute the digital calibration algorithm and to extract several dynamic performance parameters, like the ENOB, SNDR, THD and SFDR. Noise was not considered in the simulation due to the very large simulation time needed. Instead, the estimated noise in Chapter 5.4 can be used to estimate the dynamic performance of the ADC in the presence of noise. To verify the effectiveness of the offset calibration and digital calibration of the DAC mismatches, a random 1 run Monte Carlo simulation was performed, including mismatch and process variations. Figure 5.5 shows the results before digital calibration.

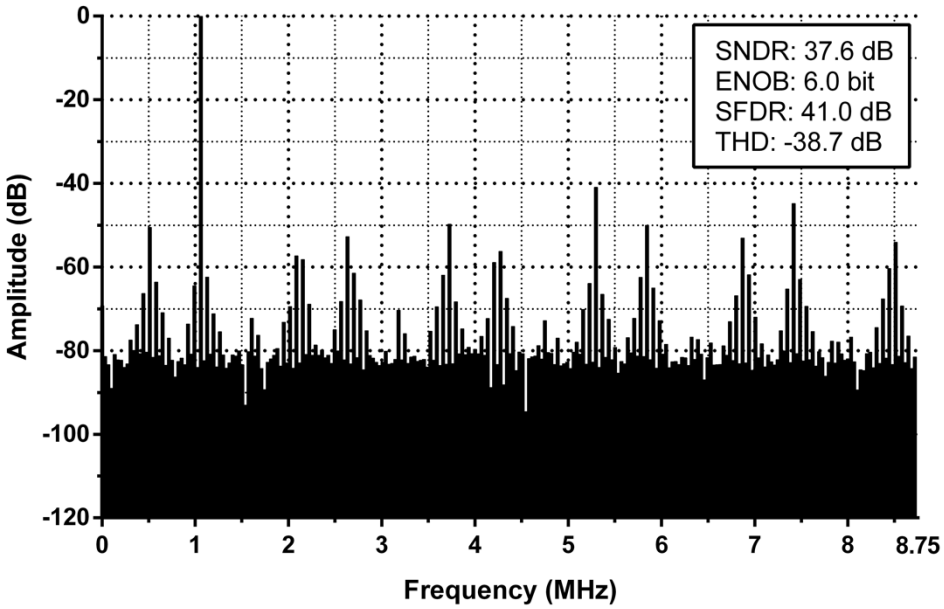

Figure 5.5 – Spectrum of the output of the ADC before digital calibration.

A SNDR of 37.6 dB, corresponding to an ENOB of 6.0 bit, SFDR of 41.0 dB and THD of -38.7 dB were measured. After applying the digital calibration, the results depicted in Figure 5.6 were obtained. A SNDR of 73.1 dB, ENOB of 11.9 bit, SFDR of 85.5 dB and THD of -80.4 dB were obtained, representing, respectively, an improvement of 35.5 dB, 5.9 bit, 44.5 dB and -41.7 dB compared to when digital calibration is not used. Regarding power consumption, an average power consumption of 380 µW was obtained. A power breakdown of the ADC is presented in Figure 5.7. A SNDR of 71.5 dB is estimated with the noise values of Table 5.1, equivalent to an ENOB of 11.6 bit. In this thesis, a dedicated calibration circuit was not designed. However, Liu *et al.* [3] estimates an area of 0.03 mm^2 and a power consumption of 230 µW for the calibration circuit in a similar 130 nm CMOS process. Finally, a FoM of 11.2 fJ/step (as defined in

Equation 5.1) can be estimated having into account the estimated total power consumption and the estimated ENOB.

$$FoM = \frac{Power}{f_s \times 2^{ENOB}} \tag{5.1}$$

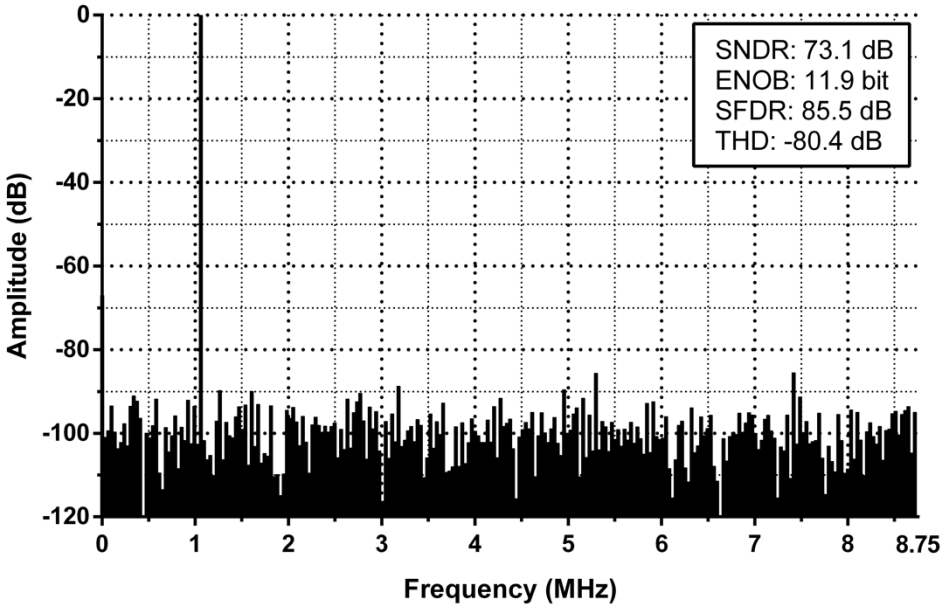

Figure 5.6 – Spectrum of the output of the ADC after digital calibration.

After calibration, the bit weights can be frozen and ODC can be disabled, doubling the sampling frequency of the ADC. An increase of 3 dB of SNDR is expectable, which is equivalent to a loss of 0.5 bit of ENOB. In this mode of operation, a FoM of 7.9 fJ/step can be estimated.

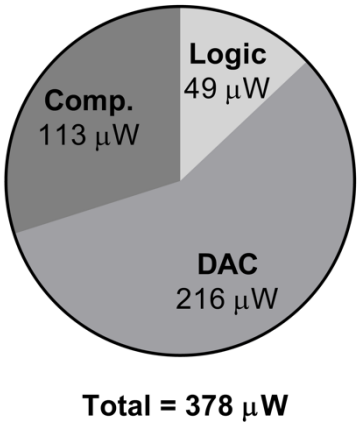

Figure 5.7 – Power breakdown of the ADC.

The estimated ENOB value of 11.6 bit at 17.5 MS/s is lower than the 12.2 bit estimated with the *MATLAB* model. This is most likely not from the distortion introduced by the sampling circuit, since a THD of -100 dB was obtained in Chapter 5.3. The calibration algorithm itself introduces noise. Ideally, the learning

rate should be very low to minimize this noise. However, the number of samples required to complete the calibration increases when the learning rate is reduced. Due to the simulation time, a higher learning rate was used in this work such that the digital calibration finishes in less than 4000 samples. Besides the noise introduced by the calibration algorithm, the calibration of the input offset voltage of the comparators also generates noise. In this work, an offset calibration cycle was triggered for every acquired sample, effectively calibrating the offset of all the comparators in less than 1000 samples. In practise, the offset calibration cycles can be less frequent. Incomplete settling of the DAC or incomplete digital calibration can also be responsible for the lower ENOB value obtained.

Chapter 6

Conclusions

6.1 General Conclusions

SAR ADCs have seen an increase in popularity because they benefit greatly from technology scaling. However, the DAC mismatches are still the linearity limiting factor of this topology. The SAR ADC developed in this thesis tackles this problem using digital calibration. With this technique, the bit weights built into the fabricated ADC are learned. To achieve this, the ODC technique proposed in [3] was used. Some techniques were used to optimize the power consumption of the circuit, namely the usage of multiple comparators as proposed in [17] and the usage of the IMCS switching scheme as proposed in [11]. Due to the non-linearities arising from the different input offset values of each comparator, the offset calibration circuit of [15] was implemented. A comparator offset calibration cycle can be triggered during the sampling phase without slowing down the ADC. The usage of a split-capacitor allowed the DAC to be small even with a significantly large unitary capacitance, minimizing the sampling noise.

The implemented SAR ADC achieves an estimated ENOB of 11.6 bit, operating at a sampling frequency of 17.5 MS/s and occupying an area of 260 × 155 μm^2 while only consuming an average power of 380 µW. The sampling frequency can be doubled after learning the bit weights at the expense of 0.5 bit of ENOB. The digital calibration algorithm used was able to digitally correct the DAC mismatches without adding circuit area or complexity.

6.2 Future Work

The unitary capacitance value used in the DAC could be reduced without much ENOB loss, significantly reducing the circuit area, the DAC power consumption, the DAC settling time and the sampling time and increasing the speed of the circuit. As this topology does not use precision amplification, effects of CMOS technology scaling are not so prominent and a more advanced CMOS process could be used. This would allow the speed of the converter to increase and the area to decrease due to smaller transistor size. The analysis of the noise/power optimization of the comparators of [17] was focused on radix-2 ADCs. Therefore, a similar analysis can be made for sub-radix-2 ADCs. The comparators could then be better optimized and power consumption could be further reduced. Since simulations of the entire ADC are very time consuming, the delay cells were tuned to a relatively high delay to have complete DAC settling. This ensured the best possible results regarding SNDR. One of the advantages of a sub-radix-2 ADC is the built-in tolerance to incomplete settling of the DAC. Therefore, it might be possible to increase the sampling rate of the converter without losing dynamic performance. A simulation of the entire ADC with parasitics extracted from the layout was only performed to check the functionality of the circuit and not to verify its performance due to the long simulation time required. Simulations with noise of the entire ADC were also, for the same reason, not performed. Instead, simulations were only performed to estimate the input-referred noise of each comparator and the total output noise of the ADC was estimated through a high-level model of the ADC developed in *MATLAB*. Fabricating the circuit would allow to verify the results of this analysis.

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