Injection Locked Oscillators with Current Reuse

Mafalda Sofia Ramos Benido

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Electrical and Computer Engineering

Supervisors: Prof. Jorge Manuel Dos Santos Ribeiro Fernandes
Dr. Taimur Rabuske Kuntz

Examination Committee

Chairperson: Prof. Francisco André Corrêa Alegria
Supervisor: Prof. Jorge Manuel Dos Santos Ribeiro Fernandes
Members of the Committee: Prof. José António Beltran Gerald

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I declare that this document is an original work of my own authorship and that it fulfills all the requirements of the Code of Conduct and Good Practices of the Universidade de Lisboa.
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Abstract

The goal of this thesis is to conduct a phase noise behavior analysis in two topologies of ring oscillators, a conventional ring oscillator and a multi-phase ring oscillator. In order to improve the phase noise values, it is also proposed to construct a coupled circuit using injection lock mechanisms.

The proposed circuit intend to minimize the occupation of the circuit die area and the energy consumption. In this way CMOS inverters are used in a 0.13µm CMOS technology and the oscillators do not require the use of inductors in their implementation.

The analysis starts with a comparative study between the conventional ring oscillator with odd number of phases and a more recent implementation circuit for an even number of phases, throughout simulation. The first simulations are performed using a stand alone circuit where only one oscillator is used. Then for the coupled circuit, two approaches are proposed: circuit stack and side-by-side. Where each circuit uses two oscillators simultaneously, with a different number of phases.

The results of the simulations were promising, being proposed at the end of this document suggestions for possible future work to be carried out in order to obtain better results.

Keywords

CMOS Inverters; Oscillators; Coupling; Current reuse; Phase Noise; Injection Lock.
Resumo

O objetivo desta tese prende-se com a realização de uma análise de comportamento do ruído de fase em duas topologias de osciladores em anel, um oscilador em anel convencional e num oscilador em anel de múltiplas fases. Para melhoria dos valores do ruído de fase é também proposta a construção de um circuito acoplado, utilizando mecanismos de ‘Injection lock’.

O circuito proposto pretende minimizar de área do circuito e o consumo energético do mesmo. Desta forma são utilizados inversores CMOS numa tecnologia CMOS 0.13µm e não requerem a utilização de bobinas na sua implementação.

A análise realizada inicia-se com um estudo comparativo entre o oscilador em anel convencional, com número de fases ímpar, e o novo circuito proposto para um número de fases par através de simulação. As primeiras simulações são realizadas com recurso a um circuito de um nível superior denominado por stand alone circuit onde é apenas utilizado um oscilador. No caso das simulações para o circuito acoplado, são propostos dois circuitos para testes, circuito stack e side-by-side. Neste último caso, cada circuito utiliza dois osciladores em simultâneo, podendo ter cada oscilador um número de fases diferentes.

Os resultados das simulações foram promissores, sendo proposto no final deste documento sugestões de trabalho futuro possível de realizar de forma a obter melhores resultados.

Palavras Chave

Inversores CMOS; Osciladores; Acoplamento; Reutilização de corrente; Ruído de Fase; Injection Lock.
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# Acronyms

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<thead>
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<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRO</td>
<td>Differential Ring Oscillator</td>
</tr>
<tr>
<td>FOM</td>
<td>Figure of Merit</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>MPRO</td>
<td>Multi-Phase Ring Oscillator</td>
</tr>
<tr>
<td>PN</td>
<td>Phase noise</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase-locked Loop</td>
</tr>
<tr>
<td>PSS</td>
<td>Periodic Steady-state</td>
</tr>
<tr>
<td>RO</td>
<td>Ring Oscillator</td>
</tr>
<tr>
<td>SERO</td>
<td>Single Ended Ring Oscillator</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage-controlled oscillator</td>
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Introduction

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1.1 Motivation and Problem Definition

Oscillators are one of the most used block in several electronic systems, as clocks in RF systems, analog systems and digital circuits. Those types of circuits usually require low power consumption, low cost, low circuit area and lower noise, while working at high frequencies. The most used oscillators in integrated circuits are LC oscillators, Relaxation oscillators and Ring oscillators. Despite the advantages of LC oscillators, lower phase noise values and high quality factor, ring oscillators can easily integrated and work with a lower supply voltage. \[1\]

This work uses ring oscillators built with CMOS inverters in order to have lower power consumption and reach oscillating frequencies in the order of gigahertz. There are two types of Ring Oscillator (RO): SERO with odd number of phases, and MPRO that can produce an even number of phases. The circuit for the MPRO was already proposed in \[2\] with 4 and 8 phases.

Phase noise (PN) is a phenomenon of oscillators that can influence the entire system where the oscillator is inserted. There are ways to improve PN, for example: circuits with high quality factor like LC circuits, but those circuits have inductors; or using Phase-locked Loop (PLL) but it requires control and reference systems; or with injection lock, connecting two oscillators, one worse than the other, where the worse one intends to approximate itself to the better one in terms of phase noise.

This work intends to use a MPRO to study the behaviour of phase noise on oscillators and compare it to the traditional ring oscillator (SERO). To improve the phase noise performance is proposed to build a circuit using injection lock. This way, the circuit can have two oscillators using multiple frequencies \((f_1 = 2f_0)\) but with phase noise values close to that of the oscillator with lower frequency.

1.2 Goals

This work aims to analyze the phase noise performance of SERO and MPRO topologies and discover a new mechanism to improve phase noise without raising the power consumption and the supply voltage. It is proposed to build a MPRO circuit with 4, 8, 16, 32 and 64 phases and study the performance due to the phase noise and compare with the SERO circuit for 5, 9, 17, 33 and 65 phases, with the expectation that PN is better with more phases on the oscillator. Then, it is proposed to build a coupling circuit, based on injection lock mechanisms, to improve the PN values for the worse oscillator of the circuit.

Our expectations are confirmed by simulation results that show that the phase noise improves with the increase in the number of phases. It also shows that coupling two oscillators, the higher frequency oscillator locks and get better phase noise with the same current for both oscillators on the circuit.
1.3 Outline

This thesis is organized in 5 chapters, split in three main parts. The first part for the introduction and first considerations. The second part for the method and results. And a third and final part for the conclusions.

The first part has two chapters. This first chapter, Introduction, briefly presents the motivation and goals to this work. In the second chapter, Background review, is made an overview to the basic concepts that are needed to understand the work done. This chapter presents a general overview of oscillators, LC oscillators, relaxation oscillators and ring oscillators, and the possible inverters to use.

The second part has also two chapters. The chapter 3, Method, where the circuits to be tested are explored and has a brief explanation of the simulations. The chapter 4, Results and Discussion, presents and discuss the results obtained from the simulations made to the circuits presented on chapter 3.

The final part is chapter 5, Conclusions, where it is presented the general conclusions and proposes future work to be done.

In Appendix A, is presented the paper for this work.

1.4 Original Contributions

The contribution of this thesis consists in the design of a new coupling architecture of an injection locked circuit with two oscillators stacked, that reuses the supply current. This circuit is able to have multiple phases in a ring oscillator with two frequencies, achieving better phase noise in the worse oscillator.

This work has one accepted paper for a lecture on ISCAS that will be presented in May 2019. The paper is presented in the appendix A of this document.
2 Background Review

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In this chapter several concepts are explained to understand the circuits to study. In addition to an introduction to the oscillators and the different topologies of oscillators, this chapter will focus on Ring Oscillators and CMOS inverters.

2.1 Oscillators

Oscillator is a circuit that produces a periodic signal, sine wave or square wave for example, from a power supply (DC signal). This output signal is characterized by frequency and amplitude. This circuit can be modelled by a linear feedback system, figure 2.1, with the transfer function (2.1).

\[
\frac{Y(s)}{X(s)} = \frac{A(s)}{1 - A(s)\beta(s)}
\]  (2.1)

![Feedback system block diagram.][2]

To oscillate, the system has to comply the Barkhausen’s criterion where \(1 - A(s)\beta(s) = 0\). It results that \(|A(j\omega)\beta(j\omega)| = 1\) and \(arg|A(j\omega)\beta(j\omega)| = 0\). Ensuring the criterion, it has the necessary conditions to oscillate. [3]

There are different types of oscillators. The three most used oscillators implemented in Integrated Circuit (IC) are the LC Oscillators, Relaxation Oscillators, and the Ring Oscillators.

2.1.1 Oscillators topologies for Integrated circuits (IC)

LC Oscillators

An LC oscillator is a circuit with an inductor-capacitor network with losses compensated by a differential pair. The main advantages for this type of oscillators are the high quality factor, low PN and the low power consumption. However, they have inductors in their implementation that occupies a considerable amount of die area, specially when it is intended to have multiple-phases generation. [4]
Relaxation Oscillators have resistors and capacitors as passive devices. They have higher phase-noise and lower quality factor when compared with LC oscillators, but they have a lower area and cost, capable to be used in integrated circuits. The circuit presented in figure 2.3 works by charging and discharging the capacitor alternately, being the frequency obtained by $f = \frac{1}{2\pi RC}$. 

Figure 2.2: Circuit for a LC Oscillator. [5]
However, this oscillator does not present a rail to rail behaviour, where the output signal does not go from 0 to $V_{DD}$.

**Ring Oscillators**

A basic topology of a RO consists of an odd number of delay cells, connected in series to make a chain, shown in the figure 2.4. Each delay cell has a propagation delay time ($t_p$) and the oscillation frequency depends directly on the numbers of stages ($N$) in the chain, $f = \frac{2}{\pi N t_p}$. Each cell output has a different phase. [1]
Although this is not the topology with the best PN performance, this circuit has a simpler implementation, lower area and consumption, and it has a rail to rail behaviour when compared to LC and Relaxation oscillators. [7] For these reasons, it was chosen to use the RO for the circuits to be developed and examined on this work, that will be explained later on this chapter.

The next section is focused on the phase noise parameter that allows to evaluate the performance of a oscillator.
2.1.2 Phase Noise (PN)

The spectrum of an ideal oscillator is a single frequency line. In reality, a practical sinusoidal oscillator has sidebands near the central frequency, as presented in Figure 2.5.

![Ideal Oscillator](image1.png) ![Non-Ideal Oscillator](image2.png)

*Figure 2.5: Oscillator Spectrum comparison. [8]*

PN is a parameter used to evaluate the performance of an oscillator. This parameter allows to measure the small phase variations on an oscillator, it compares the energy of the central frequency with the energy at a certain frequency offset, integrated in a 1Hz band. [1] It is defined by the ratio of the noise power in a specific frequency \( L(f_n) \), where \( f_n = f_0 + \Delta f \), and the power in the oscillator central frequency, \( f_0 \).

\[
L(f_n) = \frac{P(f_n)}{P(f_0)}
\]  

(2.2)

Oscillators are normally represented by single sideband PN, with an asymptotic plot of the output noise spectrum, Figure 2.6.
As it is shown in the figure above, the PN has 3 main regions: [5, 9, 10]

- The first region, before $\omega_1$, has a -30 dB/decade slope due to the noise of active devices.
- The second region, between $\omega_1$ and $\omega_2$, has a -20 dB/decade slope due to the frequency modulation by the white noise sources.
- The third region, after $\omega_2$, is due to white noise sources.

In the case of a square wave, the energy divides throughout the harmonics of the oscillator.

### 2.2 Ring Oscillators (ROs)

In this section several types of ROs are presented. It is also present a comparison between single-ended and multi phase circuits based on PN, frequency and power consumption.

#### 2.2.1 Single-ended Ring Oscillators

A single-ended ring oscillators is a chain where the delay cells are CMOS inverters, with an odd number of stages to oscillate. Each inverter output has a different phase. The frequency is directly dependent of the number of stage of the chain and the time delay of each inverter used. This way, the frequency is higher when the chain is smaller. This topology needs less die area compared to other RO topologies. [1, 4]
In order to have an even number of phases it is required another RO topology. Some topologies will be explored in the next sections.

**CMOS Inverter**

From a digital perspective, an inverter is a circuit that change the logic level of a signal. The ideal behavior of this cell is represented in figure 2.8, it is shown that the change occurs instantaneously to the output. The delay of this cell is dependent on the type of the inverter.

One type of inverter used in oscillators is the CMOS inverter, comprising two MOS transistors, a PMOS and a NMOS, as shown in figure 2.9.
Figure 2.9: Topology of an CMOS inverter.

This circuit has a voltage transfer characteristic presented in figure 2.11 and it is similar to the ideal inverter transfer function.

Figure 2.10: Voltage transfer characteristic of an CMOS inverter. [6]

This circuit die area is very small, it is only dependent on the size of one PMOS and one NMOS devices. It is a simpler cell, easy to design.
The time delay of this cell is important and it can be obtained with the equation (2.3) [3].

\[ t_p = \frac{t_{HL} + t_{LH}}{2} \]  

(2.3)

Where,

\[ t_{HL} = \frac{\Delta V}{I_{av}} C_L \]  

(2.4)

Considering the specifications used in simulation, \( V_{DD} = 1.2V \) and \( V_t = 0.3 \) \( V_{DD} \), the equation (2.4) becomes: [2]

\[ t_{HL} = \frac{1.77}{k_n} C_L \]  

(2.5)

\[ t_{LH} = \frac{1.77}{k_p} C_L \]  

(2.6)

Another advantage of this cell is the power consumption. The CMOS inverter has no static power and a dynamic power consumption (2.7) that is dependent on the supply voltage (\( V_{DD} \)) and the output node capacitance (\( C_L \)). [3]

\[ P = f \cdot C_L \cdot V_{DD}^2 \]  

(2.7)

To reduce the power dissipation in this inverter there are two strategies: using a lower supply voltage, or minimizing the output capacitance decreasing the transistors size.
### Inverter Latch

This block is built from two inverters cross-coupled in a closed loop, figure 2.12, i.e. with the input of one inverter connected to the output of the other inverter.

![Figure 2.12: Topology of a Latch with two inverter cells.](image)

This circuit has three operating points, as it is shown in figure 2.13. Two points are stable points where the circuit can stay in that state indefinitely, only with a strong variation can alter this state. One is an unstable point where the circuit is very sensitive to any small change that occurs.

![Figure 2.13: Latch operating points.](image)

### 2.2.2 Differential Ring Oscillators (DRO)

A Differential Ring Oscillator (DRO) works with an even or odd number of delay cells, generating either even and odd number of phases, figure 2.14. [4] It can be an alternative to a single-ended ring oscillators. Each delay cell is a differential inverter, built with a differential pair, figure 2.16. The inverter output is intersect and connected to the next inverter.

This topology has a better common-mode rejection of supply and substrate noise than the single-ended, and it is easier to have a higher frequency. However, it is more complex to design and it needs more area. Single-ended ring oscillators have better PN performance and have lower energy consumption. [4, 12]
Differential Inverter

An inverter can also be built with a differential pair. This topology of inverter allows the block, figure 2.15, to have two inputs \( V_{\text{in}^-} \) and \( V_{\text{in}^+} \) and two outputs \( V_{\text{out}^-} \) and \( V_{\text{out}^+} \).

This topology behavior is the same of a normal differential pair, it depends on the type of differential pair that is used. In figures 2.16 and 2.17 is presented an example of differential pair and his dynamic behavior.
This cell has a larger die area and more power consumption than a simpler inverter cell, and it does not provide full scale output signals. In contrast to CMOS inverters, this circuit has static power:

\[ P = V_{DD} \cdot I_{SS} \]  

Comparing the area and power consumption for both CMOS and differential inverters, we will build the oscillator with the latch and the ring oscillator using CMOS inverters.

### 2.2.3 Multi-Phase Ring Oscillators

The multi-phase ring oscillators topology is based on coupled ring oscillators. One topology for a multiple phase oscillator could be achieved through a combination of ring oscillators chains. For example, in a Four-Phase Ring Oscillator topology there are four 3-stage ROs interconnected. The output of each delay cell is not only connected to the next stage of the RO, but it is also connected to an intermediate level to produce other phases, resulting in the scheme of figure 2.18.
This topology main disadvantages are the increase of die area and the increase in energy dissipation. However, the PN is expected to be better compared to the conventional one. [1, 7, 14]

In this work it is chosen to study the N-phase RO with CMOS inverters. In particular, it is proposed to build the above circuit with more phases, 32 and 64 for example, and without the current mirrors.

Analyzing the information presented throughout this chapter, the circuit to study in the context of this work is a multi-phase ring oscillators similar to the figure 2.18 built with: a RO for the external chain, and latches for the internal circuit, using CMOS inverters as the basic cell.

The first design and schematic of the oscillator will be presented in the next chapter, as well as the methodology used in the course of this work.

2.3 Injection Lock and Phase Locked Loop

Injection lock happens on a oscillator when it is disturbed by another oscillator working at a nearby frequency, making them to lock at the frequency of the strong oscillator (oscillator that disturb). Injection locking is a phenomenon that can occur by coupling two or more oscillators or synchronizing with external signals, and helps to improve the phase noise value of the oscillator. If the coupling is not strong enough, the frequencies do not lock. [15, 16]

Alternatively, a Phase Locked Loop (PLL) is a powerful and complex system that generate an output signal with the phase related to input signal phase. The circuit consists of a phase detector, a low pass filter and a Voltage-controlled oscillator (VCO) in a feedback loop to generate the signal, figure 2.19. The oscillator generates a periodic signal, and the phase detector compares the phase of the signal with the phase of the input periodic signal, adjusting the oscillator to keep the phases locked. This way, PLL can track the input frequency or it can generates a multiple of that frequency.

![Figure 2.19: PLL basic diagram.](image)

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3 Method

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This chapter intends to show the circuits used to simulate and obtain values.

3.1 Oscillators used

SERO - Singled-Ended Ring Oscillator

To simulate the oscillator with an odd number of phases, the circuit for the oscillator is called SERO and it is a basic ring oscillator as presented in chapter 2, on figure 2.7. This circuit does not have the internal latches. On the next figure it is shown the diagram for the 5-phase case.

![Figure 3.1: Diagram of 5-phases SERO circuit.](image)

MPRO - Multi-Phase Ring Oscillator

In order to simulate and compare the results, the circuit implemented for the multi-phase oscillator is built expanding the circuit presented in the figure 2.18 to the 4-phase case, as presented on the diagram of the figure 3.2. This circuit is called MPRO and it has an external chain of inverters with internal latches connected to the output of the ring inverters, the latch circuit used was presented in the figure 2.12. With this topology is possible to have a large number of phases.

![Figure 3.2: Diagram of N-phases MPRO circuit.](image)
3.2 SERO and MPRO circuits

The objective of first simulations is to start a comparison between SERO and MPRO for PN values. The simulations are made with CADENCE using oscillators with CMOS inverters from a digital library implemented in 130 nm MOS technology.

In addition, these simulations helped to learn how to work with the schematic and simulation environments using CADENCE.

In this work, this circuits are implemented with 5, 9, 17, 33 and 65 for the SERO, and 4, 8, 16, 32 and 64 phases for the MPRO.

3.2.1 Inverter

The CMOS inverters used has a $\frac{W_p}{W_n} = 1.13$ relation size between the MOSFETs and it belongs to a existent library $FSC0H_D\_GENERIC\_CORE$.

![Figure 3.3: Schematic of the inverter.](image)

Beside the comparison between the number of phases of each oscillator, those simulations are also used to compare the PN values of a oscillator with different size inverters. This way, the size on the inverter of the figure 3.3 is increased with the multiplier (m) parameter available on CADENCE. This parameter builds a bigger inverter connecting the smaller inverters in parallel, maintaining the L and increasing W by m times.

The table bellow indicates the inverters used on this work.

<table>
<thead>
<tr>
<th>Multiplier (m)</th>
<th>InvC</th>
<th>InvG</th>
<th>InvK</th>
<th>InvN</th>
<th>InvQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>4</td>
<td>8</td>
<td>20</td>
<td></td>
</tr>
</tbody>
</table>

Table 3.1: Inverter size table.
3.2.2 Stand alone circuit

In order to test SERO and MPRO oscillators, a high level circuit is created and used on the test-bench. This circuit has one oscillator.

![Figure 3.4: Stand alone circuit.](image)

This test circuit is submitted to a PSS and PNoise analysis to achieve the PN waveform and the values for 3 specific $\Delta f$ (100kHz, 1MHz and 10MHz). Those simulations provide the values for the SERO and MPRO for further comparison.

3.3 Injection locked circuits

As previously explained in chapter 2, injection lock is a known technique to improve phase noise performance on oscillators. This method synchronize frequencies from oscillators whose frequency is near the slower oscillator, or near a multiple from that frequency. There are several ways to connect the devices to influence each other, in this work will be explored two different approaches: the side-by-side circuit and the stack circuit.

3.3.1 Side-by-side circuit

This circuit consists in two oscillators connected side-by-side, as shown in the next figure. The oscillators are working under the same supply voltage, sharing the necessary current between them.
3.3.2 Stack circuit

The stack circuit has two oscillators connected like a stack, as shown in the next figure. The oscillators are sharing the same supply voltage, operating with 600mV each, reusing the same current for both of them.

3.4 Analysis work flow

To evaluate the PN behaviour, several simulations were made in two different stages. The first one, the simulated circuit was the Stand Alone circuit, figure 3.4, with both types of oscillators, SERO and MPRO, for five different phases each. The selected phases wanted to be closed for both oscillators.
to have a fair comparison of the values. Later on, the same simulations were made for coupling cir-
cuits, figure 3.5 and 3.6, with both oscillators. The values were registered and the calculation of the
Figure of Merit (FOM) value is found, in accordance with the formula presented later on chapter 4. The
presentation and discussion of the results will be presented on the next chapter.

![Method flowchart](image)

**Figure 3.7:** Method flowchart.

The simulations were the same for all types of circuits and oscillators. Those simulations split up
in three types of analysis. The first was a transient analysis to verify the oscillation and accurate the
frequency value, followed by as Periodic Steady-state (PSS) and a Phase noise (PNoise) analysis to
calculate the PN value for each circuit.
Simulations Results and Discussion

Contents

4.1 Initial results ............................................................... 32
4.2 Alpha Relation ............................................................. 41
4.3 Coupling circuits ........................................................... 45
This chapter intends to show the results of the simulations. First, the initial results for the single-ended and multi-phase oscillators with the stand alone circuit. These results intend to compare the variation of PN with the number of phases and the size of the inverters. The comparison of the initial results is subsequently supported with a FOM to standardize the results. The second part of this chapter presents an hypothesis to improve PN value for the MPRO oscillator vary the size of internal and external inverters. To end the chapter, another hypothesis results are presented to improve PN, coupling circuits.
4.1 Initial results

In order to analyze the PN behaviour, the SERO and MPRO oscillators were simulated using the stand alone circuit, under the same conditions as presented on figure 3.4. The results are presented in the next subsections.

4.1.1 SERO oscillator

![Phase noise results for (a) 5-phase SERO and with (b) InvG.](image)

The PN increases in module with the increase in size of the transistors. In this case, PN improves approximately 3dB when the size is doubled. In figure 4.1 a) is possible to observe two different regions in the PN spectrum: before 10 MHz all curves has a -30 dB/decade slope, after 10 MHz the slope changes...
to -20 dB/decade. This behavior was expected as illustrated in figure 2.6.

In figure 4.1 b) is possible to observe the improvement of PN with the increase in the number of phases of the oscillator for the same size of inverters.

### 4.1.2 MPRO oscillator

For the MPRO oscillator, it has two types of inverters: one for the external ring, and other for the internal latches, as it is showed in figure 3.2. In these simulations, the inverters has the same size for both types, the external ring and internal latches.

![MPRO oscillator diagram](image)

(a) 4-phase MPRO, with different inverters.

![Inverter G for different phases](image)

(b) Inverter G for different phases.

**Figure 4.2:** MPRO phase noise results for (a) 4-phase and with (b) InvG.

The PN behavior of MPRO curves due to the size of the inverters are similar to the SERO curves. There are also a difference of -3 dB approximately between the lines of the sizes in figure 4.2 a). It is
equally possible to observe the same two regions of asymptotic spectrum of the PN as it was observed to the SERO oscillators: after 10 MHz the slope is also -20 dB/decade.

4.1.3 SERO oscillator vs MPRO oscillator

![Phase Noise (10 MHz)](image)

(a) SERO phase noise results.

![Phase Noise (10 MHz)](image)

(b) MPRO phase noise results.

Figure 4.3: SERO (a) and MPRO (b) phase noise results for $\Delta f = 10$ MHz.

Observing the figures above, the values of PN in MPRO are worse than the values of PN in SERO for the lower number of phases. For example, for SERO 9-phases and MPRO 8-phases the PN values are $-111.5$ and $-110.2$, respectively. For SERO 65-phases and MPRO 64-phases the PN values are $-129.9$ and $-130.7$, respectively.

This result was not expected. This work proposes two solutions for this problem: change the size of
external and internal inverters separately [2], or use coupling circuits with injection lock.

**Frequency behavior explanation**

In the next figure it is shown the frequency graphs for both circuits. The frequency decreases significantly as expected, once is directly dependent on the number of delay cells present in the circuit.

![SERO frequency graph](image1)

![MPRO frequency graph](image2)

**Figure 4.4:** SERO and MPRO frequency graph.

Observing the graphs, the behaviour is similar for both circuits. However, for MPRO circuit it achieves much higher frequencies (in the order of 7.3 GHz) for larger inverters, and it also achieve lower frequencies (in the order of 350 MHz) for a higher number of phases.
Power behavior explanation

In the next figure it is shown the power graphs for both SERO and MPRO. The power stays the same even though the number of inverters (stages) increase.

In figure 4.5, the power graphs are similar for both circuits. However, for MPRO circuit the power values are much higher, once the number of inverters on the circuits for each group of phases are doubled.

(a) SERO.

(b) MPRO.

Figure 4.5: SERO and MPRO power graph.
The power behavior could be explained looking into the figure 4.6. An inverter only spend energy when the signal is changing. The energy consumption is zero when the output value of an inverter is stable. In detail at the figure 4.6 it is possible to identify a small group of cells (always the same number over the time) that are in transition at the same time and that keeps the power value over the time, even if the number of phases increases. This way, the power is only dependent on the number of cells of the transition group and the size of the transistors inside of the inverters.

In other way, the current has a constant medium value. This phenomenon is due to the current used by the inverters in signal transition.

The total current has a constant medium value, noticing only peaks of current. This phenomenon happens since that is a group of cells always in transition. For a oscillator with 8 phases, example of figure 4.7, the current has 8 peak that corresponds to the 8 inverters of the external ring of MPRO oscillator, when the signal transition occurs.
Figure 4.6: Inverters in signal transition.

(a) 8 phases circuit.

(b) 32 phases circuit.
Figure 4.7: Current results in PMOS transistor and Vdd.
4.1.4 Figure of Merit (FOM)

To make a better comparison between the oscillators, it is used FOM of equation (4.1). This FOM consider the PN measurement at a certain $\Delta f$ frequency and the influence of the $\Delta f/f$ ratio, the power consumption $P_{DC}$ and a $P_{ref} = 1 \text{ mW}$.

$$FOM = L_{meas}(\Delta f) + 10 \log \left( \frac{(\Delta f/f)^2}{P_{DC}/P_{ref}} \right)$$  \hspace{1cm} (4.1)

Tables 4.1 and 4.2, show results for three different conditions: $\Delta f = 1 \text{ MHz}$, $\Delta f = 10 \text{ MHz}$, and $\Delta f/f = 0.02$.

**Table 4.1: InvG table SERO**

<table>
<thead>
<tr>
<th>Phase Number</th>
<th>Power [mW]</th>
<th>Freq. [MHz]</th>
<th>PN (\Delta f) [dBc/Hz]</th>
<th>$\Delta f$ [MHz]</th>
<th>$\Delta f/f$</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>0.42</td>
<td>6 933.3</td>
<td>-75.8</td>
<td>1.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>0.42</td>
<td>3 824.1</td>
<td>-83.5</td>
<td>1.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>0.42</td>
<td>2 024.4</td>
<td>-91.4</td>
<td>1.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>0.42</td>
<td>1 042.9</td>
<td>-99.3</td>
<td>1.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>65</td>
<td>0.42</td>
<td>529.5</td>
<td>-107.0</td>
<td>1.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>0.42</td>
<td>6 933.3</td>
<td>-103.9</td>
<td>10.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>0.42</td>
<td>3 824.1</td>
<td>-110.6</td>
<td>10.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>0.42</td>
<td>2 024.4</td>
<td>-117.2</td>
<td>10.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>0.42</td>
<td>1 042.9</td>
<td>-123.6</td>
<td>10.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>65</td>
<td>0.42</td>
<td>529.5</td>
<td>-129.8</td>
<td>10.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>0.42</td>
<td>6 933.3</td>
<td>-94.6</td>
<td>138.7</td>
<td>0.0200</td>
<td>-132.3</td>
</tr>
<tr>
<td>9</td>
<td>0.42</td>
<td>3 824.1</td>
<td>-95.6</td>
<td>76.5</td>
<td>0.0200</td>
<td>-133.3</td>
</tr>
<tr>
<td>17</td>
<td>0.42</td>
<td>2 024.4</td>
<td>-102.8</td>
<td>40.5</td>
<td>0.0200</td>
<td>-140.6</td>
</tr>
<tr>
<td>33</td>
<td>0.42</td>
<td>1 042.9</td>
<td>-120.9</td>
<td>20.9</td>
<td>0.0200</td>
<td>-158.7</td>
</tr>
<tr>
<td>65</td>
<td>0.42</td>
<td>529.5</td>
<td>-119.7</td>
<td>10.6</td>
<td>0.0200</td>
<td>-157.5</td>
</tr>
</tbody>
</table>
### Table 4.2: InvG table MPRO

<table>
<thead>
<tr>
<th>Phase Number</th>
<th>Power [mW]</th>
<th>Freq. [MHz]</th>
<th>PN (Δf) [dBc/Hz]</th>
<th>∆f [MHz]</th>
<th>(\frac{\Delta f}{f})</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>1.04</td>
<td>7324.8</td>
<td>-71.5</td>
<td>1.0</td>
<td>0.0001</td>
<td>-148.7</td>
</tr>
<tr>
<td>8</td>
<td>1.07</td>
<td>3502.5</td>
<td>-81.7</td>
<td>1.0</td>
<td>0.0003</td>
<td>-152.3</td>
</tr>
<tr>
<td>16</td>
<td>1.07</td>
<td>1749.9</td>
<td>-90.4</td>
<td>1.0</td>
<td>0.0006</td>
<td>-155.0</td>
</tr>
<tr>
<td>32</td>
<td>1.07</td>
<td>875.0</td>
<td>-99.9</td>
<td>1.0</td>
<td>0.0011</td>
<td>-157.5</td>
</tr>
<tr>
<td>64</td>
<td>1.07</td>
<td>437.5</td>
<td>-107.1</td>
<td>1.0</td>
<td>0.0023</td>
<td>-159.7</td>
</tr>
<tr>
<td>4</td>
<td>1.04</td>
<td>7324.8</td>
<td>-100.3</td>
<td>10.0</td>
<td>0.0014</td>
<td>-157.4</td>
</tr>
<tr>
<td>8</td>
<td>1.07</td>
<td>3502.5</td>
<td>-109.6</td>
<td>10.0</td>
<td>0.0029</td>
<td>-160.2</td>
</tr>
<tr>
<td>16</td>
<td>1.07</td>
<td>1749.9</td>
<td>-117.2</td>
<td>10.0</td>
<td>0.0057</td>
<td>-161.8</td>
</tr>
<tr>
<td>32</td>
<td>1.07</td>
<td>875.0</td>
<td>-124.2</td>
<td>10.0</td>
<td>0.0114</td>
<td>-162.8</td>
</tr>
<tr>
<td>64</td>
<td>1.07</td>
<td>437.5</td>
<td>-130.8</td>
<td>10.0</td>
<td>0.0229</td>
<td>-163.4</td>
</tr>
</tbody>
</table>

Comparing tables 4.1 and 4.2 and according to the FOM used, FOM values are higher for an higher number of phases of the oscillator in both cases, SERO and MPRO. However, FOM values are worse for MPRO due to the difference in power consumption on the circuits. The decrease in PN is not enough to compensate the increase in power.

Therefore, there is no advantage of MPRO (with an \(\alpha = 1\) relation, this ratio will be explained in the next section) over the conventional SERO.

### 4.2 Alpha Relation

One solution to improve the MPRO is to change the size of the inverters. For that, a parameter \(\alpha = \frac{K_{ext}}{K_{int}}\) relate the size of external and internal (latch) inverters. The table 4.3 shows the relation between the inverters, and the figure 4.8 shows the oscillation range of the alpha relation.

The first step is to run all the simulations for the possible combinations and analyses it in the same way. Extract curves and values to compare and select the best alpha ratio in order to have a better phase noise.

Then, combine the results with the reference [2] and build a oscillator to obtain experimental measurements.
Table 4.3: Alpha ratio.

<table>
<thead>
<tr>
<th>Ring</th>
<th>C</th>
<th>G</th>
<th>K</th>
<th>L</th>
<th>N</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>1</td>
<td>0.5</td>
<td>0.25</td>
<td>0.2</td>
<td>0.125</td>
<td>0.05</td>
</tr>
<tr>
<td>G</td>
<td>2</td>
<td>1</td>
<td>0.5</td>
<td>0.4</td>
<td>0.25</td>
<td>0.1</td>
</tr>
<tr>
<td>K</td>
<td>4</td>
<td>2</td>
<td>1</td>
<td>0.8</td>
<td>0.5</td>
<td>0.2</td>
</tr>
<tr>
<td>L</td>
<td>5</td>
<td>2.5</td>
<td>1.25</td>
<td>1</td>
<td>0.625</td>
<td>0.25</td>
</tr>
<tr>
<td>N</td>
<td>8</td>
<td>4</td>
<td>2</td>
<td>1.6</td>
<td>1</td>
<td>0.4</td>
</tr>
<tr>
<td>Q</td>
<td>20</td>
<td>10</td>
<td>5</td>
<td>4</td>
<td>2.5</td>
<td>1</td>
</tr>
</tbody>
</table>

With the table above, it was needed to verify the group of combinations that allows the oscillator to work properly. The results of the verification are presented in the next figure.

Figure 4.8: Oscillation according with alpha relation. NO - Non oscillate, O - Oscillate.
Alpha Simulation Results

Based on the information presented in the previews section, the same simulations were run considering the alpha ratio between the internal and external inverters. The results are displayed in the next table and figure 4.9.

Table 4.4: Results table

<table>
<thead>
<tr>
<th>Phase Number</th>
<th>Power [mW]</th>
<th>Freq. [MHz]</th>
<th>PN (Δf) [dBc/Hz]</th>
<th>Δf [MHz]</th>
<th>FOM [dBc/Hz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>α = 0.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>6.9</td>
<td>1 442</td>
<td>-117.0</td>
<td>10.0</td>
<td>-151.8</td>
</tr>
<tr>
<td>16</td>
<td>6.9</td>
<td>725</td>
<td>-124.5</td>
<td>10.0</td>
<td>-153.3</td>
</tr>
<tr>
<td>32</td>
<td>6.9</td>
<td>363</td>
<td>-131.5</td>
<td>10.0</td>
<td>-154.3</td>
</tr>
<tr>
<td>64</td>
<td>6.9</td>
<td>182</td>
<td>-138.1</td>
<td>10.0</td>
<td>-154.9</td>
</tr>
<tr>
<td>α = 0.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>3.2</td>
<td>1 972</td>
<td>-114.9</td>
<td>10.0</td>
<td>-155.7</td>
</tr>
<tr>
<td>16</td>
<td>3.2</td>
<td>997</td>
<td>-122.4</td>
<td>10.0</td>
<td>-157.3</td>
</tr>
<tr>
<td>32</td>
<td>3.2</td>
<td>501</td>
<td>-129.4</td>
<td>10.0</td>
<td>-158.3</td>
</tr>
<tr>
<td>64</td>
<td>3.2</td>
<td>251</td>
<td>-136.0</td>
<td>10.0</td>
<td>-158.9</td>
</tr>
<tr>
<td>α = 1 (Inv N)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>5.4</td>
<td>3 500</td>
<td>-116.7</td>
<td>10.0</td>
<td>-160.2</td>
</tr>
<tr>
<td>16</td>
<td>5.4</td>
<td>1 763</td>
<td>-124.2</td>
<td>10.0</td>
<td>-161.8</td>
</tr>
<tr>
<td>32</td>
<td>5.4</td>
<td>885</td>
<td>-131.1</td>
<td>10.0</td>
<td>-162.8</td>
</tr>
<tr>
<td>64</td>
<td>5.4</td>
<td>444</td>
<td>-137.8</td>
<td>10.0</td>
<td>-163.4</td>
</tr>
<tr>
<td>α = 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>4.8</td>
<td>5 038</td>
<td>-114.3</td>
<td>10.0</td>
<td>-161.6</td>
</tr>
<tr>
<td>16</td>
<td>4.8</td>
<td>2 539</td>
<td>-121.9</td>
<td>10.0</td>
<td>-163.2</td>
</tr>
<tr>
<td>32</td>
<td>4.8</td>
<td>1 276</td>
<td>-128.9</td>
<td>10.0</td>
<td>-164.2</td>
</tr>
<tr>
<td>64</td>
<td>4.8</td>
<td>640</td>
<td>-135.5</td>
<td>10.0</td>
<td>-164.8</td>
</tr>
<tr>
<td>α = 2.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>11.6</td>
<td>5 603</td>
<td>-117.6</td>
<td>10.0</td>
<td>-162.0</td>
</tr>
<tr>
<td>16</td>
<td>11.6</td>
<td>2 802</td>
<td>-125.3</td>
<td>10.0</td>
<td>-163.6</td>
</tr>
<tr>
<td>32</td>
<td>11.6</td>
<td>1 404</td>
<td>-132.3</td>
<td>10.0</td>
<td>-164.6</td>
</tr>
<tr>
<td>64</td>
<td>11.6</td>
<td>703</td>
<td>-139.0</td>
<td>10.0</td>
<td>-165.3</td>
</tr>
<tr>
<td>SERO Inv N</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>5.3</td>
<td>3 948</td>
<td>-121.6</td>
<td>10.0</td>
<td>-166.3</td>
</tr>
<tr>
<td>17</td>
<td>5.3</td>
<td>2 047</td>
<td>-128.0</td>
<td>10.0</td>
<td>-167.0</td>
</tr>
<tr>
<td>33</td>
<td>5.3</td>
<td>1 057</td>
<td>-134.5</td>
<td>10.0</td>
<td>-167.8</td>
</tr>
<tr>
<td>65</td>
<td>5.3</td>
<td>538</td>
<td>-140.8</td>
<td>10.0</td>
<td>-168.1</td>
</tr>
</tbody>
</table>
Figure 4.9: FOM results for a $\Delta f = 10$ MHz, with different $\alpha$.

Considering the results obtained for the MPRO in the first simulations, the FOM value has a continuous improvement when $\alpha$ parameter increases. However, when comparing this values with the conventional oscillator (SERO) the FOM values are still worse for MPRO. The power values follows the same pattern by keeping the same value for different number of phases.
4.3 Coupling circuits

An complementary approach to improve phase noise is to use coupling circuits with injection lock. However, to do a comparison between the stand alone circuit and the coupling circuits, it is needed to have new values with the supply voltage of 0.6 V in order to have the same conditions for both circuits. The table 4.5 presents the new values for the stand alone circuit.

Table 4.5: Results Stand alone circuit

<table>
<thead>
<tr>
<th>#-Phase</th>
<th>Power [mW]</th>
<th>Frequency [MHz]</th>
<th>PN [dBc/Hz]</th>
<th>FoM @10MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>@100kHz</td>
<td>@1MHz</td>
</tr>
<tr>
<td>$V_{DD}$=1.2 V</td>
<td>32</td>
<td>13.5</td>
<td>887</td>
<td>-80.8</td>
</tr>
<tr>
<td>$V_{DD}$=1.2 V</td>
<td>64</td>
<td>13.5</td>
<td>444</td>
<td>-89.7</td>
</tr>
<tr>
<td>$V_{DD}$=0.6 V</td>
<td>32</td>
<td>0.8</td>
<td>276</td>
<td>-88.5</td>
</tr>
<tr>
<td>$V_{DD}$=0.6 V</td>
<td>64</td>
<td>0.8</td>
<td>138</td>
<td>-96.8</td>
</tr>
</tbody>
</table>

The first coupling circuit to be simulated was the Side-by-side circuit, presented in figure 3.5. The first simulation considers two different oscillators, 32 and 64 phases. The second and third simulations consider two oscillators with the same number of phases, 32 and 64 phases respectively. The results are presented in the table 4.6. Comparing with the stand alone circuit, it is possible to conclude that the coupling factor is very weak and the oscillators are not locked.

Table 4.6: Results Side-by-side circuit (1 Ω) with 32 and 64 phases

<table>
<thead>
<tr>
<th>#-Phase</th>
<th>Power [mW]</th>
<th>Frequency [MHz]</th>
<th>PN [dBc/Hz]</th>
<th>FoM @10MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>@100kHz</td>
<td>@1MHz</td>
</tr>
<tr>
<td>$V_{DD}$=0.6 V</td>
<td>32</td>
<td>1.6</td>
<td>276</td>
<td>-97.0</td>
</tr>
<tr>
<td>$V_{DD}$=0.6 V</td>
<td>64</td>
<td>1.5</td>
<td>259</td>
<td>-84.8</td>
</tr>
<tr>
<td>$V_{DD}$=0.6 V</td>
<td>32 (x2)</td>
<td>1.5</td>
<td>138</td>
<td>-97.0</td>
</tr>
<tr>
<td>$V_{DD}$=0.6 V</td>
<td>64 (x2)</td>
<td>1.6</td>
<td>138</td>
<td>-97.0</td>
</tr>
</tbody>
</table>

The results presented in the table 4.7 corresponds to the coupling circuit of figure 3.6, the Stack circuit. The first simulation considers two different oscillators, 32 and 64 phases. The second and third simulations consider two oscillators with the same number of phases, 32 and 64 phases respectively. According to the table 4.7 and comparing the values with the table 4.5, there is an improvement on PN values. PN improves 2 dB between the 64-phase and 1.5 dB between 32-phase. However, the FOM is worse 0.7 dB between 64-phase and 1.5 dB between 32-phase. The power consumption is doubled for the stack circuit once the circuit has two oscillators working at the same time. This circuit is also reusing the current between the oscillators and allows them to work in different frequencies. This fact it is not taking into consideration at the time of FOM calculation.
Table 4.7: Results Stack circuit with 32 and 64 phases

<table>
<thead>
<tr>
<th>#-Phase</th>
<th>Power [mW]</th>
<th>Frequency [MHz]</th>
<th>PN [dBc/Hz] @100kHz</th>
<th>PN [dBc/Hz] @1MHz</th>
<th>PN [dBc/Hz] @10MHz</th>
<th>FoM @10MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DD}=1.2 V</td>
<td>32</td>
<td>1.6</td>
<td>276</td>
<td>-92.6</td>
<td>-116.5</td>
<td>-137.2</td>
</tr>
<tr>
<td>V_{DD}=1.2 V</td>
<td>64</td>
<td>1.6</td>
<td>138</td>
<td>-98.5</td>
<td>-123.1</td>
<td>-143.9</td>
</tr>
<tr>
<td>V_{DD}=1.2 V</td>
<td>32 (x2)</td>
<td>1.6</td>
<td>276</td>
<td>-91.5</td>
<td>-117.1</td>
<td>-136.6</td>
</tr>
<tr>
<td>V_{DD}=1.2 V</td>
<td>64 (x2)</td>
<td>1.6</td>
<td>138</td>
<td>-99.2</td>
<td>-123.4</td>
<td>-144.1</td>
</tr>
</tbody>
</table>

The results presented in the table 4.8 corresponds to the coupling circuit of the Stack circuit with MPRO oscillators of 32 and 128 phases. The two initial rows presents the values of the simulations for the Stand alone circuit with 128 phases, in order to compare the values on the next rows. The first simulation for the coupling circuit considers two different oscillators, 32 and 128 phases. The second and third simulations considers two oscillators with the same number of phases, 32 and 128 phases respectively.

Table 4.8: Results Stack circuit with 32 and 128 phases

<table>
<thead>
<tr>
<th>#-Phase</th>
<th>Power [mW]</th>
<th>Frequency [MHz]</th>
<th>PN [dBc/Hz] @100kHz</th>
<th>PN [dBc/Hz] @1MHz</th>
<th>PN [dBc/Hz] @10MHz</th>
<th>FoM @10MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DD}=1.2 V</td>
<td>128</td>
<td>13.5</td>
<td>222</td>
<td>-98.5</td>
<td>-125.7</td>
<td>-148.1</td>
</tr>
<tr>
<td>V_{DD}=0.6 V</td>
<td>128</td>
<td>0.8</td>
<td>69</td>
<td>-104.7</td>
<td>-127.5</td>
<td>-147.8</td>
</tr>
<tr>
<td>V_{DD}=1.2 V</td>
<td>32</td>
<td>1.6</td>
<td>276</td>
<td>-92.9</td>
<td>-117.7</td>
<td>-138.7</td>
</tr>
<tr>
<td>V_{DD}=1.2 V</td>
<td>128</td>
<td>1.6</td>
<td>69</td>
<td>-105.5</td>
<td>-129.5</td>
<td>-148.2</td>
</tr>
<tr>
<td>V_{DD}=1.2 V</td>
<td>32 (x2)</td>
<td>1.6</td>
<td>276</td>
<td>-91.5</td>
<td>-117.1</td>
<td>-136.6</td>
</tr>
<tr>
<td>V_{DD}=1.2 V</td>
<td>128 (x2)</td>
<td>1.6</td>
<td>69</td>
<td>-105.4</td>
<td>-127.8</td>
<td>-148.1</td>
</tr>
</tbody>
</table>

With the coupling of 32-phases and 128-phases using the stack circuit, there is an improvement in the PN values of 3 dB for the 32-phase oscillator when compared with the same oscillator in the stand alone circuit.

Comparing the values with the table 4.7, the 32-phase MPRO has an improvement of 1.5 dB. This indicates the oscillator with 128-phases is stronger and it has a higher influence on the 32-phase oscillator then the 64-phase oscillator had. Extrapolating this behaviour, when the slower oscillator is doubled, the faster oscillator improves the PN value by 1.5 dB due to the lower oscillator.
The results presented in the table 4.9 corresponds to the coupling circuit of the Stack circuit with SERO oscillators of 5 and 15 phases. The four initial rows presents the values of the simulations for the Stand alone circuit with 5 and 15 phases, in order to compare the values on the next rows. The first simulation for the coupling circuit considers two different oscillators, 5 and 15 phases. The second and third simulations considers two oscillators with the same number of phases, 5 and 15 phases respectively.

Table 4.9: Results Stack circuit with 5 and 15 phases

<table>
<thead>
<tr>
<th>#-Phase</th>
<th>Power [mW]</th>
<th>Frequency [MHz]</th>
<th>PN [dBc/Hz]</th>
<th>FoM @10MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>@100kHz</td>
<td>@1MHz</td>
</tr>
<tr>
<td>$V_{DD}$=1.2 V</td>
<td>5</td>
<td>5.2</td>
<td>7027</td>
<td>-56.5</td>
</tr>
<tr>
<td>$V_{DD}$=1.2 V</td>
<td>15</td>
<td>5.3</td>
<td>2326</td>
<td>-71.0</td>
</tr>
<tr>
<td>$V_{DD}$=0.6 V</td>
<td>5</td>
<td>0.3</td>
<td>1791</td>
<td>-65.9</td>
</tr>
<tr>
<td>$V_{DD}$=0.6 V</td>
<td>15</td>
<td>0.3</td>
<td>596</td>
<td>-79.8</td>
</tr>
<tr>
<td>$V_{DD}$=1.2 V</td>
<td>5 (x2)</td>
<td>0.6</td>
<td>1792</td>
<td>-70.7</td>
</tr>
<tr>
<td>$V_{DD}$=1.2 V</td>
<td>15 (x2)</td>
<td>0.6</td>
<td>597</td>
<td>-80.2</td>
</tr>
</tbody>
</table>

Coupling 5 and 15 phases SERO oscillators, the faster oscillators frequency is three times the frequency of the slower oscillator, $f_5 = 3 \times f_{15}$. Observing the values of the table 4.9, it has a similar behaviour of the values presented in table 4.7. There are an improvement for the coupling circuit, as happens with the MPRO oscillator.

Comparing the PN values between stand alone and stack circuit, the difference is -3 dB for both 5-phases and 15-phases.

Although the values for the FOM are not improving, and in some cases are worse then expected, the PN values are improving. Furthermore, the formula does not have in consideration the achievement of having two separate oscillators working simultaneously with two different frequencies reusing the same current for both oscillators.
5

Conclusions

Contents

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5.2 Future Work ................................................. 51
5.1 Conclusions

This thesis intended to build a ring oscillator with an even number of phases and to analyze the PN behaviour for the SERO and MPRO oscillators. One of the objectives was also to not use more power and supply voltage and to build it to be embed in integrated circuits (IC).

To initiate the work, a research was made to present the basic concepts to understand the work done. The first chapters included a study of concepts such as ring, RC and LC oscillators study, and a phase noise initial approach.

The design of oscillator proposed was made with ring oscillators to minimize the die area and power consumption, as the type of oscillator has no inductors in the construction circuit. However, the PN performance of ring oscillators is poor. In order to obtain the improvement in PN, a new higher level circuit was proposed using injection lock phenomenon.

The simulations were run, under the same conditions, for the circuits described in chapter 3. The initial results were not the expected and two solutions were proposed to achieve better results. This work focused more on the second approach, injection lock. However, results for the first approach, alpha relation, was presented.

As presented in chapter 4, there is an improvement on PN with the number of phases and the size of the transistors. This behaviour is not dependent on the oscillator topology (SERO or MPRO). Although the simple circuit has better PN for the SERO topology, there are methods to improve the PN values. Alpha relation variation and coupling circuits (with injection lock). The Alpha variation is not so effective as expected. On other hand, coupling circuits revealed better results.

Besides the FOM value does not had an improvement as expected, the PN value was better and the circuit allowed to have two oscillators with different frequencies, working at the same time, reusing the current through both oscillators. This last conclusion present the main advantage of the coupling circuit.

Because of the deadline time, the alpha variation approach to improve the PN performance was not deeply studied as the coupling approach. Nonetheless, this approach should be studied.

5.2 Future Work

In order to test the functioning of the proposed circuits in reality, it is recommended to build a layout to evaluate the real area occupied by the circuit and build an IC for tests.

As said in the previews section, the alpha variation scenario should be explored. This solution could lead to a better PN performance with lower die area.

In case of coupling circuits, it is suggested to increase the distance in frequency between the two oscillators of the circuit. Another possibility of work is to increase the number of oscillators on the stack.
circuit. Finally, it is also recommended to find a way to have a stronger coupling on the oscillators of the Side-by-side circuit.
Bibliography


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Appendix A - Paper
Injection Locked Oscillators with Current Reuse

Mafalda Benido, Taimur Rabuske, Jorge Fernandes
INESC-ID Lisboa, Instituto Superior Técnico, Universidade de Lisboa, Portugal
{mafalda.benido, taimur.rabuske, jorge.fernandes}@inesc-id.pt

Abstract—Injection locking of oscillators is a known technique to improve the oscillator’s phase noise performance. Generally, this is done by running two or more oscillators that are linked through a passive or active coupling mechanism. Therefore, the power consumption (at least) doubles, leading to no improvement regarding the standard figure-of-merit (FoM). This work discloses a new coupling mechanism for locked oscillators, that reuses the supply current and builds upon the fact that inverters implemented in modern CMOS processes are able to reach reasonable oscillating frequencies even without using the full nominal supply voltage range. Instead of instantiating the oscillators “side-by-side”, the proposed scheme stacks oscillators between the supply terminal, thus reusing the drawn current at the same time as dividing the available supply voltage among the oscillators. Aiming for proper voltage division, we exploit a property of the ring oscillators, in which they are able to keep the same power consumption while the number of phases is increased/decreased. In the presented approach, the phase-noise performance improves without a penalty in power consumption, thus also improving the FoM. Simulation results show that by coupling two oscillators at $f_0$ and $2f_0$, the higher frequency oscillator locks and inherits the better phase noise performance of the lower frequency oscillator, while reusing the same current, demonstrating the effectiveness of the proposed topology.

Keywords—Oscillators, injection lock, coupling, current reuse

I. INTRODUCTION

Electrical oscillators are basic building blocks used in RF, analog, mixed-mode and digital circuits. Electrical oscillators can be generally categorized into linear and non-linear, being the linear based in a resonant mechanism and the non-linear based in a hysteresis mechanism. Coupling oscillators is used to ensure synchronization, improve phase-noise performance, or to allow the generation of quadrature signals or other multi-phase synchronous outputs [1,2]. Many types of coupling have been reported using direct injection locking [3-5] or specific feedback circuits as a phase-locked loop (PLL) structure [2,6,7]. Coupling to achieve quadrature outputs using active or passive coupling, have also been reported [8]. All these mechanisms have been reported with the underlying assumption that the oscillators are supplied by a $V_{DD}$ voltage and that the source is also $V_{DD}$.

The basic ring oscillator has an odd number of inverters (Fig. 1 (a)), however many applications require quadrature signals or 4 or 8 phase signals. An even number of differential inverters can be used but then no longer simple CMOS inverters are used. Another approach is to add feedforward inverters [9-11], as represented in Fig. 1 (b).

The ring oscillators represented in Fig. 1 can be implemented with CMOS inverters and can both be studied as an RC oscillator being the $R$ due to the transistors on-resistance and $C$ as the node capacitance.

![Fig. 1 (a) Basic odd-phase ring oscillator and (b) even-phase oscillator using feedforward inverters (gray inverters are weaker than the others).]

For the oscillators in Fig. 1 a CMOS inverter is the basic cell, it has negligible static power (only due to leakage) and a dynamic power consumption (1):

$$P \propto C_i V_{DD}^2$$

where $C_i$ is the output node capacitance and $V_{DD}$ is simultaneously the power supply and output swing voltage (rail-to-rail), being the power proportional to the number of transitions per second.

In the past decades, the CMOS process trend has been to increase transistor speed at the same time as shrinking its size, consequently reducing the parasitic capacitances. To cope with the high-power density inherent to high levels of integration of active devices in a chip, the nominal operating voltage is reduced, together with the threshold voltage of the transistors. Under such circumstances, ring oscillators built with digital inverters can reach reasonable oscillating frequencies on the range of hundreds of megahertz even when using only half of the nominal supply voltage.

Thus, if only half of the nominal voltage is enough to provide a fundamental tone at a reasonable frequency, it is open the possibility of stacking multiple oscillators, and possibly reuse the current required to drive one of the oscillators to drive the next one on the cascade, instead of immediately feeding the current into the negative supply terminal [12].

Additionally, as the chip core operates with a low voltage in modern nodes (generally lower than 1 V for ultra-deep submicron processes), some sort of voltage step-down conversion is usually needed within the system, and this takes place very commonly on-chip. In such scenario, we could devise multiple stacked oscillators operating with the nominal supply voltage, at the price of having to cope with voltage limits of the technology, latch-up and other issues.

Stacking different circuit blocks to reuse supply current comes with some challenges. Take the circuit from Fig. 2, that...
depicts two generic circuit blocks that are connected in series with a voltage supply \( V_{DD} \). The circuits \( X_1 \) and \( X_2 \) can be modeled by load resistances \( R_{load1} \) and \( R_{load2} \). The circuit \( X_1 \) is supplied with \( V_{DD} - V_x \), while \( X_2 \) is supplied with \( V_x \). With balanced loading, \( V_x \) is \( V_{DD}/2 \). If \( X_1 \) and \( X_2 \) are time-invariant from the \( V_{DD} \) perspective, \( V_x \) is constant. If, on the other hand, the loadings of \( X_1 \) and \( X_2 \) vary in time, as in oscillators, which tend to drain more power during transitions, \( V_x \) also varies and consequently also the fraction of \( V_{DD} \) allocated to each circuit. These interactions cause coupling between the circuits, and in the case of ring oscillators, they can cause injection lock.

In this paper, we propose a method to lock oscillators at integer multiple frequencies to improve phase noise performance without extra circuit elements and without a penalty in power consumption, taking advantage of the above-mentioned considerations. As it will be shown in Section II, the power consumption of ring oscillators using the same underlying inverters (even when working at different frequencies) have the same current consumption, allowing for current reuse. In Section III a comparative study using a commercially available 130nm CMOS technology shows the feasibility and the advantages of the proposed technique. Finally, in Section IV, we draw conclusions and perspective future developments.

II. UNDERLYING CIRCUIT ASSUMPTIONS

A. Ring Oscillator Power Consumption

The ring oscillators of Fig. 1 are implemented with standard cells inverters in a 130nm CMOS technology for several combinations of NMOS and PMOS. As an example, we show the power consumption results in Table I for one case of dimensioning (Library UMC Inv_\( Q \) (m=20), that corresponds to 20x \( W_P=600\text{nm}/W_N=530\text{nm} \) and \( L_{N,P}=120\text{nm} \)) having the others a similar behavior.

As can be observed from Table I for each circuit the power is almost equal while the frequency reduces by a factor of two each time the number of phases (loop inverters) doubles. The frequency effect is easily understood while the power consumption must be seen as “in each instant only a few inverters are changing” (Fig. 3), being all the others seated at a high or low voltage. While only the inverters changing state are consuming energy it becomes independent of the total number of inverters that only affects the total time for a period. Furthermore, it also happens that the total current drawn is approximately constant during the whole period, as represented in Fig. 4 for the case of 8-phase oscillator. It can also be seen, in Fig. 4, that the current carries spikes relative to the 8-phase (8-inverters ring) oscillator. This means that we can use oscillators at different frequencies implemented with equal inverters and reusing the same current, while the AC component of this current will cause the injection lock of the oscillators.

<table>
<thead>
<tr>
<th>Oscillator</th>
<th>Power ([\text{mW}])</th>
<th>Frequency ([\text{MHz}])</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ring</td>
<td>5</td>
<td>6915</td>
</tr>
<tr>
<td></td>
<td>9</td>
<td>3948</td>
</tr>
<tr>
<td></td>
<td>17</td>
<td>2047</td>
</tr>
<tr>
<td></td>
<td>33</td>
<td>1057</td>
</tr>
<tr>
<td></td>
<td>65</td>
<td>538</td>
</tr>
<tr>
<td>Fig.1(a)</td>
<td>4</td>
<td>7352</td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>3533</td>
</tr>
<tr>
<td></td>
<td>16</td>
<td>1771</td>
</tr>
<tr>
<td></td>
<td>32</td>
<td>887</td>
</tr>
<tr>
<td></td>
<td>64</td>
<td>444</td>
</tr>
</tbody>
</table>

B. Oscillators Injection Locking Mechanisms

In the case of PLL based locking mechanisms one of the objectives is, usually, to inherit the excellent phase noise performance of a mechanical element (crystal) to improve the phase noise performance of an electronic circuit. This is accomplished in within the bandwidth of the PLL.

When coupling similar types of oscillators, simpler mechanisms are used, either active or passive [8] with improvement in the phase noise performance [2, 8]. The commonly used strategy is shown in Fig. 5, where two equal
TABLE II. 32 AND 64 PHASE OSCILLATOR PERFORMANCE UNDER DIFFERENT COUPLING TOPOLOGIES.

<table>
<thead>
<tr>
<th>#-Phase</th>
<th>Power [mW]</th>
<th>Frequency [MHz]</th>
<th>PN [dBc/Hz] @100kHz</th>
<th>PN [dBc/Hz] @1MHz</th>
<th>PN [dBc/Hz] @10MHz</th>
<th>FoM [dB] @10MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single V_{DD}=1.2V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>13.5</td>
<td>887</td>
<td>-80.8</td>
<td>-109.9</td>
<td>-135.1</td>
<td>-162.8</td>
</tr>
<tr>
<td>64</td>
<td>13.5</td>
<td>444</td>
<td>-89.7</td>
<td>-118.0</td>
<td>-141.7</td>
<td>-163.4</td>
</tr>
<tr>
<td>128</td>
<td>13.5</td>
<td>222</td>
<td>-98.5</td>
<td>-125.7</td>
<td>-148.1</td>
<td>-163.7</td>
</tr>
<tr>
<td>Single V_{DD}=0.6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>0.8</td>
<td>276</td>
<td>-88.5</td>
<td>-114.3</td>
<td>-135.7</td>
<td>-165.4</td>
</tr>
<tr>
<td>64</td>
<td>0.8</td>
<td>138</td>
<td>-96.8</td>
<td>-121.1</td>
<td>-141.8</td>
<td>-165.5</td>
</tr>
<tr>
<td>128</td>
<td>0.8</td>
<td>69</td>
<td>-104.7</td>
<td>-127.5</td>
<td>-147.8</td>
<td>-165.4</td>
</tr>
<tr>
<td>Side-by-side V_{DD}=0.6V</td>
<td>32/64</td>
<td>1.6</td>
<td>276/138</td>
<td>-97.0</td>
<td>-121.7</td>
<td>-142.6</td>
</tr>
<tr>
<td>Side-by-side V_{DD}=0.6V</td>
<td>(2x) 64</td>
<td>1.6</td>
<td>138</td>
<td>-97.0</td>
<td>-121.7</td>
<td>-142.6</td>
</tr>
<tr>
<td>Stack V_{DD}=1.2V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>1.6</td>
<td>276</td>
<td>-92.6</td>
<td>-116.5</td>
<td>-137.9</td>
<td>-163.9</td>
</tr>
<tr>
<td>64</td>
<td>1.6</td>
<td>138</td>
<td>-98.5</td>
<td>-123.1</td>
<td>-143.9</td>
<td>-164.9</td>
</tr>
<tr>
<td>Stack V_{DD}=1.2V</td>
<td>(2x) 64</td>
<td>1.6</td>
<td>138</td>
<td>-99.2</td>
<td>-123.4</td>
<td>-144.1</td>
</tr>
<tr>
<td>Stack V_{DD}=1.2V</td>
<td>32</td>
<td>1.6</td>
<td>276</td>
<td>-92.9</td>
<td>-117.7</td>
<td>-137.9</td>
</tr>
<tr>
<td>128</td>
<td>1.6</td>
<td>69</td>
<td>-105.5</td>
<td>-129.5</td>
<td>-148.2</td>
<td>-162.8</td>
</tr>
</tbody>
</table>

oscillators are coupled resulting in a phase noise improvement of 3dB while the power also doubles resulting in a neutral balance in the conventional FoM (2) number.

\[
\text{FoM} = L_{\text{measured}} + 10 \log \left( \left( \frac{P_{DC}}{P_{\text{ref}}} \right)^2 \right) \tag{2}
\]

The locking mechanism is most times explicit, implemented with dedicated components to ensure strong coupling (a differential pair, resistors or capacitors) but it can also be through circuit non-idealities or parasitics (substrate, common mode nodes with non-ideal zero/infinity resistance, etc.).

Therefore we envisage that we can couple two oscillators by stacking them at different voltage planes, improving phase noise while reusing current. This improvement can also be leverage by locking oscillators at different (multiple) frequencies making the faster oscillator inheriting the better phase noise performance of the slower oscillator. The proposed topology is presented in the next section.

III. PROPOSED TOPOLOGY

The proposed and studied topology is shown in Fig. 6. The floating node between oscillators will allow for the in-phase coupling mechanism of two even-phase oscillators. For clarity we show an example where we have a V_{DD} of 1.2V, with similar oscillators, with 32, 64 and 128 phases, each operating 0.6V at different planes, reusing the same current and being locked in phase and frequency.

Due to the long convergence and simulation times required to simulate the oscillators the comparison study is restricted to the case of 32, 64 and 128 phases oscillators and the combinations among them. The results for the circuits represented in Fig. 7 are shown in Table II.

Several interesting results can be observed from Table II:

1) Single oscillators exhibit, as expected, a phase noise performance improvement over 6dB at the same frequency offset due to the increase in the number of inverters in the loop and to the larger relative distance to the center frequency; The much higher power consumption is due to the higher operating voltage, much higher than the transistors’ threshold voltage and the higher operating frequency.

2) side-by-side oscillators show marginal improvement due to very weak coupling (it is being carried out by the voltage supply non-ideal series resistance with a 1Ω value); it would...
be required an explicit coupling mechanism to further improve the phase-noise.

3) Stack oscillators, have better phase noise performance than single or side-by-side oscillators;

4) the higher frequency oscillator on the stack structure inherits the good phase noise performance of the slower one and the difference is marginal when compared with two stacked slower oscillators;

5) Benefiting from current reuse the stacked oscillators can lead to significant improvements in the FoM of the faster clocks.

6) In the context where the oscillators are operating with supply voltage lower than the LDO voltage the difference would further benefit the stack structure.

7) In the context where it is required a divider the proposed approach allows for a “free” divider for ratios of powers of 2

IV. CONCLUSIONS

In this paper it is shown that ring oscillators designed with the same native inverter lead to a defined drive current that does not depend in first order with the number of inverters, only the frequency changes. With the above result in mind it is proposed to couple oscillators in a stack structure to allow current reuse. By doing so either we have two oscillators working at $V_{DD}/2$ or even more advantageous if $V_{DD}$ is obtained from a higher shared supply voltage by an LDO, as it commonly exists in many circuits. In this case it would further improve efficiency and therefore the FoM. Locking at multiple frequencies with a stack topology can be an interesting way to obtain improved phase-noise performance at higher frequencies without a penalty in power consumption, or, when operated by batteries, in the total charge drawn from the battery.

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REFERENCES
