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Sigma-Delta Analog-to-Digital Converter for IoT Applications in 130nm CMOS Technology

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Declaration

I declare that this document is an original work of my own authorship and that it fulfills all the requirements of the Code of Conduct and Good Practices of the Universidade de Lisboa.

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Abstract

An Analog-to-Digital Converter (ADC) is an electronic circuit that performs the conversion of an input signal, continuous in time and amplitude, into a digital signal, discrete in time and amplitude. As most of the information is transmitted and processed in digital domain, the demand for ADCs and DACs has greatly increased over the years. When energy is limited such as in a battery-powered device, these ADCs and DACs must present low power consumptions and small area.

The Sigma Delta (ΣΔ) ADC is a versatile topology that is able to achieve a broad range of resolutions and sampling rates. ΣΔ ADCs employing oversampling and noise shaping techniques have been widely used for different applications due to their ability to trade-off bandwidth and accuracy. This type of ADCs can be broadly categorized into discrete time (DT) and continuous time (CT) implementations. Nevertheless, typical implementations of both classes require active integrators. These integrators generally demand operational amplifiers with high gain and high unity-gain frequency requirements, which are increasingly difficult to be achieved in short channel CMOS technologies due to the limited intrinsic gain of the transistors.

Alternatively, some works were recently proposed with quasi-passive switched capacitor (SC) integrators, resulting in low power and high-speed modulators. These implementations are not affected by short channel lengths, which represents a strong advantage over the active counterparts. The biggest drawback, however, is the fact that passive integrators are lossy, causing distortion on the ADC output. To overcome this problem, in this thesis it is proposed a SC integrator implemented with MOS capacitors (MOSCAP) taking advantage of the variable capacitance to reduce charge leakage during integration. A quasi-passive 1st order ΣΔ modulator is presented, employing a transconductor to transform the input voltage into current. The resulting current is then integrated into the charge-domain in the MOSCAPs. It is demonstrated that with proper biasing of the MOSCAPs, the negative feedback loop that is inherent to the ΣΔ modulator ensures that the integration takes place at the zone of minimum charge loss.

The topology is validated by the implementation of a ΣΔ modulator prototype in a 130 nm process. Simulation results show that the ADC consumes 0.08 mW while sampling at 100 MSps and performs with an SNDR of 51.13 dB for an OSR of 128, which corresponds to an ENOB of 8.23 bits. The resolution is limited by the nonlinear properties of the passive integration, that is leaky because of the MOSCAPs parasitic capacitances. In contrast, due to the absence of high-gain amplifiers, the circuit can fit in a very small area of approximately 40 x 60 μm^2. Future work and possible improvements are suggested in end of this thesis, as well as practical applications of the achieved circuit.

Keywords: Analog-to-Digital Converter, ΣΔ ADC, CMOS 130 nm, quasi-passive 1^{st} order single loop, IoT.

Resumo

Um Conversor Analógico-Digital (ADC) é um circuito elétrico que permite converter um sinal de entrada analógico, continuo no tempo e em amplitude, num sinal digital, discreto no tempo e em amplitude. Dado que a maioria da informação é transmitida e processada no domínio digital, a procura por ADCs e DACs tem vindo a aumentar ao longo dos anos. Em aplicações onde a energia é limitada (circuitos com baterias), os ADCs devem apresentar baixos consumos de potência e áreas reduzidas.

Uma das topologias mais versáteis de ADCs são os Sigma Delta (ΣΔ), apresentado um vasto leque de resoluções e de frequências de amostragem. Os ADCs ΣΔ utilizam técnicas de sobre amostragem e de filtragem de ruido tendo a capacidade de trocar largura de banda por resolução e vice-versa. Este tipo de ADCs pode ser implementado em tempo continuo ou em tempo discreto. Contudo, em qualquer dos casos, a implementação típica requere integradores ativos. Estes integradores geralmente obrigam à implementação de amplificadores operacionais com elevado ganho, o que é cada vez mais difícil de se obter em tecnologias CMOS de canal curto devido ao ganho intrínseco dos transístores ser cada vez menor.

Em alternativa às implementações típicas, trabalhos recentes propuseram implementar integradores quase-passivos com condensadores comutados, resultando em moduladores ΣΔ com baixos consumos de potência e elevadas frequências. Estas implementações não são afetadas por transístores com canal curto, o que constitui uma forte vantagem em relação às implementações ativas. A grande desvantagem deve-se ao facto da integração passiva ser um processo com perdas, o que causa distorção na saída do ADC e degrada o seu desempenho.

Para resolver o problema, nesta tese é proposto um integrador quase-passivo com condensadores MOS (MOSCAPs), explorando-se a capacidade variável destes dispositivos de forma a diminuir a perda de carga durante a integração. Um modulador quase-passivo de 1ª ordem é apresentado sendo utilizado um transconductor para transformar a tensão de entrada numa corrente. A corrente resultante é integrada nos MOSCAPs no domínio da carga, demonstrando-se que através da polarização dos MOSCAPs, é possível assegurar que a integração ocorre com o mínimo de perdas.

Esta nova topologia é validada através da implementação de um modulador ΣΔ em tecnologia CMOS de 130 nm. Os resultados da simulação demonstram que o ADC consome 0.08 mW de potência com um ritmo de amostragem de 100 MSps e que atinge um SNDR de 51.13 dB para um OSR de 128, o que corresponde a um ENOB de 8.23 bits. A resolução é limitada pelas propriedades não lineares da integração passiva, no entanto, devido à ausência de amplificadores, o circuito consegue ser implementado numa área muito reduzida de 40 x 60 μm^2. No capítulo final da tese são apresentadas diversas aplicações do circuito implementado, e é proposto trabalho futuro assim como métodos para melhorar o desempenho desta nova topologia

Palavras Chave: ADC ΣΔ, CMOS 130 nm, quase-passivo 1ª ordem *single loop*, IoT.

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List of Acronyms

ADC	Analog-to-Digital Converter
AFF	Anti-aliasing Filter
BP	Band Pass
CMFB	Common Mode Feedback
CMOS	Complementary Metal-Oxide Semiconductor
CT	Continuous time
DAC	Digital-to-Analog Converter
DEM	Dynamic Element Matching
DOR	Digital Output Rate
DNL	Differential Non-Linearity
DR	Dynamic Range
DT	Discrete time
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FoM	Figure of Merit
FSO	Full-Scale Output
I/H	Integrator and Hold
IIR	Infinite Impulse Response
INL	Integral Non-Linearity
IoT	Internet of Things
LP	Low Pass
LSB	Least Significant Bit
MOSCAP	MOSFET Capacitor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MSB	Most Significant Bit
MSps	Mega Samples Per Second
MASH	Multi-Stage Noise Shaping
NMOS	N-type MOS
NTF	Noise Transfer Function
OPAMP	Operational Amplifier
OSR	Oversampling Rate
OTA	Operational Transconductor Amplifier
PMOS	P-type MOS
PSD	Power Spectral Density

PSS	Periodically Steady-State
SC	Switched Capacitor
S/H	Sample and Hold
SNR	Signal to Noise Ratio
SNDR	Signal to Noise-plus-Distortion Ratio
Sps	Samples Per Second
STF	Signal Transfer Function
T/H	Track and Hold
THD	Total Harmonic Distortion

1. Introduction

1.1. Motivation

Telecommunications had a very fast development in the past few years, especially in the wireless field, and although most of the information that we perceive in the world is analog, transmission, storage, and processing are increasingly done in the digital domain. Consequently, the demand for Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) has increased due to the need for bridging these two domains [1], [2], [3]. If energy is limited, such as in battery-powered devices, these ADCs and DACs must present low-power consumptions and in many cases, a small area. A Digital-to-Analog converter, as the name suggests, allows the transformation of an analog signal (continuous in time and amplitude) into a digital signal (discrete), converting an analog value into a series of bits commonly called as a digital word. Fig. 1 shows a simplified representation of a generic ADC, where an analog signal is fed on the input, and a digital signal is obtained at the output.

The processing and storage of digital information have a clear advantage in comparison with analog signals given the fact that noise affects mainly the signal amplitude. If the signal has a discrete amplitude (zero or one) and the critical information is the instant of time of when each pulse occurs, the information is less affected by the presence of noise. [4]

Fig. 1 – Generic ADC.

Given the vast amount of applications, many circuits have been developed to implement ADCs, being flash, SAR, pipeline and Sigma Delta (ΣΔ) the most known. Each type of implementation results in a different series of specifications, always having a trade-off between resolution and sampling frequency as shown in Fig. 2. Higher resolutions with low sampling rates are commonly obtained by ΣΔ ADCs while low resolutions with high sampling rates are normally obtained by pipeline and flash ADCs.

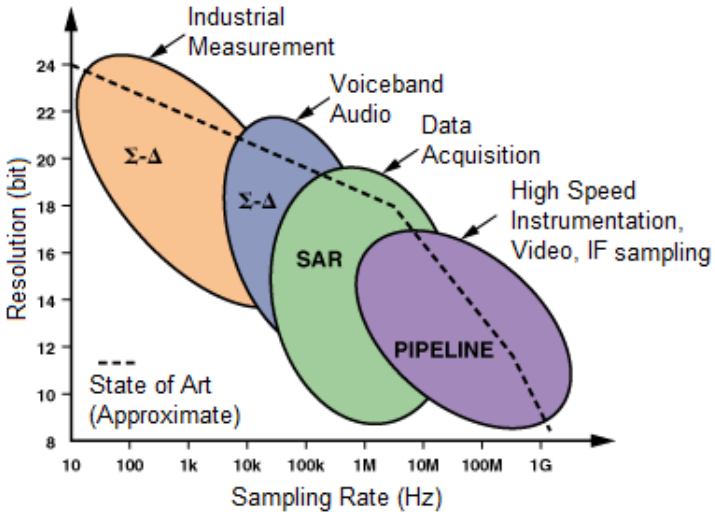


Fig. 2 – ADC architectures and typical specifications. [5]

In this dissertation, a specific type of ADCs is studied and investigated, namely the ΣΔ ADC, which is a versatile topology, being able to achieve a broad range of resolutions and sampling rates. This characteristic allows the use of ΣΔ ADCs in a vast number of applications [4]. As the converter targets IoT (Internet of Things) applications, it is important to achieve a low power, small size circuit choosing a power-efficient architecture and exploring new implementations. For this purpose, this thesis presents a new topology of ΣΔ modulators employing quasi-passive integrators.

1.2. Objectives

The objectives of this thesis are to study, implement and validate passive implementations of ΣΔ ADCs. The principle focus of this work is on implementations with low power consumption and a small area footprint, avoiding operational amplifiers and other sorts of power-hungry circuits whenever possible. To accomplish the objectives, general concepts of converters are presented, as well as a study of the different ΣΔ ADC topologies. After considering the different advantages and drawbacks of each implementation, the produced research is used to formulate a new circuit of a quasi-passive ΣΔ ADC.

1.3. Thesis Outline

The present dissertation has six chapters:

- Chapter 1: Presentation and introduction of the theme and proposed objectives.
- Chapter 2: Fundamentals of ADCs, MOS capacitors, and State-of-Art.
- Chapter 3: Presentation, study and circuit design of the chosen topology.
- Chapter 4: Circuit sizing and intermediate stage results
- Chapter 5: ΣΔ Modulator simulations and results.
- Chapter 6: Conclusions and future work.

1.4. Original Contributions

Part of the original content of this thesis was submitted and accepted for publication at ISCAS 2019 (IEEE International Symposium on Circuits and Systems) and also as a lecture presentation. The published paper [6], is a resume of the developed work in this thesis, focusing on the implementation of a ΣΔ modulator employing a low-power quasi-passive integrator. The integration process is implemented with MOS capacitors instead of linear capacitors, which allows to improve passive integrators while reducing the charge leakage. Although the proposed design targets relatively low resolutions due to the nonlinear nature of passive integration, the absence of operational amplifiers enables the topology to fit in a very small area and achieve a low power consumption.

2. Review on ADCs

An ADC performs the conversion of an analog signal into a digital word, having different types of topologies and implementations that allow the ADC to achieve a certain set of specifications. The performance of an ADC is generally characterized by the triad power, resolution and sampling rate, all affected by a large number of parameters that are presented and explained in this section.

Besides the basic concepts of the ADC, a presentation and a study of the ΣΔ ADC topologies is done, in order to understand which suits best the project objectives. In this section, there is also a review of active and quasi-passive ADC implementations, in which the advantages and disadvantages are explained. The chapter ends with an introduction to the MOS capacitors (MOSCAP) working principle in order to contextualize the reader for the third chapter where the proposed topology is presented.

2.1. Basic Concepts

The working principle of an ideal ADC is based on the idea represented in Fig. 3 (a). An analog signal is inserted in the input of the converter, and a digital word is obtained at the output, being LSB the least significant bit, and MSB the most significant bit. The resolution of a converter dictates how many discrete values are possible at the output of the converter, in order to represent an analog value. When the resolution increases, the number of discrete values that the output can have also increases, which leads to a smaller quantization error.

For an N bit resolution, there are 2^N different combinations to quantize the analog signal. For example, in Fig. 3 (b) the output of an ideal 3 bit ADC is presented, where a sinusoidal input is converted into a set of 2^3 discrete values. In reality, the resolution is affected by many factors that are translated into noise or distortion, being limited by the Signal to Noise plus Distortion Ratio (SNDR). With this aspect in mind, another performance specification is defined, the Effective Number of Bit (ENOB). Both formulas will be presented in the list of the ADCs dynamic specifications, later in this chapter.

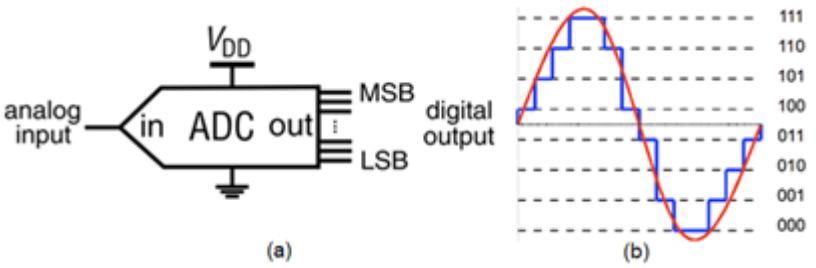


Fig. 3 – Generic and ideal ADC (a) Output of a 3 bit ADC (b).

In addition to SNDR and ENOB, there are other essential metric parameters used to classify ADCs. Therefore, it is important to understand the meaning of each one and to analyze the way they affect the ADC performance for a given application. The most important ADC parameters are the following:

- Resolution – Number of bits used to represent an analog signal into a digital signal. The higher the resolution, the smaller the steps between quantization levels, and the smaller the quantization error. An N-bit resolution corresponds to 2^N discrete levels.

- Dynamic Range – Specifies the range between the noise floor of a device and its specified maximum output level. It defines the range of signal amplitudes which the ADC can resolve.
- Latency – Time needed since the converter captures the analog signal until the digital output is ready for retrieval.
- Input Signal Bandwidth – Maximum input frequency that the ADC can digitize with a loss of 3 dB in SNDR. It is a parameter that depends of the sampling rate and the Nyquist theorem.
- Quantization Error – Result from the conversion of an analog signal to digital, being the difference between the ideal analog value and the discrete value where it is mapped (Fig. 4).

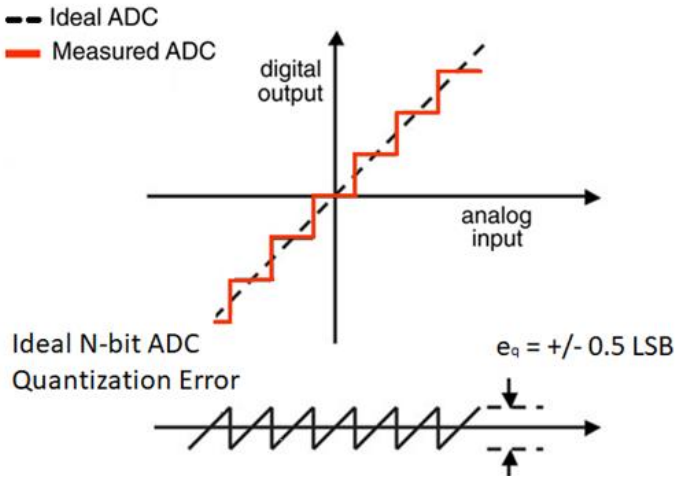


Fig. 4 – Quantization Error.

The parameters presented until this point are general concepts. The following parameters can be divided between static specifications and dynamic specifications, obtained via frequency-domain analysis.

Static Specifications:

- Monotonicity – An ADC is monotonic if the output increases progressively when applying a ramp at the converter input.
- Offset Error – Defined as the constant DC offset of the ADC transfer function in relation to the ideal transfer function (Fig. 5).

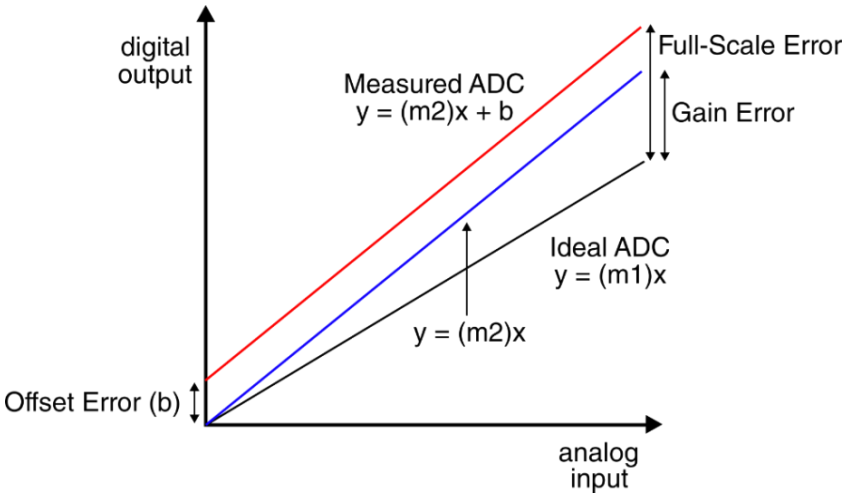


Fig. 5 – Offset Error, Gain Error and Full-Scale Error.

- Gain Error – Defined as the deviation of the transfer function slope compared with the ideal transfer function theoretically specified (Fig. 5).
- Full-Scale Error – Maximum deviation of the ADC transfer function to the ideal transfer function (Fig. 5).
- Integral Non-Linearity Error (INL) – Represents the worst case deviation of the transfer curve obtained by the ADC from the ideal transfer function. It measures at each state how much the transfer function deviates from the ideal one. A good INL results in a good accuracy and low distortion of the analog waveform being converted (Fig. 6)
- Differential Non-Linearity Error (DNL) – Measures the worst case deviation between the actual and the ideal step size on two adjacent codes showing if the steps between the codes are uniform. A good DNL results in a good resolution and noise performance since all the steps have almost the same size (Fig. 6).

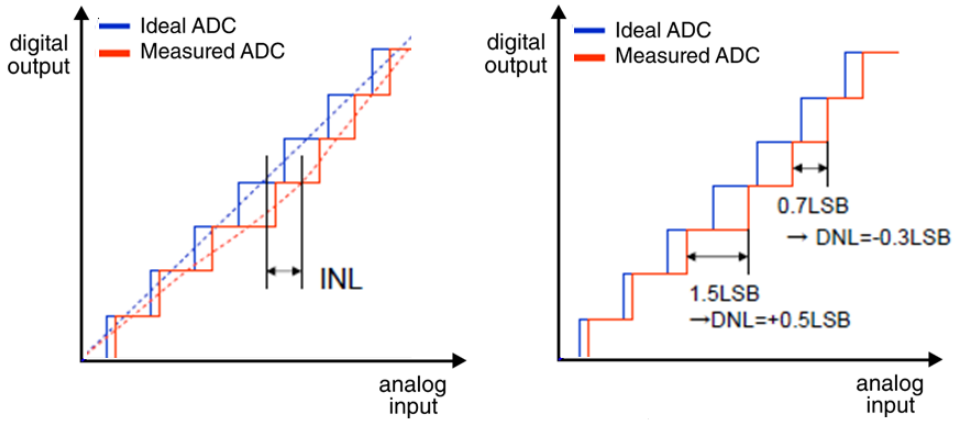


Fig. 6 – INL and DNL.

Dynamic Specifications:

- Signal to Noise Ratio (SNR) – Ratio between the root mean square (RMS) power of the input signal to the RMS noise power, excluding harmonic distortion. SNR can be expressed in dB as shown in (1).

$$\mathrm{SNR_{dB}} = 20\log\left(\frac{V_{\mathrm{signal(rms)}}}{V_{\mathrm{noise(rms)}}}\right) \quad (1)$$

For a given resolution *N*, the theoretical best SNR caused by quantization error can be calculated with (2).

$$\mathrm{SNR_{[MAX]dB}} = 6.02N + 1.76 \quad (2)$$

- Signal to Noise plus Distortion Ratio (SNDR) – Ratio between the RMS power of the input signal (P_s) to the RMS noise power (P_n) including the harmonics power (P_i). SNDR can be expressed by (3) for a given sinusoid input.

$$\mathrm{SNDR_{dB}} = 10\log\left(\frac{P_s}{P_n + \sum_{i=2}^{\infty} P_i}\right) \quad (3)$$

- Effective Number of Bit (ENOB) – Defines the number of bits that a converter would have in an ideal scenario, expressed by (4).

$$\mathrm{ENOB_{bit}} = \frac{\mathrm{SNDR_{dB}} - 1.76}{6.02} \quad (4)$$

2.2. Conceptual Scheme of an ADC:

Without delving into a specific topology, the conceptual scheme of an ADC is based on four fundamental processes described in Fig. 7 with four blocks. These processes allow the conversion of an analog signal into a signal with discrete time and amplitude.

- The first block implements an anti-aliasing filter (AAF), being responsible for filtering high frequency components of the input signal. Otherwise, according to the Nyquist sampling theorem, high frequency components of the input signal would be folded or aliased into the signal bandwidth (B_w) which would corrupt the signal information.
- The second block samples the resulting band-limited signal coming from the AAF at a rate of f_s. This block is based on a sample and hold (S/H) circuit and allows to retain the signal for a given period T_s. With this process, the analog signal is transformed into a discrete time (DT) signal.
- The third block following the S/H is the quantizer, mapping the continuous range of amplitudes into a discrete set of levels. With this process, the signal is now discrete in time and amplitude.
- The fourth and last block is a coder that assigns a unique binary number to each level, providing the digital output data.

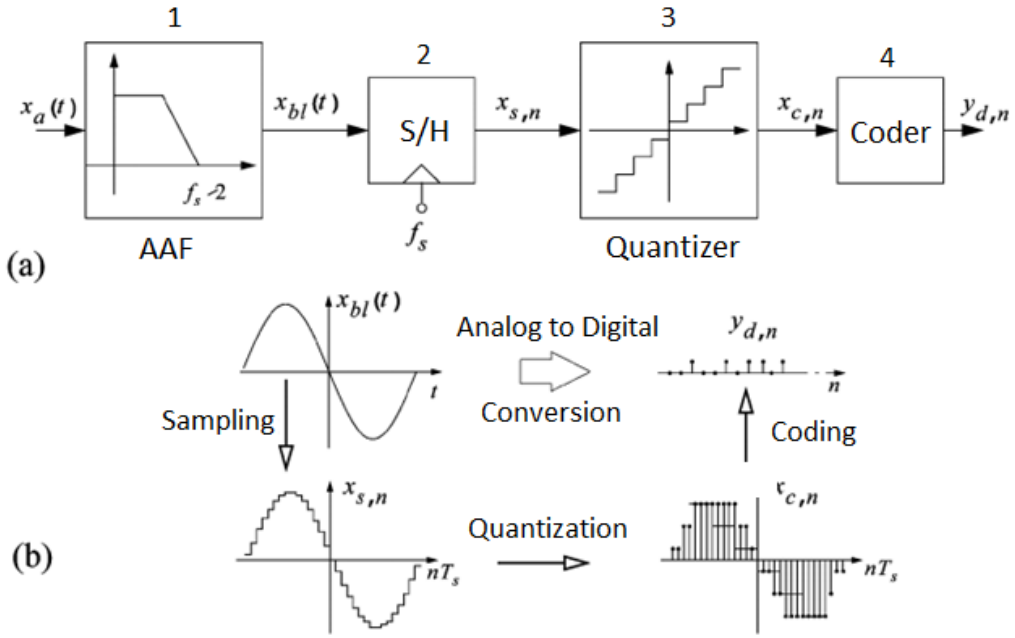


Fig. 7 – ADC conceptual scheme (a) Resulting signals from each process (b). [4]

Given these four processes, it is important to highlight that the main conditioning blocks and those that limit the ADCs performance are the sampling and quantization, which according to the topology, are explored in different ways. ADC topologies can be divided in two groups, Nyquist-rate ADCs, and oversampling ADCs.

2.2.1. Nyquist-rate ADCs

A Nyquist-rate ADC samples the input signal at the minimum frequency, which is twice the signal bandwidth. Many ADC architectures use this type of sampling such as Flash, SAR, and Pipeline. As the main scope of this thesis is the study of oversampling ADCs, this section presents only the main strengths and weaknesses of each type of Nyquist-rate ADC and briefly explains their working principle.

Starting with the Flash ADC, this type of converter has a very fast sampling rate converting the input analog signal into a digital signal using a parallel set of comparators. A *n*-bit Flash ADC consists of a parallel combination of $2^n - 1$ comparators connected to an encoder. It is a topology that privileges speed having a consequent cost on the size and power consumption due to all the comparators that need to be switched concurrently. For a practical example, an ADC with 8 bit requires 255 comparators, for a 9-bit implementation, the number of comparators is 511 and so forth. This fact limits the topology to low resolutions.

For the SAR ADC, the topology is based on the successive approximation technique, implementing a binary search algorithm using only one comparator. This architecture is frequently used in medium-to-high resolution applications, presenting low power consumption. The downsides of this topology are the lower sampling rates and the requirements that the building blocks (DAC and comparator) impose in order to accomplish an accurate ADC.

Another Nyquist ADC architecture is Pipeline, which covers a large range of resolutions starting from 8 bits up to 16 bits, and sampling frequencies from a few megasamples per second (MSps) up to 100 MSps. The working principle of this ADC is based on using different stages in series to determine the bits of the output signal at different points in time. When a stage finishes processing a sample, determining the bit, it can start processing the next sample received from the sample and hold embedded within each stage. This pipelining action allows a high throughput presenting, however, lower sampling rates than Flash and lower resolutions than SAR.

2.2.2. Oversampling ADCs

An oversampling ADC samples the input signal at a frequency higher than twice the signal bandwidth. This architecture normally designated by ΣΔ ADC allows noise shaping, using feedback loop techniques. Fig. 8 shows the basic principle of a ΣΔ modulator. The quantization error from the comparator is injected in the feedback loop and subtracted from the input signal. This process is only possible on oversampling ADCs and allows the filtering of quantization noise with consequent improvements on the resolution.

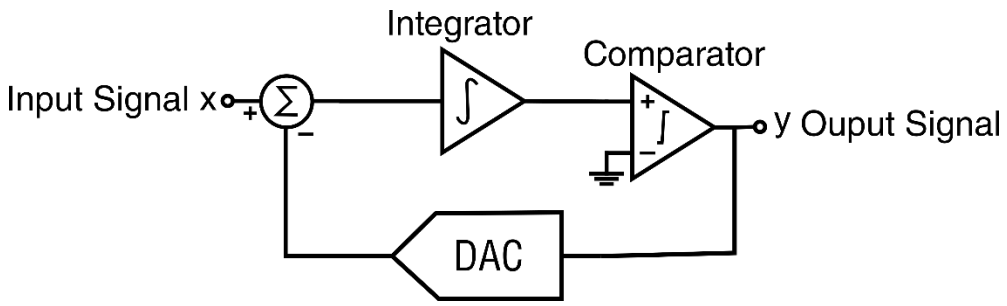


Fig. 8 – Basic ΣΔ modulator.

2.3. Fundamentals of ΣΔ ADCs

The fundamental operations involved in the A/D conversion are sampling and quantization, as shown in the conceptual scheme of an ADC (Fig. 7). On one hand, the sampling process converts the input signal from continuous to discrete in the time domain. On the other hand, the quantization process converts the continuous amplitude of the input signal into discrete values. These two transformations inherently impose limitations on the performance of an ADC, even if implemented with ideal components.

2.3.1. Quantization

The quantization process itself introduces a fundamental limitation on the performance of an ideal ADC, degrading the quality of the analog input signal by mapping it into a finite set of discrete levels. This continuous to discrete transformation amplitude generates an error, commonly referred to as quantization error, e_q. Considering that the input signal *x,* is confined to the full-scale input range [-X_{FS}/2, X_{FS}/2], the quantization error is bound by [-Δ/2, Δ/2], where Δ is the quantization step, defined as the separation between adjacent output levels in the quantizer. As stated before, a *B*-bit quantizer has 2^B quantization levels, and Δ is defined by (5),

$$\Delta \equiv \frac{Y_{\mathrm{FS}}}{2^B - 1} \tag{5}$$

being Y_{FS} the full-scale output range of the quantizer. When *B* grows, the quantization step gets smaller and consequently, the quantization error is reduced.

Under some assumptions which are generally met in practice, it can be shown that the quantization error is distributed uniformly in [-Δ/2, Δ/2], with rectangular probability density, having a constant power spectral density (PSD). For this reason, quantization error can be modeled as an additive white noise source (e) and therefore, the total quantization noise power $\sigma^2(e)$ is uniformly distributed in the range [-f_s/2, f_s/2], being the resulting PSD given by (6).

$$S_E(f) \equiv \frac{\sigma^2(e)}{f_s} = \frac{1}{f_s}\left[\frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2\, de\right] = \frac{\Delta^2}{12 f_s} \tag{6}$$

2.3.2. Oversampling:

According to the Nyquist theorem, the minimum value of the sampling frequency (f_s) must be twice the signal bandwidth being designated by f_N.

$$f_N = 2 \times B_w \tag{7}$$

Based on this theorem, if $f_s = f_N$ the converter is called a Nyquist-rate ADC, while if $f_s > f_N$ the resulting ADC is known as an oversampling ADC, having an oversampling ratio (OSR) given by (8).

$$\mathrm{OSR} \equiv \frac{f_s}{f_N} \tag{8}$$

One of the many advantages of oversampling ADCs is the simplification of the requirements placed on the AAF. In Nyquist-rate ADCs the transition of the filter must be sharp, which often introduces phase distortion in signal components located near the cut-off frequency. This principle is shown in Fig. 9 where two sampling frequencies are used to sample a signal. In Fig. 9 (a) f_s is twice the signal

bandwidth which imposes a sharp AAF. Alternatively, in Fig. 9 (b) it is used an f_s with an OSR, which simplifies the requirements of the AAF and reduces the distortion.

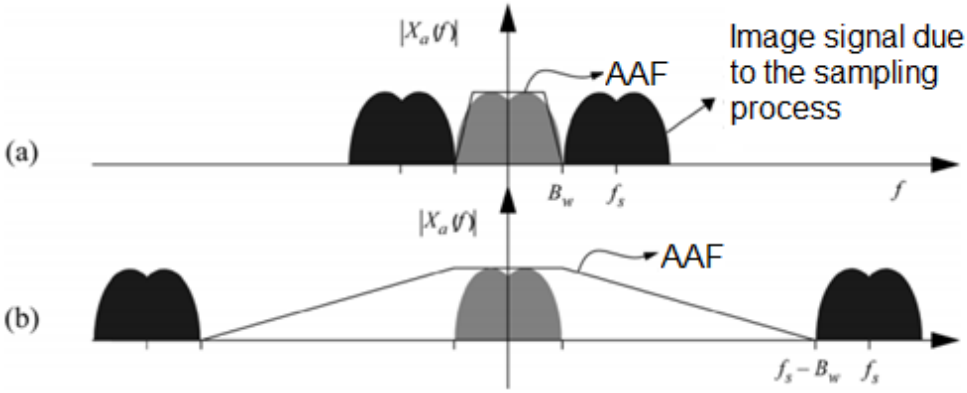


Fig. 9 – Oversampling effect over AAF requirements. $f_s = f_N$ (a), $f_s = OSR \times f_s$. (b). [4]

The other strong advantage of OSR is the reduction of the in-band noise power P_E which is given by expression (9).

$$P_E \equiv \int_{-B_w}^{B_w} S_E(f)\, df = \frac{\Delta^2}{12\mathrm{OSR}} \tag{9}$$

P_E decreases with OSR at a rate of 3 dB/octave because, while the quantization noise power is the same, with oversampling it is distributed in a larger frequency band, thus attenuating the in-band quantization noise power when compared to the one achieved by Nyquist-rate ADCs. This idea is represented in Fig. 10 where different f_s are used to quantize a signal. Three sampling rates are used being $f_{s3} > f_{s2} > f_{s1}$. For higher f_s, the amount of noise in the signal bandwidth decreases, improving the quantization process.

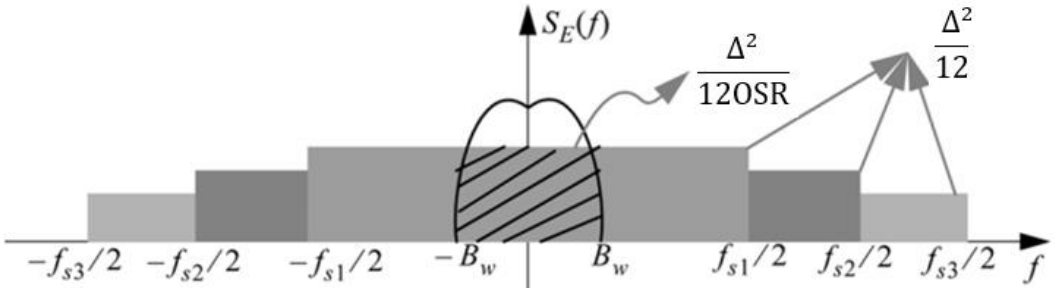


Fig. 10 – In-band noise power for different OSR. [4]

2.3.3. Noise Shaping

The accuracy of an ADC can be further increased by filtering the quantization noise so that most of its power lies outside the signal band. Conceptually this can be done by subtracting the quantization noise to the input signal with feedback. The obtained noise transfer function (NTF) is normally a high-pass filter, filtering the noise around DC. The noise shaping model is presented in Fig. 11.

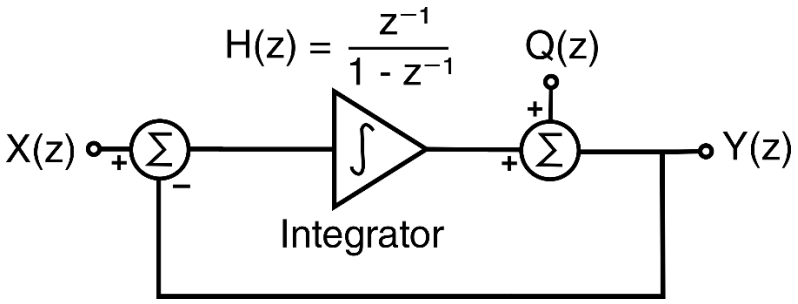


Fig. 11 – Noise shaping model.

In Z-domain, considering *X(z)* as the input signal, and *Q(z)* as the noise introduced by the quantization process, NTF(*z*) = 1 – z^{-1} and the transfer function applied to the signal (STF) is given by z^{-1}. This way, a low pass filter is obtained for the signal, and a high pass filter is obtained for the quantization noise, therefore reducing the in-band noise power P_Q.

$$P_Q \equiv \int_{-B_w}^{B_w} \frac{\Delta^2}{12 f_s} |\mathrm{NTF}(f)|^2 \, df = \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)\mathrm{OSR}^{2L+1}} \tag{10}$$

According to expression (10) when the order of the loop filter (*L*) and OSR increases, P_Q decreases approximately 6*L* dB/octave which is considerably more when compared to the 3 dB/octave of oversampling.

2.3.4. ΣΔ Modulator Introduction

In order to use oversampling and noise-shaping in an ADC, a quantizer is embedded in a feedback loop obtaining a circuit generally known as ΣΔ modulator (ΣΔM). Considering that the *B*-bit quantizer generates an error e_q, the system can be viewed as having two inputs, *x* and e_q, and one output *y*, which can be represented in the Z-domain by (11).

$$Y(z) = \mathrm{STF}(z)X(z) + \mathrm{NTF}(z)Q(z) \tag{11}$$

X(z) and *Q(z)* represent the Z transform of *x* and e_q respectively, and $\mathrm{STF}(z)$ and $\mathrm{NTF}(z)$ are the signal and noise transfer functions given by (12),

$$\mathrm{STF}(z) = \frac{g_q H(z)}{1 + g_q H(z)}; \ \mathrm{NTF}(z) = \frac{1}{1 + g_q H(z)} \tag{12}$$

where g_q represents the gain of the quantizer, and $H(z)$ is a low pass filter.

Inspecting $\mathrm{STF}(z)$ and $\mathrm{NTF}(z)$ it is clear that when $|H(z)| \to \infty$, $|\mathrm{STF}(z)| \to 1$ and $|\mathrm{NTF}(z)| \to 0$ i.e., the input signal is allowed to pass whereas the quantization error is ideally canceled. However, in practice, quantization error cannot be completely nulled because *H*(z) has a limited gain, so an ideal integrator cannot be implemented and consequently an ideal filter is not obtained. For this reason, it is important to measure the SNR and the DR of the modulator output. For a sinewave input with an amplitude A_x, SNR and DR are defined by (13).

$$\mathrm{SNR} \equiv \frac{A_x^2}{2P_Q}; \mathrm{DR} \equiv \frac{(X_{FS}/2)^2}{2P_Q} \tag{13}$$

Replacing P_Q for expression (10), the ideal value of DR is obtained by (14).

$$\mathrm{DR} \approx \frac{3(2^B-1)^2(2L+1)\mathrm{OSR}^{2L+1}}{2\pi^{2L}} \tag{14}$$

To obtain DR in dB, the expression is given by (15).

$$\mathrm{DR}|_{\mathrm{dB}} \approx 20\log_{10}(2^B-1) + 10\log_{10}\left(\frac{2^L+1}{\pi^{2L}}\right) + (2L+1)\times 10\log_{10}(\mathrm{OSR}) + 1.76 \tag{15}$$

For an ideal *N*-bit Nyquist-rate ADC, DR can be obtained by replacing *B* = *N*, *L* = *0* and OSR = 1 in expression (15), obtaining (16).

$$\mathrm{DR}|_{\mathrm{dB}} \approx 6.02N + 1.76 \tag{16}$$

2.4. ADC Topology Choice

As discussed before, there are different topologies to implement an ADC, each having strong and weak points in terms of resolution and speed. Fig. 12 shows a comparison between the types of ADCs developed and the specifications that they achieved. The data was taken from [7].

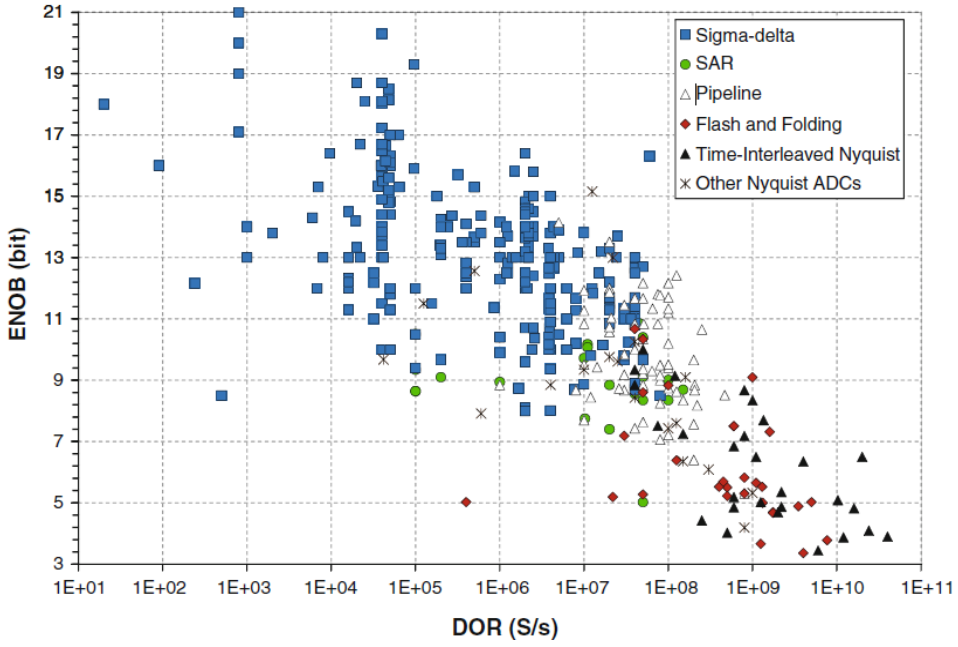


Fig. 12 – State of Art of CMOS ADCs. [8]

Although ΣΔ ADCs were originally built for low frequencies and high-resolution applications such as audio and precision instruments, over the years, with new techniques and different implementations, ΣΔ ADCs have achieved medium to high frequency applications with lower resolutions. Fig. 12 allows the comparison between the ENOB and the digital output rate (DOR) measured in the number of samples per second (Sps) obtained by the different topologies. It can be observed that ΣΔ ADCs cover a large area of specifications due to the broad range of frequencies (10 Hz to 50 MHz) and ENOB, which ranges from 7 to 21 bit for the sampled data, although higher resolutions may be achieved. For high-speed applications, other ADCs are preferential (Flash, SAR, Pipeline) due to signals with high bandwidths requiring extremely fast sampling frequencies. Therefore, oversampling techniques became less efficient, due to power consumption and excessive sampling rates.

Given the advantages of oversampling and noise shaping and having in mind the objectives of developing an ADC with a small area and low power consumption, it becomes evident that the most versatile topology to achieve these specifications is the ΣΔ ADC. The next section (2.5) will focus on the different implementations of ΣΔ modulators in order to choose the best candidate for the thesis objectives.

2.5. ΣΔ Modulator

Apart from the modulator already introduced in section 2.3.4, a ΣΔ ADC is composed by two other blocks represented in Fig. 13. Two different implementations are presented in Fig. 13, (a) shows a discrete time implementation (DT), while (b) shows a continuous time implementation (CT). Both schemes are composed by three main blocks: AAF, ΣΔM, and Decimator, being the ΣΔM the most important block for the ADC performance. For this reason, this section presents a study of the different architectures used to implement a ΣΔ modulator.

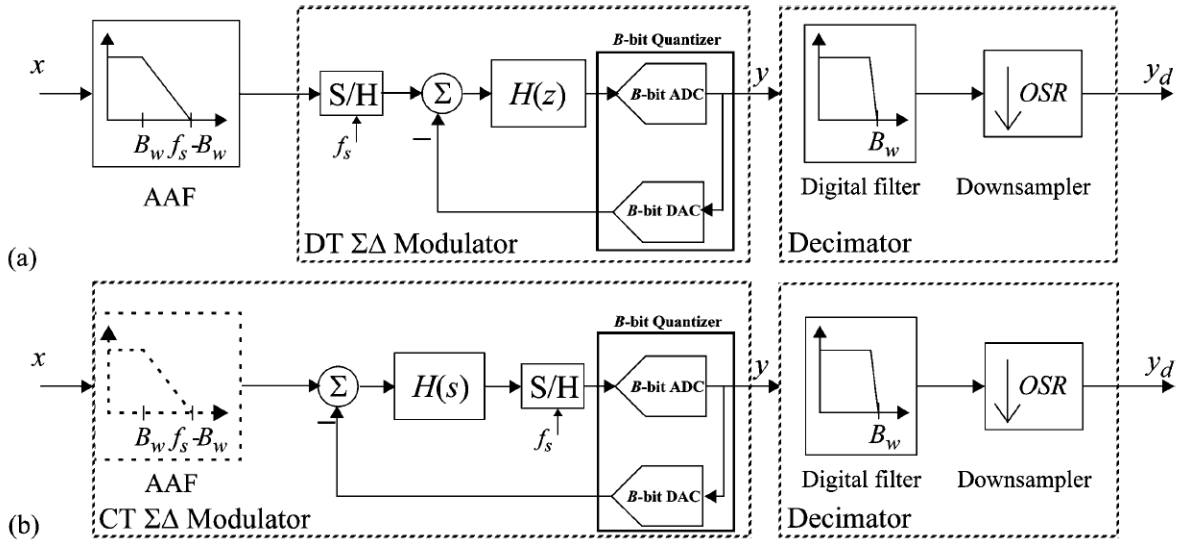


Fig. 13 – ΣΔ ADC DT (a) and ΣΔ ADC CT (b). [4]

2.5.1. Taxonomy of ΣΔ Modulators

Based on the concepts discussed previously and the way they affect the ΣΔ ADC, three different strategies can be used to improve its resolution:

- Increasing *L*: According to (14), for a given OSR, increasing the filter order results in an increased DR, allowing for stronger attenuation of the quantization error at low frequencies. However, the use of high-order modulator loop filtering (usually $L > 2$) can result in stability problems, making the design of the modulator more challenging.

  The increase of DR with *L* and OSR can be expressed by (17).

$$\Delta \mathrm{DR}_{\mathrm{dB}} \approx 10 \log_{10} \left[\frac{2L+3}{2L+1} . \left(\frac{\mathrm{OSR}}{\pi} \right)^{2} \right] \tag{17}$$

- Increasing OSR: DR increases by (L+1/2) bit/octave with OSR level increment. However, for wideband signals, the use of high values of OSR is impractical due to the prohibitive sampling frequencies required, with consequent high-power consumption.

- Increasing *B*: Every increment in the quantizer bit number translates into 6 dB (1 bit) in the ADC DR. However, multi-bit feedback is not inherently linear because of the multi-bit DAC present in the feedback loop.

The strategies can be classified according to the:

- Nature of the signals, resulting in LP and BP ΣΔM.
- Number of bit of the internal quantizers, dividing ΣΔMs into single-bit and multi-bit topologies.
- Number of quantizers employed. Topologies with one quantizer are called single loop, whereas those that use multiple quantizers give rise to different topologies such as cascade and dual-quantization.
- Circuit nature of the loop filter, dividing discrete time modulators from continuous time modulators.

2.5.2. ΣΔ Modulator Architectures

Low Order Single loop:

The simplest way of building a ΣΔM is combining a DT forward-Euler integrator ($H(z) = z^{-1}/(1 - z^{-1})$, with a loop filter with a single bit quantizer. The resulting architecture is known as a first order single-bit ΣΔM, represented in Fig. 14.

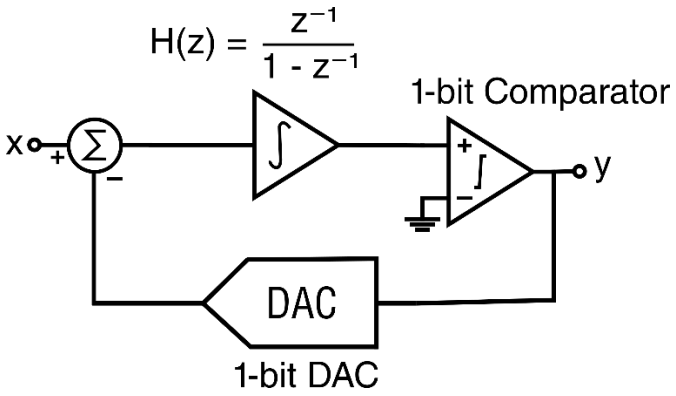


Fig. 14 – First order single-bit ΣΔM. [9]

This topology results in an ADC that is always stable presenting, however, two main disadvantages. The first is the fact that DR only increases with OSR at a rate of 1.5 bit/octave, which implies using very high values of OSR to achieve medium-high effective resolutions. The second is the presence of pattern noise and idle tones, which are a direct consequence of the strong correlation existing between the input signal and the quantization error. This correlation leads to a quantization error different from the white noise model and gives rise to an in-band error power higher than the predicted by the linear model. Both disadvantages can be avoided replacing the 1-bit quantizer (comparator and DAC) by a first order ΣΔM as represented in Fig. 15. This new topology results in a second order ΣΔM where two integrators are used.

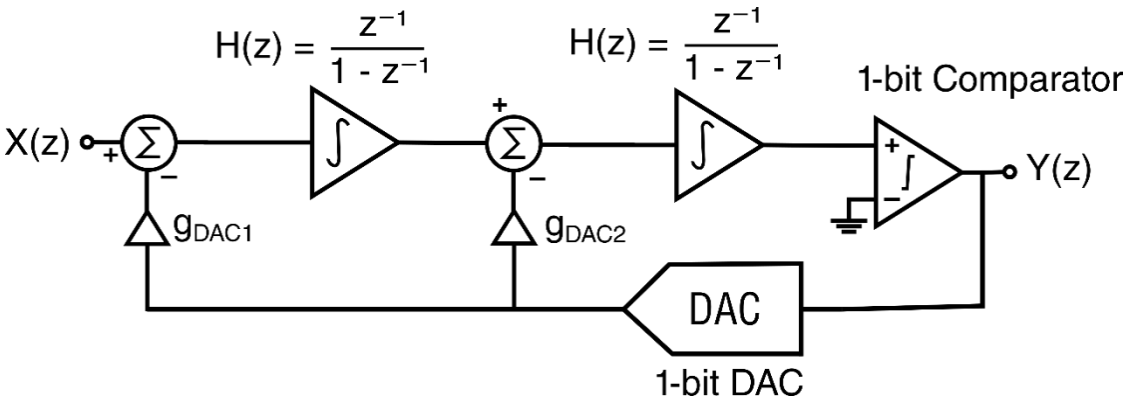


Fig. 15 – Second order ΣΔM.

The second order ΣΔM, is always stable if $g_{DAC2} = 2g_{x(z)}\, g_{DAC1}$ [10] allowing for an increase in DR of 2.5 bit/octave with OSR, which significantly improves the performance of the first order modulator in terms of requires sampling frequency. Besides, the use of two integrators also contributes to decorrelate the input signal and the quantization error, thus decreasing the presence of idle tones in the output spectrum. Fig. 16 shows the relation of OSR with DR and ENOB. By looking at the graphic, it is clear that the increase of the modulator order allows to achieve a much higher ENOB and DR for the same sampling frequency.

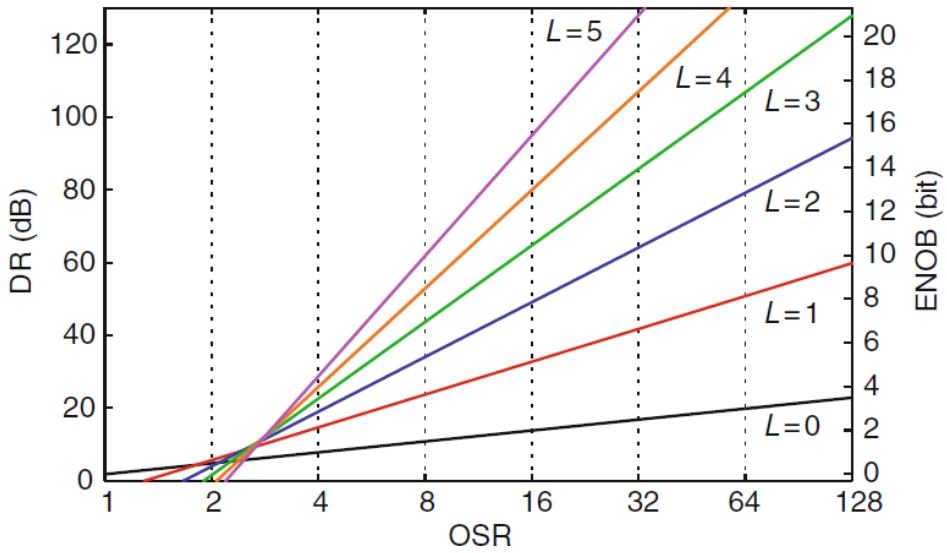


Fig. 16 – Comparison of DR and ENOB with OSR for different *L*. [8]

High Order Modulator:

Based on the concept underlying first and second order single loop ΣΔMs, the same can be extended towards L^{th}-order filtering, resulting in a modulator with $STF(z) = z^{-L}$ and $NTF(z) = (1 - z^{-1})^{-L}$. However, the theoretical performance is not achieved because of stability problems related to the noise transfer function NTF, which stability can only be conditionally guaranteed for a limited range of input amplitudes when $L > 2$. In order to solve this problem, other implementations using infinite impulse response (IIR) filters were proposed by Lee and Sodini [11] synthetizing $NTFs = (z - 1)^L / D(z)$ where $D(z)$ is a polynomial determined by the feedforward analog coefficient. This technique has a clear

disadvantage because of the increased circuit complexity due to the large number of analog coefficients required. An alternative to IIR NTFs that also allows high order modulators consists of using multistage noise-shaping, normally called (MASH). Fig. 17 shows a conceptual block diagram of a MASH architecture.

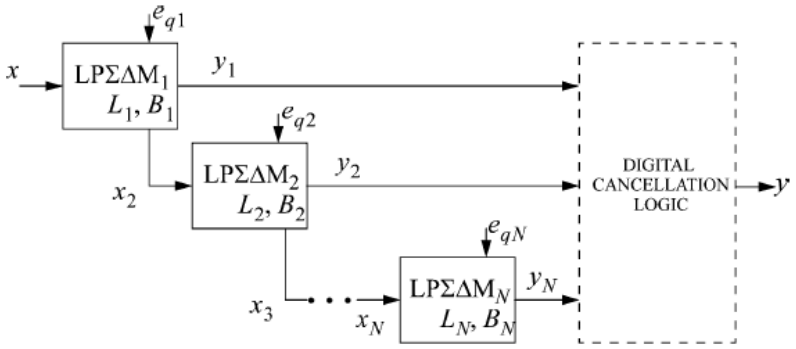


Fig. 17 – MASH architecture. [4]

Each stage of the modulator consists in a low-order single loop modulator that contains the quantization error generated in the previous stage. The output of each stage is processed and combined by a digital cancellation logic unit so that only the quantization error of the last stage remains. In practice, the number of stages and consequently *L* is limited by circuit nonidealities, particularly mismatch, which cause incomplete cancellation of low order quantization errors causing noise leakage.

Multi-bit Quantizer:

According to (16), an alternative way to improve the resolution of an ADC consists of using embedded multi-bit quantization (*B* >1). A multi-bit modulator consists in a *B*-bit ADC and a *B*-bit DAC. The ADC is obtained by connecting *B* comparators in parallel which is relatively simple, however, to implement the DAC, 2^B-1 unit elements (capacitors, resistors, current sources, and others) are used to reconstruct the analog feedback signal in the modulator loop with 2^B levels. Thus, the analog signal is generated by summing all the contributions from the unit element outputs, which are sensitive to mismatches. When there is a mismatch, a nonlinear input-output DAC characteristic is obtained, and the analog signal with error is injected at the modulator input, degrading the modulator performance. Therefore, in practice, the linearity required in the DAC equals the wanted for the ΣΔM.

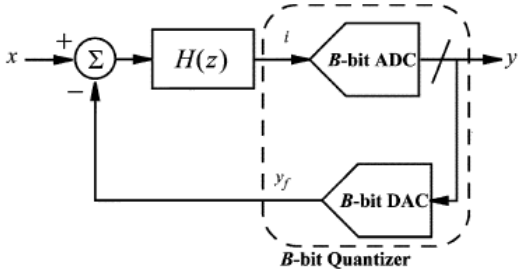


Fig. 18 – Multibit modulator. [4]

In order to solve the nonlinear DAC characteristic, it is necessary to implement a technique to obtain high multi-bit ΣΔMs. Among others, one of the most popularly used is the dynamic element matching (DEM) [12]. The basic idea behind DEM consists in varying the unit elements that generate de DAC output level over time. The selection of the unit elements is done by a control unit that drives

the average error in each DAC level to zero over time. Other alternatives to reduce the impact of DAC nonlinearities are based on deterministic techniques such as analog calibration, digital correction, and dual quantization.

Continuous Time Modulator (CT ΣΔM):

Given the need for even faster and lower power consumption converters, CT ΣΔM has gained popularity in technical journals and industry. The key difference between CT and DT implementations is where the sampling operation takes place. In DT, the input sampling takes place before the loop filter, whereas in the CT, the sampling process is done in the loop filter just before the quantizer as can be seen in Fig. 19.

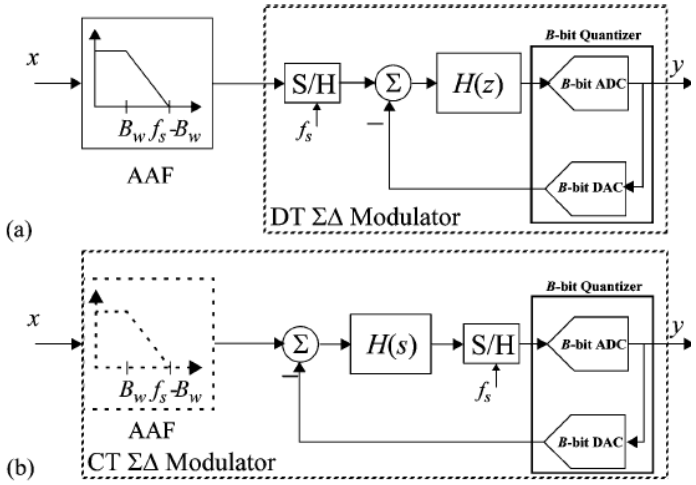


Fig. 19 – ΣΔM DT (a) e ΣΔM CT (b). [4]

With a CT implementation, the loop filter in now continuous time, using continuous time integrators (RC or gm/C), in contrast to the switched-capacitor integrators used for discrete time ADC. Besides, the feedback DAC can be implemented either in discrete time using switched-capacitor circuits or in continuous time using current-steering DACs. Current-steering DACs reduce power consumption and enable high-speed operation. However, they are more sensitive to clock jitter than switched-capacitor implementations as shown in Fig. 20.

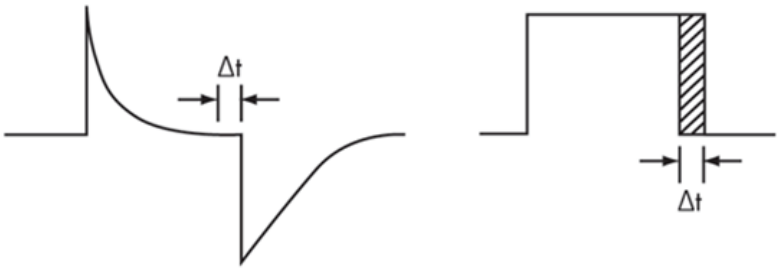


Fig. 20 – Comparison between clock jitter effect on a DT and CT ΣΔM. [13]

With a switched-capacitor DAC, the charge is transferred to the integrator mainly at the onset integration phase, decaying exponentially over time. For a continuous time design with current source feedback, a constant charge is transferred to the integration capacitor during the entire integration phase. This leads to significant noise when the feedback clock has jitter associated with it.

Looking at the complete CT ADC topology, it can be concluded that it presents some advantages such as high frequency rates, which allow the conversion of even higher bandwidth signals, low power consumption, and the elimination/reduction of the requirements placed on the AAF. This happens because the input signal enters in the loop filter before being sampled, which means that the loop filter acts as an anti-aliasing filter. For this reason, the quantization error and the input signal are filtered in the loop, relaxing the requirement on any external AAF. The main disadvantage of this implementation is that it can only operate at a fixed clock frequency as the pole locations of the integrators do not scale with frequency as in discrete time design. As a result, continuous time ADCs are mostly used as a part of large system-on-chip designs where the clock is well defined and not readily changed.

2.6. ΣΔM Architectures State-of-Art

The comparison between ΣΔ ADCs and other types of ADC was already done in section 2.4 to support the choice of using a ΣΔ implementation to accomplish the proposed objectives. In this section, a more specific comparison is done between the different existing topologies to explain which one is more suitable for this project. The data presented in Fig. 21 has been taken from [7].

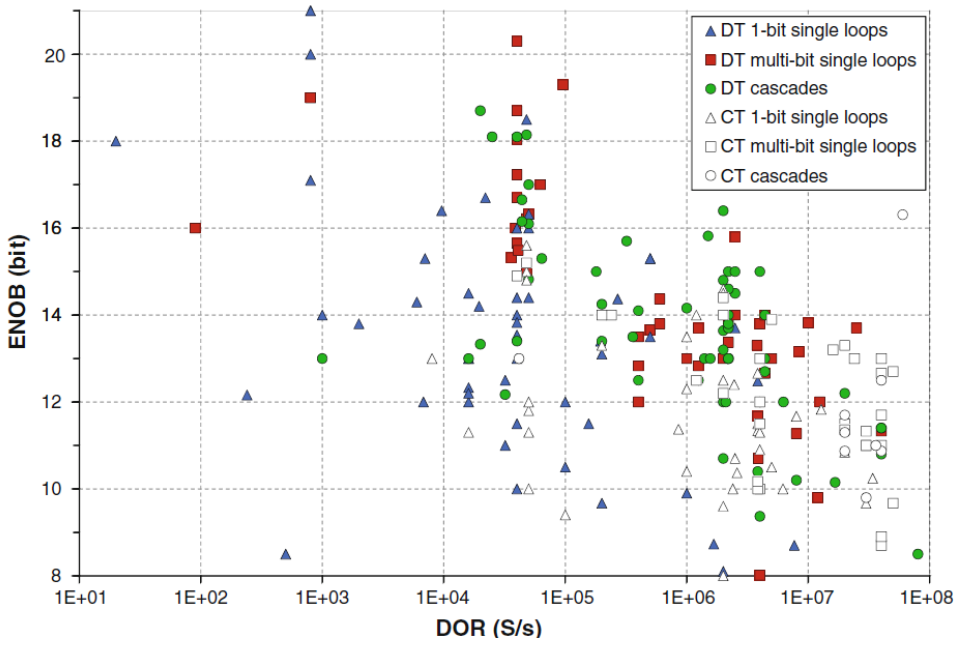


Fig. 21 – State of Art CMOS ΣΔ ADCs. [8]

For comparison purposes, the converters are classified into three categories: 1-bit single loop, multi-bit single loop, and cascade, distinguishing DT from CT implementations. Note from Fig. 21, that most implementations correspond to DT ΣΔ, which is dominant for high resolutions, whereas CT dominates for large bandwidth applications. For large-bandwidth, medium-resolution (10-14 bit) both implementations coexist.

The single loop 1-bit topology stands out from the others, due to the ability to obtain a wide range of resolutions (from 8 to 22 bit) with signals with small to medium-high bandwidth (100 Hz to 10 MHz). From Fig. 21 it can be seen that most ADCs with this topology achieve around 13-bit ENOB with

500 kHz of samples per second. In this project, as the purpose is studying and validating a new topology of ΣΔ ADC, the chosen topology was the single loop 1-bit, having the advantages of low power consumption, small stability problems and a circuit with moderate complexity when compared to the other implementations. Table 1 presents more details on some implementations of DT ΣΔ with single loop.

Table 1 – Examples of DT ΣΔ with single loops.

Reference	Technology [nm]	ENOB [bit]	OSR	DOR [S/s]
[14]	28	10	48	10 M
[15]	180	14	750	100 k
[16]	350	14	256	20 k
[17]	180	13	24	1 M

ΣΔ ADC performance can be globally quantified regarding their main specifications (effective resolution, signal bandwidth and power consumption of the circuit) through the following figures of merit (FoMs) proposed by [18], [19] and [20]

$$\mathrm{FoM}_1|_{\mathrm{pJ/conv}} = \frac{\mathrm{Power(W)}}{2^{\mathrm{ENOB(bit)}}\mathrm{DOR(Sps)}} \tag{18}$$

$$\mathrm{FoM}_2 = 2kT \times \frac{3 \times 2^{2\mathrm{ENOB(bit)}}\mathrm{DOR(Sps)}}{\mathrm{Power(W)}} \tag{19}$$

where *k* is the Boltzmann constant and T is the circuit temperature (measured in K). FoM_1 emphasizes power consumption whereas FoM_2 emphasizes effective resolution, which translates to: the smaller the FoM_1, and the larger the FoM_2, the better the ΣΔ ADC.

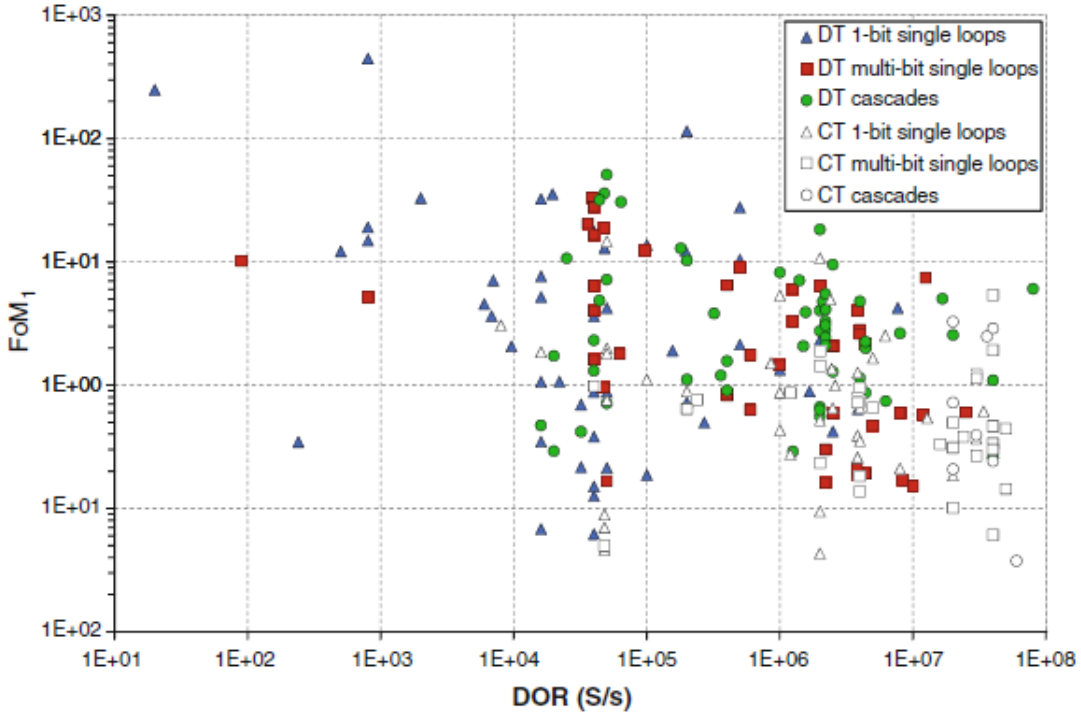


Fig. 22 – FoM_1. [8]

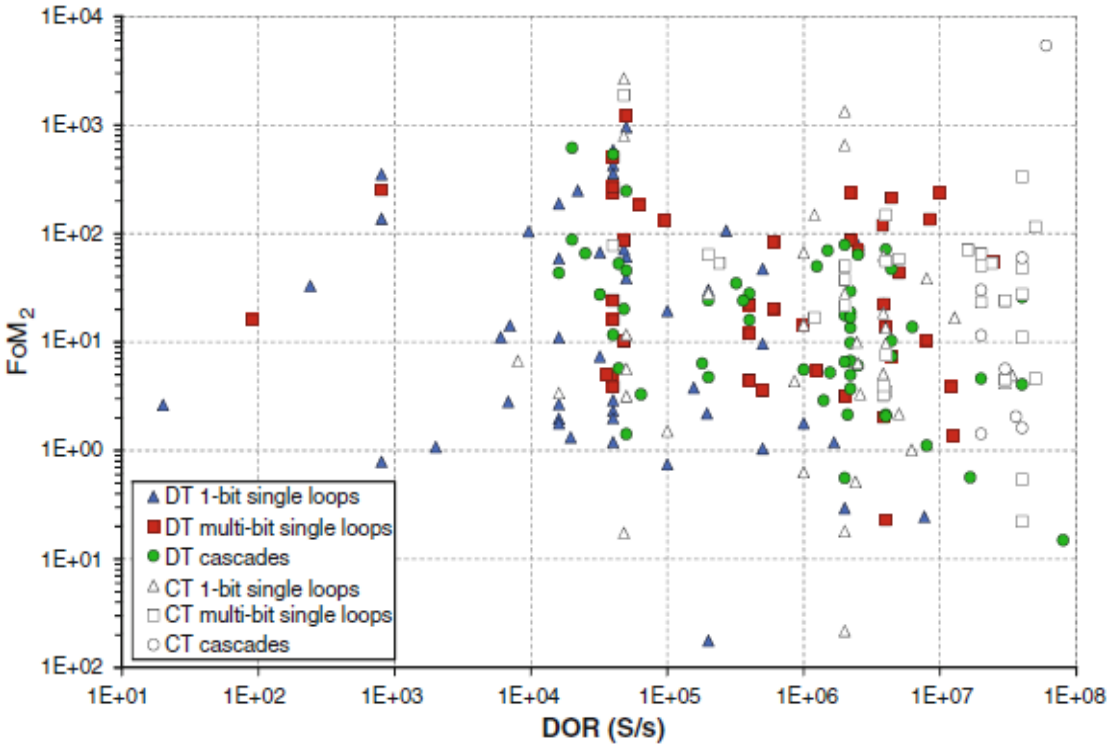


Fig. 23 – FoM_2. [8]

Power consumption in a 1-bit single loop topology is low, especially for low order implementations, presenting a medium FoM_2 which allows medium resolutions and medium to high sampling rates with low power consumption, which is ideal for the project objectives.

2.7. Active VS Quasi-Passive ADCs

ADCs can also be divided in two different groups, active ADCs, and quasi-passive ADCs. Within the scope of this thesis, an ADC is considered active if the circuit contains at least one active block, such as an operational amplifier (opamp) or an operational transconductance amplifier (OTA). This type of active devices have the ability to amplify signals transferring energy from its power supply to the load. When the circuit is only composed by passive devices, such as resistors, capacitors, inductors, and transformers it is considered a passive circuit. These devices do not require any form of electrical power to operate, and for this reason, they can only store or dissipate energy. Note that the circuit uses transistors to implement MOSCAPs, switches and logic gates hence, it cannot be considered as a passive circuit according to the presented definition, hence in this thesis, the circuit was designated as a quasi-passive ADC, even though the topology is opamp free.

In ADCs most of the power consumption is caused by the opamps or OTAs used in the integrator. A lot of effort can be made to reduce the total power consumption of an ADC, although the most important part is the design of the amplifier that is being used. ADC integrators generally demand operational amplifiers with high unity-gain frequency requirements, which are increasingly difficult to be achieved in short channel CMOS technologies due to the limited intrinsic gain of the transistors. Alternatively, a few works were published with passive integrators, replacing some of the amplifiers to

reduce the power consumption while maintaining the resolution and sampling frequency. Examples of this principle are presented in [21], [22], [23] and [24]. For this reason, a study of the active and passive integrators is presented in this section, in order to explore the major advantages and drawbacks of each implementation.

2.7.1. Active Integrators

An active integrator is composed by an operational amplifier performing the mathematical operation of integration. With this device, an output voltage is produced which is proportional to the integral of the input voltage. The circuit presented in Fig. 24 implements an integrator using one opamp, two resistors, and one capacitor.

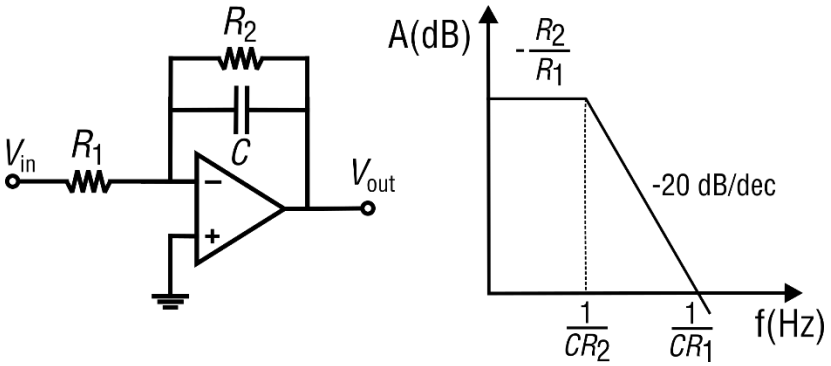


Fig. 24 – Active integrator circuit and frequency response.

The working principle of this circuit is based on the opamp ability to keep the voltage of the inputs at the same potential. When a voltage is applied to the input (V_{in}), the uncharged capacitor (C) acts like a short circuit allowing maximum current to flow via the input resistor R_1. As the non-inverting input of the opamp is connected to ground, no current flows to the inverting input. When the capacitor begins to charge up, its impedance slowly increases in proportion to its rate of charge determined by the RC time constant. The opamp is forced to produce an output voltage to maintain a virtual earth at the inverting input, and since the capacitor is connected between the opamp inverting input and the output, the potential voltage developed across C is the integral of V_{in}. The output voltage continues to increase until the capacitor is fully charged, resulting in the saturation of the integrator.

By connecting R_2 in parallel with C, the voltage gain and the corner frequency can be changed, being described by the following equations:

$$A_0 = -\frac{R_2}{R_1} \tag{20}$$

$$f_0 = \frac{1}{2\pi C R_2} \tag{21}$$

It is important to mention that these equations are only valid if the opamp is considered an ideal circuit, however in reality, some imperfections affect the opamp behavior. In DC domain, opamps present imperfections being the most important the finite gain, finite input impedance, non-zero output impedance, input current, input offset voltage, and common-mode gain. For the AC domain, opamps present finite bandwidth which can cause stability problems and distortion, and they also generate noise. There are others non-linear imperfections such as saturation, slewing and non-linear input-output relationship which affects the integrator performance. As a result of these imperfections, the opamp

needs to be carefully designed in order to fulfill the integrator requirements, which generally correspond to a high-power consumption amplifier.

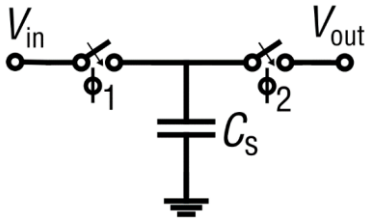


Fig. 25 – Switched capacitor resistor.

When implemented in CMOS technology, the resistors of the circuit are replaced by switched capacitors allowing to implement the circuit in a smaller area. The working principle of a switched capacitor resistor is based on one capacitor and two switches, which are connected to the capacitor with a given frequency using two non-overlapping signals. As the capacitor takes time to charge, it acts like a resistor when used with high frequencies, being the equivalent resistance described by (22) where *f* is the working frequency of the switches.

$$R = \frac{1}{C_s f} \tag{22}$$

The implementation of an active switched capacitor integrator is presented in Fig. 26. In this circuit, two different phases are used (ϕ_1 and ϕ_2). The dynamic properties of the opamp, such as the unity-gain frequency and slew rate determine the speed of the integration, while the DC voltage gain establishes the quality of the integration function.

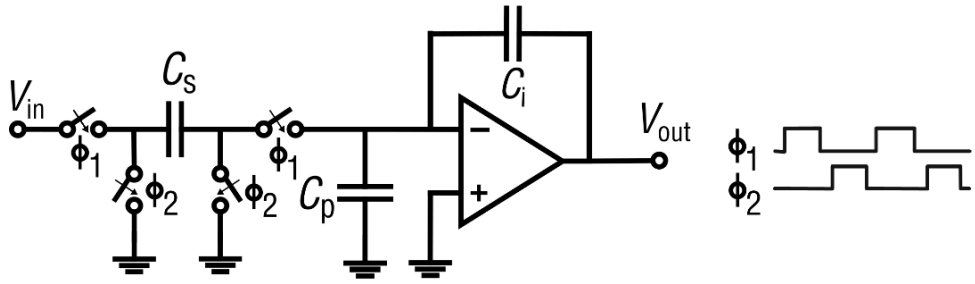


Fig. 26 – Active SC integrator.

The resulting transfer function of a conventional active switched capacitor integrator is given by (23).

$$\frac{V_{out}}{V_{in}} = \frac{\alpha z^{-1}}{1 - \beta z^{-1}} \tag{23}$$

With infinite gain on the opamp, α is given by C_s/C_i and β = 1. With finite gain, β is then given by (24),

$$\beta = \frac{A_0 C_i + C_i + C_p}{A_0 C_i + C_i + C_p + C_S} \tag{24}$$

where A_0 is the open-loop gain of the opamp. In practice, as the value of A_0 decreases, the value of β further deviates from the ideal unity, and the integrator becomes leakier, performing worse in terms of SNDR. Thus, an SC integrator employing an opamp with finite gain exhibits integration leakage and is therefore lossy. This fact weakens the noise-shaping ability of the modulator, leading to a degraded SNDR [25]. To avoid power hungry amplifiers and its design difficulties, passive SC integrators have

been studied and developed to reduce the area and power consumption of the circuits and increasing their speed.

2.7.2. Quasi-Passive Integrators

Passive integrators, as stated before, can only be implemented using passive devices. The simplest implementation is the passive RC integrator circuit presented in Fig. 27, where the input is connected to a resistor while the output voltage is measured across the capacitor that is being charged.

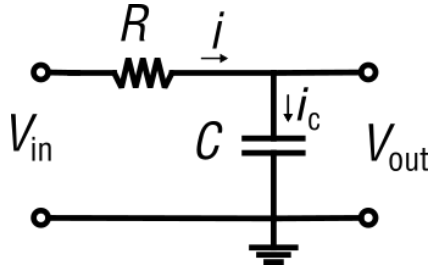


Fig. 27 – Passive RC integrator.

As the capacitor is a frequency dependent element, the amount of charge stored in the capacitor is equal to the time domain integral of the current flowing through the capacitor. i_c. This current can be expressed by (25), and the capacitor charge (*Q*) by (26).

$$\mathrm{i}_c(t) = C\frac{dV_{out}(t)}{dt} \tag{25}$$

$$\mathrm{Q} = \mathrm{C} \times \mathrm{V}_{\mathrm{out}} \tag{26}$$

Combining equation (25) with (26), Q can be expressed in relation to i_c resulting (27).

$$\mathrm{Q} = \int \mathrm{i}_{\mathrm{c}}\, dt \tag{27}$$

Since the input of the circuit is connected to the resistor R, the current that flows through the resistor (i) is the same as the current that goes to the capacitor (i_c).

$$\mathrm{i(t)} = \frac{\mathrm{V_{in}}}{\mathrm{R}} = C\frac{dV_{out}(t)}{dt} \tag{28}$$

Therefore, V_{out} can be expressed in relation to the current by (29), and in relation to the input voltage by (30).

$$V_{out} = \frac{Q}{C} = \frac{\int \mathrm{i}\, dt}{C} = \frac{1}{C}\int \mathrm{i}\, dt \tag{29}$$

$$V_{out} = \frac{1}{RC}\int V_{in}\, dt \tag{30}$$

Similarly to the active integrator, the resistor R can also be replaced by a switched capacitor leading to the circuit presented in Fig. 28. This circuit is controlled by two non-inverting clock signals ϕ_1 and ϕ_2. When ϕ_1 is active, C_s samples the charge supplied by the input signal (V_{in}). When ϕ_2 is active, the charge in C_s is transferred to C_i, which holds the total charge supplied by V_{in} along the cycles. Before the next integration takes place, C_s is disconnected from C_i. While the voltage in C_i is not affected by disconnecting C_s (assuming ideal switches), the integration takes place on the charge domain, and some charge is still leaked given the fact that C_s has a non-zero value of capacitance. This affects the modulator performance in a similar way to the leakage caused by finite amplifier gain in an active ΣΔ modulator.

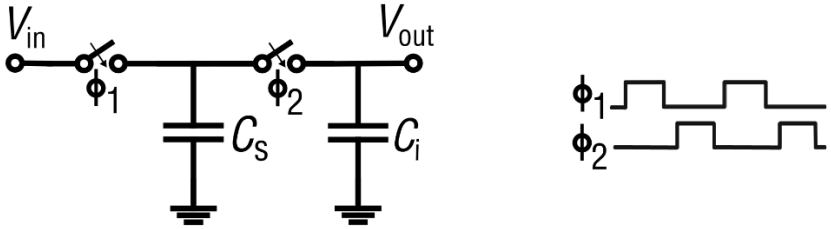


Fig. 28 – Passive switched capacitor integrator.

For the passive integrator presented in Fig. 28, α and β are given by (31).

$$\alpha = \frac{C_s}{C_s + C_i};\ \beta = \frac{C_i}{C_s + C_i} \tag{31}$$

In expression (31), α is always less than 1 which results in an attenuation of the input signal. However, the most interesting result is in the formula of β. Notice that β in (24) and (31) are identical if $A_0 = 0$, which is a reasonable result since passive integrators do not employ any amplifier at all. The absence of A_0 as a knob in β, makes the design of high-accuracy quasi-passive ΣΔ modulators much more challenging. While the integrator leakage can be digitally calibrated [25], in this work, the focus is evaluating the potential of passive integrator implementations without any sort of error correction.

In order to reduce the leakage on the passive-integrator, the portion of the total charge that is lost while disconnecting C_s from C_i must be reduced (and thus the relationship C_s/C_i at that instant). At the same time, C_s cannot be made too small in a ΣΔM implementation, because the integrator dynamic range is also a function of C_s/C_i. A solution to these issues is to use a capacitor with a variable capacitance: C_s should be relatively large while sampling and present the minimum possible capacitance during integration, so that the leaked charge is minimized. In the context of an integrated circuit, a MOS capacitor is a good candidate for such device, and its properties have been already explored in ADCs towards amplification, with the “parametric amplifier” [22] [24] [26] [27].

2.8. MOS Capacitor

The MOS Capacitor, also known as MOSCAP, consists of a MOS transistor with the source and drain terminals shorted. With this configuration, MOS transistors act like a capacitor being able to hold a charge between the gate and bulk. The main advantage of using MOSCAPs instead of linear capacitors is the variable capacitance that they present, which can be used to amplify signals and reduce charge leakage, presenting ideally no noise and being able to work with high sampling rates with almost no static power consumption.

The gate-bulk capacitance (C_{GB}) of the MOSCAP is dependent on the voltage at which the source and drain terminal are tied. There are two different types of MOSCAPs, *n*-type and *p*-type depending on the MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) channel being used. For an n-MOSCAP, C_{GB} can be expressed by the curves presented in Fig. 29.

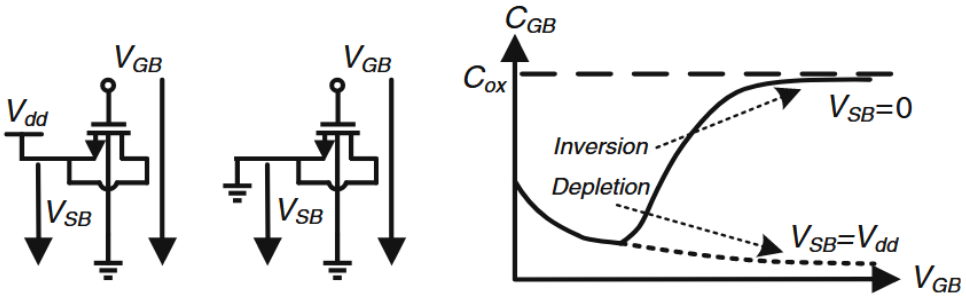


Fig. 29 – MOSCAP capacitance VS voltage for different V_{SB}.

When the source-drain terminal is tied to GND ($V_{SB} = 0$), and there is a high enough V_{GS} the transistor is in the strong inversion zone, which creates a large capacitor described by equation (32),

$$C_{GB} = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \tag{32}$$

where ϵ_{ox} represents the dielectric constant of the oxide and t_{ox} the thickness. For $V_{SB} = V_{DD}$, the transistor is in the depletion zone, as the high potential of the source-drain terminal prevents the formation of the inversion layer. In consequence, C_{GB} is now expressed by C_{ox} || C_{dep} where the symbol || represents a series capacitors connection and C_{dep} the capacitance of the depletion region beneath the gate.

Recently, passive amplifiers were implemented in a low power ΣΔ ADC exploiting the use of MOSCAPs [22] [24]. In those works, the main idea is to achieve voltage amplification reduction the capacitance C_{GB}, while keeping the total charge equal. As the charge is expressed by (26) where *C* is multiplied by *V*, when *C* is reduced, *V* needs to increase in order to keep the charge *Q* constant. This principle is accomplished through the variable capacitance that MOSCAPs present, by changing the working region from inversion to depletion. There is also another example of MOSCAPs implemented in ADCs, [28] where the DAC of a charge sharing SAR ADC is implemented with MOSCAPs, allowing to improve the tolerance of the ADC to the comparator offset and noise. In this work, the MOSCAPs are explored not for voltage amplification, but to decrease the charge leaked during passive integration.

3. Quasi-Passive 1st Order ΣΔ Architecture

After analyzing the different topologies to implement ΣΔ ADCs and based on the project objectives of implementing a small and low power circuit for IoT applications, a quasi-passive 1st order ΣΔ topology is presented in this section. The modulator requirements and the theoretical results for an ideal ΣΔ modulator are explored, in order to have an idea of the best results achievable. The proposed circuit is explained, and the different components are presented. This section ends with a simplified schematic of the complete circuit and an explanation of its working principle with simulation waveforms.

The proposed ΣΔ architecture presents a moderate complexity and is unconditionally stable, achieving a low power consumption, and occupying a very small area given the absence of an operational amplifier. These characteristics make the proposed architecture very promising for the dissertation objective of developing an IoT circuit.

3.1. Modulator Requirements Analysis

Based on the expressions presented in the last section, the theoretical results of the modulator can be calculated using (15) by replacing the filter order, *L* by 1 and the quantizer number of bit, *B* by 1. The obtained expression (33) gives DR in dB as a function of OSR.

$$\mathrm{DR}|_{\mathrm{dB}} \approx 6.131 + 30\log_{10}(\mathrm{OSR}) \tag{33}$$

With expression (33) and using *Matlab* the maximum value for DR can be obtained for different oversampling rates, the results are presented in Fig. 30. For a first order modulator, with an OSR of 128, the ADC can theoretically achieve a maximum DR of 69.3 dB which corresponds to approximately 11.2 bit ENOB.

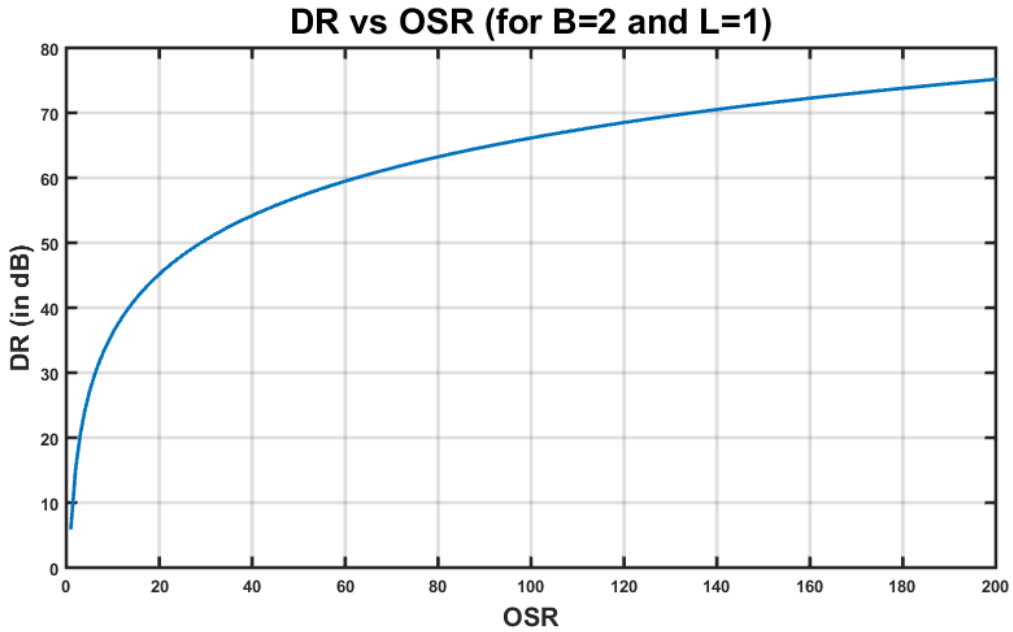


Fig. 30 – DR as a function of OSR for different *L*.

In order to get the best performance out of a ΣΔ modulator, the different gain blocks of the feedback loop must be dimensioned. This is especially important in high order ΣΔ modulators. In general, selecting the coefficients involves solving several trade-offs between architectural, circuit and technological aspects of the practical implementation. More precisely, keeping the integrator outputs bound to ensure the modulator stability; maximizing the overload level of the ΣΔM to ensure a high peak SNR; minimizing the required signal swing at the integrator output; and simplifying the implementation of the coefficients since in switched capacitors, the coefficients are implemented as capacitor ratios. For this purpose, a helpful tool is used [29], which tests millions of combinations for a given ΣΔ ADC topology and presents the best one, keeping the integrator stable, maximizing SNR, reducing integrator output swings and simplifying the implementation. The scheme used to implement a first order ΣΔ is presented in Fig. 31.

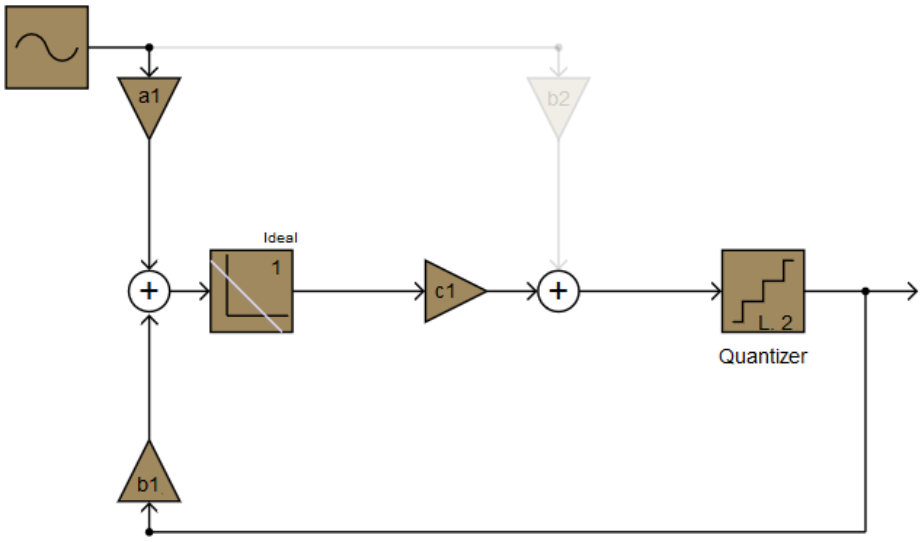


Fig. 31 – ΣΔ Modulator scheme.

A total number of three gain blocks needs to be dimensioned: a1, b1 and c1. A two level quantizer is used, and one integrator is placed in the feedback loop. The obtained coefficients generated by the program are presented in Table 2. As expected, a1 and b1 have the same value in module as in a first order implementation the input and the DAC gains are generally equal. This ensures the correct working function of the feedback loop, without saturating the modulator.

Table 2 – Coefficient list.

Coefficient	Value
a1	0.9
b1	- 0.9
c1	1

Besides the coefficients gains, the tool also simulates the results of the ΣΔM, calculating the best SNR, the power spectrum, STF, and NTF. It is important to highlight that the following results are calculated considering an ideal first order ΣΔM, which means an active ADC with an infinite opamp gain. As the proposed circuit does not employ any opamp, these results are merely a reference of the best

performance achievable. The obtained SNR with the coefficients generated by the program is represented in Fig. 32.

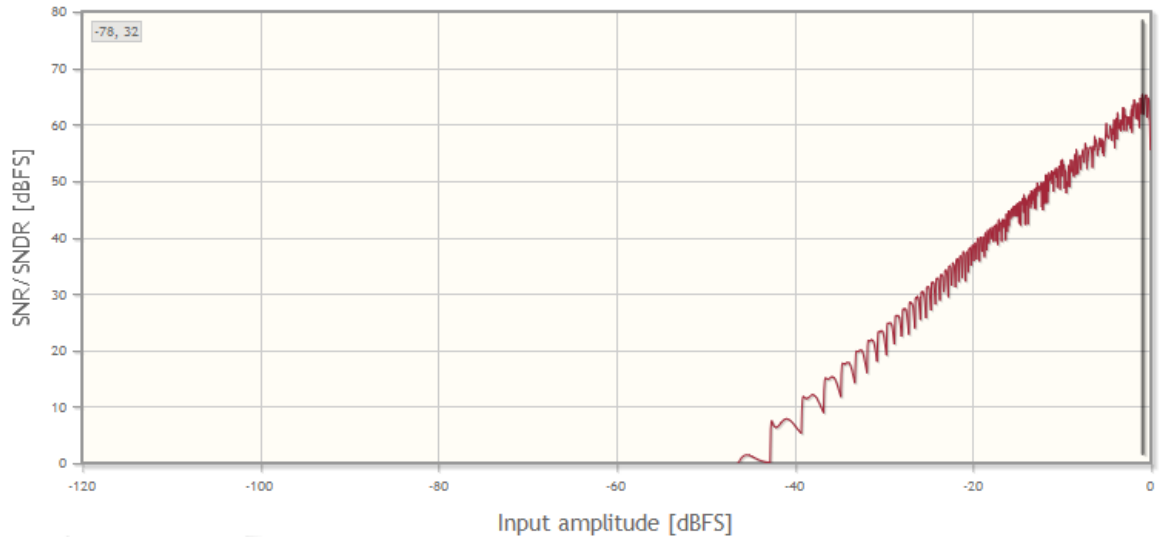


Fig. 32 – Obtained SNR.

The SNR increases with the input signal amplitude, presenting a peak of 66 dB for an OSR of 128. The SNR peak is followed by a sharp drop when the amplitude of the signal gets to the overload level, causing an increase of the in-band error. Another significant result of the simulation is the output spectrum of the signal represented in Fig. 33.

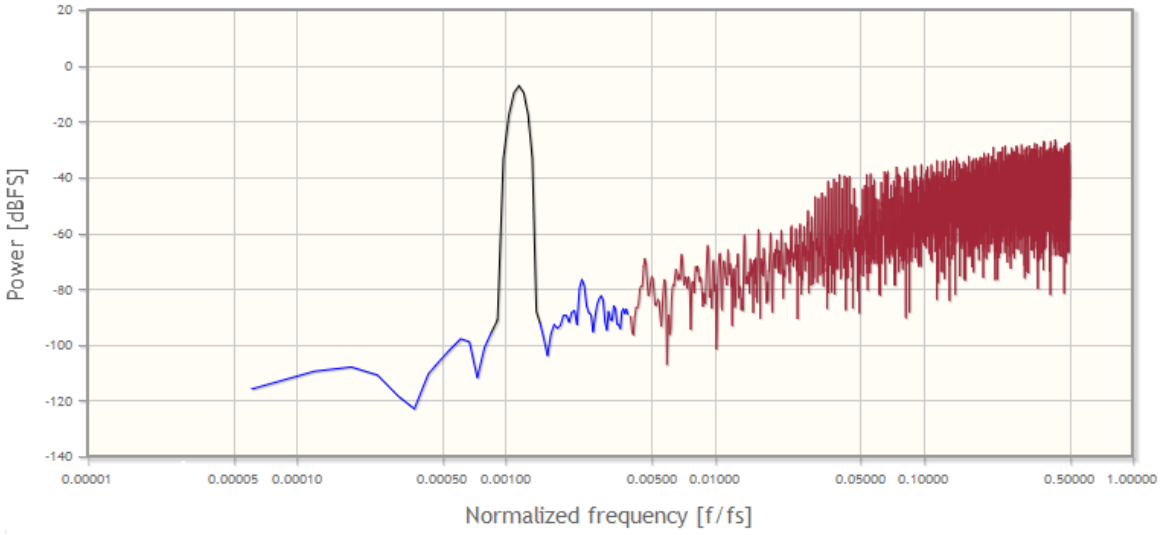


Fig. 33 – Power Spectrum.

In this simulation, the effect of the first order feedback loop can be clearly seen. The power is maximum at the input frequency which corresponds to the input signal. In relation to the power of the quantization error, it increases with the frequency, as the quantization noise is filtered by a high pass filter. A slope of approximately 20 dB can be visualized as the modulator has a first order loop. The transfer function applied to the input signal is presented in Fig. 34, having a unitary gain for low frequencies, a cut off frequency one decade above the input signal frequency, and a slope of -20 dB/dec, typical of a first order modulator.

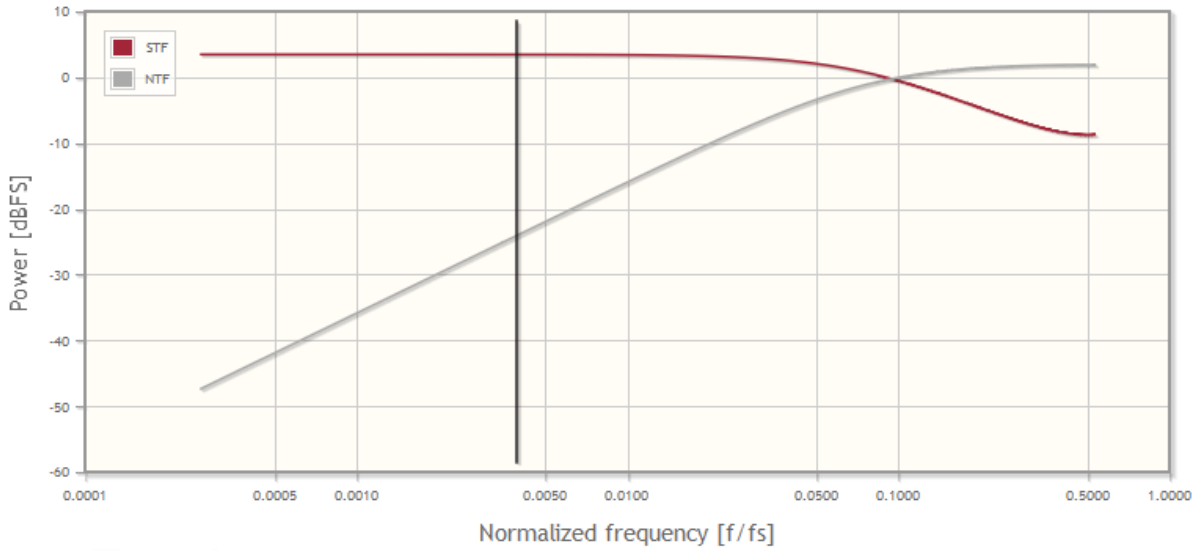


Fig. 34 – Signal and Noise transfer function (STF and NTF).

Now that the performance of an ideal first order ΣΔ was analyzed and the best achievable results calculated, the next section focuses on the implementation of the proposed circuit. A new type of a quasi-passive integration is presented and discussed, targeting an improvement on opamp-free integrators.

3.2. Quasi-Passive integration

As introduced in section 2.7, the aim of this project is to avoid power hungry amplifiers and its design difficulties for short channel CMOS technologies, in order to produce a small size and low power circuit. Having in mind the basic concepts of passive integration and the working principle of MOSCAPs, this section combines these two fields in order to achieve a high linearity quasi-passive integrator. The different components of the circuit are presented and explained, and the mathematical expressions are derived.

3.2.1. Integrator and Hold (I/H)

Traditionally, the input signal is sampled in ADCs through a Track and Hold (T/H), which is a voltage-based circuit that uses a switch and a capacitor. The T/H is represented in Fig. 35, where a clock signal is used to start and end the tracking of the input, and the capacitor is used to hold the voltage to be quantized. When the switch is closed, the output voltage V_{out} is equal to the input voltage V_{in}, while during the hold phase, V_{out} is maintained at the sampled voltage.

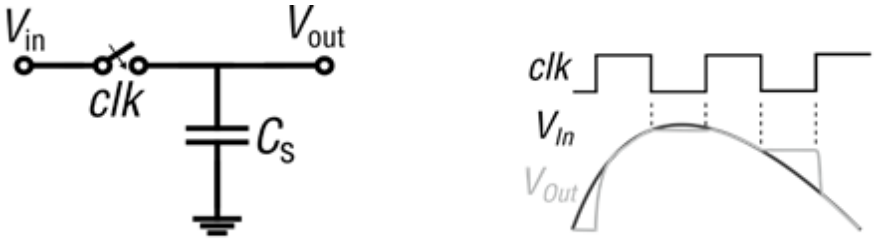


Fig. 35 – Track and Hold circuit and waveforms.

For this work, a different design must be implemented in order to use MOSCAPs instead of linear capacitors. As stated before, MOSCAPs present a non-linear capacitance, which translates in a non-linear voltage. Thus, a different circuit must be used to convert the input voltage into a linear current before the integration takes place. This allows to process the information in the charge domain and at the same time, take advantage of the MOSCAPs non-linearity to reduce the charge leakage.

In [30], the authors present a transconductance-based sampling circuit that operates on the charge domain, designated Integrator and Hold (I/H). The working principle of the I/H is simple, as the T/H, it uses one switch and one capacitor, but it also employs a Gm cell and a *reset* switch, as presented in Fig. 36. The input voltage is converted to current with the Gm cell, and then it is integrated into the capacitor during a certain amount of time. This current based circuit carries the input signal in current (or charge) and, in addition, the Gm-based frontend presents a *sinc* (sin(x)/x) filter response, which helps to increase tolerance to clock jitter, time skew, non-zero rise and fall times of the sampling clock and switch resistance when compared to T/H, as explained in [31] and [32].

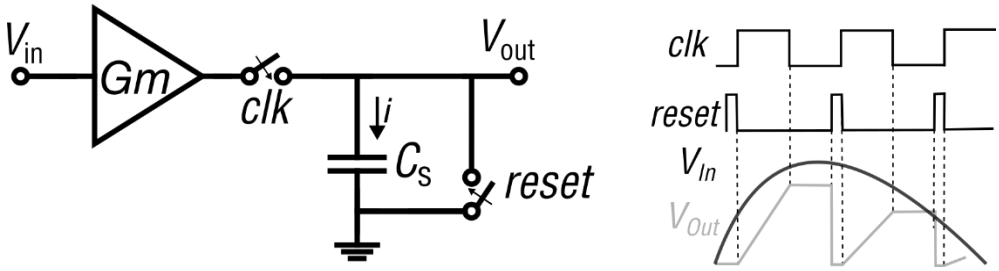


Fig. 36 – Integrator and Hold circuit and waveforms.

At this point, it is important to introduce the concept of voltage mode and current mode, which are two working regions for the I/H. For the track and hold circuit, C_s is always charged by a potential difference between one side of the capacitor and the other, hence the charge being transferred to the capacitor is linearly dependent to the input voltage. For the integrator and hold, C_s is charged with a current that is proportional to the input voltage multiplied by a constant transconductance. While charging the capacitor, the charge is linearly dependent on the current i and the circuit is working in current mode. However, in a practical implementation, as it will be presented later in this thesis, when the capacitor voltage approaches the input voltage, the current i drops and the voltage across the capacitor follows the input voltage. When this happens, the charge that is being transferred to the capacitor is no longer linear with the current, and the circuit enters in voltage mode degrading the linearity of the modulator and consequently the SNDR. For the modulator purposes, the charge that is transferred to the MOSCAPs must always be proportional to the current, by keeping the I/H working in current mode.

3.2.2. Gm cell

To implement the I/H, the most critical part is the design of the Gm circuit. Ideally, the circuit will work as a perfect Gm cell, presenting a well-defined transconductance so that the equation that relates the current with the voltage is expressed by (34).

$$I = gm \times V \tag{34}$$

A rudimentary transconductor can be achieved with a simple digital inverter (Fig. 37) which, in the context of digital circuits, implements the Boolean operation of negation or inversion.

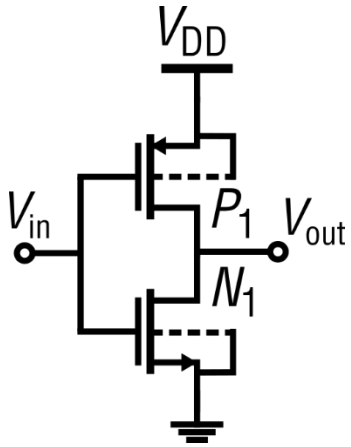


Fig. 37 – CMOS inverter circuit.

To achieve the functionality of a transconductor, the CMOS inverter must keep its operating point at a small-signal around a fixed biasing input voltage. Within a given biasing range, around the transition region, both NMOS and PMOS transistors work in saturation mode. Around this DC point, the inverter produces an output current i_{out} linearly dependent to the input voltage V_{in}. An approximate mathematical expression for the output current can be derived by linearizing the circuit. Considering that the transconductance is defined by (35),

$$g_m = \frac{\partial i_{out}}{\partial V_{in}} \tag{35}$$

and describing the output current as a function of V_{in} and V_{out}, by expression (36)

$$i_{out} = g_m(V_{in}, V_{out}) \approx \frac{\partial i_{out}}{\partial V_{in}} \Delta V_{in} + \frac{\partial i_{out}}{\partial V_{out}} \Delta V_{out} \tag{36}$$

it is possible to derivate the expression that correlates the different variables. If the inverter is working at the DC bias point and the signal swings are small enough, the voltage variations can be approximated to V_{in} and V_{out} and expression (37) can be derived.

$$i_{out} = g_m V_{in} + g_o V_{out} \tag{37}$$

g_m represents the transconductance and g_o represents the output conductance of the inverter. The value of g_m is the sum of the NMOS and PMOS transconductance in saturation mode of operation.

$$g_m = g_{mN} + g_{mP} \tag{38}$$

Working on a linear region, for small signals, g_{mN} and g_{mP} are described by (39)

$$g_{mN,P} = \mu_{N,P} C_{ox} \frac{W}{L} \left(V_{GS,SG} - V_t\right) \tag{39}$$

Fig. 38 shows the schematic of the implemented circuit adapted from [30], which exploits the inverter transconductance mode and uses source degeneration, that is also used for common mode feedback (CMFB). Besides the input voltages and the CMFB, the circuit is also controlled by two other signals, *enable* and *disable*, which allow to switch the cell on and off. This Gm cell converts the input voltage to an output current continuously, with a gain that can be controlled by the number of cells that are used in parallel and by the width and length of the different transistors. Calculating the mathematical expression of the total harmonic distortion (THD) of the Gm cell is out of the scope of this work, hence

a more experimental approach based on mathematical expressions is presented to size the different components.

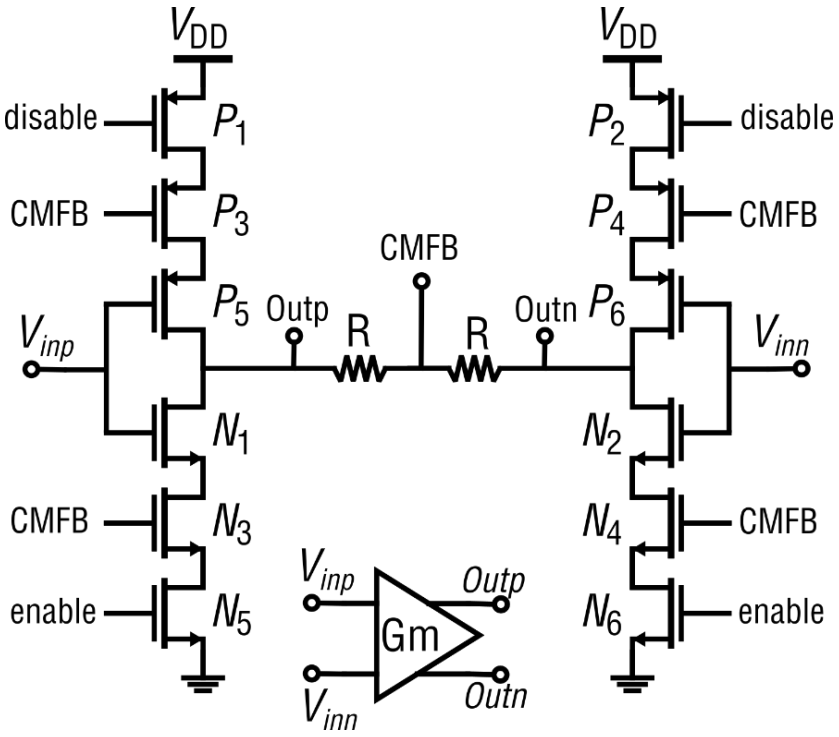


Fig. 38 – Inverter based Gm cell.

3.2.3. I/H mathematical expressions derivation

Three main aspects are important when dimensioning the Gm cell. The first one is the linearity: the current must be sufficiently linear so that a constant charge is transferred in a certain amount of time. The second important aspect is the common mode voltage which must be above the threshold voltage (approximately 0.5 V for the employed 130 nm process employed) in order to bias the MOSCAPs on the high capacitance region. The last aspect is the output differential voltage which should be maximized to increase the dynamic range inside the ADC. For these reasons, it is helpful to derive the mathematical expressions that translate the circuit working function.

The expressions of the common mode voltage and the differential voltage for a double ended circuit are commonly represented by (40) and (41) respectively.

$$V_{CM_{out}} = \frac{V_{outp} + V_{outn}}{2} \tag{40}$$

$$V_{dif_{out}} = V_{outp} - V_{outn} \tag{41}$$

Considering now the Gm cell as a perfect transconductor and the MOSCAP with a fixed capacitance a simple, but very informative equality can be derived.

$$Q = \int_0^{Ts} (V_{in} \times g_m)\, dt = V_{out} \times C \tag{42}$$

With equation (42) the relation between five parameters of the I/H are expressed: input voltage (V_{in}), transconductance gain (g_m), integration time (Ts), output voltage (V_{out}) and capacitance (C). Manipulating equation (42), V_{out} can be expressed in order to the other parameters.

$$V_{out} = \frac{V_{in} \times g_m \times Ts}{C} \tag{43}$$

Considering (43) and replacing V_{in} by the differential and common-mode components, V_{outp} and V_{outn} can be derived after some mathematical manipulation.

$$V_{outp} = \frac{\left(V_{CM_{in}} + \frac{V_{dif_{in}}}{2}\right) \times g_m \times Ts}{C} \tag{44}$$

$$V_{outn} = \frac{\left(V_{CM_{in}} - \frac{V_{dif_{in}}}{2}\right) \times g_m \times Ts}{C} \tag{45}$$

Replacing (44) and (45) in (40) and (41), the relation between $V_{CM_{out}}$ and $V_{dif_{out}}$ with the other parameters can be expressed.

$$V_{CM_{out}} = \frac{V_{CM_{in}} \times g_m \times Ts}{C} \tag{46}$$

$$V_{dif_{out}} = \frac{V_{dif_{in}} \times g_m \times Ts}{C} \tag{47}$$

Inspecting equations (46) and (47), it is clear that both $V_{CM_{out}}$ and $V_{dif_{out}}$ are directly proportional to g_m and Ts, and inversely proportional to C. Consequently, there are three options to increase the differential voltage and the common mode voltage at the output: increasing the transconductance of the Gm cell; increasing the amount of time that the Gm cell is converting the input voltage into current; or decreasing the capacitance of the output. It is also important to note that $V_{dif_{out}}$ is proportional to $V_{dif_{in}}$ and $V_{CM_{out}}$ to $V_{CM_{in}}$. The derived equations will be especially helpful when sizing the different I/H components on chapter 4.

3.2.4. Sampling MOSCAPs

The sampling MOSCAPs are placed after the Gm circuit and are responsible for integrating the current. The chosen topology for this purpose is presented in Fig. 39 where two complementary MOSCAPs are connected in parallel. The reader is referred to [28] for a detailed study of this topology. Fig. 39 also presents the capacitance curve for different voltages. Notice that the two capacitance curves are complementary in order to sample the signals of the double ended circuit. The capacity of the MOSCAPs for the two working regions was obtained through simulation for an area of 1μm² and compared with the theoretical equation (32).

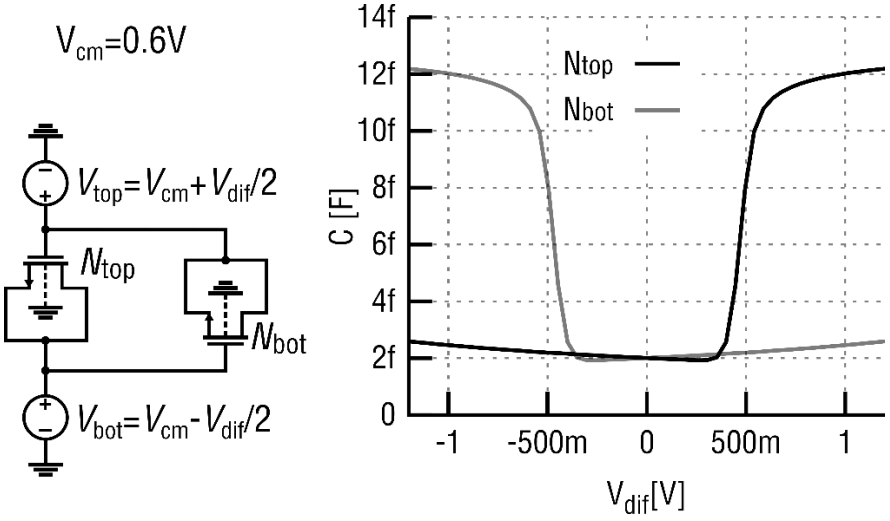


Fig. 39 – Complementary MOSCAP topology and C x V curve.

To obtain a high linear passive integrator, the MOSCAPs capacitance must be carefully designed. As explained in the last section, the capacitance of the MOSCAPs (C), affects the output common mode and differential voltage. When the capacitance increases, $V_{CM_{out}}$ and $V_{dif_{out}}$ decrease. This can be obtained by changing the dimensions of the MOSCAPs or increasing its number. As the objectives are to maximize $V_{dif_{out}}$ to use all the dynamic range inside the ADC, and to obtain a $V_{CM_{out}}$ above 0.5 V, to guarantee the correct operation principle of the MOSCAPs, a low capacitance would be the obvious choice. However, another important trade-off imposes a limit to the minimum capacitance of the MOSCAPs. The capacitance must be high enough so that during the charge sampling period, the MOSCAPs do not saturate, or the transconductor enters in voltage mode. For a given transconductance and charge period, the MOSCAPs must have a high enough capacitance to always work in current mode and never saturate. If the MOSCAPs saturate, the resulting charge will no longer be linear to the input current and the ENOB will reduce drastically. In conclusion, the I/H MOSCAPs must be designed to obtain a $V_{CM_{out}}$ above 0.5 V, a high $V_{dif_{out}}$, and to maximize the linearity of the circuit by keeping the I/H working in current mode.

3.3. DAC MOSCAPs and Logic

The DAC MOSCAPs are responsible for the ΣΔ modulator feedback. These MOSCAPs are charged with voltage being connected to V_{DD} or GND according to the comparator output, y. The employed topology is similar to the one used with the sampling MOSCAPs, although in this application they are charged when connected to V_{DD} or GND instead of receiving a current.

In order to implement the typical feedback loop of the ΣΔ modulator, the charging and discharging of the DAC MOSCAPs are controlled by two signals. The first, as already presented, is the comparator output, and the second is the clock signal, which controls the charge and discharge phases of the MOSCAPs. To avoid placing two switches in series with the clock signal and the output of the comparator, four logic gates are used to generate the control signals for the switches. Fig. 40 presents the DAC MOSCAPs and the logic applied to the different switches.

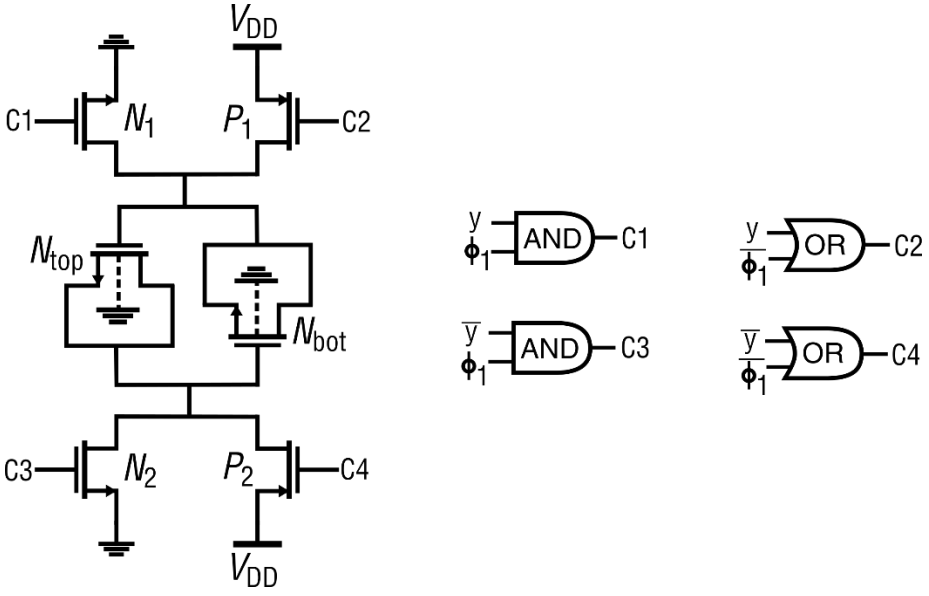


Fig. 40 – DAC implementation and logic.

The four logic gates are composed by two ANDs and two ORs, and the used switches are PMOS and NMOS, being chosen according to the voltage at which they are connected. As the feedback of the modulator is negative, when the comparators output y is 1, the MOSCAP that is charged is the one attached to the negative end (N_{bot}), whereas, if y is 0, the MOSCAP that is charged is the one connected to the positive end (N_{top}). ϕ_1 is a clock signal which is set to 1 when the modulator is in the sampling phase. The working principle of the modulator will be further explained on chapter 3.5.2. with the respective waveforms.

3.4. Latched Comparator

The employed comparator is a StrongARM latch, which is a popular topology presenting zero static power consumption, producing directly rail-to-rail outputs and having an input-referred offset dominated by the differential pair [33]. This type of comparator consists of a clocked differential pair composed by transistors P_2 and P_3, two cross-coupled pairs (P_4, P_5 and N_4, N_5) and four switches (N_2, N_3, N_6 and N_7) which are connected to GND when the signal *reset* is set to 1. The outputs of the circuit V_{outp} and V_{outn} are rail-to-rail, changing according to the polarity of $V_{inp} - V_{inn}$ when *reset* is set to 0.

The implemented StrongARM latch comparator presented in Fig. 41 was optimized for low power following the procedure described in [34]. It was implemented with a PMOS differential pair as the input frequencies are relatively low (10 MHz), which also help to reduce the flicker noise.

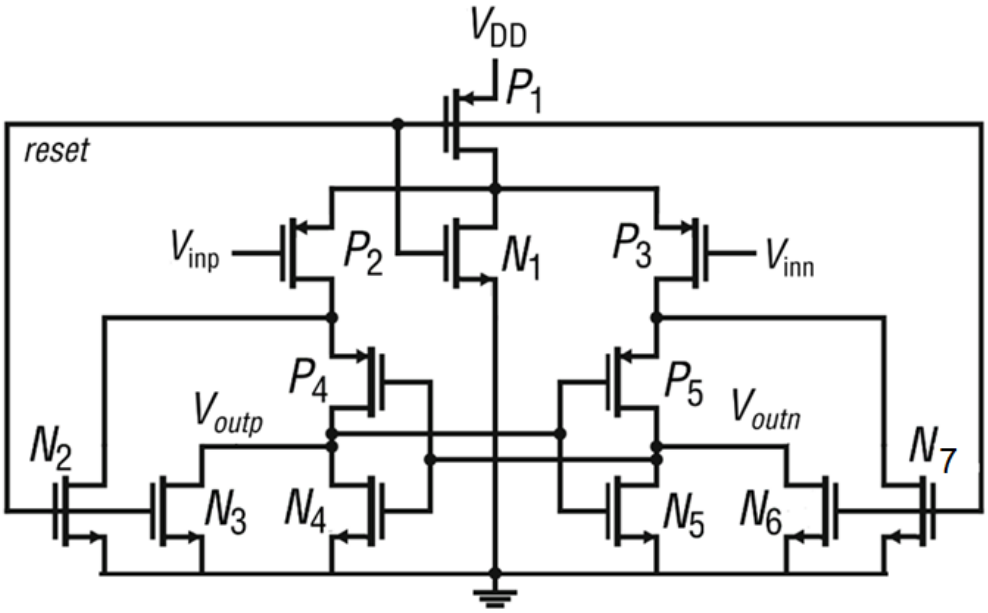


Fig. 41 – Strong Arm Latched Comparator with a PMOS differential pair.

3.5. Complete ΣΔ Modulator

3.5.1. Top-Level Circuit

Now that all the main parts of the passive ΣΔ modulator had been introduced and explained, this section presents the top-level architecture of the implemented modulator. Fig. 42 shows a simplified version of the circuit where all MOSCAPs are represented by symbols of conventional capacitors, and all the switches are represented with a generic symbol, for the sake of simplicity. However, it is important to emphasize that the capacitances in the circuit are not static and change according to the phase that is active.

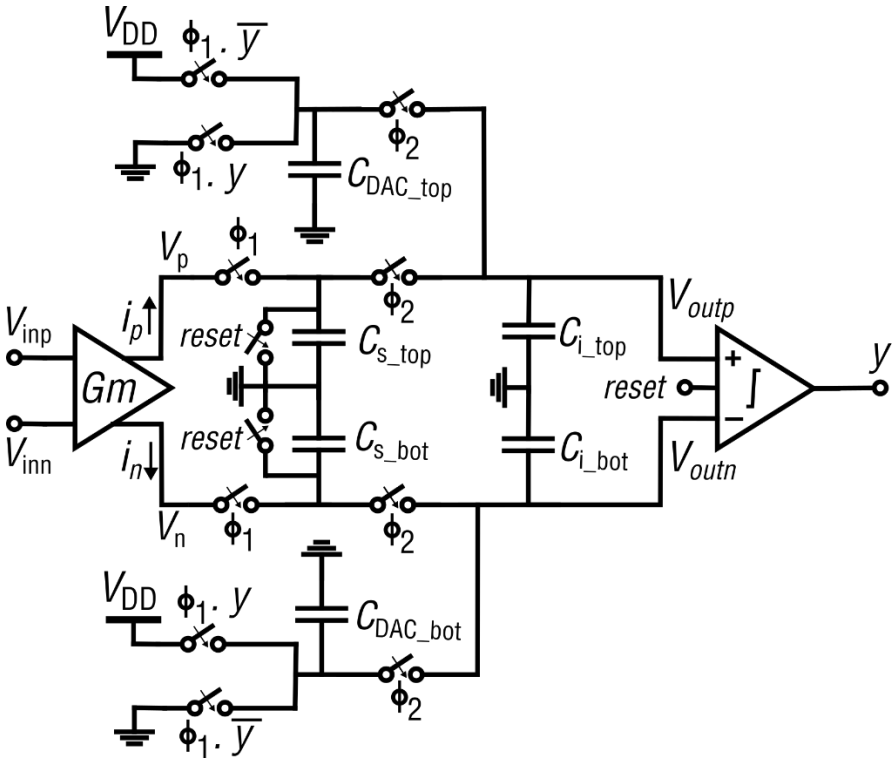


Fig. 42 – Top level schematic of the ΣΔ modulator (note: capacitors are implemented with MOSCAPs presenting a variable capacitance).

Examining the circuit, the absence of an operational amplifier stands out. Instead, a Gm cell is implemented with an inverting based circuit which transforms the input voltages into linear currents. The implemented modulator operates differentially presenting a symmetry between the positive and negative end. On the positive side, the signals have a denomination *p* and the MOSCAPs have the designation *top*. For the negative side, the signals have the designation *n* and the MOSCAPs the denomination *bot*. The circuit is composed by several MOSCAPs, a Gm cell, a latched comparator and different types of switches according to the node voltage and current. These switches are controlled by three non-overlapping clock signals, ϕ_1, ϕ_2 and *reset* which set the circuit into the sampling phase, the integration phase and the reset phase respectively. The different operating phases and the working principle of the circuit are explained in detail in the next section.

3.5.2. Working principle and Waveforms

The easiest and more efficient way of explaining the working principle of the passive ΣΔ modulator is by analyzing the waveforms of the circuit generated by the simulation tool. Therefore, in Fig. 43, the different waveforms of each signal of the modulator are represented.

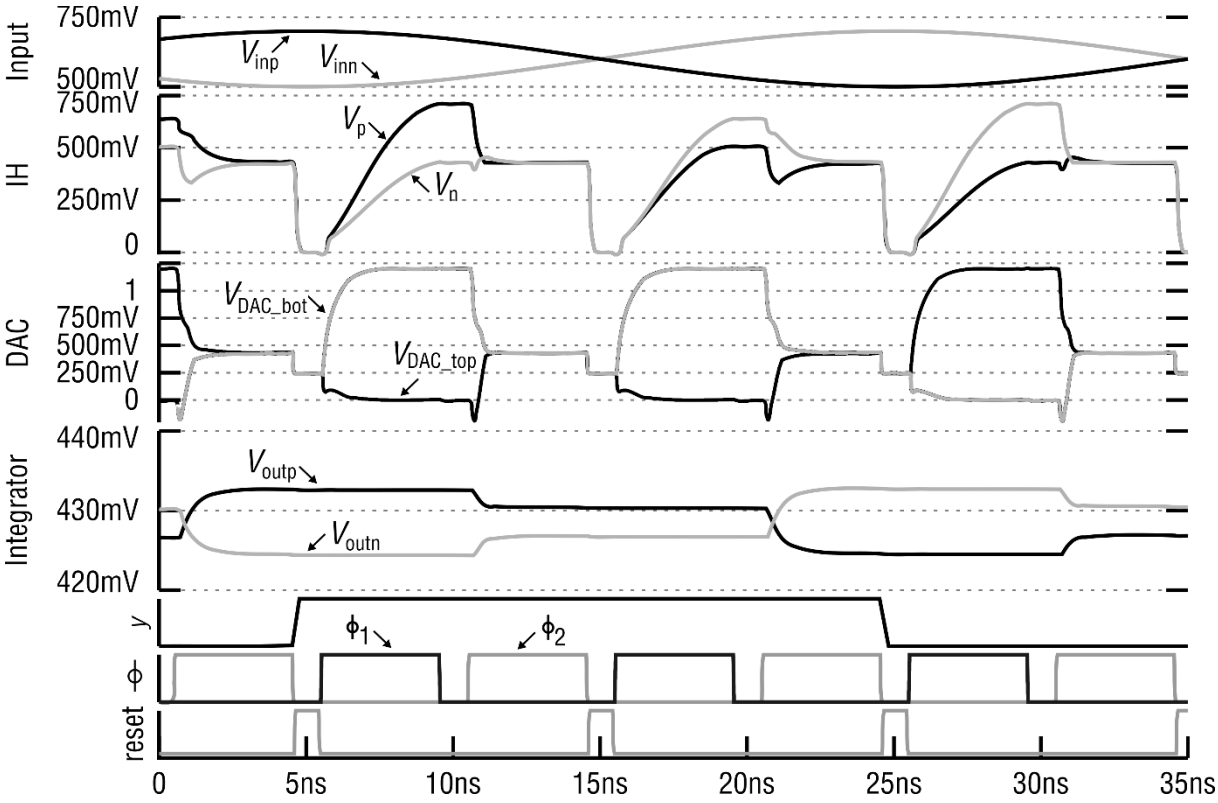


Fig. 43 – ΣΔ Modulator waveforms.

Three clock cycles are represented in the simulation, showing the circuit waveforms for three different input voltages. Taking as reference ϕ_1, on the first clock cycle, V_{inp} is greater than V_{inn}, on the second V_{inp} is slightly smaller than V_{inn}, and on the third cycle, V_{inp} is smaller than V_{inn}. Initially, the input voltages are converted into linear currents (i_p and i_n) with the Gm cell. The two currents are then transferred during ϕ_1 to the sampling MOSCAPs, C_{s_top} and C_{s_bot} respectively. A high linearity is needed in this conversion as it will affect the overall performance of the modulator. Inspecting the simulation results, for the first clock cycle, it can be clearly seen that the C_{s_top} is charged with a higher current than C_{s_bot}, as it presents a higher voltage at the end of the charge (V_p higher than V_n).

Following the signal path, the charge that is stored in the sampling capacitors is transferred to the integrating capacitors (C_{i_top} and C_{i_bot}) during ϕ_2, resulting in two output voltages V_{outp} and V_{outn}. These capacitors are designed to be at least 10 times larger than C_{s_top} and C_{s_bot} in order to reduce the charge leakage and to integrate the current over multiple cycles. Once the charge transfer is complete, the voltages at C_{i_top} and C_{i_bot} are measured by a latched comparator. Based on the result, represented in Fig. 43 by *y*, a feedback signal is generated, switching the bottom plates of the DAC to the positive or negative reference (supply voltage or ground respectively) as shown by V_{DAC_top} and V_{DAC_bot}. Examining the waveforms, for the first clock cycle, as V_{outp} is greater that V_{outn}, the output of the comparator is 1,

so V_{DAC_top} is set to 0 V and V_{DAC_bot} is set to 1.2 V in order to implement the negative feedback of the ΣΔM.

The charging of the DAC capacitors happens at the same time as the sampling process of the input signal (ϕ_1) so that during the integration phase, both charges are transferred to the integration MOSCAPs. At the end of each integration, the two voltage values across the integrating capacitors are measured by the comparator to generate a new result. Between each cycle, a reset signal is used to discharge the sampling capacitors completely and to activate the latched comparator. The resulting word from the comparator output is a digital conversion of the analog input signal.

3.5.3. Transfer Function

Considering that the input signal X is amplified by a factor a_1 and the feedback signal is amplified by factor b_1, the generic transfer function of the circuit is the following:

$$\frac{Y(z)}{X(z)} = \frac{a_1 z^{-1}}{1 - b_1 z^{-1}} \tag{48}$$

On a typical ΣΔ Modulator, a_1 and b_1 can be controlled by changing the gain on the input and at the DAC, which is achieved by the opamp gain and by the capacitance relation between the different capacitors. Although, for the implemented circuit, the input and feedback gain are controlled by the relation of capacitances between the input, DAC and integrating MOSCAPs. In order to find the gain expressions of the quasi-passive modulator, it is helpful to start with a simple integrating circuit composed by two linear capacitors, one to sample the signal (C_s), and the other to accumulate the charge over the sampling periods (C_i).

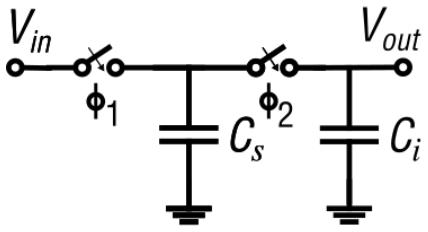


Fig. 44 – Passive integrator with linear capacitors.

Considering that at iteration $n-1$ the switch controlled by ϕ_1 is closed, and the capacitor C_s is charging, the charge at capacitor C_s is given by the input voltage times the capacitance of C_s, which leads to expression (49). It is also important to calculate the charge at C_i at iteration $n-1$ which can be expressed by (50).

$$Q_s(n-1) = C_s \times V_{in}(n-1) \tag{49}$$

$$Q_i(n-1) = C_i \times V_{out}(n-1) \tag{50}$$

During the next iteration (n), ϕ_1 is opened and ϕ_2 is closed, and the charge at the sampling capacitor is transferred to the integrating capacitor. Using first order charge redistribution analysis in ϕ_1 and ϕ_2, the charge at $Q_s(n)$ and $Q_i(n)$ is given by:

$$Q_s(n) = C_s \times V_{out}(n) \tag{51}$$

$$Q_i(n) = C_i \times V_{out}(n) \tag{52}$$

Considering that there are no loss of charge during ϕ_1 and ϕ_2, equation (53) relates the four expressions above.

$$Q_i(n) = Q_i(n-1) + Q_s(n-1) - Q_s(n) \tag{53}$$

To clarify the above result, equation (53) shows that the final stored charge in the integrating capacitor, $Q_i(n)$, is equal to the charge stored in the integrating capacitor during the last iteration $Q_i(n-1)$, plus the charge that was stored in the sampling capacitor $Q_s(n-1)$, minus the charge that is leaked to the sampling capacitor $Q_s(n)$.

Replacing equations (49)(50)(51)(52) in (53) the following result is obtained after some mathematical manipulation:

$$V_{out}(n) = \frac{C_i}{C_i + C_s} V_{out}(n-1) + \frac{C_s}{C_i + C_s} V_i(n-1) \tag{54}$$

Applying Z-transformation to (54), equation (55) is achieved.

$$V_{out}(z) = \frac{C_i}{C_i + C_s} V_{out}(z)\, z^{-1} + \frac{C_s}{C_i + C_s} V_i(z)\, z^{-1} \tag{55}$$

Finally, the transfer function of the passive integrator using linear capacitors is obtained.

$$H(z) = \frac{\frac{C_s}{C_i + C_s} z^{-1}}{1 - \frac{C_i}{C_i + C_s} z^{-1}} \tag{56}$$

For the complete circuit, considering that the ΣΔM presents feedback, DAC capacitors need to be considered as well. Maintaining the integration capacitor as C_i, as well as the sampling capacitor as C_s, and adding C_{DAC} as the feedback capacitor, the following circuit is obtained.

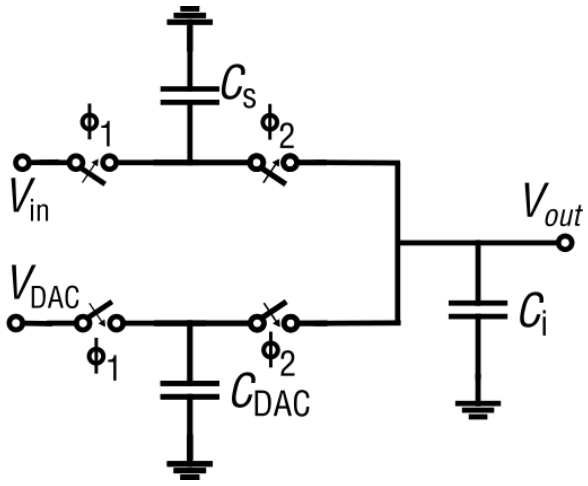


Fig. 45 – Passive integrator with a feedback capacitor.

It is important to note that the voltage charging the DAC capacitor (V_{DAC}) is dependent of V_{out} according to the following expression.

$$V_{DAC} = \begin{cases} 1.2\ V\ , V_{out} < 0 \\ 0\ V\ , V_{out} > 0 \end{cases} \tag{57}$$

The charge equations for Q_s and Q_i remain the same for $n-1$, and the charge for $Q_{DAC}(n-1)$ is expressed by (58).

$$Q_{DAC}(n-1) = C_{DAC} \times V_{DAC}(n-1) \tag{58}$$

For iteration *n*, the charge equations for Q_s and Q_i will also remain unchanged and the charge for $Q_{DAC}(n)$ is given by (59).

$$Q_{DAC}(n) = C_{DAC} \times V_{out}(n) \tag{59}$$

Considering that during the integration phase ϕ_2, part of the charge in C_{DAC} and C_s is transferred to C_i and the other part remains in the two capacitors, the equation that relates all the charges on the circuit during $n-1$ and n is given by (60).

$$Q_i(n) = Q_i(n-1) + Q_s(n-1) + Q_{DAC}(n-1) - Q_s(n) - Q_{DAC}(n) \tag{60}$$

Replacing (48)(49)(50)(51)(58)(59) in (60) and performing some mathematical manipulation to isolate the gains of each signal, the following expression is obtained.

$$V_{out}(n) = \frac{C_i}{C_i + C_s + C_{DAC}} V_{out}(n-1) + \frac{C_s}{C_i + C_s + C_{DAC}} V_i(n-1) + \frac{C_{DAC}}{C_i + C_s + C_{DAC}} V_{DAC}(n-1) \tag{61}$$

Making an analogy with the expression for a first order ΣΔM topology, and replacing the capacitances of the circuit according to the phase of the circuit, the gains a_1, b_1 and c_1 can be derived.

$$V_{out}(n) = c_1 V_{out}(n-1) + a_1 V_i(n-1) + b_1 V_{DAC}(n-1), \tag{62}$$

$$a_1 = \frac{C_s\,(\phi_1)}{C_i + C_s\,(\phi_2) + C_{DAC}\,(\phi_2)} \tag{63}$$

$$b_1 = \frac{C_{DAC}\,(\phi_1)}{C_i + C_s\,(\phi_2) + C_{DAC}\,(\phi_2)} \tag{64}$$

$$c_1 = \frac{C_i}{C_i + C_s(\phi_2) + C_{DAC}\,(\phi_2)} \tag{65}$$

Concluding, the gains that affect the modulator signals are strongly related to the size of the MOSCAPs used in the implementation. Inspecting the equations for the gains a_1, b_1 and c_1, it becomes evident that their values are less than unity if implemented with linear capacitors. Therefore, the importance of using MOSCAPs with a variable capacitance, which are controlled by the phase of the circuit (ϕ_1: sampling phase, ϕ_2: integrating phase). This characteristic allows to reduce charge leakage during integration and consequently improve the modulator linearity.

4. Circuit Design

Now that all the ΣΔ modulator parts were presented, this section targets the sizing of the different components, explaining the reasons behind each decision. Starting with the type of switch that was used to reduce the distortion, this chapter focuses mainly on the implementation. The I/H is sized as well as all the MOSCAPs and the comparator. Another important part of the dissertation is presented in this section where the method of measuring the charge transfer linearity is explained and implemented with a Verilog-A code.

4.1. Bootstrapped Switch

MOSFETs are the common device to implement switches, but they exhibit an input dependent on resistance, which introduces distortion. In ADCs, switches must be carefully designed according to the voltage that goes through their terminals to minimize the produced distortion. The most common types of switches are implemented with a NMOS or PMOS transistor and sometimes with both, which is called a transmission gate (TG). However, all of these switches present a strong input dependent on resistance, not being appropriate for every node of an ADC.

One way to solve the dependency between the input and the on resistance of MOSFETs is by "bootstrapping". This circuit technique minimizes the switch on resistance variation in the presence of large input and output voltage swings. The idea behind bootstrapping is to keep the V_{GS} of the transistor independent of the input voltage. This can be done with a capacitor tied between the gate and source of the switch, acting like a battery. With this arrangement, the gate and the source voltage change evenly, which minimizes the distortion introduced by the switch. The implemented circuit is represented in Fig. 46, where the switch N_3 is bootstrapped [35].

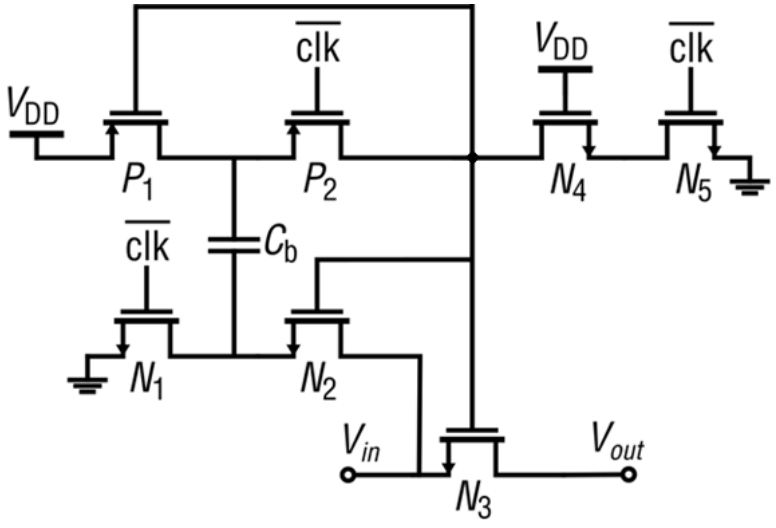


Fig. 46 – Bootstrapped Switch.

In order to implement the bootstrapping, seven switches and one capacitor C_b are used. The capacitor is charged to V_{DD} when the bootstrap switch N_3 is closed. During this phase, N_5 turns N_3 off, P_2 and N_2 are disconnected from C_b, and P_1 and N_1 charge the capacitor. After charging C_b to V_{DD}, the capacitor is bootstrapped to N_3 allowing the voltage on the gate to rise above V_{DD}, containing both the

pre-charge voltage and the input voltage V_{in}. N_4 is used to reduce the drain-source and drain-gate voltages experienced by N_5 to $V_{DD} - V_{th\_N_4}$.

With this bootstrapping topology, a high linearity and high-speed switch is achieved, being frequently used in ADCs. Performing several simulations to measure the linearity and speed of the switch, the transistors were sized with a minimum width of 160 nm and a minimum length of 120 nm. Both dimensions were chosen to minimize the area of the circuit and increase its speed. The capacitance of C_b was set to 20 fF, guaranteeing that for the used clock cycle, the stored charge is enough to maintain the switch bootstrapped. The simulations of the switch for the different dimensions are presented in section 5.1.

4.2. Integrator and Hold

The integrator and hold dimensioning is divided in three parts: Gm cell sizing, where all the transistors of the inverter based transconductor are sized; sampling MOSCAPs sizing, where the total capacitance and dimensions of the transistors are chosen; charge linearity measurement, where the implemented code for measuring the charge transfer is presented and explained.

4.2.1. Gm cell transistor sizing

The implemented circuit adapted from [30] to implement the Gm cell is presented in Fig. 47. To appropriately size the Gm cell and achieve a high linearity transconductor, seven variables must be taken into account. Considering that the circuit must be symmetric, transistors can be grouped into pairs: first pair P_1 and P_2, second pair P_3 and P_4, third pair P_5 and P_6, fourth pair N_1 and N_2, fifth pair N_3 and N_4 and finally sixth pair N_5 and N_6. Altogether, six transistors and one resistor must be sized. Both PMOS and NMOS are implemented with a channel length of 500 nm for high output impedance and low 1/f noise. This length does not generate non-quasi-static (NQS) effects for input signals with frequencies within a few MHz [30].

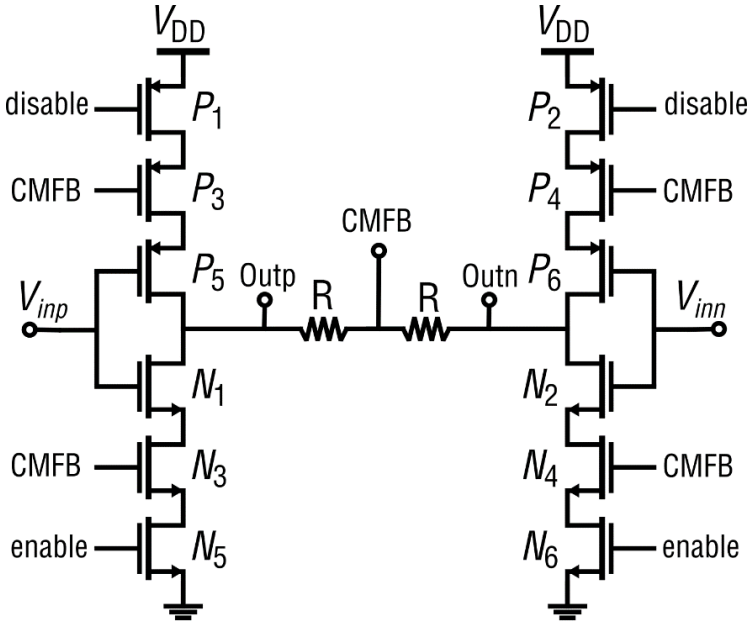


Fig. 47 – Gm cell circuit.

The reasoning used for the circuit sizing is straightforward, avoiding complicated small-signal expressions whenever possible. This proved to be a good choice because the circuit behavior is greatly dependent on the large-signal behavior of the transistors. The transistors connected to the “disable” and “enable” signals are used to turn off the Gm cell, while also limiting the current flowing through the branch. Increasing the PMOS width increases the branch current, which results in an increase to the current going to the output of the cell. Increasing the NMOS width increases the current flowing to GND, which reduces the cell transconductance. For this reason, the first pair of PMOS transistors (P_1 and P_2) has a width of 2 µm and the sixth pair of NMOS transistors (N_5 and N_6) has a width of 250 nm.

The MOSFETs connected to CMFB (P_3, P_4 and N_3, N_4) sense the output common-mode voltage, stabilizing the output common-mode voltage. These transistors are biased in the triode region and work together with two sensing resistances. As the width of the transistors increases, the cell becomes more sensitive to the output common-mode voltage. By reducing the resistance of *R*, the sensitivity is also increased although charge leakage also increases. The two sensing resistances are chosen as 50 kΩ to avoid charge leakage. The transistors from the second pair (P_3 and P_4) are implemented with a width of 2 µm, and the transistors of the fifth pair (N_3 and N_4) with a width of 500 nm to implement a moderate common-mode feedback and enhance the linearity of the cell.

The transistors from the third and fourth pair (P_5, P_6 and N_1, N_2 respectively) are connected to the input signal acting as an inverter based transconductor. By increasing transistors width, the Gm cell output becomes more dependent on the input signal, which improves the circuit linearity. With this aspect in mind, the chosen width for the transistors must be larger compared to the others. The third pair with PMOS transistors has a width of 5 µm, and the fourth pair with NMOS transistors has a width of 2 µm. Table 3 summarizes the circuit design.

Table 3 – Gm cell transistor sizes.

Transistor	**Width** (μm)	**Length** (μm)
P_1 / P_2	2	0.5
P_3 / P_4	2	0.5
P_5 / P_6	5	0.5
N_1 / N_2	2	0.5
N_3 / N_4	0.5	0.5
N_5 / N_6	0.25	0.5

To estimate the transconductance of the resulting Gm cell, a DC analysis is performed to measure the transistors gm. For this analysis the important transistors are the ones that implement the inverting circuit, presenting the dominant impact on the transconductance of the Gm cell. Using expression (38) to calculate the transconductance of an inverting circuit and applying it to a double ended circuit, the estimated transconductance is 37 µS. It is important to mention that this value is estimated with a small signal model and, as stated before, the Gm cell is especially dependent of large signals. For this reason, a more accurate method to measure the Gm cell transconductance must be performed using both the transferred charge, the sampling time, and the input voltage. This calculation

is presented in section 5.3 of the results, after being explained the method of measuring the transferred charge to the MOSCAPs.

4.2.2. Sampling MOSCAPs

Although the sampling MOSCAPs are simply implemented in a complementary topology with few parameters, they strongly affect the overall linearity of the I/H. As already demonstrated with equations (46) and (47), the common mode voltage and the differential voltage at the output of the Gm cell is dependent on the sampling MOSCAPs. With the objectives of the I/H in mind, the main target is to maximize its linearity, by assuring a $V_{CM_{out}}$ above 0.5 V (to bias the MOSCAPs on the high capacitance region) and by achieving a high $V_{dif_{out}}$ (to maximize the dynamic range inside the ADC and hence its resolution).

The two restrictions to the design are the following: the lowest capacitance of the MOSCAPs is imposed by keeping the I/H working in current mode, and the highest capacitance is imposed by $V_{CM_{out}}$ which needs to be above 0.5 V. The MOSCAPs width is set to the minimum value for this technology (160 nm) in order to achieve a low W/L ratio, which according to [28] enhances the difference of capacitance presented by the MOSCAPs for the two working regions. Inspecting Fig. 48, it can be clearly seen that low W/L ratios increase the difference of capacitance between the inversion and depletion region. These simulation results are especially helpful as the target of using MOSCAPs is to sample the signal on the high capacitance region and discharge at the low capacitance region, reducing the leaked charge during integration.

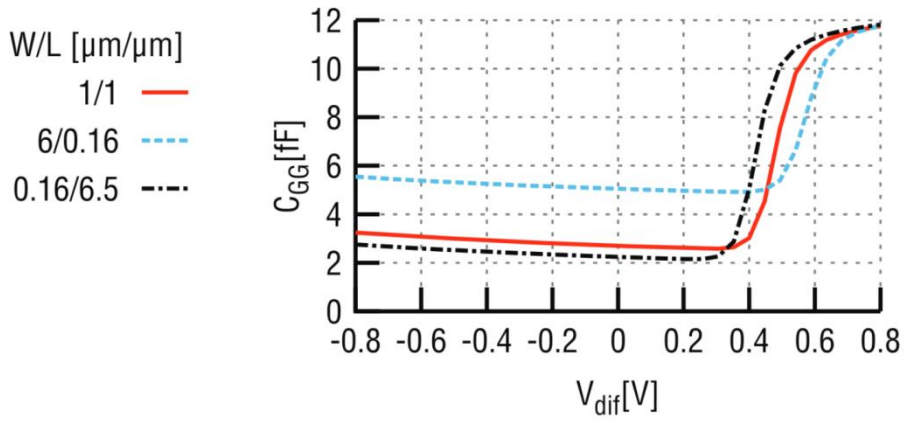


Fig. 48 – MOSCAP C(V) curve for three different W/L ratios, with the same area. [28]

With *W* set to 160 nm, two other parameters still need to be scaled: the length of the transistors, *L*, and the number of MOSCAPs placed in parallel, *m*. To implement a low W/L ratio and accomplish a layout with a small area, *L* was set to 12 µm. Multiplying W for L, the obtained area is 1.92 µm^2, which translates on an approximate maximum capacitance of 22.5 fF according to (32) and supported by the simulation results of Fig. 48.

The parameter *m* plays an essential role in the sizing of the sampling MOSCAPs. As it is important to have the lowest *W*, the area of the transistors is small, which results in a MOSCAP with low capacitance. The parameter *m* allows to increase the capacitance of the sampling MOSCAPs by connecting several in parallel. Simulating the charge transfer at the I/H and experimenting different

values, *m* is set to 12. This value allows to achieve a $V_{CM_{out}}$ of approximately 0.58 V, a $V_{dif_{out}}$ of 0.63 V and an ENOB of 12.07 bit. Choosing the value for *m* is a trade-off between these three results, which lead to a sampling MOSCAPs bank of 270 fF. Next section explains how the charge linearity is measured and how the 12.07 bit of ENOB is obtained.

Table 4 – I/H sampling MOSCAPs parameters.

Parameter	Value
W	160 nm
L	12 µm
m	12
Total Capacitance (C_s)	270 fF

4.2.3. Linearity Measurement

To the best of the author´s knowledge, a technique to measure the linearity in charge domain is not available in the literature. In this project, charge-domain linearity is an important part of the ΣΔ modulator design. Measuring the charge transfer linearity allows the dimensioning of the I/H as a separate part of the modulator, which translates in lower simulation times and intermediate results. The transferred charge can be calculated by two equations, $Q = C \times V$ and $Q = \int_o^t i\, dt$. In the I/H, as the sampling capacitor is implemented with MOSCAPs, their capacitance varies with the biasing, thus measuring the voltage to calculate the charge would not lead to accurate results. For this reason, the most promising way of determining the charge that is transferred to the MOSCAPs is by measuring the current and integrating it during the period that the I/H is sampling the signal. For this purpose, a new Verilog-A block was created to implement a data saver in charge domain.

Fig. 49 presents a section of the implemented code, being the complete version presented at appendix A. The implemented code measures two different variables, the input voltage and the current flowing through the two terminals. As the charge is expressed by the integral of the current, it is possible to calculate the charge produced by the Gm cell measuring the transferred current to the sampling MOSCAPs during the sampling phase. The code has three inputs and two outputs. The inputs are *inn*, *inp* and *sample*. *inn* and *inp* are connected to the output of the Gm Cell, and the *sample* receives a clock signal that activates the measuring and writing of the data in a file. The outputs are *outn* and *outp* which are connected to the sampling MOSCAPs. The voltage across *inn* and *inp* is measured and saved in a file and the current flowing through *inp* to *outp,* and through *inn* to *outn* is integrated to calculate *charge_p* and *charge_n.* To calculate the total charge for the double ended circuit, *charge_n* is subtracted to *charge_p*. Then, to obtain the amount of charge that is produced in the cycle, a variable named *prev_charge* containing the previous charge is subtracted. The result, containing the charge that was produced in the cycle, is saved on a file together with the instant of time when the charge transfer occurred. With this information, it is possible to measure the I/H linearity with ENOB, SNDR and THD.

```
analog
  begin

     @(cross( (V(clk)-threshold) , +1))
        begin
          $fwrite(file_q, "%0.18f, %0.18f\n",$abstime, charge - prev_charge);
          $fclose(file_q);
          prev_charge = charge;
        end

   @(cross( (V(clk)-threshold) ,-1))
       begin
          $fwrite(file_v, "%0.18f, %0.9f\n",$abstime, V(inp, inn));
          $fclose(file_v);
       end

     V(inp,outp) <+ 0.0 ;
     V(inn,outn) <+ 0.0 ;

     charge_p = idt(I(inp, outp), 0);
     charge_n = idt(I(inn, outn), 0);

     charge = charge_p - charge_n;
 end
```

Fig. 49 – Section of the implemented code to measure the charge transfer linearity.

In order to validate the code, a simple schematic was created where the Gm cell output was connected directly to two ideal resistors with 1 mΩ instead of MOSCAPs with variable capacitance. With this circuit and measuring the voltage drop between each side of the resistor, it is possible to calculate the amount of current that the Gm cell is generating to each output. Using a Periodically Steady-State (PSS) analysis in the *Cadence Spectre* and calculating the THD, the result can be compared to the achieved with the data saver. A difference of approximately 0.064 dB was obtained, which approves the correct implementation of the code. This experiment is explained with more detail in the simulation section 5.2.

4.3. DAC MOSCAPs

The DAC MOSCAPs use the same complementary topology as the sampling MOSCAPs. Nevertheless, instead of being charged with an input current, they are connected to V_{DD} or GND according to the comparator output. From equation (59), that presents the modulator transfer function, the gain at the input a_1 is multiplied by the input voltage. Similarly, the gain at the DAC b_1 is multiplied by the DAC voltage. Considering that the DAC voltage is much larger than the input voltage, the capacitance of DAC MOSCAPs (C_{DAC}) must be considerably smaller than C_s in order to avoid modulator saturation. Another important aspect is the fact that the sampling MOSCAPs are charged with a limited current, imposed by the transconductance of the Gm cell and by the sampling time. However, for the DAC MOSCAPs, the charge is transferred much faster as they are connected to V_{DD} or GND.

To size the DAC MOSCAPs, it is still important to reduce the charge leakage during integration, therefore W is set to the minimum value of the technology, 160 nm. Measuring the charge that is

transferred to the sampling MOSCAPs with the implemented code, it is possible to determine the values of charge that are stored in the MOSCAPs during each iteration. The results present a maximum charge of around 18.20 fC which are obtained when the modulator input voltage is at the maximum value. As already explained in the theorical results, the gains on a 1st order ΣΔ modulator must be similar for the input and DAC signal. Translating this principle to a charge-based ΣΔM is equivalent to dimensioning the DAC MOSCAPs to hold a charge similar to the sampling MOSCAPs.

Using the simple equation $Q = C \times V$, an estimation of the DAC capacitance can be obtained in order to size the length and the parameter *m* of the DAC MOSCAPs. Considering a charge of 18.20 fC and a voltage of 1.2 V, the estimated capacitance is 15.17 fF which can be implemented with a MOSCAP area of 1.30 μm^2. The length of the transistors, L, after several iterations to maximize the ENOB of the modulator, was set to 4.3 μm with m = 2, which corresponds to 16.1 fF of maximum capacitance. By charging the DAC MOSCAPs with 1.2 V, the resulting charge is 19.31 fC which as predicted is similar to the charge that is stored on the sampling MOSCAPs. Table 5 summarizes the chosen values for the DAC MOSCAPs.

Table 5 – DAC MOSCAPs parameters.

Parameter	Value
W	160 nm
L	4.3 μm
M	2
Total Capacitance (C_s)	16.1 fF

4.4. Integrating MOSCAPs

The remaining capacitances that need to be dimensioned are the integrating MOSCAPs. There is a strong correlation between the leaked charge at the sampling and DAC MOSCAPs, and the capacitance of the integrating MOSCAPs. To reduce the charge that is lost while disconnecting C_s and C_{DAC} from C_i, the relationship C_s/C_i and C_{DAC}/C_i must be reduced. The use of MOSCAPs in C_s and C_{DAC} already helps in this task. Nevertheless, the capacitance relationship can be further decreased by implementing C_i with a capacitance significantly larger than C_s and C_{DAC}.

Two restrictions impose the maximum capacitance of the integration MOSCAPs: the first one is the input-referred noise of the latched comparator, if C_i is implemented with a large capacitor the resulting voltage from integration gets smaller than the comparator noise, which causes measurement errors and affects the performance of the modulator. The second one is the size, as this new topology presents the advantage of having a small area, it is important to size C_i with a good trade-off between area and resolution.

Simulating the complete ΣΔ modulator and measuring its performance, two possible sizes for C_i are obtained: one to maximize the resolution, and other with the trade-off between area and resolution. Maximizing the resolution, the chosen capacitance for the integration MOSCAPs is 4.61 pF. For a good trade-off between resolution and area, C_i is set to 3.74 pF. For the first implementation an ENOB of 8.23 bits is obtained while for second one, an ENOB of 8.01 bits is achieved. To size C_i, several

simulations were performed with different capacitances. The resulting ENOB of each simulation is presented in section 5.4.

4.5. Latched Comparator

For the implemented ΣΔ modulator, the comparator is designed to operate with a clock frequency of 100 MHz presenting an input-referred noise of approximately 0.1 mV. The StrongARM latch comparator was reused from a previous design that had slightly more demanding specifications. For this reason, the power efficiency of the current implementation has room for improvements with a custom-tailored comparator. Considering the scheme presented in Fig. 41, Table 6 presents the different transistor sizes.

Table 6 – StrongARM latch comparator transistor sizes.

Transistor	**Width** (μm)	**Length** (μm)
P_1	2.5	0.12
P_2 / P_3	12	0.12
P_4 / P_5	6.24	0.12
N_1	0.96	0.12
N_2 / N_3 / N_6 / N_7	0.96	0.12
N_4 / N_5	1.11	0.12

4.6. Complete ΣΔ Modulator Circuit

Now that all the different components of the ΣΔ modulator had been presented and dimensioned, in this section they will be connected all together to implement the ΣΔM circuit presented in Fig. 50. The schematic implemented in *Cadence Virtuoso* and used for simulation is also presented in this document at appendix B.

Starting from the left side of the circuit, two wave generators are used. The first one represents the input signal which for performing the FFT is chosen to be a sinusoid with 200 mV. The second one is the common mode voltage that is set to 0.6 V which is half of the supply voltage. Both signals are fed into a balun transforming the signals from unbalanced to balanced in order to be used in a double ended circuit. The two generated signals (V_{inp} and V_{inn}) with a common mode voltage of 0.6 V and a differential voltage of 200 mV are placed at the input of the Gm cell. In the Gm cell, the inverter-based circuit with an approximately linear transconductance transforms the two input voltage signals into linear currents. During the sampling phase, these currents are transferred to the sampling MOSCAPs carrying the input signal information in the charge domain. At the same phase, the DAC MOSCAPs are charged to V_{DD} or GND according to the comparator output of the last iteration implementing the feedback loop of the ΣΔM.

During the integration phase, both charges at the sampling MOSCAPs and at the DAC MOSCAPs are transferred to the integrating MOSCAPs. The resulting voltages at the integrating

MOSCAPs (V_{outp} and V_{outn}) are measured by a StrongARM latched comparator controlled by the clock signal r*eset*, and a new output and feedback signal is obtained (y).

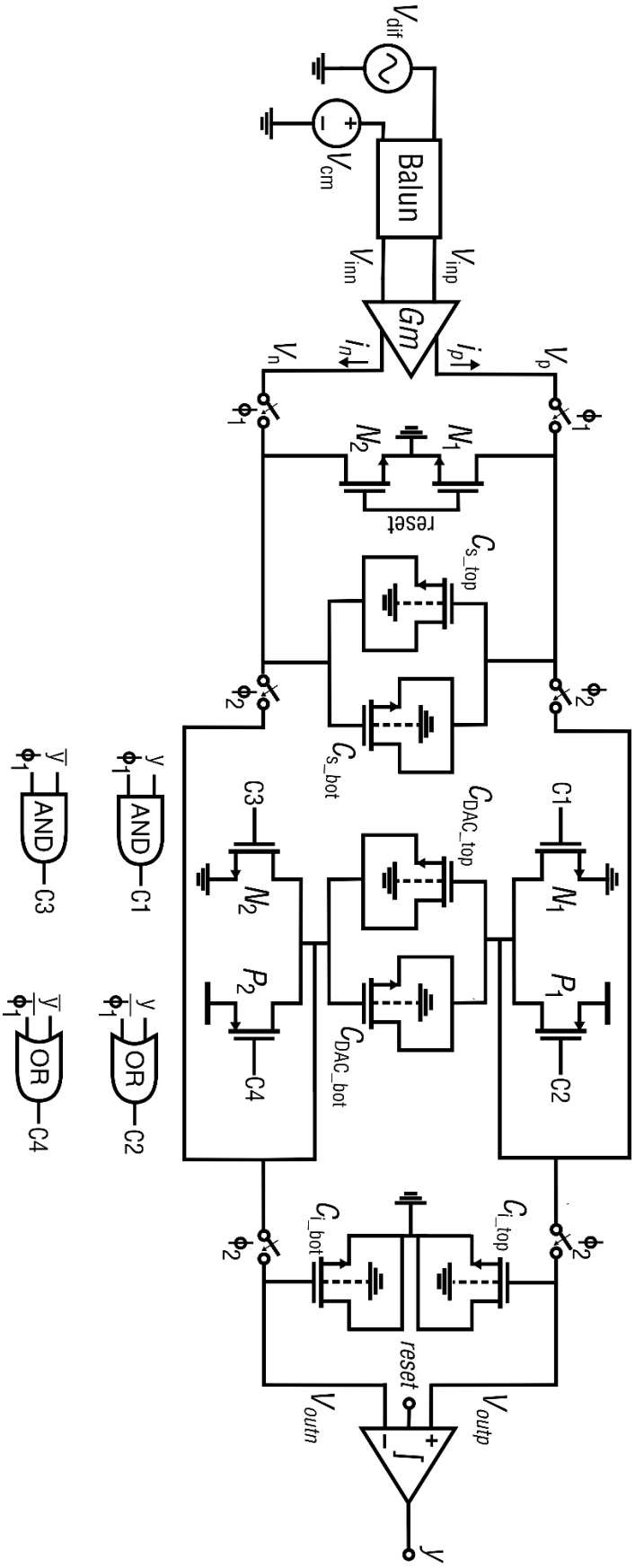


Fig. 50 – Complete ΣΔ Modulator.

5. Simulations and Results

In this section, the intermediate and final results of the ΣΔ modulator are presented, as well as the results of other circuit components such as the bootstrap switch and the charge data saver block. The time response of the bootstrap switch is tested for different transistor sizes in order to choose the fastest one. Implementing the modulator with fast switches is very important in a ΣΔ as the sampling frequency is several times higher than the frequency of the input signal. A simulation to test the accuracy of the charge data saver and the code to calculate the linearity of the charge transfer is also performed in this section. The resulting THD calculated with the implemented code is compared with the THD measured by C*adence Spectre* in order to validate the proposed method of measuring the charge transfer linearity.

Intermediate results of the ΣΔ modulator are presented, where the linearity of the I/H is measured, in order to approve the correct working function of the Gm cell, and the correct sizing of the sampling MOSCAPs. The resulting common-mode voltage and differential voltage at the sampling MOSCAPs are also presented, being accordingly to the project objectives. Finally, the results of the complete ΣΔ modulator are presented. Various linearity measurements are performed with ENOB, THD, SNR, and SNDR. An estimation of the circuit area and power consumption is also presented.

5.1. Bootstrap Switch

With the bootstrapping topology, a high linearity and high-speed switch is achieved. By performing several simulations to measure the linearity and speed of the switch, the transistors are sized with a minimum width of 160 nm and a minimum length of 120 nm. Both dimensions are chosen for minimizing the area of the circuit and increase its speed.

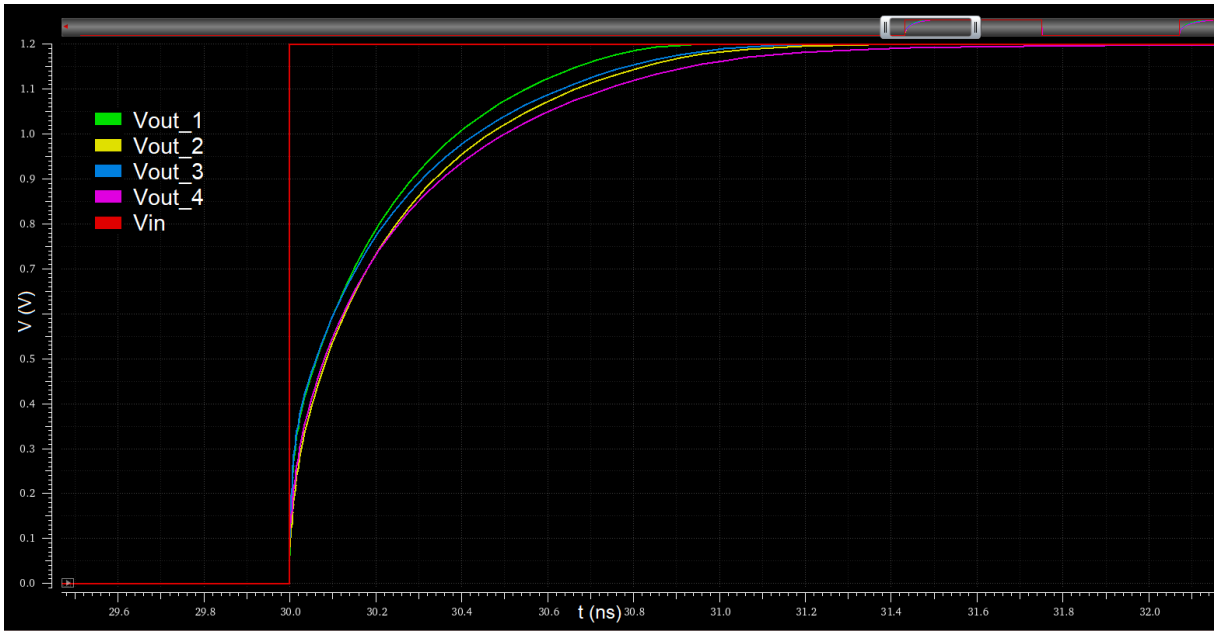


Fig. 51 – Bootstrap Switch simulation results.

In Fig. 51 it is presented the simulation results for different sizes of the bootstrapped switch. As expected, the smaller the dimensions of the transistor implementing the switch, the faster the response. The result of the implemented switch and the one that was used in the modulator is represented with the green line, presenting a rise time of approximately 0.9 ns which is less than 1/10 of the clock period. The blue line (Vout_3) corresponds to a switch with W = 300 nm and L = 120 nm which allows to flow more current, with a consequent decrease in speed in comparison with minimum W. The yellow line (Vout_2) corresponds to W = 160 nm and L = 240 nm, and the purple line (Vout_4) to W = 300 nm and L = 240 nm, both presenting a worse performance in speed when compared to the implemented switch with minimum dimensions. For the fall time, all the switches presented approximately the same response, changing from V_{DD} to GND almost immediately (0.01 ns), which is a characteristic of the used bootstrapped topology. With the bootstrap switch dimensioned for high speed, the time between the non-overlapping clocks can be small (1 ns) which helps to increase the modulator sampling frequency.

5.2. Charge Data Saver

In order to validate the correct working principle of the implemented Verilog-A block, a simple experiment with the schematic presented in Fig. 52 was performed. The sampling MOSCAPs were replaced for ideal resistors with a well-defined resistance of 1 mΩ. With this arrangement the current flowing through the data saver is the same as the one flowing through the resistors, and it can be calculated measuring the voltage drop at resistors R. Performing a PSS analysis in *Cadence Spectre,* the THD of the current flowing through the resistors can be calculated and compared to the one obtained with the data saver after computing the FFT.

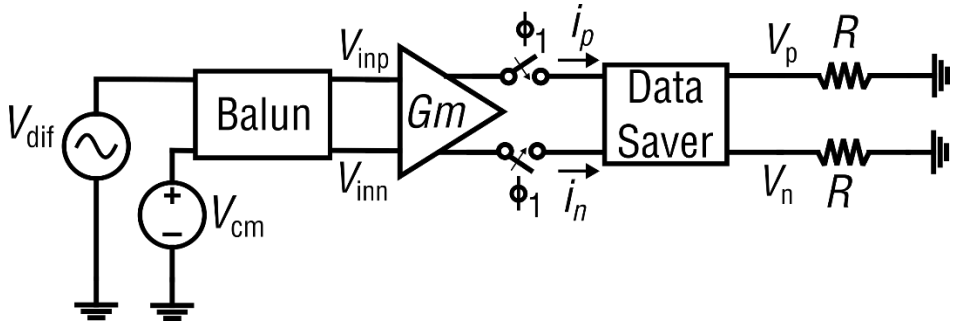


Fig. 52 – Charge data saver testing.

A transient analysis was performed to acquire 128 points with the data saver. In order to perform coherent sampling, the frequency of the input signal was set to 781.25 kHz for a sampling frequency (used to commute ϕ_1) of 10 MHz. Processing the 128 points of the data saver and computing the FFT, the resulting THD was 53.164 dB while on *Cadence Spectre* the result was 53.210 dB, resulting in a difference of only 0.046 dB. This result gives some certain and support to the correct working principle of the implemented code, turning the data saver into a useful tool for future works where it is important to measure the linearity of charge transfer.

5.3. I/H Results

As the I/H strongly affects the ΣΔM linearity, this section presents the intermediate results of the I/H showing the waveforms and the important results used to dimension the Gm cell and the sampling MOSCAPs. The results of the I/H were achieved with two tools. The first one, was the circuit simulation program *Cadence*, and the second one with the data saver and computing the resulting FFT to calculate the linearity of the charge transfer.

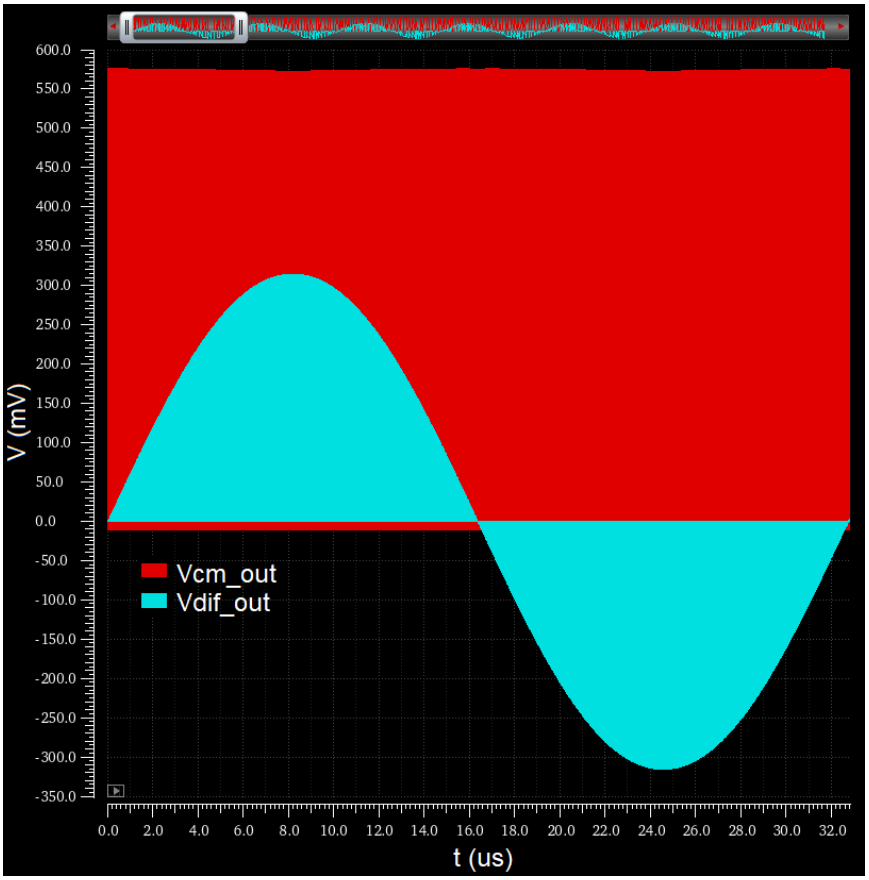


Fig. 53 – Common mode and differential voltage at the Gm cell output (V_{CM_out} and V_{dif_out})

Fig. 53 presents the common mode voltage and differential voltage at the output of the Gm cell. V_{CM_out} is stable at about 575 mV allowing to bias the MOSCAPs on the high capacitance region, and V_{dif_out} presents a peak-to-peak voltage of 630 mV, resulting in a wide dynamic range inside the ADC. Notice from V_{dif_out} waveform that the circuit is working in current mode, which means that the voltage at the sampling MOSCAPs does not saturate when the current is maximum. For instance, if the capacitance of the sampling MOSCAPs were smaller, V_{CM_out} and V_{dif_out} would increase which is a positive change as the I/H objectives are to maximize V_{dif_out} and to accomplish a V_{CM_out} above 500 mV. However, this would lead to the saturation of the sampling MOSCAPs, and the waveform V_{dif_out} would saturate for the higher values affecting the I/H linearity.

With the data acquired by the data saver it is possible to estimate the Gm cell transconductance based on the charge that was transferred to the MOSCAPs. From equation (42), the Gm cell transconductance can be expressed by (66).

$$gm = \frac{Q}{V_{in} \times T_s} \tag{66}$$

As the input voltage and the sampling time are two known variables, gm can be obtained. Considering that the maximum charge transferred to the sampling MOSCAPs is 18.20 fF, for an input voltage of 200 mV and a sampling time of 4 ns, the estimated transconductance is 22.8 µS.

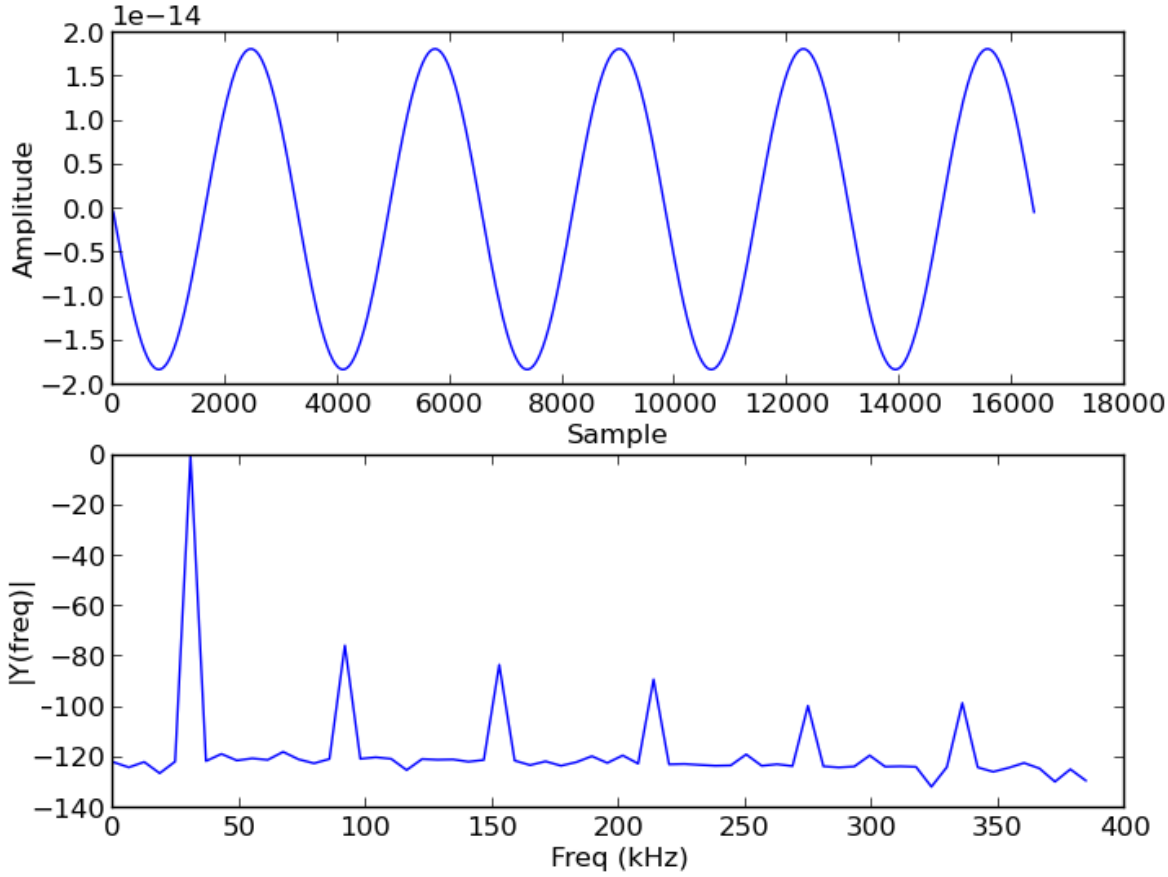


Fig. 54 – Spectrum of the charge transfer.

The sinusoid wave at Fig. 54 represents the charge transferred to the sampling MOSCAPs presenting an identical waveform to the input voltage of the modulator. Computing the FFT of the resulting sinusoid, the parameters that translate the linearity of the I/H can be calculated. The resulting FFT for the integrator and hold is presented also presented in Fig. 54. The FFT was calculate with 16384 points, a sampling frequency of 100 MHz and an input voltage of 200 mV with a frequency of approximately 30.5176 kHz which was chosen to perform coherent sampling. With the above spectrum, an ENOB of 12.07 bit was achieved, with an SNDR of 74.433 dB and a THD of 74.43 dB.

These results support the correct working principle of transforming the input voltage into a linear current with a quasi-passive transconductor, transferring the information in charge domain to the MOSCAPs. Other combinations of transistor sizes could be used to obtain the same results, although the accomplished ones fulfill the project requirements.

5.4. ΣΔ Modulator Results

In order to test the implemented ΣΔ modulator and measure its performance, a sine wave with a differential voltage of 200 mV and approximately 21.3623 kHz frequency was placed at the input. Given that the modulator sampling frequency is 100 MHz, and acquiring 32768 points to calculate the FFT, the chosen input frequency allows to perform a coherent sampling, avoiding the use of special windows and having in consideration the number of harmonics. To export the results of the modulator, a Verilog-A block was created to measure the output of the comparator and save the data in a file. After completing the simulation, the generated file containing the information of the input signal in discrete values is processed to compute the FFT and calculate various parameters, namely the ENOB, THD, SNR and SNDR.

As shown by the mathematical expressions of the modulator gains, implementing C_i with a capacitance several times larger than C_s and C_{DAC} reduces the leaked charge during the passive integration. In order to study the influence of C_i in the overall circuit linearity, several simulations were performed with different transistor sizes. The results are summarized in Table 7.

Table 7 – ΣΔ Modulator results for different integrating capacitors

Transistor Size	**C_i Capacitance**	**ENOB @ OSR 64**	**ENOB @ OSR 128**
W = *L* = 21 µm	5.09 pF	7.547	7.913
W = *L* = 20 µm	4.61 pF	7.755	8.232
W = *L* = 18 µm	3.74 pF	7.401	8.009
W = *L* = 16 µm	2.95 pF	6.938	7.553
W = *L* = 10 µm	1.16 pF	6.106	6.879

Inspecting Table 7 it is clear that the capacitance of C_i has a big impact on the results of the ΣΔ modulator. For a small integrating capacitor with 1.16 pF, the achieved ENOB for an OSR of 128 is just 6.88 bits. Although, increasing the size of the integrating capacitors, the resolution also increases presenting a maximum ENOB of 8.23 bits for an OSR of 128. This result is achieved by implementing the integrating MOSCAPs with a capacitance of 4.61 pF. For higher capacitances, besides the area getting larger, the ENOB is also affected, as the voltages across the integrating capacitors start to get smaller than the comparator noise, which causes errors at the output of the comparator and affects the conversion.

With the results of Table 7, two possible sizes for C_i can be chosen to implement the ΣΔ modulator: one to maximize the performance, and the other to achieve a tradeoff between area and resolution. For the first case, C_i is implemented with a capacitance of 4.61 pF. For the second case, C_i is implemented with a capacitance of 3.74 pF, which corresponds to an ENOB of 8.01 bits and an area 23% smaller when compared to the first implementation. The resulting FFT for the first implementation is presented in Fig. 55 with a logarithmic scale and with an oversampling ratio equal to 1, and in Fig. 56 with an OSR of 128 in a linear scale.

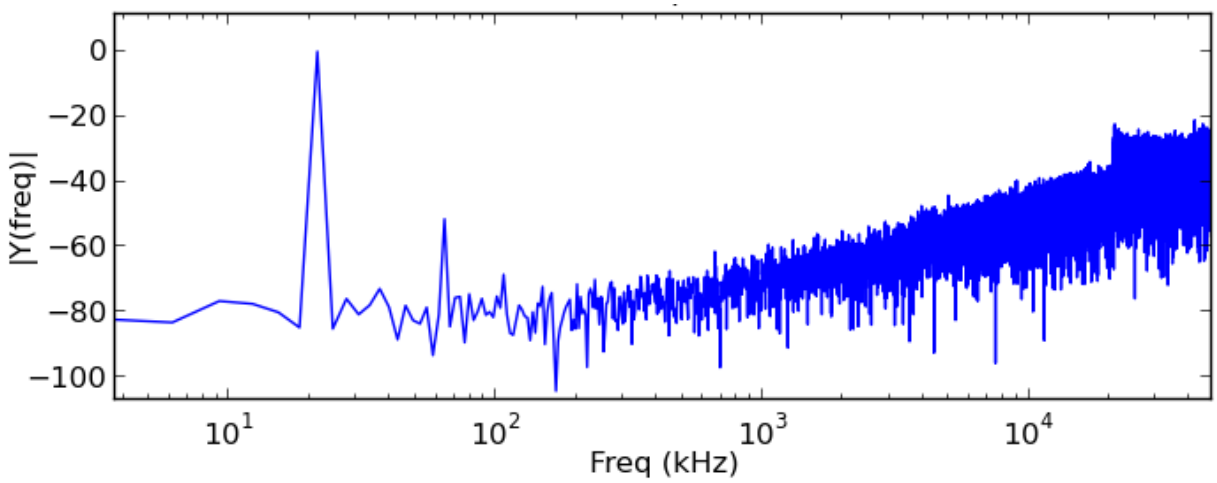


Fig. 55 – ΣΔ Modulator FFT without oversampling ratio.

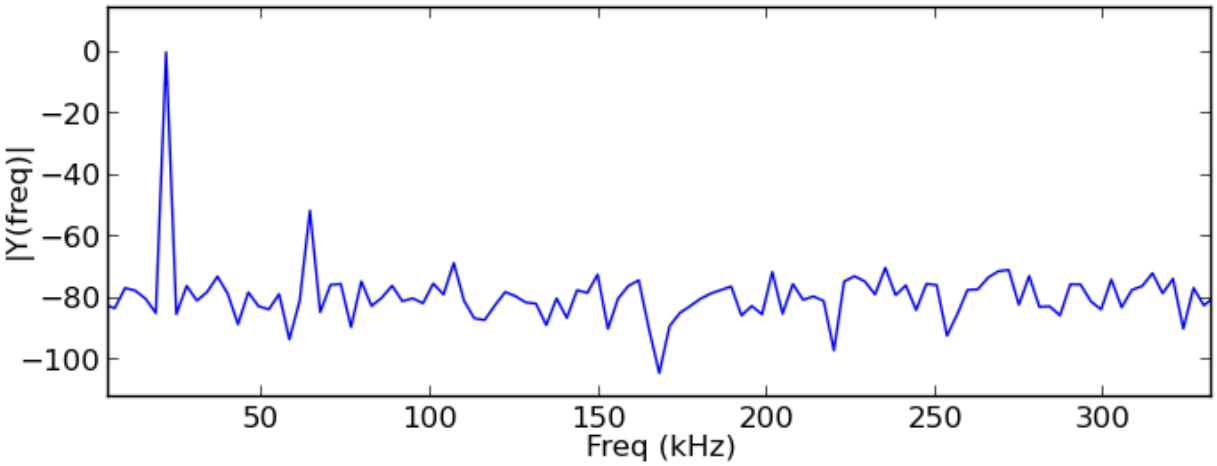


Fig. 56 – ΣΔ Modulator FFT with OSR = 128.

Starting with Fig. 55 where it is presented the computed FFT with a logarithmic scale, the effect of the first order loop is noticeable. The quantization error is filtered at low frequencies increasing approximately 20 dB/dec. A high amplitude is obtained for 21.36 kHz which corresponds to the input signal frequency. Several other peaks can also be visualized in the plot corresponding to the signal harmonics, being the third harmonic at 64.08 kHz the most noticeable.

For Fig. 56, an OSR of 128 is used, which allows to calculate the linearity parameters and to visualize with more detail the frequencies of interest. An SNDR of 51.34 dB is obtained, which corresponds to an 8.23 bit ENOB. In terms of power, an average consumption of 0.08 mW is obtained.

5.5. Estimated Circuit Area

In order to have an estimation of the total circuit area, the several components of the ΣΔ modulator were instantiated in a layout. As expected, the area of the circuit is especially influenced by the integration MOSCAPs, by the sampling MOSCAPs, and by the comparator. In Fig. 57 is represented a simplified 3D view of the implemented circuit where the areas of the most important components are presented with subtitles. Notice that both DAC and sampling MOSCAPs are implemented with a very short width in order to enlarge the difference of capacitance between the two working regions of the

transistors. The integration MOSCAPs occupies a large area of the circuit, which is mandatory in this passive topology as the charge leakage is directly related to the capacity of the integration MOSCAPs.

An estimated area of 40×60 μm^2 was achieved which, considering that the circuit were implemented in 130 nm CMOS technology, is a size considerably smaller when compared to conventional ΣΔ modulators with opamps.

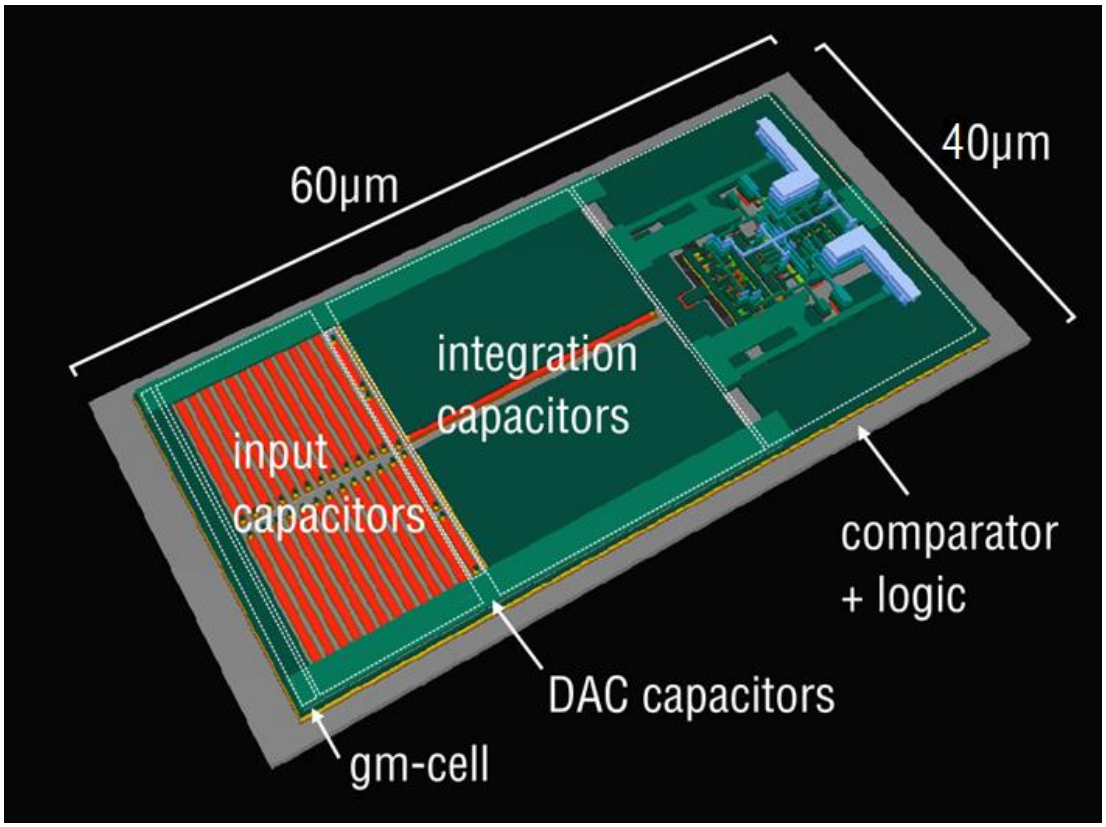


Fig. 57 – Area estimation with subtitles on important zones.

6. Conclusions

In this final chapter, the general conclusions of the new quasi-passive ΣΔ modulator topology are discussed, as well as possible applications of the final circuit in IoT, biomedical applications, image capture and others. A list of future work and possible improvements in terms of resolution, area and power consumption are also presented in this section.

6.1. General Conclusions and Applications

A new and innovative ΣΔ modulator topology was studied, implemented and tested in this thesis. The main objectives of designing a ΣΔ modulator for IoT applications with a small area and low power consumption were achieved with the proposed topology, and most important, the presented work validates a new technique to implement ΣΔ modulators, proving the feasibility of amplifier free topologies. The resulting circuit presents a low resolution when compared to typical high order ΣΔ, although this result is compensated by the small size and low power consumption of the circuit, which are two valuable aspects for battery-powered portable devices.

IoT is a fast-growing field, with many subthemes in which this circuit could be implemented. For instance, in systems that measure multiple sources of data at the same time, such as CMOS image sensors, by using small size ADCs it is possible to implement a matrix of ADCs. Other possible applications are in the biomedical field, where many small sensors are measuring information and is essential to acquire the results at a precise moment. Once again, a matrix of small-footprint ADCs would lead to concurrent sampling of all sensors.

The implemented 1st order ΣΔ modulator without amplifiers to perform the integration process achieves an ENOB of 8.23 bits with a very small area and a power consumption of 0.08 mW. Next section presents a list of future work to give continuity to the research of the quasi-passive ΣΔ modulator proposed in this thesis.

6.2. Future Work

- Fabrication

The first point of the future work list is the fabrication of the developed circuit in order to perform tests and validate the topology. Given the limited time of a master thesis, it was not possible to fabricate the circuit and perform tests as this process usually takes several months. Instead, this thesis focused on the study and implementation of a new topology of ADCs which enables ΣΔ to target a completely new set of specifications. It is expected to fabricate the circuit in a few months taking opportunity of an existing run.

- Reducing circuit size

The achieved circuit already presents a very small area when compared to other ADCs. On the other hand, one simple way to further reduce the area is to use more advanced CMOS processes with smaller transistor dimensions. As this topology does not employ amplifiers the effects of short channel length are less prominent. Another possibility is reducing the transconductance of the Gm cell, this would lead to smaller sampling MOSCAPs and consequently smaller DAC and integrating MOSCAPs to

maintain the same gains. Some problems of implementing the Gm cell with smaller transistors may arise due to mismatch which will affect the overall linearity of the ADC. Another possible way of reducing the circuit area and also the power consumption is designing a custom-tailored comparator for this ADC. Since the comparator was reused from a previous work that had slightly more demanding specifications it has room for improvements.

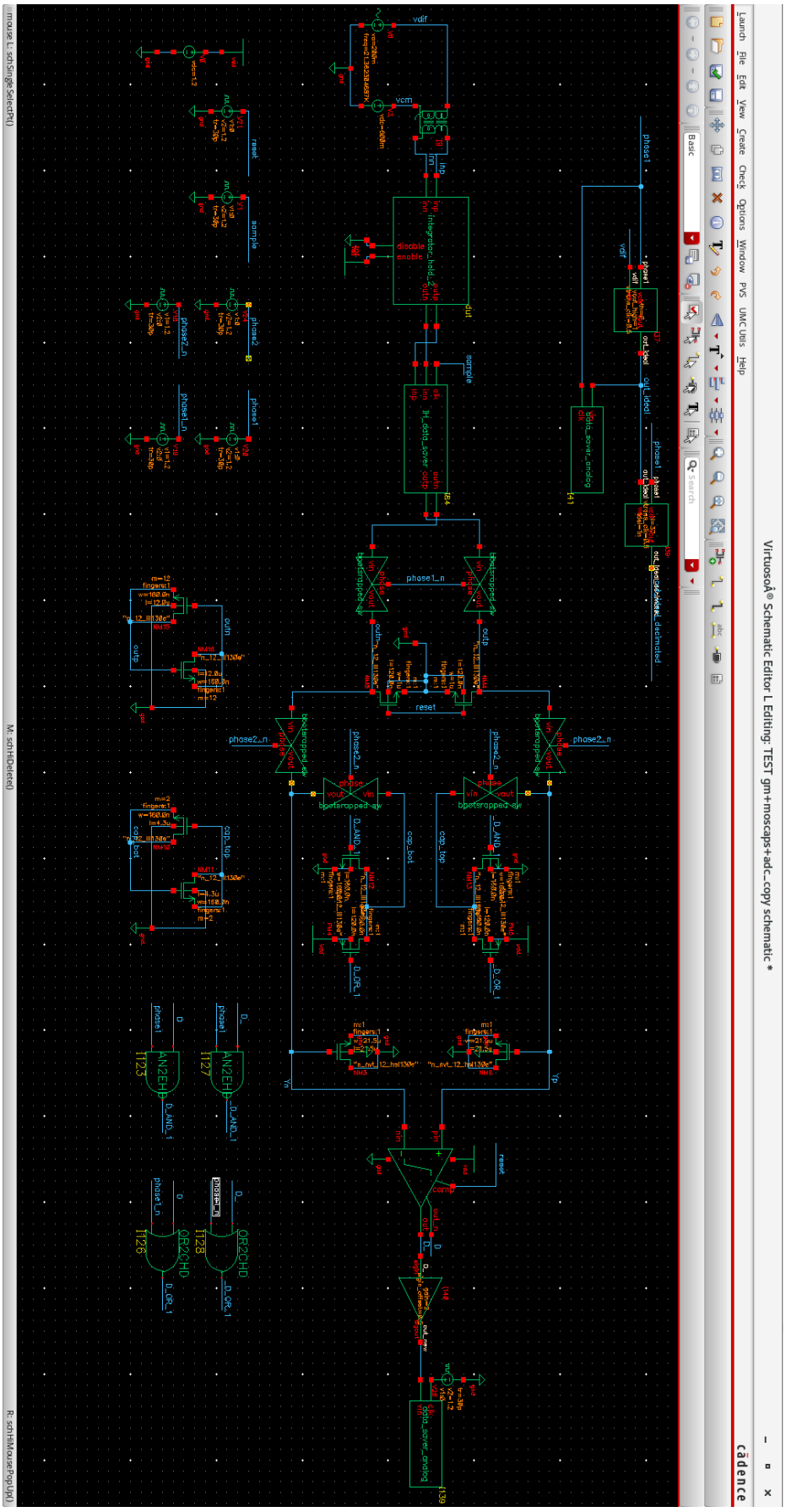
- High Resolution

The implemented circuit targets relatively low resolutions which is normal given the absence of amplifiers, although this does not exclude the proposed topology from medium resolution applications. The resolution of the ADC can be possibly increased with the following methods. The first one and most challenging, is increasing the order of the modulator which is not as simple as in the conventional ΣΔ. It is important to emphasize that this topology works in charge mode, in order to increase its order placing several integrators in series, every time that an integration takes place, it would need a Gm cell to transform the resulting voltage of that integration into charge again. This imposes some limitations, as the Gm always introduce some error, and does not present a good linearity with small input voltages. This fact might force this topology to first order implementations. The second option is maximizing the linearity of the modulator with an optimizer instead of designing the circuit based on formulas and simulations, finding the maximum performance instead of local maximums. The third optimization is to use digital calibration methods to compensate the charge leakage from the passive integration. This technique is already used with active amplifiers and it is well explained in [25]. Another promising technique to improve the ΣΔ modulator is using MOSCAPs with dynamic body biasing. This principle is proposed in [24] and can be used to improve the passive integration.

Appendix A:

```
`include "constants.vams"
`include "disciplines.vams"

module data_saver_V_Q (inp, inn, outp, outn, clk);
 input inp, inn;
 electrical inp, inn;
 output outp, outn;
 electrical outp, outn;
 input clk;
 electrical clk;
 parameter real threshold  = 0.25;
 parameter string filename_v = "a_v.csv";
 parameter string filename_q = "a_q.csv";
 parameter string filemode = "w";
 real flag, charge_n, charge_p, charge, prev_charge;
 integer file_v, file_q;

 analog
   begin
      @(initial_step)
         begin
           prev_charge = 0;
           file_v = $fopen(filename_v,filemode);
           file_q = $fopen(filename_q,filemode);
           $fwrite(file_v,"#format table ## [WaveView Analyzer] saved \nXVAL, VIN\n");
           $fwrite(file_q,"#format table ## [WaveView Analyzer] saved \nXVAL, QIN\n");
          end

      @(cross( (V(clk)-threshold) , +1))
         begin
           $fwrite(file_q, "%0.18f, %0.18f\n",$abstime, charge - prev_charge);
           $fclose(file_q);
           flag    = 1;
           prev_charge = charge;
         end

    @(cross( (V(clk)-threshold) ,-1))
        begin
          $fwrite(file_v, "%0.18f, %0.9f\n",$abstime, V(inp, inn));
          $fclose(file_v);
        end

      V(inp,outp) <+ 0.0 ;
      V(inn,outn) <+ 0.0 ;



      charge_p = idt(I(inp, outp), 0);
      charge_n = idt(I(inn, outn), 0);



      charge = charge_p - charge_n;
  end
endmodule
```

Appendix B:


Launch File Edit View Create Check Options Window PVS UMC Utils Help
VirtuosoÂ® Schematic Editor L Editing: TEST gm+mosscaps+adc_copy schematic *
cadence

7. References

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