TÉCNICO LISBOA

Digital Controlled Oscillator for Wireless Bluetooth Low Energy Sensor Networks

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Abstract

Wireless communication systems are one of the largest growth areas in Radio-Frequency and its progress keeps renewing interests in new architectures and applications. The numerous applications available go from short to long range communications systems, very low to high data bit rates so each one has different requirements of power consumption. All these different requirements have one thing in common for battery operated mobile devices, the need for low power operation. The ever-increasing integration of what used to be stand-alone devices, such as cameras and radios, into single multi-functional electronic devices, makes autonomy increase a big challenge.

This thesis proposes a digitally controlled oscillator (DCO) for 2.4 GHz ISM band with significant improvement in power consumption, optimized frequency tuning range, very fine-tuning resolution and optimized phase noise performance. The circuit is designed using CMOS 130 nm from United Microelectronics Corporation (UMC) technology. The work presented is to be included in a frequency synthesizer which will be incorporated in a radio transceiver using Bluetooth Low energy (BLE) protocol, whose applications target low data bit-rates under very low power consumption.

A DCO is an oscillator whose frequency is controlled by a digital word. A review of the most important oscillator models and frequency tuning methods is done. As it will be specified in the following chapters, the chosen criteria for oscillation start-up is the one-port admittance method.

The cross-coupled differential pair is used to generate a negative conductance and meet oscillation parameters. Recent developments have enabled reducing power consumption using Class-C architectures. For digital tuning control three banks of capacitors/varactors are used with different characteristics. The DCO covers the 2.4 GHz ISM band between 2.4 – 2.485 GHz. Its frequency resolution step is approximately 20 kHz.

The design and simulation of the circuits was made with Virtuoso Design Environment software from Cadence. In conclusion, the proposed DCO has a power consumption of 500 µW with a 1.2 V power supply and a maximum phase noise of -119 dBc/Hz at 1 MHz.

Keywords

DCO, frequency synthesizer, radio-frequency, Bluetooth Low-Energy

Resumo

Nos dias de hoje os sistemas de comunicação de radio frequência são uma das maiores áreas de crescimento. O constante desenvolvimento nesta área mantém renovado o interesse em descobrir novas arquiteturas e aplicações. Existe uma grande variedade de aplicações disponíveis que vão desde sistemas de comunicações de curto a longo alcance, taxa de bits de dados baixas a muito altas, no entanto todos com especificações diferentes em relação a consumos de energia. Independentemente da variedade de aplicações existe um objetivo em comum para todos os dispositivos móveis operados por bateria, a necessidade de operarem com um baixo consumo energético. Cada vez mais existe a integração do que antes eram dispositivos independentes, como câmaras e rádios, para dispositivos eletrónicos multifuncionais individuais, fazendo com que a autonomia seja um grande desafio.

Esta tese propõe a elaboração de um oscilador controlado digitalmente, a funcionar na banda 2.4 GHz ISM com uma significante melhoria no consumo de energia, otimização da banda de frequências e da resolução e otimização do ruido de fase. O circuito realizado utiliza a tecnologia CMOS 130 nm da United Microelectronics Corporation (UMC). O trabalho apresentado vai ser incluído num sintetizador de frequências, que por sua vez será incorporado num transciver. O protocolo Bluetooth Low Energy (BLE) é utilizado, devido ao baixo consumo de energia e baixas taxas de bits de dados.

Um DCO é um oscilador cuja frequência é controlada por uma palavra digital. Neste projeto, é realizada uma revisão dos mais relevantes diferentes tipos de modelos de oscilador. Como será especificado nos capítulos seguintes, o critério escolhido para a realização da oscilação é o método da admitância utilizando um porto.

O par diferencial de acoplamento cruzado é usado para gerar uma condutância negativa e cumprir os parâmetros para obter oscilação. Desenvolvimentos recentes permitiram reduzir significantemente o consumo de energia utilizando arquiteturas que trabalham em classe C. Para o controlo digital, são usados três bancos de condensadores com diferentes características. A resolução mínima do DCO é de cerca 20 kHz e cobre a banda de 2.4 GHz ISM entre 2.4 – 2.485 GHz.

O design e as simulações foram efetuadas com recurso ao software Virtuoso Design Environment do Cadence. Em conclusão, o DCO proposto tem um consumo de energia de 500 µW, uma fonte de alimentação de 1.2 V e um ruído de fase máximo de -119 dBc / Hz a 1 MHz.

Palavras Chave

DCO, sintetizador de frequências, radio frequência, Bluetooth Low-Energy

Contents

List of Figures

List of Tables

Acronyms

CMOS	Complementary Metal-Oxide Semiconductor
IoT	Internet-of-Things
RF	Radio Frequency
SoC	System-on-Chip
BLE	Bluetooth Low Energy
TX	Transmitter
RX	Receiver
PLL	Phase Locked Loop
WPAN	Wireless Personal Area Network
VCO	Voltage Controlled Oscillator
DCO	Digitally Controlled Oscillator
ADPLL	All Digital Phase Locked Loop
UMC	United Microelectronics Corporation
LPF	Low Pass Filter
PD	Phase Detector
FCW	Frequency Control Word
Q	Quality Factor
LTI	Linear Time Invariant
NMOS	n-channel MOSFET
PMOS	p-channel Metal Oxide Semiconductor
FoM	Figure of Merit
PSS	Periodic Steady State
L	MOS transistors length
W	MOS transistors width

Acknowledgments

Foremost I would like to thank my supervisor Professor João Caldinhas Vaz for all the support, help, guidance and patience during this work. Without his guidance this work would not be possible.

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1 Introduction

1.1 Purpose and motivation

Throughout the years, CMOS systems have been widely developed, allowing high performance and miniaturization in wireless communications. From this evolution the concept Internet-of-Things (IoT) emerged, which connects everyday objects resulting in a highly-distributed network of devices capable to communicate with humans and other devices. Radio-Frequency (RF) System-On-Chips (SoC) transceivers are the key to receive and transmit data between devices.

Contemporary wireless communication devices are equipped with advanced processors for high functionality and flexibility supporting all kinds of communication standards such as GSM, Bluetooth, Zigbee, WiFi, WiMax, LTE and so on. Since most of these applications take great consideration for low power consumption, performance and high levels of RF/analog/digital integration, CMOS technologies are preferable. They have been extensively studied, since the scaling-down leads to performance improvement due to faster devices.

The work presented in this document is part of a SoC radio prototype. It is planned that it must contain all functions for transmission and reception of data packets compliant with the Bluetooth Low-Energy standard. These particular devices can incorporate temperature and magnetic field sensors, being also prepared to accept external analog signals provided by off-chip sensors. Monitoring the temperature, humidity, pressure of a process where it is difficult to access, or reporting the soil conditions, are some examples of where this kind of devices can be applied.

The power consumption of battery powered sensor nodes is dominated by the wireless link, so energy efficient transceivers (TxRx) have to be developed. To conceive high performance radio transceivers, the frequency synthesizer is typically used as the local oscillator who secures fine tuning with high spectral purity.

One important block of the synthesizer is the Phase Locked Loop (PLL) which fixes the channel frequency. RF PLLs for frequency synthesis and modulation consume a significant share of the total transceiver power, making sub-mW PLLs the key to build ultra-low power radios for wireless personal-area-network (WPAN) radios.

In communication systems, it is necessary to meet various working frequency bands, to satisfy different communication standards. Voltage controlled oscillators VCOs are found in systems that require a source of variable frequency like frequency synthesis, clock, data recovery and other applications. For instance, most RF systems contain an oscillator which generates the sinusoidal output signal used to modulate and demodulate the transmitted and received signals, respectively. VCOs are essential building blocks in communication systems.

The DCO is an improvement of the conventional voltage or current controlled oscillator. It is integrated in an all-digital PLL (ADPLL) which comparing to analog PLLs, are preferable over their analog counterparts. Since they are controlled with a digital tuning word, they offer benefits like smaller area, programmability, exhibiting better noise immunity and distortion reduction [4,16]. Since the DCO core is a conventional VCO without the digital tuning part, to develop and understand it, the VCO is studied to realize how it is possible to achieve enhanced trade-offs between key characteristics.

The classical VCO using cross-coupled differential pair and a LC tank topology is widely employed, but the Class-C harmonic VCO, that improves the phase noise characteristics and, most important, the power consumption, was initially proposed in [8] and [9]. This topology exploits the advantages of biasing cross-coupled transistors in Class-C. However, because it is impossible to start oscillations in Class-C, it is required to change the required initial Class-A or AB bias point, where oscillation startup is possible, to a steady state Class-C operation. To make Class-C VCOs robust in real applications, a method is necessary to relieve the startup difficulty and hence allow the VCO to operate in the optimal state. Several techniques have been studied [10-14]. Regarding digital tuning, as shown in [17-21], oscillators are tuned by digital signals generated as inputs of DCO. The most common way to lock to a certain frequency is by using switched capacitors and varactors in parallel.

1.2 Framework

The DCO to develop will be part of a multi-sensor SoC radio prototype that can be used in an ultra-low power consumption wireless sensor node. The chip will include all functions for transmission and reception of data packets compliant with the Bluetooth Low-Energy standard, being a perfect candidate for the IoT network.

1.3 Goals and challenges

This thesis focuses on the design of a new DCO, which will be an improved version of an already available prototype. The most demanding parameters of the DCO are the frequency finest tuning step and the ultra-low power consumption. The following topics are aimed for being achieved:

- Study of available circuit components to verify their behavior. The technology study is imperative to analyze which components are more suitable to use;
- Study of the blocks that integrate the DCO (Capacitors banks and VCO architectures);
- Improving the tuning range by assuring the oscillator 2400 MHz – 2485 MHz frequency band is covered. An estimated safety margin is settled to fulfill all

frequencies in the band taking into count fabrication dispersion and parasitic capacitances;

- Reduce the DCO total power consumption. The prototyped DCO should have a maximum phase noise of -125 dBc/Hz at 1 MHz offset with a total power consumption in steady state regime below 450 µW inside the tuning range;
- The phase noise requirements are relaxed, reduce power consumption is the priority;
- Finally, the finest tuning frequency step size should be equal or smaller than 12 kHz.

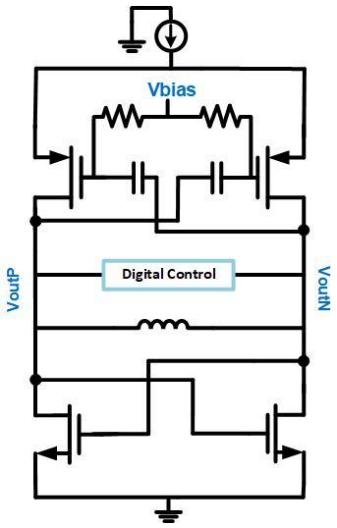

Figure 1 – Schematic of a typical cross-coupled DCO.

1.3 Specifications

The chip monolithic technology will be CMOS 130nm, featuring 1 poly layer, 8 metal layers (2 thick), spiral inductor, CMOM capacitors, PMOS and NMOS transistors and power supply of 1.2 V. The required specifications regarding the digital control oscillator are presented in the following table.

Table 1 - Oscillator design specifications.

DCO Specifications	
Frequency Tuning Range [MHz]	2400 – 2485
Phase Noise	-125 dBc/Hz @ 1 MHz
Power Consumption [µW]	< 550
Fine step size [kHz]	12
Voltage supply [V]	1.2

1.4 Document organization

This work is organized in 7 different chapters, starting with an introduction, where the main subjects of this thesis are presented, following goals and challenges remarking key specifications to be achieved and organization.

Chapter 2 presents the state-of-art. It starts by summarizing a brief architectural background on frequency synthesizers, along with a literature review of previous research. Following is a comparison between VCO topologies where various architectures are presented and discussed. An improvement of the traditional cross-coupled differential pair LC tank, the Class-C VCO, is also reviewed.

Chapter 3 contains all theoretical work about frequency-controlled oscillators, from the oscillation startup condition to the large signal conductance analysis. It also covers important parameter characteristics like phase noise, resolution and tuning range including a more detailed emphasis in digital tuning.

In Chapter 4 the LC tank circuit process design is presented. Dimensioning the digital tuning using capacitor banks can be considered the most critical part of the project. In this chapter it is carefully explained the design and switch control of each cell in the different banks as well as the chosen inductor. In the end is presented the layout of each bank capacitor.

The negative conductance block is implemented in Chapter 5. The Class-C bias technique is applied for the active part design to reduce power consumption. Following is presented the circuit and layout implementation of the full DCO with a detailed simulation results. Some aspects on how to optimize the layout to achieve minimum loss and parasitic effects are also presented.

In Chapter 6, important aspects related with the developed work are presented and discussed, a comparison is made with the previous prototype and also with some published results. Finally, some guidelines for future work are suggested.

2 State of the art

The state of the art embodies the most important scientific work developed in the past years that in same way is essential to study and understand topologies, as well as techniques more suitable to use in the project. First, a brief summary about the differences of analog and digital frequency synthesizers is described. The main difference between a DCO and a VCO is the oscillator frequency control where the DCO uses discrete tuning while the VCO uses continuous tuning. Since there are similarities in the oscillator core, several VCO cross-coupled topologies are introduced, followed by the improved Class-C topology.

2.1 Frequency Synthesizer

High-performance frequency synthesizer is crucial for wireless communication systems. A frequency synthesizer is used when it is necessary to produce a tunable frequency from one fixed reference frequency. The basis of this system is a PLL where a feedback loop is used. Recently, radiofrequency analog PLLs have been frequently replaced by all-digital PLLs. As the technology progresses into submicron CMOS, we will witness decreases in the propagation time as well as in the structure size and lower power consumption. Therefore, it has led to a supply voltage reduction, which in case of analog circuits, reduces the maximum theoretical signal-to-noise ratio (SNR), compromising their performance [16]. Furthermore, any digital circuit can be described by any hardware language becoming easier the porting between different technology nodes. However, despite the continues improvements in this field, DCOs remain one of the most critical blocks of RF transceivers.

Throughout the years, the classical Integer-N frequency synthesizer, whose step size is limited by a small reference frequency, has been replaced by the Fractional-N type, which improves frequency resolution without compromising the reference frequency [1-5].

2.2 Voltage Controlled oscillator

In a PLL the VCO is a key block and it has been extensively studied in the last years, with several papers being published. The VCO can be considered one of the most important components in modern communication systems since wireless applications require oscillators to be tunable, meaning their output frequency is a function of a control input. It is expected to provide excellent performance, so it won't compromise the entire RF link.

The key property of the VCO is the output frequency being a linear function of the control voltage, allowing different oscillating frequency values. This frequency variation can be achieved by different methods, commonly using capacitors or varactors. A well designed VCO must meet very stringent requirements such as phase noise, power consumption, tuning range, frequency step, harmonic distortion and spurious.

Oscillators can be separated into two major classifications, those who create sinusoidal outputs as opposed to those with square (or triangular) outputs wave. Square output wave is usually produced by relaxation or ring oscillators and used for frequencies up to mega Hertz range. Sinusoidal oscillators can be divided into RC and LC circuits. Generally, RC circuits are cheaper since they require smaller area and can provide wide tuning range, but they are mainly used for low frequencies like audio. Sinusoidal waveforms are usually desired for high frequency applications. Although, crystal oscillators are included in the LC circuits and are frequency stable with high Q factor, crystal oscillators have fixed oscillation frequency, not allowing variable channels. LC oscillators are extremely used in generating and receiving RF signals where variable frequency is tunable. The downside is the use of an integrated circuit inductor which occupies a large area. [6,7]

Regarding topologies to implement the active part, they all have the same goal, overcome the LC tank losses. The most common used topologies are the cross-coupled LC Tank and the differential Colpitts [8-15]. As will be discussed later, the cross coupled topology has several alternatives, in Figure 2 the NMOS topology is presented, composed by two transistors connected in loop were each drain is connected to the other transistor gate. The Colpitts oscillator uses two capacitors in series. To guarantee a startup positive feedback the two capacitors must have a determined ratio. This turns out to present higher loading impedance in parallel with the LC tank. Although Colpitts is also capable of good phase noise performance for the same power consumption, the cross-coupled pair can achieve better results [8]. Since the LC Tank can also allow higher tuning range this topology is chosen. From now on the cross-coupled differential pair LC oscillator will be designated as LC cross-coupled.

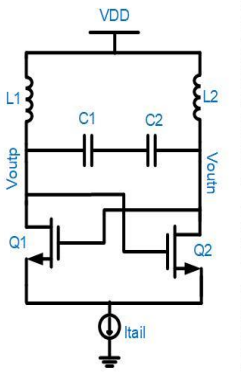

Figure 2 - Schematics of differential LC cross-coupled (left).

In Table 2 is presented a summary of some published works. To evaluate VCO topologies and their performance among each other it is common to use a Figure of Merit (FoM). Its equation considers the oscillation frequency f_0, the phase noise, $L(\Delta\omega)$, for an offset from carrier $\Delta\omega$, and power consumption, P_{diss}, and is expressed by

$$FOM = L(\Delta\omega) - 20 \cdot \log\left[\left(\frac{f_0}{\Delta f}\right)\right] + 10 \cdot \log\left(\frac{P_{diss}}{1mW}\right) \ [dBc/Hz]\,. \quad (1)$$

Table 2 - VCO state of the art performance comparison.

Reference	[10]	[11]	[12]	[13]	[14]	[15]
Process [nm]	180	90	180	180	180	180
Topology	Colpitts	Ring	LC VCO	LC VCO	LC VCO	LC VCO with tunable inductor
Year	2013	2012	2015	2016	2007	2006
Power Consumption [mW]	1	0.9	2.6	3.23	0.97	6~28
Output Frequency [GHz]	--	1.1-3.2	2.29-2.55	2.25-2.52	2.11-2.42	0.5~3
Phase Noise [dBc/Hz]	-132.7 @3MHz	-94 @1MHz	-118.9 @1MHz	-119.4 @1MHz	-111 @1MHz	-101~-118 @1MHz
Supply Voltage [V]	1	1.2	0.5	0.5	1.5	1.8
FOM [dB]	-190.5	-162	-181.6	-181.3	-179.2	--

The comparison presented in Table 2 results from different topologies. A low power technique is presented with Colpitts design in [10]. In addition to the classical Colpitts oscillator, it uses an inductive gate degeneration as a second path of positive feedback. In [11], to meet the performance requirements with low cost design the ring VCO is chosen. Compared with other topologies it has the worse phase noise performance. Although, it has smaller chip area, lower power consumption and as very simple design, the output frequency can be strongly affected by supply voltage. From [12-15] the LC VCO topology is used. Papers [12-13] had the important role of improving the phase noise performance. In [12] an ultra-low supply voltage is used, being only 0.5 V. In this circuit, there is no current source to enlarge either the transconductance or the voltage swing of the cross-coupled. Instead a control voltage is added in the bulk terminal of the cross-coupled for lowering on-resistance. Research [13] is an improvement of [12] by adding a simplified and effective noise filtering technique to enhance the phase noise performance by inserting at the tail of LC VCO a LC filter. Paper [14] uses a robust current reuse design for low power operation and [15] focus on ultra-wide band operation using a tunable active inductor.

2.3 Class C oscillator

A Class-C VCO circuit design is presented in Figure 3, where the main difference from the classical LC cross-coupled is the pair gate bias, v_{bias}, which allows to control the transistors bias level and respective class of operation. The LC cross-coupled Class-C VCO is an evolution of the LC cross-coupled, and it can provide lower power consumption in the steady state regime. But of course, the oscillator startup cannot occur with a Class-C bias point. To overcome the startup issue under low supply voltage, several techniques have been studied such as, a dual-conduction VCO [17,21], an adaptive bias scheme [18], and an amplitude control loop [19,20].

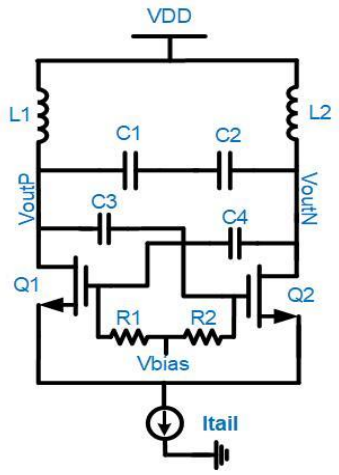

Figure 3 - Schematic of a LC cross coupled Class-C VCO.

All of them contain a mechanism that enforces switching from a specific mode allowing startup and gradually bringing down gate bias voltage for the Class-C region. An adaptive bias scheme [16] is generally considered to guarantee startup at the beginning of oscillation with a simple and small bias circuit without degrading the phase noise performance achieving a fast-robust startup. The dual-conduction topology consists in an additional switching pair placed in parallel which ensures a robust startup by initially operating in Class-B. The drawback for this low power consumption approach involves the Class-C waveform distortion because of the auxiliary pair and steady state phase noise performance deterioration. Nevertheless, Class-C VCO containing amplitude detectors [19,20], are divided in two loops, one for startup operation achieving the automatic optimal bias point and other to guarantee constant and stabilized amplitude control for all operations conditions. It's obvious that adding auxiliary circuitry will introduce additional noise sources and power dissipation leading to phase noise and power consumption decline. In Table 3 there are several comparisons between different types of Class-C VCOs.

Table 3 - Summary and comparison of Class-C VCOs with different robust start up techniques.

Reference	[17]	[18]	[19]	[20]	[21]
Process [nm]	180	90	180	180	65
Date	2009	2011	2011	2015	2016
Robust startup technique	Dual Conduction	Adaptive bias scheme	Automatic startup loop	Bias loop + Amplitude detector	Adaptive bias + auxiliary Class-B pair
Power Consumption [mW]	0.114	0.86	1.57	2.78	6
Carrier Frequency [GHz]	4.5	5.11	3.1	5	2.46
Phase Noise [dBc/Hz]	-104 @1MHz	-127 @3MHz	-123 @1MHz	-123.3 @1MHz	-132.41 @1MHz
Supply Voltage [V]	0.2	0.6	1		1.2
FOM [dB]	-187	-192.3	-191.1	-192.8	-192.45

3 Oscillators fundamental theory

RF radios are widely used to transmit and receive data. The main stages of a radio frontend include generating a carrier signal, filtering unwanted signals and noise, amplification to boost signal level and mixing to either change the carrier frequency to RF band in a transmitter or to base band in a receiver. In modern wireless communications, the frequency is generated by a frequency synthesizer.

This chapter starts with a brief review of analog and digital PLL mechanisms. Following is a theoretical overview of the VCO, starting with oscillation theory and its characteristics. Stringent requirements must be accomplished to get a low-cost and low-power consumption without degrading phase noise. Since the oscillator developed has digitally controlled frequency, this chapter presents more detailed information about digital tuning.

To fulfill the oscillation condition a negative resistance circuit is needed. The cross-coupled differential pair topology is used. As seen further there are several topologies, NMOS, PMOS and CMOS but as it will be explained later, the chosen is the CMOS topology.

3.1 Phase Locked Loops

PLL is essential in most wireless application, radio and other electronic circuits. They are exploited for frequency synthesis and clock/data recovery. A typical basic architecture of an analogue PLL is shown in Figure 4, which consists on a VCO, low-pass filter (LPF) and a phase detector (PD). The PD compares reference signal phase with the feedback signal phase, producing up and down signals. The signals are then fed into the charge pump which charges or discharges the loop filter according to the phase error. The filter in response produces a control voltage which is fed to the voltage-controlled oscillator, thereby it changes the frequency of the VCO which output is feedback to the phase detector, thus it operates in a loop. The LPF function is to suppress spurs produced by the phase detector not to cause unacceptable frequency modulation in the VCO [22]. The PLL is locked when both inputs of the PD have equal frequency and their phase difference has the right value to control the VCO output frequency [22]. This basic PLL structure is synchronized when $f_{out} = f_{ref}$. While in synchronism, it is a system where the phases of the VCO and reference signal are compared, resulting in an error signal proportional to the phase difference.

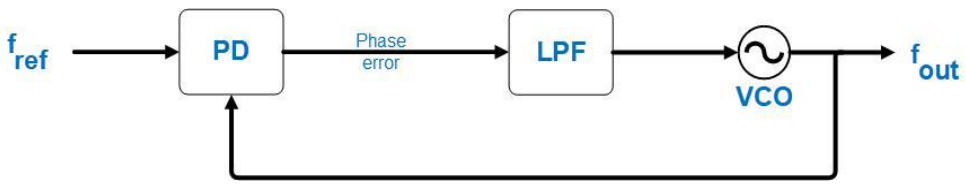

Figure 4 - Phase locked loop basic diagram.

3.1.1 Synthesizer with Analogue PLL

A basic synthesizer system consists in a PLL with a programmable divider in its feedback loop, which allows an output frequency value multiple of reference frequency. A fixed divider (N) can be added to the loop varying f_{out} with the divider, now f_{out} depends on the divider modulus.

There are two different architectures used, depending on the divider type used, Integer-N and Fractional-N PLL. The Figure 5 shows the Integer-N topology, where output frequency is an exact integer multiple of the reference frequency.

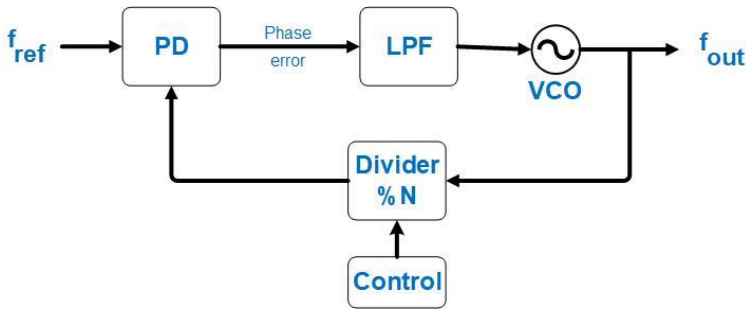

Figure 5 - Integer-N frequency synthesizer.

In the Integer-N type the output frequency is given by

$$f_{out} = N * f_{REF}, \quad (2)$$

where f_{REF} is the channel spacing and N is an integer number from 1 to N. In this case the synthesizer is synchronized when the two signals entering the phase detector have the same frequency. To implement small steps between channels frequencies, f_{ref} has to be low requiring high division ratio, N, resulting in a slow synchronism, to avoid this situation it is suitable to use the Fractional-N.

Fractional-N topology produces fractional increments of the reference frequency at the output, allowing very high frequency resolution. Thus, increasing reference frequency reduces the switching speed and increases the loop bandwidth. Typically, divider modulus alternates between N and N+1, the percentage of time given to each value is determined by the required fractional frequency. Figure 6 presents the Fractional-N frequency synthesizer.

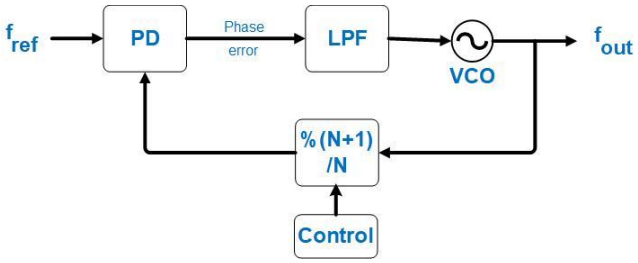

Figure 6 - Analog frequency synthesizer; Divider using Fractional-N type.

The method used to implement a dual modulus consists in knowing the effective division total pulses, P pulses. For the first S pulses, the divider has N+1 modulus, and during the remaining P-S pulses has N modulus. The output frequency is the average of those values, being a fractional value between $N \cdot f_{ref}$ and $(N+1) \cdot f_{ref}$ that depends on S value. Here a high frequency resolution is achieved. The divider implementation can be achieved by

$$f_{out} = f_{ref}\frac{S}{P}(N+1) + f_{ref}\frac{P-S}{S}(N) \Leftrightarrow f_{out} = f_{ref} * \left(N + \frac{S}{P}\right). \quad (3)$$

3.1.2 Synthesizer with Digital PLL

Comparing a digital PLL with an analog PLL it's clear that many advantages for the former one arise. The smaller implementation area and less sensitivity to process variations are two of them. As digital circuits, the blocks implemented can be scaled down easily as the way of technology improves further on, making it possible to work with ultra-low supply voltages.

The digital PLL exchanges the input frequency reference for a frequency control word (FCW), a DCO is also used instead of a VCO and the frequency divider is replaced by a RF counter as seen in Figure 7. Also, the LPF is digital and included in the control block. Although at RF frequencies the DCO output signal is still a sinewave, this system is usually called an all-digital PLL.

The DCO analog output enters the RF counter which gives a digital output number equal to the ratio f_{out}/f_{clk}, where f_{clk} is the low frequency clock reference. In reality, the RF counter counts how many RF periods fit in one clock period. Then this output is compared with the FCW control word, meaning that when the FCW digital word equals the counter output, the DCO is synchronized.

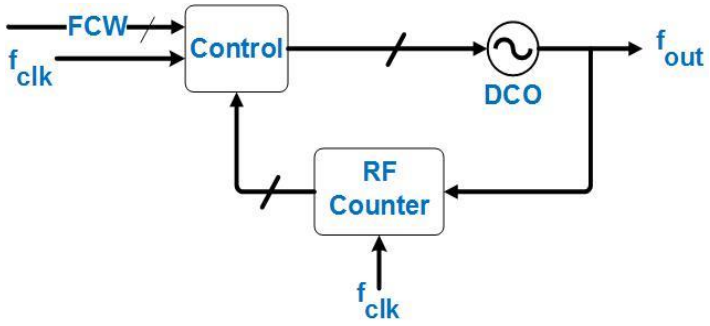

Figure 7 - Basic scheme of a digital phase locked loop.

3.2 LC tank oscillator

LC tank oscillators are widely used in both academia and industry. The LC tank is built to act as a resonator. In an ideal LC tank, oscillation occurs when a startup impulse is given to the circuit. It would oscillate indefinitely at a certain frequency, by transferring the energy present from the electric field of the capacitor to the magnetic field of the inductor and vice versa. In practice,

exists resistances and capacitances which will influence the operation. The next section explains the oscillation working principle.

3.2.1 Working principle

Oscillators are key building blocks in RF transceivers and take much influence in the overall system, mainly due to phase noise. A typical oscillator circuit requires positive feedback around a gain stage to sustain the oscillation. The working principle can be studied by the Barkhausen's criteria, based on a feedback system, as seen in Figure 8, which transfer function is expressed as

$$X_0 = \frac{A(s)}{1 - A(s)B(s)} X_i. \tag{4}$$

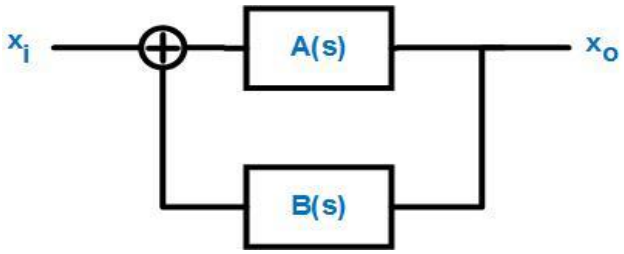

Figure 8 - Positive feedback system.

There are two-time periods that are important to consider. After bias turn-on, the oscillator must enter the startup regime where the signal increases its amplitude which reduces gain A of the non-linear block until it gets to the steady state regime where the amplitude and frequency became, ideally, time invariant. Without the proper startup regime, the oscillator can't reach the expected working behavior in the steady state regime. In steady oscillation, the circuit must satisfy the Barkhausen criteria given by

$$A(j\omega) \cdot B(j\omega) = 1. \tag{5}$$

The one-port method is another oscillator analysis technique. The oscillator circuit can be divided into two blocks, A and B, as seen in Figure 9.

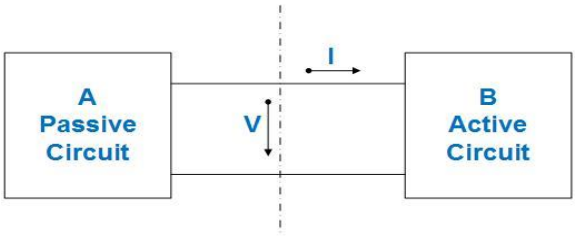

Figure 9 - Oscillator representation for one-port analysis method.

Block A is composed by passive elements with a linear behavior. Since its components have resistive losses, it dissipates energy causing an amplitude exponential decay. Therefore, an active circuit is needed to compensate for the resistive losses effect. Thus, for the oscillation to

be sustained, block B must compensate the energy lost in each period [23]. As a consequence, block B must contain active elements with non-linear behavior.

Admitting that a cross-coupled LC will be used, block A is composed by an inductor and a capacitor in parallel. Not considering any reactive effects coming from block B, the resonant frequency defines the oscillation frequency which is given by

$$\omega = \frac{1}{\sqrt{LC}}. \tag{6}$$

At resonance the LC impedance is infinite. However, in reality, the parasitic resistance results in a loss behavior. The conductance losses in the passive part must be compensated by the negative conductance of the active part, to fulfill the startup conditions described as

$$\mathrm{Re}[Y_A + Y_B(\omega)] < 0, \tag{7}$$

$$\mathrm{Im}[Y_A + Y_B(\omega)] \approx 0. \tag{7a}$$

With the active circuit exhibiting an input resistance of -R attached across the tank to cancel the effect of R, results in an ideal scenario where the oscillator verifies the steady state condition, to sustain a stable periodic signal, given by

$$[Y_A(V, \omega) + Y_B(\omega)] = 0. \tag{8}$$

3.3 Performance parameters

There are several parameters who have great influence in a VCO design, such as phase noise, frequency tuning range, frequency resolution and power consumption. The choice of these metrics results in a large number of possible circuit designs. Following, each one is analyzed.

3.3.1 Frequency tuning range

Wireless applications require a range of oscillation frequencies, not only necessary to cover the protocol bandwidth but also to compensate for variations that could be caused by the process or some external condition. The output frequency must be a function of a control input signal. Before getting into detailed calculations of the frequency tuning range, in this section is reviewed the operation of analog and digital tuning with emphasis on digital tuning covering bank of capacitors and MOS varactors.

The output frequency of an ideal VCO is a linear function of its control voltage, V_{ctrl} that can be seen in Figure 10 and expressed as

$$f_{out} = f_0 + K_{VCO} * V_{ctrl}, \tag{9}$$

where f_0 is the output frequency for $V_{ctrl} = 0$ and K_{VCO} denotes the gain or sensitivity of the oscillator in MHz/V.

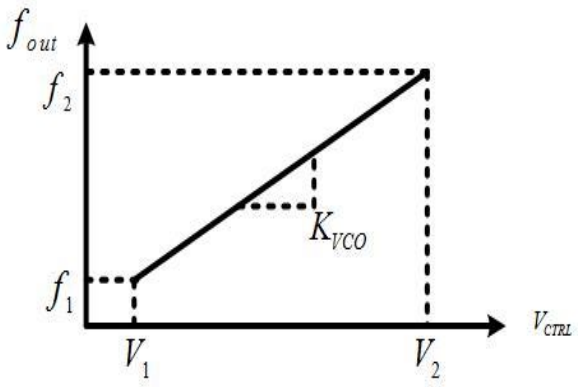

Figure 10 - Definition of gain K_{VCO}.

The frequency tuning band means the range from the maximal frequency, f_2, to the minimal frequency, f_1, the VCO output can reach. So, the output frequency of the VCO can continuously change in the frequency tuning band based on the change of the tuning signal.

The oscillation frequency of a cross-coupled LC VCO is equal to (6) so that only the inductor and capacitor values can be varied to tune the oscillation frequency. In practice it is common to use the capacitor variation due to the difficulty to vary the value of monolithic passive inductors. The varactor is usually chosen to change the capacitance value using its voltage dependent capacitance.

Contrary to the analog VCO, whose frequency variation is continuous, the DCO frequency variation is discrete. Fixed and variable capacitors are widely used to tune the oscillation frequency inside a band. These elements can be turned on or off and are controlled by an input digital word resulting in a resonance frequency variation of the LC tank. So, the DCO output frequency is a function of the input FCW.

$$f_{out} = f(FCW) \tag{10}$$

From equation (10) it may seem that modelling of the tuning characteristics is a straightforward task, but it can be a challenge due to parasitic capacitances and capacitance value dispersion.

As said before, different frequency steps are used to simplify the tuning range design, fixed capacitors are often used for channel selection, higher ΔC, and varactors for fine tuning, smaller ΔC [24]. The digital control with individual capacitors changes equation (6) to

$$f_{out} = \frac{1}{2\pi\sqrt{L \cdot \sum_{k=0}^{N} \cdot C_k}}. \tag{11}$$

Being N the total number of capacitors and c_K the capacity of every unit cell. If a straightforward approach using very small capacitances was used for 2.4-2.485 GHz band, and a frequency resolution of 12 KHz, a great number of capacitors would be necessary. It is evident that it is extremely difficult to achieve this kind of precision. Using different capacitors banks, it is possible to dynamically change the frequency resolution whenever a different range is expected; this way it is possible to maintain the same matching precision.

Reviewed research typically uses three modes of operation [24-25] to achieve different resolutions. Two modes can also be found [26-27]. In both modes of operation, the cells design are in parallel. Usually, there exists a first operational mode which covers all band. The second bank covers the step capacitance of the first mode and finally, the third step, with the narrowest band range precisely controls the oscillation frequency resolution.

These multi-mode operations allow the use of multiple capacitor banks, who work independent of each other in terms of component matching. In Figure 11 a capacitor bank schematic is presented in CMOS technology implementation. This type of bank is binary weighted controlled, where each component line is controlled by the supply voltage. When supply voltage is 1,2 V corresponds to binary '1', and if voltage is 0, corresponds to binary '0'.

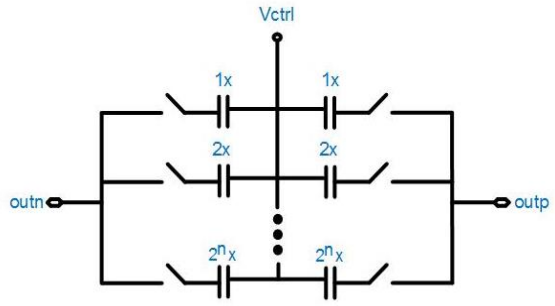

Figure 11 - Example of a bank using binary weighted capacitors.

There are two types of capacitors available in the technology, the metal-insulator-metal (MIMs) and the metal-oxide-metal (MOMs). A MIM capacitor is formed horizontally on the oxide region, with two metal plates sandwiching a dielectric layer parallel to the wafer surface. The other one is the MOM where the big difference from the MIM is the inter-digitated multi-finger formed by multiple metal layers separated by inter-metal dielectric. Due to this multi-finger characteristic it is possible to maximize capacitance and reduce resistance leading to a better Q value.

For smaller capacitance values, as will be discussed later, MOS based varactors stand a better choice. In this case each varactor is unitary weight controlled to achieve smaller capacitance steps.

3.3.2 Frequency resolution

An important parameter who influences the sizing of the tuning range is the frequency resolution. The frequency resolution is an important metric in the DCO design since it will affect the phase noise. Ideally, frequency quantization phase noise should be much smaller than the phase noise caused by tank losses and noise in active circuits [28].

In this project, a specific frequency resolution must be meet, 12 kHz. The chosen tuning range method design will be scrutinized ahead, however if one chooses to build a bank with only capacitors dimensioned with a small frequency step, to meet frequency resolution specification an exaggeration number of capacitors will be needed. To solve this problem different frequency steps are used to cover the whole tuning range. Frequency steps values are related with the capacitor cells in use. It can be analyzed by the ratio $r = \frac{C_{off}}{C_{on}}$, where C_{off} is the off state capacitance and C_{on} the on-state capacitance of the capacitor. Using this indicator, one can determine the capability of different types of capacitors/varactors used in the frequency planning. For example, to cover the whole band, a high frequency step is needed, the resolution of this capacitor is usually much higher than the one needed for DCO lowest frequency tuning step. To obtain a higher resolution very small values of capacitor must be used, so the smaller the capacitor, the smaller the change in capacitance. In this case we have a ratio close to one, the capacitance step is much smaller having less parasitic capacitances [29].

3.4 Cross-coupled differential pair LC oscillator

To meet the Barkhausen criteria, one of the most prominent ways to produce -R is by using the cross-coupled pair. Three cross-coupled circuits with different topologies are presented in Figure 12. Further it is discussed an improvement of the traditional cross-coupled differential pair LC tank, the Class-C VCO.

3.4.1 Negative conductance

As presented above, a negative conductance is needed to reassure oscillation. As mentioned the VCO is composed by an LC resonator and an active circuit. The minimum negative conductance is acquired by the active circuit to compensate the losses in the LC tank circuit, in this case provided by the cross-coupled differential pair [28]. In Figure 12 a cross-coupled NMOS, PMOS and a combination of NMOS and PMOS differential pairs (also called CMOS) are shown.

NMOS transistors carrier mobility is roughly two times of the PMOS transistors. They are advantageous because they can offer the required gain with minimal sizing while the PMOS architecture has to be at least two times larger. It is also reported that PMOS have lower flicker noise and contributes less drain current thermal noise for the same transconductance than NMOS [23,30].

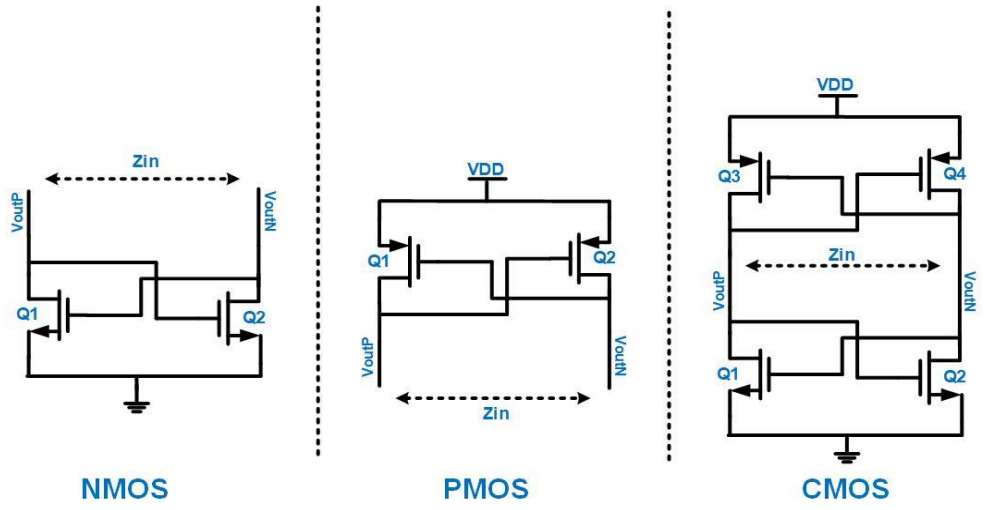

Figure 12 - Different topologies of cross-coupled circuits.

To calculate the small signal negative conductance presented to the LC tank by an NMOS cross-coupled, the circuit in Figure 13 is used. The equations to get the negative conductance are given by

$$V_x = V_1 - V_2, \tag{12}$$

$$V_1 = V_{gs2} = \frac{V_x}{2}, \tag{12a}$$

$$I_x = -i_{d2} = i_{d1} = -gmV_1, \tag{12b}$$

$$G_{NMOS} = \frac{i_x}{v_x} = -\frac{gm}{2}. \tag{13}$$

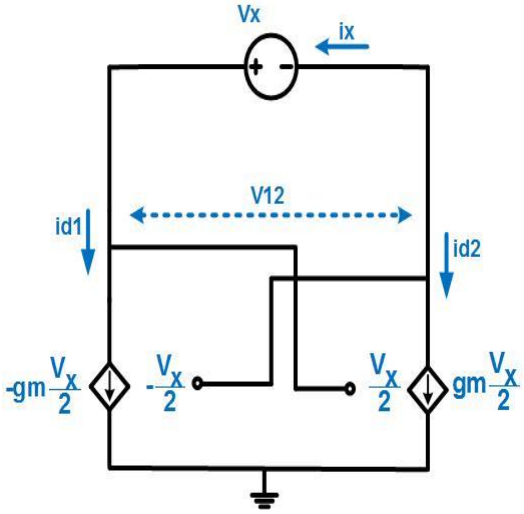

Figure 13 - Small signal model used to calculate the negative conductance of the NMOS cross-coupled differential pair.

In the CMOS topology, for the same bias current, the same current flows through both PMOS and NMOS and the available transconductance can be twice larger than the transconductance of the NMOS/PMOS topology, good for oscillation startup. Therefore, for the

same power supply the configuration yields a negative resistance twice as large while the phase noise remains unchanged if the output amplitude is the same [30,31]. The total negative conductance of the CMOS can be expressed as

$$G_{CMOS} = -\frac{gm_p + gm_n}{2}. \quad (14)$$

3.5 Class-C

The Class-C is an improvement of the cross-coupled LC VCO. Comparing both, the Class-C VCO provides better phase noise performance due to its low gate-bias voltage. This design exploits the advantages of biasing cross-coupled transistors in a Class-C condition, resulting in a more efficient generation of oscillation currents under Class-C operation. For a predetermined power consumption, the phase noise performance of a Class-C harmonic VCO is significantly superior to that of a standard cross-coupled LC VCO. In [14] and [6] the Class-C VCO achieves a theoretical phase noise improvement.

As can be seen in Figure 14, the Class-C VCO drain current is a pulse waveform instead of a near rectangular wave the cross-coupled LC VCO has. The pulse wave current can generate higher voltage oscillation fundamental amplitude than the rectangular one with the same average value which is one advantage of Class-C VCOs making it suitable for low power applications. The phase noise improvement can also be explained by the ISF theory, oscillators are most sensitive at the zero-crossing instant of oscillation voltage vo(t) and insensitive at peak instants. The Class-C delivers drain currents noise to LC-tank mainly at the time when the oscillator is insensitive and hence small phase noise is induced [13].

However, the Class-C needs major circuit complexity compared to a standard architecture, due to startup problems. It needs a dedicated startup circuitry as will be explained later.

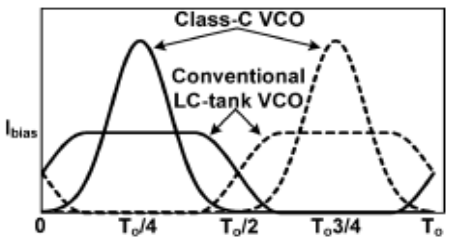

Figure 14 - Drain current of the switch pair for conventional cross-coupled LC and Class-C VCO. Image taken from [13].

Two different solutions for conventional Class-C were study in [8] and are presented in Figure 15. The discussed results considered that the transconductance of the differential pair is high enough to ensure the oscillation startup with V_{bias} being a fixed low value. Both circuits don't have feedback loop, so the authors changed manually the V_{bias} to a lower value after a period of

time noticing that oscillation was still secured. In practice, without a feedback loop, startup problems are inevitable.

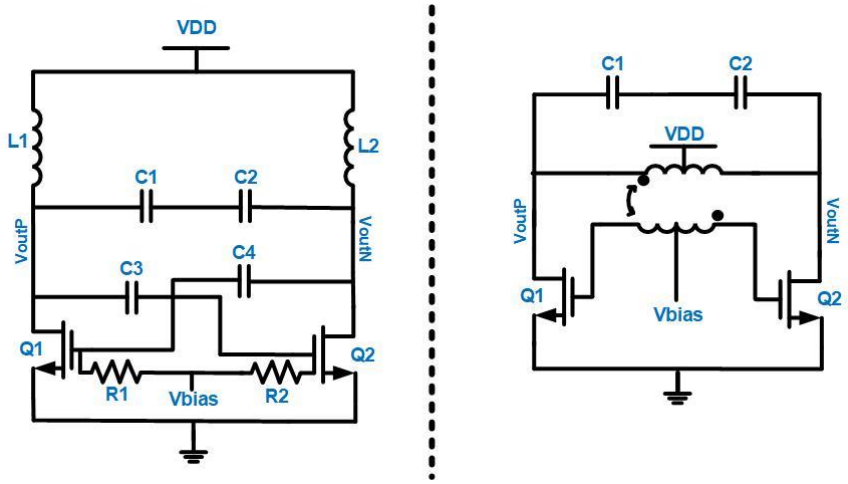

Figure 15 - Schematic views of the Class-C oscillator. MOS gate bias is provided with a low-pass RC filter (left); MOS gate bias is provided by a center-tapped secondary winding of a transformer (right).

The circuit presented with a transformer has its advantages, it occupies the same area than one inductor. The secondary winding is put over the primary one and doesn't need so many components to accomplish gate bias polarization. However, in a practical view there aren't transformers from the technology ready to be simulated and extracted. It would be necessary to build one from the start. For that reason, the presented left side circuit is preferable. From now on the cross-coupled LC operating in Class-C is referred to Class-C VCO.

3.5.1 Startup design for Class-C VCOs

The major challenge when designing ultra-low power RF systems consists in the compromise between performance and power consumption. It is necessary to get a close insight into analysis of the startup conditions, enhanced oscillation swing, and amplitude stability.

In the startup regime, it is necessary to have a small signal gain in block A to startup the oscillation. Classes A or even A/B must be a choice for transistors bias point. During startup the gain compresses and in the steady state regime the oscillation condition is fulfilled. Assuming the oscillation condition solution is stable, any sudden disturbance in the oscillation amplitude is compensated by the oscillator itself. This means, for example, that an amplitude reduction will increase gain, and the amplitude returns to the initial level.

A recent idea to reduce oscillators power consumption is to change the transistors bias point to Class-C when the oscillator reaches the steady state. If a large amplitude reduction is experienced, a danger that the oscillator won't start again exits because Class-C small signal gain is null. The solution is to use a real-time control mechanism that stabilizes the steady state amplitude by increasing the bias point again if this appends. This mechanism requires a feedback circuit.

The usual way to change the oscillator core bias point is biasing the cross-coupled pair gate terminals independently as shown in Figure 15. In case the bias is applied to gate terminals, two situations can arise. If the cross-coupled pair has a tail current source, due to channel modulation effect in the MOS sources terminals, changing the gates bias results in a change in the tail current source voltage. Moreover, if the cross-coupled pair sources terminals are connected to ground, the bias change directly affects V_{gs} MOS voltage.

Several designs achieve robust startup, what they all have in common is a mechanism that dynamically allows the change of an initial V_{bias} , when amplitude is small, to a pre-defined value for the optimal low power consumption.

3.6 Phase noise

This parameter is perhaps the most important in oscillators and it deserves great attention. The phase noise of a controlled oscillator determines the system performance in wireless communication systems, because in this case the oscillator phase noise directly affects the phase noise in the PLL far away from the carrier.

The output of an ideal oscillator can be expressed as:

$$V_{out} = A\cos[\omega_0 t + \varphi], \tag{15}$$

where A is the amplitude, φ the phase and $\omega_0 = 2\pi f_0$ being f_0 the oscillation frequency; all of them are constant values. Thus, in the frequency domain, the spectrum of an ideal oscillator will be a Dirac impulse. However, in a real oscillator, the amplitude and the phase are affected by noise, so the output is

$$V_{out}(t) = A(t)\cos[\omega_0 t + \varphi(t)], \tag{16}$$

where $V_{out}(t)$ and $\varphi(t)$ are functions of time. Due to these fluctuations the spectrum will have sidebands close to the oscillation frequency, as shown in Figure 16.

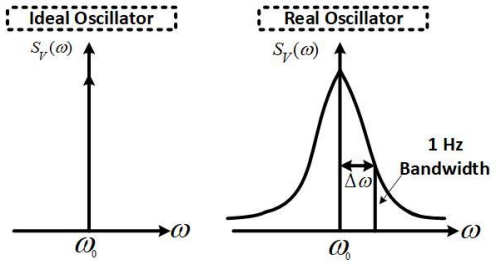

Figure 16 - Spectrum of the signal around the oscillation frequency showing his sidebands and the phase noise at $\omega_0 + \Delta\omega$ ($\omega_0 = \text{carrier frequency}$; $\Delta\omega = \text{frequency offset from } \omega_0$).

Phase noise is defined as the ratio between the noise power in a 1 Hz bandwidth at a certain frequency offset [23], to the carrier power. The result is expressed in dBc/Hz unit and calculated by the signal to noise relationship.

$$L(\Delta\omega) = 10\log_{10}\left(\frac{P_{NOISE}}{P_{SIGNAL}}\right)[dBc/Hz]. \quad (17)$$

There are several models to quantify phase noise, but the Lesson-Cutler model is the chosen to be analyzed. This model assumes that the oscillator, in terms of internal or external noise sources to output phase noise, behaves like a Linear Time Invariant (LTI) system. It identifies each individual noise source contribution by calculating each linear transfer function to the output.

Assuming an LCR VCO, with R representing thermal losses of C and L, and a noiseless negative resistance to sustain the oscillation. In this simplified case, the only source of noise is the tank resistance's white thermal noise, which can be represented as a current source across the tank, whose square mean value is given by

$$\overline{i_n^2} = 4kTG\Delta f. \quad (18)$$

In steady-state regime $G_{Total} = 0$, it means that to maintain oscillations the positive resistance of the tank is cancelled by the restoration element with negative conductance. The impedance of the parallel RLC tank, for $\Delta\omega \lll \omega_0$ is calculated by

$$|Z(\omega_0 + \Delta\omega)| = \frac{1}{G}\frac{\omega_0}{2Q\Delta\omega}. \quad (19)$$

Here it is possible to state that phase noise is greatly influenced by quality factor, Q. For an inductor-based oscillator, Q refers to the quality factor of the tank circuit, the higher the value of the inductor the closer it comes to an ideal behavior. It can be found that

$$Q = \frac{\omega_0 L}{R}. \quad (20)$$

Equation (19) shows a 1/ Δf passband characteristic around ω_0. From (18) and (19) the output mean square voltage noise at the tank terminals is obtained

$$\overline{v_n^2} = \overline{i_n^2}\,|Z|^2 = 4kTR\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2. \quad (21)$$

Equation (21) shows that improving quality factor can lead to a phase noise reduction. From (21) and (23) it is possible to calculate phase noise by:

$$L(\Delta\omega) = 10\log_{10}\left[\frac{2kT}{P_{SIGNAL}}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]. \quad (22)$$

From this equation, more effects are possible to recognize, the $1/\Delta\omega^2$ behavior is due to thermal noise filtered by the LC tank. But this model only predicts $\Delta\omega^2$ band region and flicker noise is not included.

A more complete model is needed to describe the phase noise. Leeson proposed the following semi-empirical equation based on (22):

$$\mathrm{L}(\Delta\omega) = 10\log_{10}\left[\frac{2\mathrm{FkT}}{\mathrm{P_{SIGNAL}}}\left(\frac{\omega_0}{2\mathrm{Q}\Delta\omega}\right)^2\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right], \tag{23}$$

where a behavior is predicted as well as an empirical fitting parameter (F). This parameter models the additional noise that comes from transistors and other elements not generated by the tank losses.

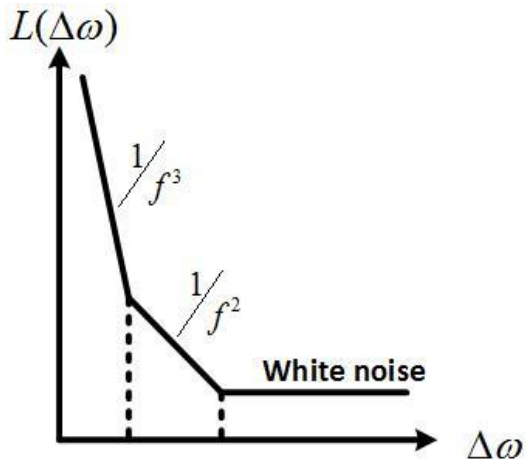

Figure 17 - Asymptotic graphic of phase noise.

4 LC Tank circuit design

For this application, the oscillator needs to be tunable and able to select all channel frequencies in the system band. The capacitor bank is made with digitally controlled capacitors, where a tuning word is applied, which will determine the capacitive mode (on or off) of each capacitor. This chapter presents the circuitry of the DCO tuning tank.

This chapter starts with investigating the method to be used in sizing the banks of capacitors, afterwards the inductor study and finally the critical part, the sizing of the bank of capacitors. From the frequency tuning range design, to the total tank capacitance and its flexible parameters like width, length and number of fingers which result in a large number of approaches to improve performance. Moreover, extracted post-layout are presented to get real components behavior, allowing to study additional parasitic capacitances.

4.1 Bluetooth Low Energy

Bluetooth Low Energy wireless standard is an ultra-low power 2.4 GHz RF technology that ensures short-range, low-power and low-rate communications. The high demand in wireless systems pushed the need of devices running from low capacity batteries into periods of months or years without recharge or replacement.

The low energy system operates in the 2.4 GHz band at 2400-2483.5 MHz, and it uses 40 RF channels. These RF channels have center frequencies in

$$f_0 = 2402 + k \cdot 2\ \text{MHz},\ \ k = 0, \dots, 39. \tag{24}$$

The modulation used is Gaussian Frequency Shift Keying (GFSK). A binary one shall be represented by a positive frequency deviation, and a binary zero shall be represented by a negative frequency deviation in terms of the transmit frequency. For both symbols the time duration is 1 μs. For both deviations, the minimum frequency cannot be less than 185 kHz for better recognition.

The deviation of the center frequency during the reception/transmission packet shall not exceed ±150 kHz, including both the initial frequency offset and following drift. The frequency drift during any packet shall be less than 50 kHz.

4.2 Proposed method

Although most of the reviewed papers use three banks of capacitors, one is going to demonstrate tuning range sizing with the smallest change in capacitance. The possibility to achieve very fine resolution and cover all band by using the smallest capacitor.

From equation (25a), it is evident the high number of capacitors, N, needed to reach a frequency resolution of Δf = 12 KHz, with f_{min}= 2,4 GHz and f_{max}= 2,485 GHz. Furthermore, it would take a great amount of area and consequently off parasitic capacitances. In this example, even without fabrication dispersion influence, the capacitors number is very high.

$$\Delta f = \frac{f_{max} - f_{min}}{N}, \tag{25}$$

$$N = \frac{f_{max} - f_{min}}{\Delta f} \leftrightarrow N > 7000. \tag{25a}$$

If an inferior N is used, the resolution decreases, thus using small capacitors for digital control is not a viable solution. However, adding a series capacitor with higher value to the smallest capacitor in the tank circuit can be another solution. In this case the smaller capacitor is much more dominant in terms of equivalent capacitance. This can be exploited by making the small capacitor fixed while varying the bigger capacitor. The fixed capacitor value could be change for a lower value, however with this method only a few megahertz of resolution can be achieved, which is not satisfactory. This is mainly due to the limit of how small a capacitance is switchable in the available capacitors. So, to achieve kilohertz resolutions and cover the tuning range, the three banks of capacitors technique is chosen.

In the following sections the frequency tuning is proposed using three tuned capacitor banks, coarse, fine and thermometer, each one composed of several unit cells that can be individually switched. Each bank has a different tuning range and frequency resolution, used to cover the whole band.

4.2.1 Frequency tuning range using three banks of capacitors

The process of designing an oscillator starts by determining the inductor value and total capacitance variation. By modeling their losses by a parallel resistor the quality factor of the LC tank is given by

$$\frac{1}{Q_{tank}} = \frac{1}{Q_L} + \frac{1}{Q_C}, \tag{26}$$

where Q_L and Q_C represents the inductor and total equivalent capacitance quality factor, respectively. Consequently, Q_{tank} is dominated by the component which has the lower quality factor, usually the inductor. Quality factor has great influence, it defines the performance quality of the RF passive components in terms of their losses. The losses in tank circuit are represented by two resistances, the parallel equivalent resistance of the inductor r_{Leq}, and the parallel equivalent resistance of the capacitor, r_{Ceq}. The resistance, R_{tank}, is calculated through the parallel of the first two. To achieve ultra-low power performance the losses of the tank circuit must be minimized. The equivalent parallel resistance of the tank is given by

$$R_{tank} = \omega_0 \cdot L \cdot Q_{tank} \,, \tag{27}$$

where L is the differential inductance. The main source of parasitic capacitances is provided by the switchable capacitors, so its reduction to minimum is vital.

The frequency range sizing starts by studying the banks unitary cells and finishes with the banks implementation. Firstly, to size the banks, DCO frequency tuning range is constrained by the number of components in the circuit and, as a consequence, is limited by parasitic capacitances. The total DCO capacitance can be estimated by

$$C_{total} = C_{fix} + \Delta C \,. \tag{28}$$

In (28) C_{fix} represents all the DCO capacitance values that exist when all banks capacitors are turned off, and ΔC is the capacitance increment that depends on the bank controlling digital words. Parasitic capacitances will be considered later, during C_{fix} and ΔC circuits layout design. From Figure 18 scheme, it is possible to understand the technique used to size the whole tuning range. The capacitance limits are calculated by

$$C = \frac{1}{4\pi^2 {f_{osc}}^2 L}. \tag{29}$$

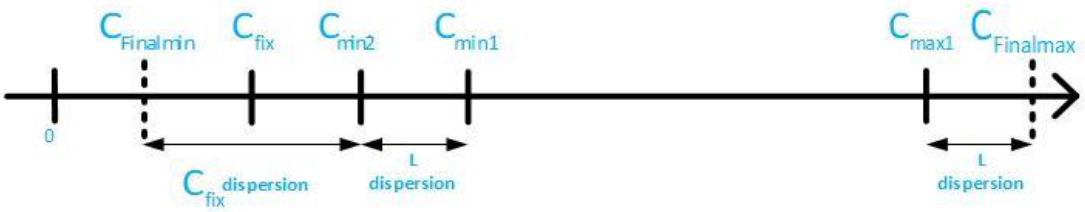

Figure 18 – Scheme used to dimension the covered band.

The tuning range sizing is performed considering components fabrication dispersion. It starts by specifying the tuning range between F_{min} and F_{max} that should be covered under inductance and capacitances maximum or minimum corners. Using equation (29), with typical capacitance and inductance values, C_{max1} and C_{min1} are calculated. Taking into consideration inductor dispersion, $C_{Finalmax}$ and C_{min2} are presumed. The minimum tank's capacitance is

$$C_{min2} = \frac{1}{4\pi^2 {f_{max}}^2 L_{max}}. \tag{29a}$$

T and the maximum tank's capacitance is

$$C_{Finalmax} = \frac{1}{4\pi^2 {f_{min}}^2 L_{min}}. \tag{29b}$$

For lower frequencies, when capacitance is higher, the inductor's worst-case corner occurs with minimum value, and vice-versa for higher frequencies. The critical situation happens

at the highest frequencies, when the C_{total} has a smaller value. The typical capacitance value C_{fix} represented in Figure 18, is chosen considering its tolerance and not to exceed C_{min2}. The final range is finally obtained between minimum C_{fix} value, which is named $C_{Finalmin}$, and $C_{Finalmax}$. While dimensioning, it is important to assure that total DCO capacitance for this case is lower or equal to $C_{Finalmin}$. It is preferable to be lower and to use a fixed C_{extra} to match the necessary $C_{Finalmin}$. This way it's possible to control inaccuracies of parasitic capacitances estimation after post-layout simulation results or to accommodate an output buffer input capacitance.

4.2.2 Bank cells operation

From the operational perspective, equations 30 to 32 describe how the three different banks adjust the capacitance. Capacitors are controlled by bits to obtain a high or a low capacitive state. The control bit toggles between the highest and the lowest power supply voltages which are 1.2 V and 0 V, respectively. The capacitive difference between high and low capacitive states is considered to be the switchable capacitance. Capacitance values in each mode can be calculated by

$$C_{CT}(N, n, f) = N \cdot C_{CLU}(f) + n \cdot \Delta C_{CHL}(f), \tag{30}$$

$$C_{FT}(M, m, f) = M \cdot C_{FLU}(f) + m \cdot \Delta C_{FHL}(f), \tag{31}$$

$$C_{TT}(P, p, f) = P \cdot C_{TLU}(f) + p \cdot \Delta C_{THL}(f). \tag{32}$$

Parameters $C_{CT,}$ C_{FT} and C_{TT} correspond to the total capacitance of each bank. C_{CLU}, C_{FLU} and C_{TLU} correspond to the unitary cells capacitance in low-capacitance mode and ΔC parameters are the capacitance increments that each unitary cell can provide when turned on. Parameters N, M and P are fixed numbers indicating the total number of cells in each bank and n, m and p are the number of capacitances turned on, in charge of frequency tuning. The generic center resonant frequency can be expressed by

$$f = \frac{1}{2\pi\sqrt{L \cdot (C_{CT} + C_{FT} + C_{TT})}}. \tag{33}$$

The inductor value is fixed, and the capacitance is the sum of all capacitors cells. The used capacitors are responsible to cover the frequency range that is assigned to the DCO. The highest frequency of the DCO is achieved when all cells are in their off-state, low capacitance mode, whereas the lowest frequency is achieved with the highest capacitance value.

Before getting into details it is important to clarify differences between unitary and binary weighted banks. Using a unitary weighted bank structure there are no restrictions concerning the number of capacitors or step capacitance, each cell is connected individually. Meanwhile, using binary weighted banks, as the name suggests, they are connected binary. However, there is one hypothesis where all capacitors are on and the last increment does not happen, the capacities

after the last increment are achieved by other bank cells. And in the second option, the last increment reaches C_{max} and following bank steps are also added. Figure 19 illustrates both cases. Now, giving these two hypotheses there will be different ways of dimensioning the step capacitance. Being k the number of bits and N the number of intervals, $N=2^k-1$ in the first case and ΔC is calculated by equation (34). If the bank is chosen to be binary weighted using $N=2^k$ the band is planned to use a step slightly higher than the first case to reach C_{max}, using equation (35).

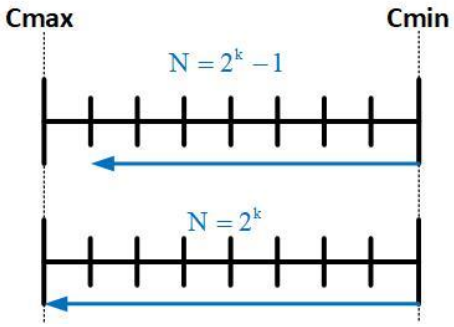

Figure 19 - Illustration of two methods for sizing binary weighted banks .

$$\Delta C_{binaryStep} = \frac{C_{max} - C_{min}}{2^k}. \quad (34)$$

$$\Delta C_{binaryStep} = \frac{C_{max} - C_{min}}{2^k - 1}. \quad (35)$$

To design the LC tank, all variables from equations (30-32) are related and must fulfill determined specifications. Firstly, one must calculate the capacitance tuning range sizing (C_{max}-C_{max}). Afterwards, the step capacitance of each bank is calculated considering some notions. As will be explained thoroughly ahead, these notions go through a first coarse hypothesis (2,3,4 or 5-bit) and a pre-determined fixed ΔC thermometer (12 kHz). Having the tuning range and ΔC for each bank, the number of P.M and N are provisionally estimated, using an excel sheet. Later is designed a cell to meet each ΔC found and so unknown parameters of equations (30-32) can be estimated, off state capacitance and step capacitance, without capacitor dispersion.

Analyzing all capacitors characteristics and parasitic and by going through several iterations and considerations, it is possible to find an optimal solution for each cell. The capacitance step and the total off state capacitance is identified proceeding to post-layout simulations. The chosen cell must satisfy minimum case dispersion of both capacitor and inductor.

The next equations were used in the excel sheet to make sure that the number of capacitors of each bank and the value of on and off state capacitance would comply with the worst case dispersion.

The number of coarse unit cells is calculated by

$$N = \frac{C_{FinalMax} - C_{FinalMin}}{\Delta C_{CoarseMin}}, \quad (36)$$

where the minimum corner scenario for N, is calculated with the whole tuning range divided by the coarse capacitance step, $\Delta C_{CoarseMin}$, for the minimum corner.

In the case of the fine bank the minimum corner case is given by

$$M = \frac{\Delta C_{CoarseMax}}{\Delta C_{FineMin}}, \quad (37)$$

where $\Delta C_{CoarseMax}$ is the capacitance step of the coarse bank for the maximum corner and $\Delta C_{FineMin}$ represents the fine step for the minimum corner.

Frequency resolution is determined by the thermometer bank because is the finest frequency step. In the design, 12 kHz resolution for thermometer bank must be accomplished.

$$P = \frac{\Delta C_{FineMax}}{\Delta C_{ThermometerMin}}, \quad (38)$$

where $\Delta C_{FineMax}$ is the capacitance step of the fine bank for the maximum corner and $\Delta C_{ThermometerMin}$ the capacitance step of the thermometer bank for the minimum corner whose Δf value must be equal or lower than 12 kHz.

Resuming, it is desirable to find capacitor cells where the worst dispersion cases of each step can be obtained. The next sections have detailed information about variables which influence the performance of the inductor and varactors/capacitors in each bank.

4.2.3 Parameters

Before choosing any number of capacitors it is relevant to state some notions. The coarse bank will have a higher frequency range than fine and thermometer banks, therefore it dominates the losses. Designing the LC tank circuit will meet various difficulties and challenges, the primary one is the frequency tuning band. The coarse bank is responsible to cover the whole band. There are two possible variable parameters to cover a tuning band, the number of capacitors and the capacitance step size. From equations (29a) and (29b), the capacitance step size is related with the wanted frequency step by

$$\Delta C = \frac{1}{L[2\pi(f_2 - f_1)]^2}. \quad (39)$$

There must be a trade-off between the number of capacitors and the step capacitance. Therefore, the following parameters have to be analyzed and compared:

- Equivalent parallel capacitance in ON and OFF state;

The capacitance analysis is the key to size the banks. Requiring high or low capacitance, their ratio r must be analyzed.

- Equivalent parallel resistance in ON and OFF state;

An ideal situation would be an equivalent resistance as high as possible in ON or OFF capacitance states.

- Layout area;

It is without doubt an advantage to have as lower area as possible.

There is another requirement that can't be forgotten. There is a relationship between the capacitance step of a bank with the capacitance range of the other bank that will fulfill the first bank step. Ideally these values would be equal. To overcome any potential matching problems, it is necessary to have a small overlap between the range of the banks. The relation between capacitance step and total capacitance variation of consecutive banks is shown in Figure 20.

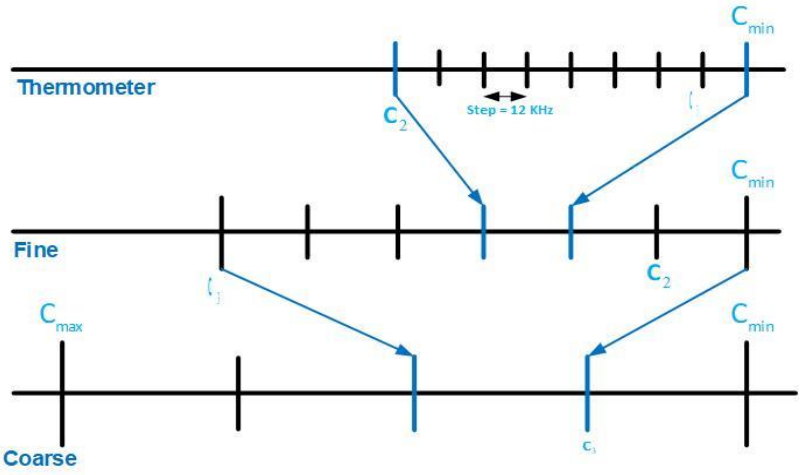

Figure 20 - Implemented DCO using three modes of operation.

4.3 Inductor

In this resonator an inductor is used in parallel with the capacitor banks. It is a passive element which can highly influence the performance of the resonator. Monolithic inductors fabricated as simple planar spirals are widely used in RF designs. As described in [33], the monolithic inductor value is defined solely by its geometry. Tight geometric tolerances inherent to most modern photolithographic processes ensure small fabrication dispersion. The circular spiral inductor can be found in the available components provided by 130 nm technology.

The model used to characterize the inductor is based on a π network. Thus, for a better understanding of inductor behavior, a differential simulation was made to obtain its equivalent admittance, given by equation 40:

$$Y_L = G_L + jB_L = \frac{1}{r_{Leq}} + j\,\frac{-1}{\omega Leq}. \tag{40}$$

Figure 21 presents equivalent parallel resistance and quality factor obtained with a small-signal analysis. Taking equation (2) in mind, it's possible to compute Q_L by

$$Q_L = \frac{r_{Leq}}{\omega L_{eq}}, \tag{41}$$

and equivalent inductance by

$$L_{eq} = \frac{-1}{\omega B_L}. \tag{42}$$

For several values of inductor, from 1 nH to 4 nH, the equivalent parallel resistance and quality factor are analyzed. Achieving ultra-low power consumption is the main goal, thus it is desirable to achieve at all costs higher r_{Leq} as possible, in order to reduce the oscillator load effect. Please note that maximizing r_{Leq} does not means that Q_L is maximized and, consequently, phase noise minimized. But because phase noise requirements are relaxed, the power consumption is more important.

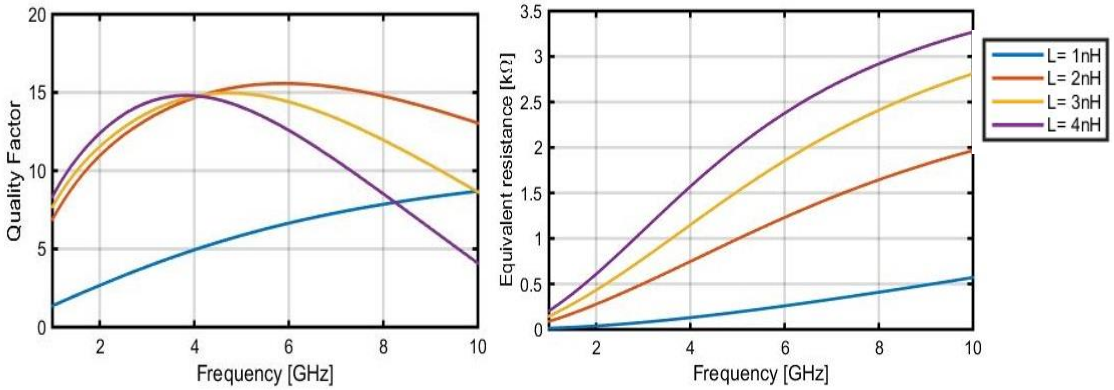

Figure 21 - Simulation results for the inductor values 1 nH, 2 nH, 3 nH and 4 nH; (left) – quality factor; (right) –inductor equivalent parallel resistance.

For higher inductor values, Figure 21 (right) shows lower losses, being what best fits for the design. Quality factor is almost the same for lower frequencies, slightly better for 4 nH. As the frequency gets higher the Q factor is dominated by subtract losses.

4.4 Bank unitary cells analysis

4.4.1 Capacitors and varactors analysis

The perfect solution for a capacitor would require having low C_{off} capacitance, high Q and low layout area. As mentioned before, when comparing MIM and MOM capacitors, the switched MOM shows more advantages. In practice, both provide similar C_{off} , however Q factor is higher in MOM capacitors, but the huge disparity that makes MIM capacitors an invalid solution is the occupied area. For the same value, MIM capacitors present three times the area of MOM capacitors. Comparing both minimum capacitances, MIM capacitor is ≈ 105 fF and MOM capacitor ≈ 68 fF. MOM capacitors are preferred due to lower area occupation.

In case of a high-resolution bank covering a small frequency range, the solution goes through the use of varactors. The following figure compares the three existent varactors available in the technology, VARDIOP_RF, VARMIS_12_RF and VARMIS_33_Rf.

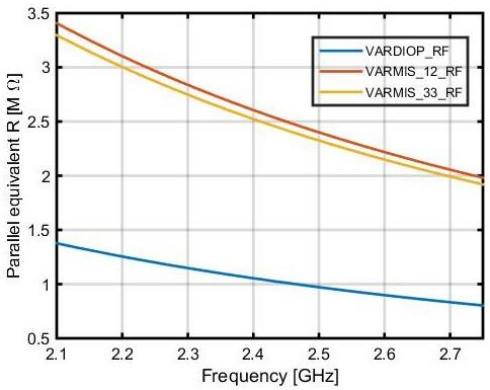

Figure 22 – Parallel equivalent resistance for three different varactors models presented in the technology.

Figure 22 presents three varactors values with their minimum capacitance value (8 fF). The best trade-off value is reached by VARMIS_12_RF, which achieves 8 fF and 3.4 MΩ of parallel equivalent resistance (R_{eq}). The corresponding area of this varactor is 4.85 x 2.92 μm², times two due two differential circuit. Although we can get satisfactory results, there is an alternative approach commonly used for very fine resolution which has less area occupation, which is a cell composed by two almost equal MOS transistors. For the same capacitance value, the area is reduced by half comparing to VARMIS_12_RF. With minimum MOS transistors length, width and finger size, the equivalent parallel resistance can be extremely large whereas the minimum capacitance value is low as ≈ 59 aF. Let's not forget that these values still don't have any consideration for fabrication dispersion and post-layout capacitances, so in reality they will be higher.

The following sections will present circuit designs for each bank cell. This first approach small-signal analysis did not take into account neither fabrication dispersion nor parasitic capacitances.

4.4.2 Coarse unity cell

The main purpose of this bank is to cover the total frequency range, so high frequency steps are more suitable. To design the capacitor bank, it is common to control the binary-weighted MOM capacitors with MOS switches. The downside of this bank is the resistance and parasitic capacitances of the switch, which degrade the losses and capacitance tuning range. Figure 23 represents a simplified schematic of coarse unit cell. It consists in two MOM capacitors connected differentially with a series switch M0.

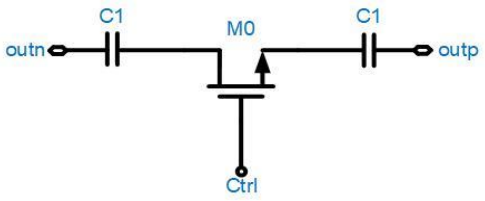

Figure 23 - Basic schematic of a coarse unity cell.

To choose values for the switch it's important to get the best trade-off between losses and tuning ratio (C_{off}/C_{on}). When the control bit is high, meaning Ctrl equals to V_{dd}, transistor M0 is on and shows a resistance depending on transistor parameters

$$R_{on} = \frac{1}{K\frac{W}{L}(V_{GS} - V_{th})}, \tag{43}$$

where W is channel width, L its length, K depends on technology, V_{GS} gate-source voltage and V_{th} threshold voltage. The equivalent capacitance is a series of the two C_1, the maximum capacitance is achieved in this on state.

The loss effect can be examined using the quality factor in equation (44). For higher Q the on-resistance of the switch must be as low as possible.

$$Q_{on} = \frac{1}{R_{on}C_{on}\omega}\ . \tag{44}$$

There are two ways to reduce the on resistance of the NMOS. One is reducing R_{on} by decreasing width and length parameters and consequently having lower drain and source parasitic capacitance. Another solution is to provide maximum gate-source voltage in order to minimize the on resistance. Two pull-down transistors are added to effectively turn the cell between its high and low capacitance states as shown in Figure 24. Like this during on-state the capacitors internal plates are grounded. This modification allows good frequency stability and noise immunity with respect to the digital control line voltage [34]. These transistors are chosen to be as small as possible to reduce the switches capacitance effect in the off state.

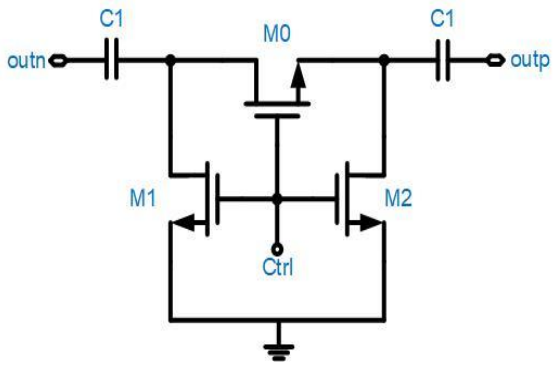

Figure 24 – Schematic of the final coarse cell.

The total capacitance is determined by the MOM capacitors and a small capacitance which models the switch in off state. The minimum capacitance is achieved in off state.

For a proper analysis, M0 available in the technology is examined in a small-signal simulation where it is floating. Parameters like length (l) and width (w) were changed.

The size of the transistors was chosen always taking in consideration equivalent series resistance as low as possible. Low series resistance is obtained by having high values of w and l. However, this will be accomplished at the cost of higher parasitic capacitances and area. A trade-off between these characteristics was achieved ahead.

Since coarse bank has wider frequency steps, binary weighted variation is the selected approach, rather than altering each unit cell. This ensures that the parasitic capacitance due to fringing electric fields, which is quite significant for a deep-submicron CMOS process and is extremely difficult to control and model, is well rationed and matched [28].

In Figure 25 a small-signal (S-parameters) coarse cell analysis is presented by simulating the equivalent parallel capacitance and resistance in on and off state, varying the finger length (10 µm - 40 µm), the number of the metal layer (3 - 6) and finger number (10 - 40). It's noticed that for higher values of step capacitance, the higher the number of fingers and layers, and consequently higher off capacitance (C_{off}). Theoretically, R_{eq} needs to be maximized in on and off state, more significant in on state, so looking at the bottom part of the image, using high a number of fingers is less favorable.

Possible solutions for the number of capacitors include having 4,8,16 and 32 capacitors. Considering using 4 capacitors, it would require huge capacitance steps. Such big step capacitance values would require the following banks (fine and thermometer) to cover a wider range, inevitably needing more capacitors, which increases C_{off}. In case of using 32 capacitors it would happen the exact opposite, requiring very small step capacitance, not achievable by this cell circuit, since the minimum step capacitance achievable is 21 fF. In conclusion, the only hypothesis worth to consider are the ones using 8 and 16 capacitors. Figure 26 shows several options of finger lengths to use in either 8 or 16 capacitors. To solve this problem, a detailed S-

Parameters is done to exactly find the best compromise between step capacitance and losses. The simulation is identical to Figure 25, however the number of fingers is fixed as 10 and the number of layers is changed between 3 and 6.

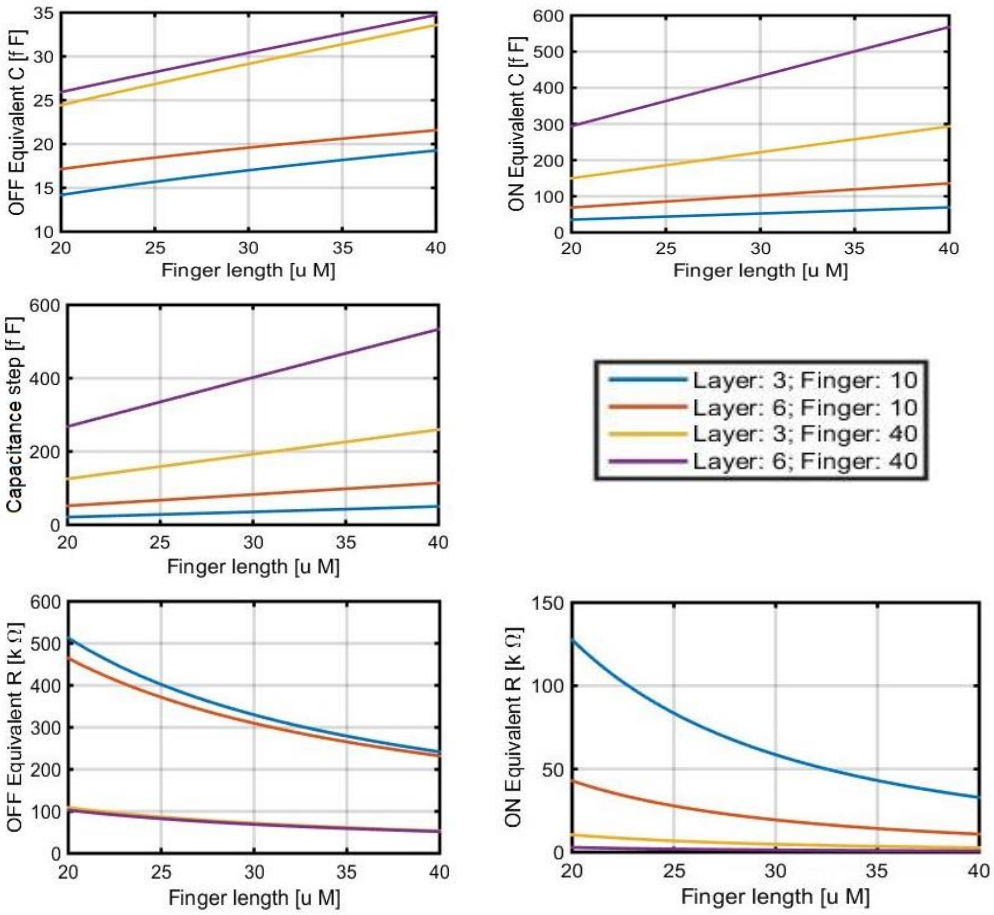

Figure 25 - Simulation results of the coarse cell capacitance in on and off state (top); step capacitance (middle); equivalent parallel resistance in on and off state (bottom); varying finger length between 20 and 40 µm and for different values of layers and fingers.

Comparing both, the first hypothesis needs higher step capacitance however using less capacitors. As the capacitance step increases more layers need to be used. The higher the number of metal layers, the lower the space between the subtract and metals, increasing parasitic capacitances as seen above. In case of 16, the step capacitance is smaller, so less influence from subtract losses. However, increasing the number of capacitors has the major drawback of reducing the maximum achievable frequency by the DCO since increasing the number of varactors will introduce more parasitics to the tank which will also increase the total off state capacitance of the bank. After this analysis, it's possible to reduce the possibilities of design to 3 and 4-bit coarse control.

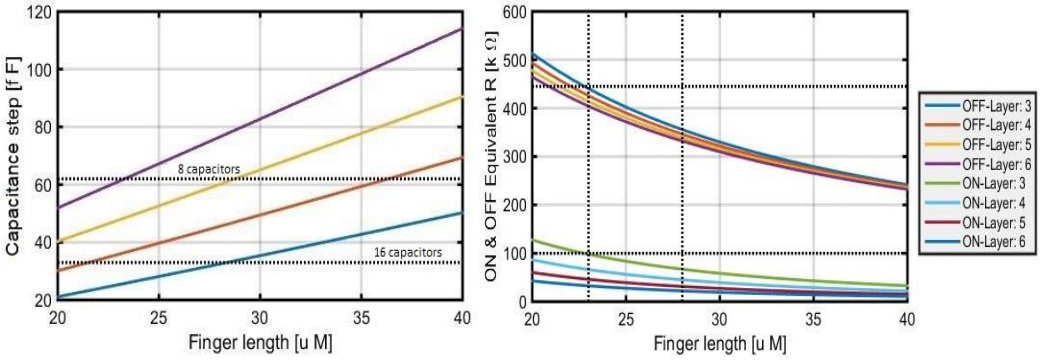

Figure 26 - Simulation results for the coarse step capacitance (left) and equivalent parallel resistance in on and off state (right), varying finger length between 20 and 40 µm and for different values of layers and finger = 10.

4.4.2 Fine unity cell

The fine bank main purpose is to provide higher frequency resolution over a specified frequency range, therefore, smaller ΔC than coarse bank cell and also binary weighted. To reach small values of ΔC and to avoid the effect of on-resistance of the switches, MOS transistors are used. Although NMOS varactors have less parasitic capacitances, to have the same control logic level as coarse bank, PMOS varactors were chosen. In this case the Q factor and tuning ratio depend only on the varactors because additional components do not exist. A simple schematic is introduced in Figure 27.

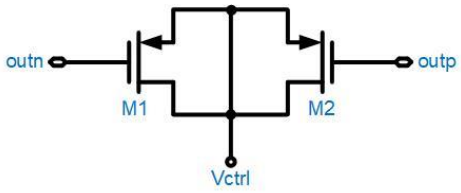

Figure 27 - Schematic of the fine bank varactor with PMOS.

For such small step values, a small-signal analysis of capacitance varying width is performed as shown in Figure 28. The length parameter is examined between maximum and minimum possible values. The number of fingers is fixed to 1, to get minimum values, and therefore to be able to obtain a high frequency resolution.

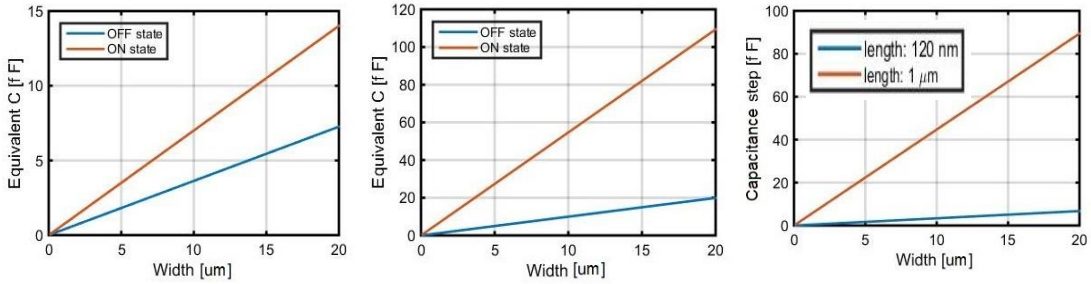

Figure 28 - Simulation results for capacitance in on and off state depending on the width of the transistors and varying the length; (left) – length of 120 nm; (middle) – length of 1 µm; Step capacitance for each length (right).

Figure 28 illustrates the range of values that can be obtained by the varactor, being the minimum capacitance value 59 aF. In this bank, there aren't many alternatives regarding capacitors number since it's binary weighted. It will also be reliant on the number of coarse cells chosen. In Figure 29, is presented a more insightful way to analyze the fine cell. The possible number of fine cells is 63,127 and 255 for the tuning band range pretended.

As the resolution gets higher, more influent it becomes with parasitic capacitances. Thus, as observed on the left of Figure 29, lower width turns into lower C_{off}. On the right of Figure 29 is illustrated the comparison between different values of length, 120 nm and 130 nm, the off parallel equivalent resistance ($R_{eq,off}$) is similar in both cases. The main concern is in the $R_{eq,on}$, it can be noticed a subtle increase for lower length. Regarding C_{off}, the difference between both is practically minimum but is lower for lower length.

Based on schematic simulations, it would be ideal to use as low values of length as possible and width wide enough to get on and off equivalent resistance as high as possible. The next step consists in analyzing the extracted typical fine step and its respective parasitics, and as will be seen, the increase of length will diminish the additional capacitance parasitic.

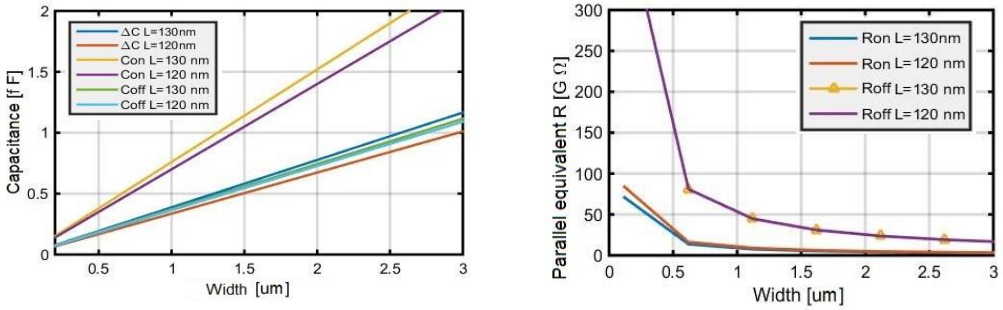

Figure 29 - Simulation results for capacitance (left) and equivalent parallel resistance (right) depending on the width of the transistors and varying the length, in on and off state.

4.4.3 Thermometer unity cell

The last bank is unity weighted encoded mainly to achieve the smallest frequency step. The unit cell is composed by PMOS varactors to achieve the smallest values of capacitance possible. The thermometer bank provides the desired frequency resolution which brings the ratio C_{max}/C_{min} close to one. In a first approach, the circuit arrangement was the same used in the fine bank, but it was impossible to meet the 12 kHz frequency resolution specification. The minimum C_{on} value would go down to 112 aF but, due to high C_{off}, the tuning ratio wasn't even close to one, so a finest step capacitance couldn't be achievable.

Another method to get a very fine resolution is to use the circuit on Figure 30. There are two pairs of transistors (M1 & M2 and M3 & M4) with a small difference in widths and opposed controlling voltages. The working mechanism controls the capacitance step using the difference of the two switched varactors. The switching process is made by small transistors M5 to M8, which have the minimum values (l=120 nm, w=160 nm).

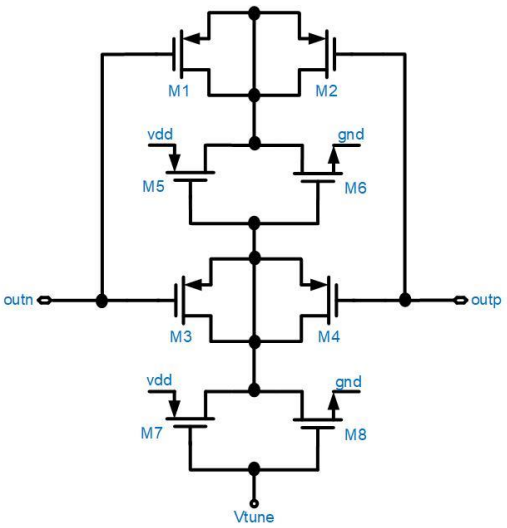

Figure 30 - Schematic of the thermometer unity cell.

A typical small-signal analysis is realized to understand the influence of the width and length difference between the transistors pairs. Figure 31 presents the step capacitance from the circuit with l=120 nm and 130 nm and with several increments (D) between pairs. For example, if D = 10 nm and width = 200 nm, the respective values for M1 & M2 and M3 & M4 is 210 nm 200 nm, and the capacitance step can be as low as 4 aF.

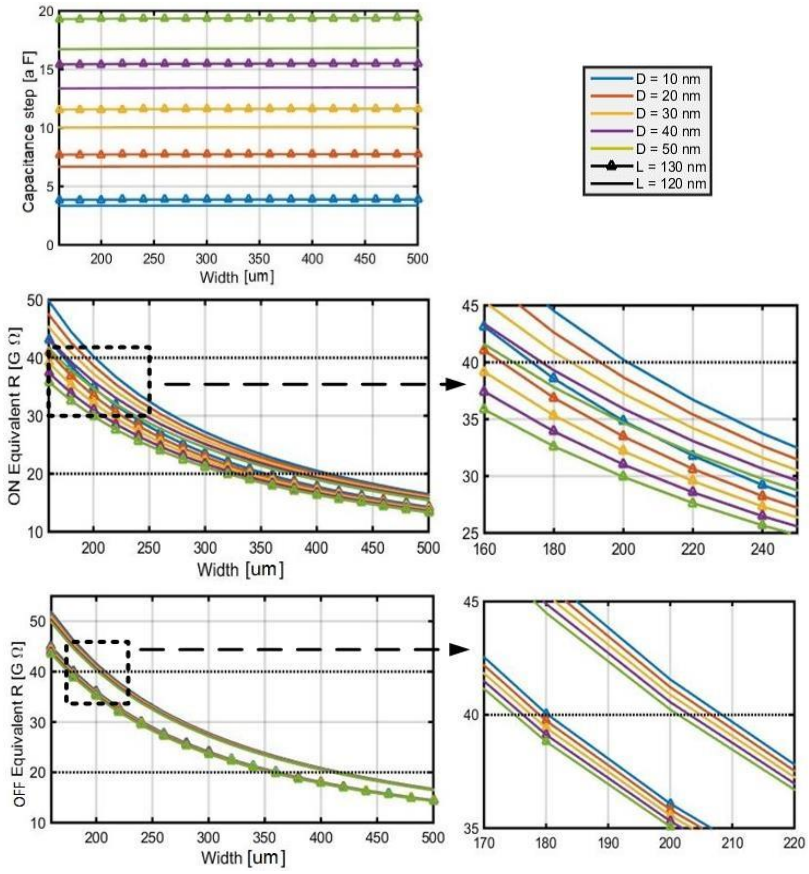

Figure 31 - Simulation results for the thermometer cell capacitance step (top); R_{eq} in on state (middle); R_{eq}in off state (bottom); varying width between 160 and 500 nm and for different increments.

The estimated thermometer capacitance step using equation (39) is around 5 aF, so as seen on top of Figure 31, with this circuit it's possible to achieve this range of value. As occurred in the cells analysis before, the equivalent resistance in on and off state diminishes for wider width. However, to maximize $R_{eq,on}$, it's known that lower increments and lower lengths are preferable. Even though these simulations help get through basic transistors analysis and possibilities, to have an idea of possible values, and to get a conclusion an extracted simulation of the thermometer cell must be made.

4.5 Banks design and layout

4.5.1 Number of cells

With optimizing features available in the design kit, a typical inductor value of 3.6 nH is chosen, where Q and r_{Leq} have the best trade-off. For the chosen inductor value, the equivalent inductance is presented in Table 4 for different process corners.

Table 4 - Inductor extracted values.

Inductor process corners [nH]	Maximum	Typical	Minimum
	3.8	3.6	3.4

For the desired band, F_{min} = 2,4 GHz and F_{max} = 2,485 GHz, C_{max1} and C_{min1} are calculated with equation (29), using the inductor typical value presented in Table 4. In order to mitigate inductor dispersion, one looks to corner values, the maximum process corner variation was 5%, so, as a safe margin, a 10 % dispersion was chosen. The final inductor values used are presented in the following table.

Table 5 - Inductor values assuming 10% fabrication dispersion.

Inductor process corners [nH]	Maximum	Typical	Minimum
	3.96	3.6	3.24

For this dispersion new capacitance values are calculated using the new inductor values, $C_{Finalmax}$ = 1,292 pF and C_{min2}=1,080 pF. The critical situation happens at the highest frequencies, when the capacitor values are smaller. Capacitance C_{fix}, that takes into account all the fixed DCO typical capacitance, also suffers from fabrication dispersion. A deviation of 15 % was assumed for this dispersion, thus $C_{fix} = C_{min2}/1{,}15$. Finally, the worst case minimum capacitance for ΔC calculation is $C_{Finalmin} = C_{fix} - C_{fix} * 0.15$. Table 6 shows all capacitance values calculated, being the total capacitance range obtained between $C_{Finalmin}$ and $C_{Finalmax}$.

Table 6 - Capacitance values for the tuning range band.

Capacitance [pF]	C_{max1}	$C_{Finalmax}$		
	1.222	1.292		
	C_{min1}	C_{min2}	C_{fix}	$C_{Finalmin}$
	1.139	1.080	0.939	0.798

While simulating process corners of each cell the maximum percentage of variation obtained by the coarse cell was 10%, so 15% is chosen to secure coarse dispersion. To make sure the band is covered with safe margin, 20% capacitor variation was chosen for fine bank and 30% for thermometer. For C_{fix}, represented in equation 28, it is estimated a maximum deviation of 15%.

The three banks are parameterized according to the defined range band. After a schematic analysis of each cell and resorting to an excel sheet it's possible to understand the relation between number of capacitors and step capacitance of all banks. After ΔC estimation it will be possible to obtain the on and off state capacitance. In case of coarse cell sizing, it is chosen the 4-bits control word hypothesis, the estimated ΔC is 33 fF, meaning this value represents the minimum coarse ΔC. The minimum capacitance step parameters for each cell are represented in Table 7, where fabrication dispersion and post-layout extractaction is overlooked.

Table 7 - Minimum capacitance step values and number of capacitors, theoretically calculated.

	Coarse	Fine	Thermometer
Minimum Δc	33 fF	260 aF	5 aF
Number of capacitors	15	127	32

The following sections present the extracted simulations analysis with fabrication dispersion for each cell bank. The minimum step capacitances obtained must not be lower than the ones shown in Table 7 to succeed in covering all tuning range.

4.5.2 Coarse bank

In the latter section 4.4.2, two hypotheses are valid to examine, 3 and 4-bit step. As seen in Figure 32, as the capacitors finger lengths get larger,the equivalent resistance in on and off states reduces. Hence, it's needed to minimize the length to maximize $R_{eq,on}$. Comparing results between layers, it is also clear that the higher the layer, the lower the $R_{eq,on}$. Based on these considerations, to obtain around 33 fF of minimum step capacitance, 3-bit control word with 6 layers and ≈24 μm of finger length or 4-bit control word using 4 layers and ≈25 μm, can be used. The option whose parallel equivalent resistance can get maximized is the 4-bit choice.

Nevertheless, the coarse cell layout area for 7 capacitors can be estimated to be 75.8 x 7.44 = 563.952 μm², times 7 gives an equal to ≈ 3947 μm². For 15 capacitors, its respective

estimated total area is 69.8 x 6.64 = 463.472 μm², that times 15 is equal to ≈ 6952 μm². In terms of area the 3-bit choice is preferable. Although, looking at the whole design banks, getting higher coarse steps will require more fine and thermometer cells to cover the range, meaning more area and more metal connection between those bank cells which contribute to ohmic losses.

From all the analysis realized until now, it is desirable to use 15 identical unit cells, binary weighted connected through a 4-bit control word. Now, due to parasitic effects, extracted post-layout simulations are necessary to evaluate the performance and requirements of each cell and consequently of the whole block.

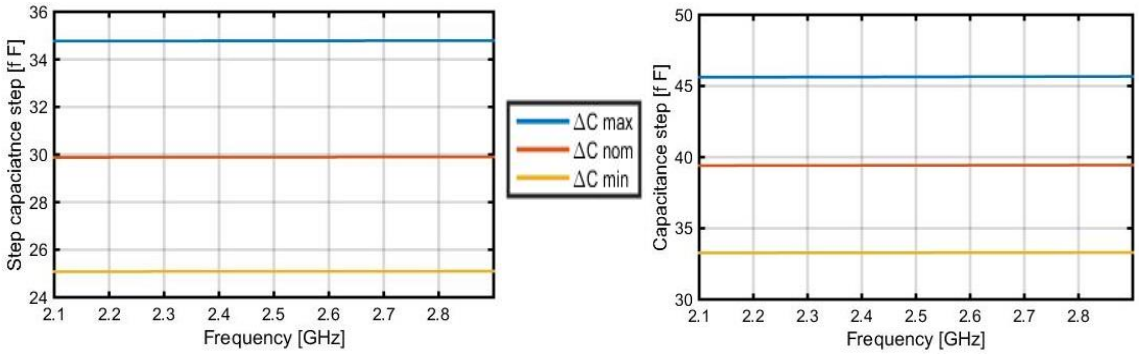

Figure 32 - Simulation results for the capacitance step for a fixed value of fingers,4, and different values of finger length; 20 μm (left) and 25 μm (right).

To achieve the capacitance required, using 15 coarse cells to cover a total range band of 494 fF, the minimum estimated unitary cell capacitance step is 33 fF. In Figure 32 is illustrated a first extracted analysis, with fixed finger number and different widths. Since MOM capacitors corner values can be reliable, it's not necessary to add 15% to $\Delta C_{\mathrm{coarse,min}}$. Using finger length equal to 25 μm, $\Delta C_{\mathrm{coarse,min}}$ = 33 fF can be achieved. The coarse cell equivalent parallel resistance characteristic is presented in Figure 33.

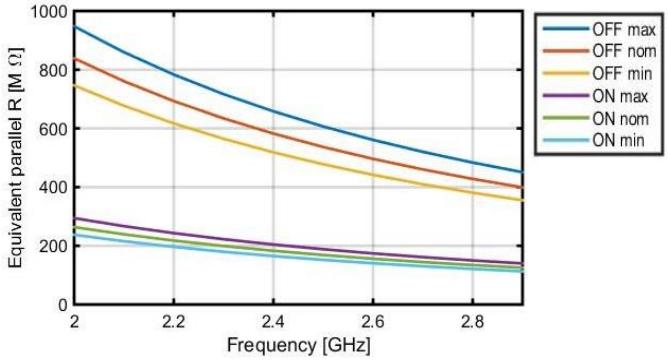

Figure 33 - Coarse cell post-layout simulation of the equivalent parallel resistance, using width equal to 25 μm, for different corners.

The targeted frequency range uses 15 identical unit cells, binary weighted. After post-layout RC extraction, the coarse bank produces about 10 % more of parasitic capacitance. Coarse

bank post-layout results are shown in Figure 34. The worst-case values in on state are $R_{eq,on}$ ≈ 31 kΩ and Q ≈ 38; evidently the quality factor was depreciated at the expense of getting R_{eq} high as possible to minimize power consumption.

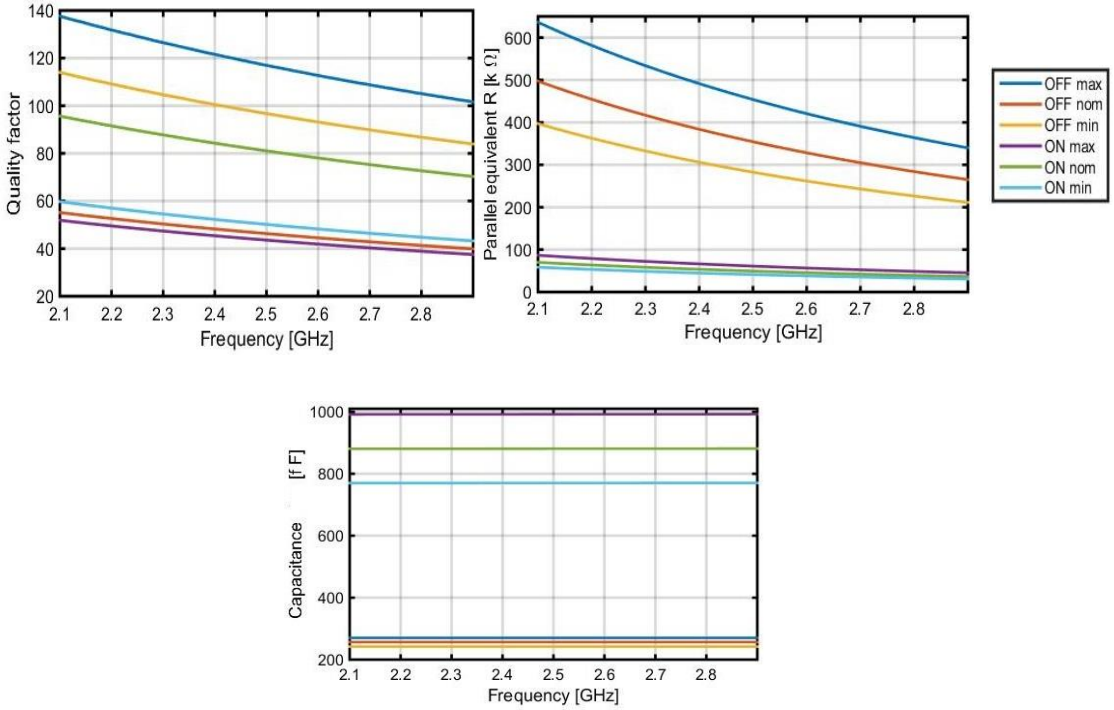

Figure 34 - Post-layout simulation results of the coarse bank using 4-bit control. Quality factor, parallel equivalent resistance and capacitance in on and off state for different process corners.

4.5.3 Fine bank

An extracted simulation was made for a fine cell, more important in this case because as the step values decreases, the more influent parasitic capacitances can be. Both simulated extracted cells have width equal to 2.5 μm but different lengths, 120 nm and 130 nm. The depicted results show that using a wider length can minimize parasitics influence, the difference between schematic and extracted is ≈ 55 aF for 120 nm case and ≈48 aF for 130 nm.

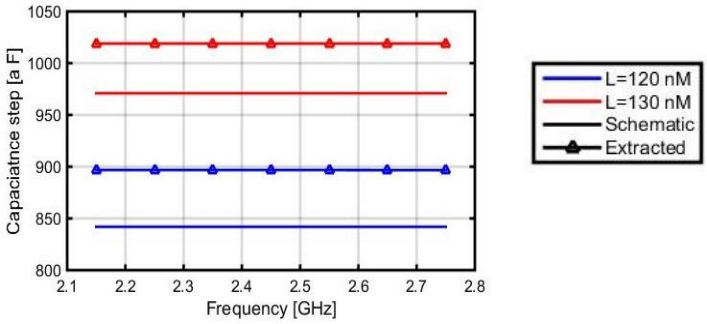

Figure 35 - Typical extracted and schematic fine step with w=2.5 μm and length equal to 120n and 130n.

Another important criteria one must not forget is the balance between the number of cells. The number of fine cells has to be chosen considering the area of each cell, the capacitance step

and its direct influence on the thermometer cells number. Table 8 helps to understand the co-relation between the three banks. With the 4-bit coarse control chosen, remain three plausible options for number of cells, 63,127 or 255. All steps presented were calculated using equations (36), (37) and (38) for the respective case and extracted $\Delta C_{coarse,max}$ = 46 fF.

Table 8 - This table aims to present the several alternatives for M's and P's for N=15.

M fine	63	127	255
ΔC fine min [aF]	730	362	180
P therm	204	101	54
ΔC therm min [aF]	5	5	5

In the beginning of the design, M= 255 was chosen to start the sizing, however, as will be stated later, the thermometer cell area is 3 times larger than fine cell. If the M=63 alternative is chosen a higher number of thermometer cells would be needed, and thus more occupied area. For the solution with 255 fine cells, one gets the desired trade-off between keeping high equivalent resistance and smaller area.

Using equation (36), the fine bank has to cover a band of maximum 46 fF, with 255 capacitors the minimal step capacitance calculated is 180 aF, but due to fabrication dispersion, a safety margin of 20% is added resulting in 216 aF. In opposition to what happened in the coarse cell, 20% of fabrication dispersion is added to $\Delta C_{fine,min}$ because this small value transistors corners are not guaranteed to be reliable. Fine cell main characteristics are presented in Figure 36.

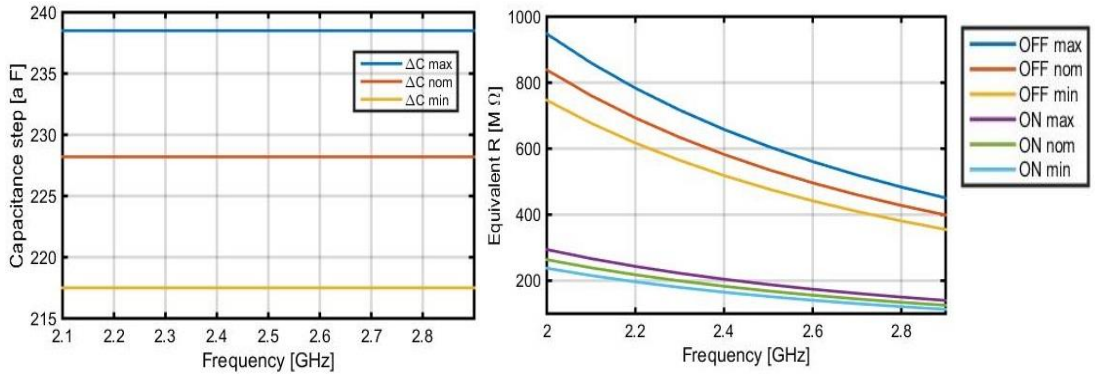

Figure 36 - Fine cell post-layout simulation of capacitance step and equivalent parallel resistance, for different corners.

The customized capacitor is realized by using 255 active PMOS varactors with 3 metal layers with a total size of 2.56 µm x 1.59 µm. Comparing post layout off state, extraction and schematic simulation, the fine bank produces more 90 % of RC parasitic capacitance. Fine bank post-layout analysis is presented above.

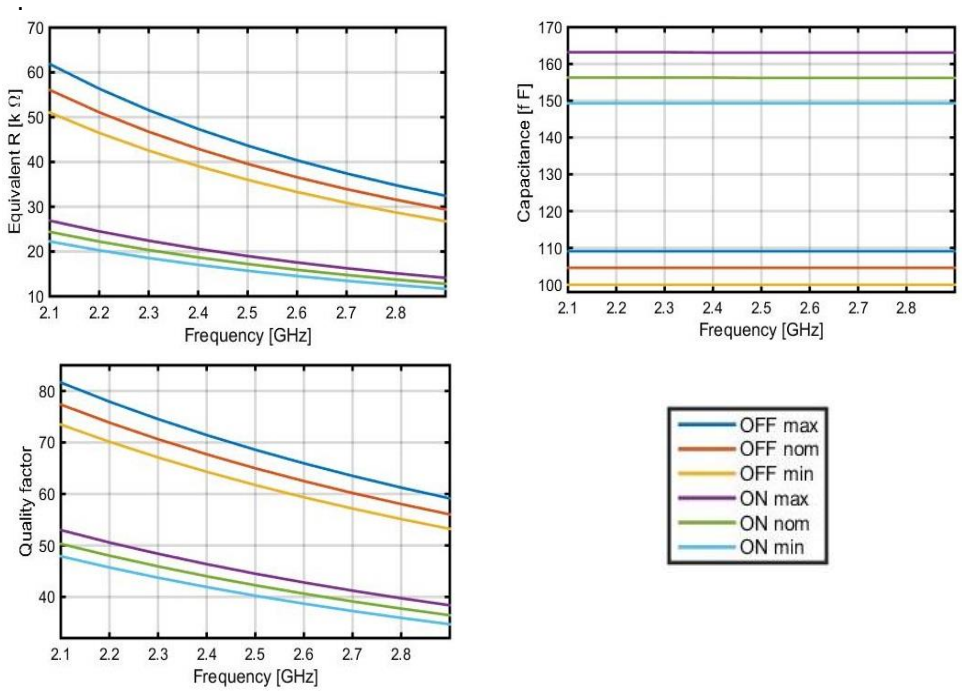

Figure 37 - Post-layout simulation results of the fine bank using 7-bit control. Quality factor, parallel equivalent resistance and capacitance in on and off state for different corners.

As seen in Figure 37, the worst case value in on state is $R_{eq,on}$ ≈ 14 kΩ and Q ≈ 35, being an improvement of the previous fine bank.

4.5.4 Thermometer bank

Finally, for thermometer cell the same method is used. The theoretically $\Delta C_{thermomter}$ calculated to achieve 12 kHz is in order of 5 aF, a value this low is even more susceptible to parasitics. From Figure 38, it is conclusive that lower width can get better results regarding $R_{equivalent}$, but before any parameters are chosen, the additional capacitances must be accounted for. The preceding analysis compares schematic and post-layout results for the minimum increment and two values of width.

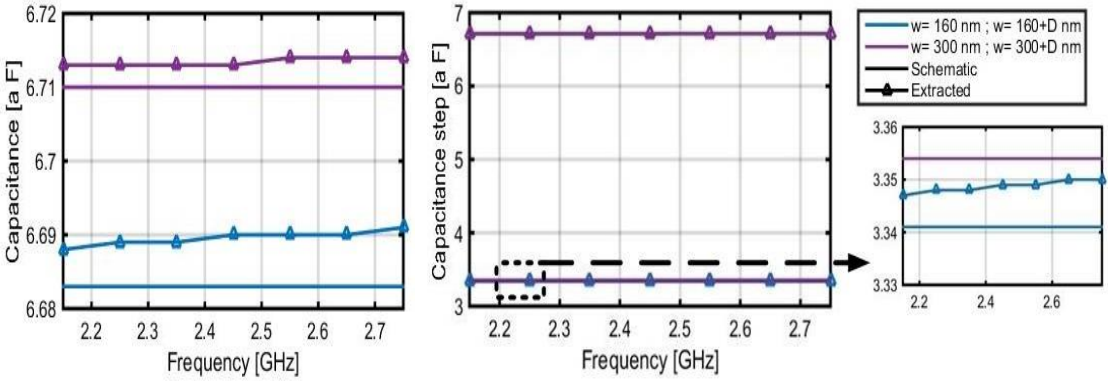

Figure 38 - Simulation results for the step capacitance extracted and schematic typical corner for D=20 nm (left) and D=10 nm (right); Different ranges of width are also compared.

Using equation (37), the thermometer bank must cover a maximum range of $\Delta C_{fine,max}$ = 239 aF. Due to fabrication dispersion, a safety margin of 30% is added resulting in 3.5 aF. To achieve the step capacitance required, the solution chosen is composed by the pairs M1 & M2 and M3 & M4 equal to 170 nm 160 nm respectively and length = 120 nm. The minimum possible values were chosen to achieve maximum possible resolution.

$$P = \frac{\Delta C_{fine,max}}{\Delta C_{thermometer,min}} = \frac{239\ aF}{3{,}2\ aF} = 75\ . \quad (45)$$

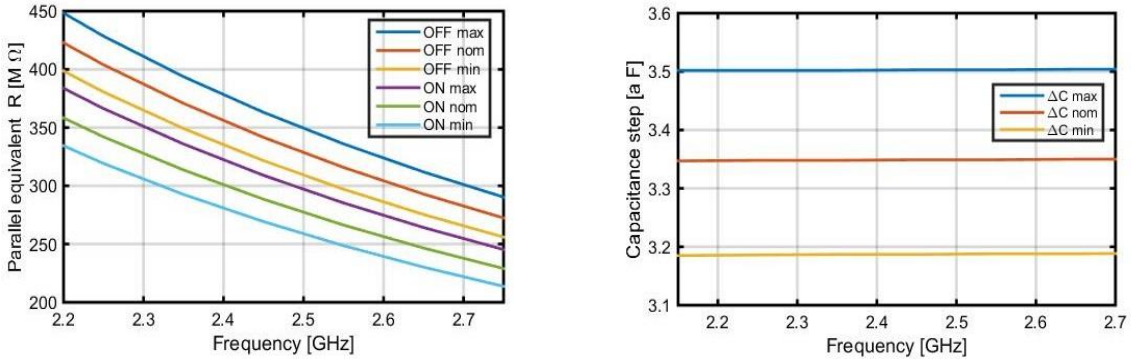

Figure 39 - Thermometer cell post-layout simulation of capacitance step and parallel equivalent resistance, for different process corners.

In Figure 40 is illustrated the main characteristics of the final thermometer bank. This bank is controlled by 75 unitary weighted capacitors As verified in Figure 40 (right), the minimum step capacitance is valid. Comparing post layout off state, extraction and schematic simulation, the thermometer bank produces more 503 % of RC parasitic capacitance.

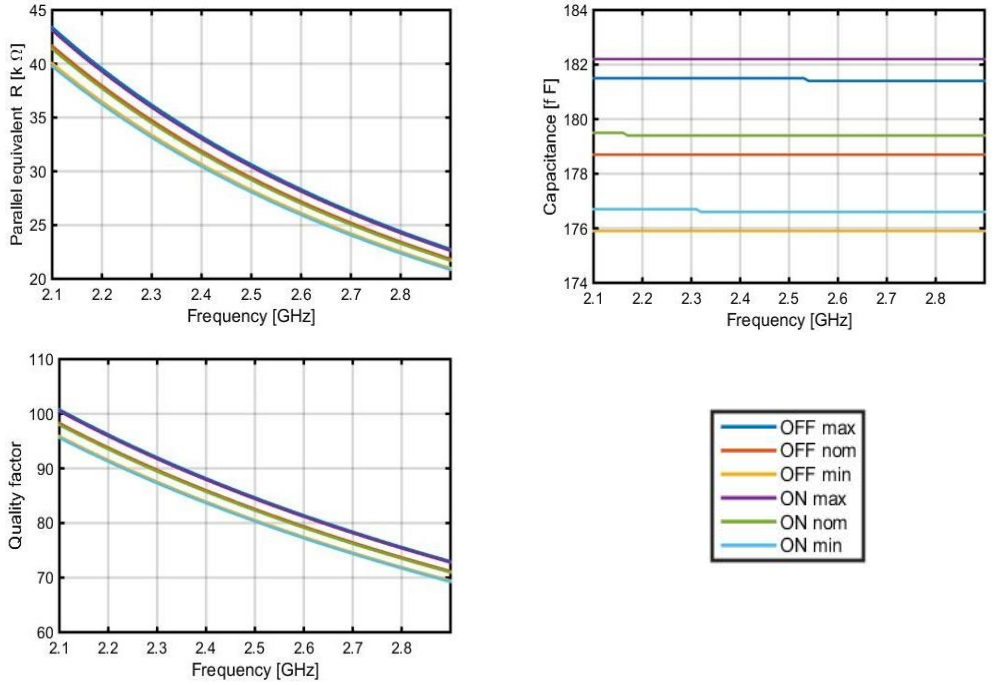

Figure 40 - Post-layout simulation results of the thermometer bank using 75 unitary bits. Quality factor, parallel equivalent resistance and capacitance in on and off state for different corners.

4.5.5 Total number of cells

To obtain a higher frequency tuning range, capacitors sizes had to be rectified The post-layout rectification for coarse bank was an increase from 25 µm to 26 µm. This was necessary because after post-layout analysis it was needed to increase the maximum capacitance in order to achieve lower frequencies. Table 9 shows each bit capacitance and respective step for the 4-bit binary weighted capacitors, being $C_{OFF,min}$ = 265.3 fF, the capacitance with all capacitors in off state and $C_{ON,min}$= 792.7 fF, in on state. The minimum step capacitance is now 35 fF.

Table 9 - Post-layout minimum corner capacitance values and respective step capacitance changing the number of capacitors in on state for the coarse bank

ON Capacitors	C_{min} [fF]	ΔC [fF]
L L L H	300.5	35.2
L L H L	335.7	70.4
L H L L	406	140.7
H L L L	546.7	281.4

For the same reason, fine cell was also increased to 600 nm, being the minimum step value ≈ 221 aF. Final parameters of the fine bank are presented in Table 10, presenting each bit capacitance and respective step for the 7 binary weighted capacitors, being $C_{OFF,min}$ = 100.034 fF, the capacitance with all capacitors in off state and $C_{ON,min}$= 149.302 fF, in on state.

Table 10 - Post-layout minimum corner capacitance values and respective step capacitance changing the number of capacitors in on state for the fine bank.

ON capacitors	C_{min} [fF]	ΔC_{min}[fF]
L L L L L L L H	100.254	0.22
L L L L L H L L	100.903	0.87
L L L H L L L L	103.565	3.53
L H L L L L L L	114.177	14.14
H L L L L L L L	121.24	21.21

Finally, in the thermometer bank post-layout analysis it was verified an increase of the $\Delta C_{thermometer,min}$. Hence, the number of cells was increased to 93 unitary weighted capacitors. In Table 11 are presented the extracted parameters for different number of capacitors on, being $C_{OFF,min}$ = 91.857 fF, the capacitance with all capacitors in off state and $C_{ON,min}$= 92.156 fF, in on state.

Table 11 - Post-layout minimum corner capacitance values and respective step capacitance changing the number of capacitors in on state for the thermometer bank.

ON Capacitors	C_{min} [fF]	ΔC_{min}[aF]
<93xL,1xH>	91.859	0.2
<84xL,10xH>	91.888	3.1
<64xL,30xH>	91.952	9.5
<44xL,50xH>	92.015	15.8
<24xL,70xH>	92.080	22.3
<1xL,93xH>	92.154	29.7

The final capacitance parameters for each cell are represented in Table 11, where the maximum, minimum and step capacitance values are presented, with respective fabrication dispersion for each bank. As observed the number of fine and thermometer capacitors changed from Table 7 to Table 12. To reduce the area occupation, the number of thermometer cells was reduced.

Table 12 - Extracted values of each cell, respective capacitance step and number of capacitors.

	Coarse	**Fine**	**Thermometer**
High [F]	58.7 f	579.7 a	408.7 a
Low [F]	17.1 f	347.3 a	405.3 a
Δc [F]	41.6 f	232.3 a	3.4 a
Number of capacitors	15	255	93

The LC tank post-layout analysis regarding conductance and susceptance, with different process corners is presented in Figure 41. From the following figure one can see the amount of negative conductance the class-C cross-coupled must have to accomplish oscillation.

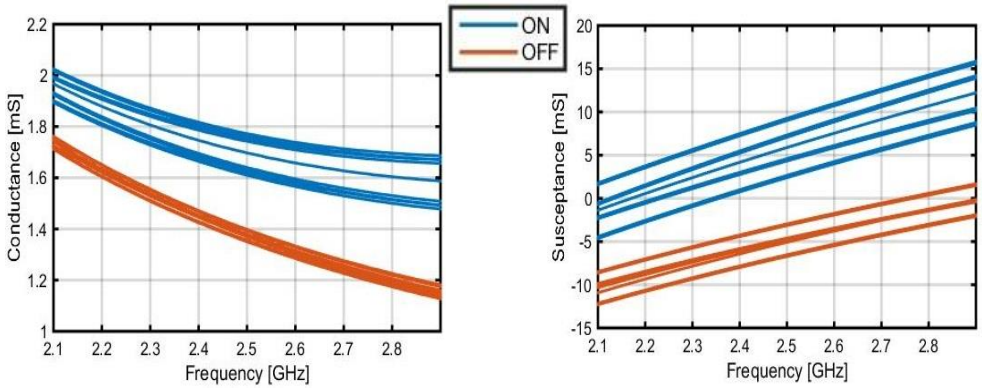

Figure 41 - Simulated results for LC tank corners post-layout conductance (left) and susceptance (right).

4.6 Layout

In this section a detailed analysis of the banks and cells physical layout is presented. In the beginning of the oscillator design it would be impossible to get a prediction of the parasitic effects which would directly influence power consumption

Before designing the layout, some considerations have to be taken into account. The entire design is symmetric, and the three banks together must occupy the minimum area possible by having the best rearrangement between them.

Regarding metals use, for the three banks the same notions were applied. Although, using lower metal layers one gets higher parasitic capacitances, metal layer M1, is used to connect all ground connection and for power supply metal layer M2 was used.

In a primary layout trial using mainly lower metal layers to connect cells between each other it was clear the parallel equivalent resistance degradation. In order to reverse this problem higher metal layers were used. Since maximizing Q is not concerning, instead having lower losses is desired. For capacitors bank design priority was given to use higher metal layers to connect vout+ and vout-). For matching purposes, to each bank is also added a ring of dummy cells around the matrix.

In the coarse and fine bank, wider routings cause larger parasitic capacitances. However, equivalent parallel resistance had to be maximized, so larger width was used in some interconnections. In the thermometer bank using higher level metals is inevitable due to the high number of interconnections. There are 93 bits without even taking into account the dummies. Although a parasitic capacitance increase appears, it's still acceptable. Also, due to the use of a great number of metal levels some of the cells were directly connected with poly1 layer.

The total dimensions of each bank including the dummy's ring is presented in Table 14.

Table 13 - Total area values for each capacitor bank.

	Coarse	Fine	Thermometer
Total area [μm²]	15.76	1.47	4.64

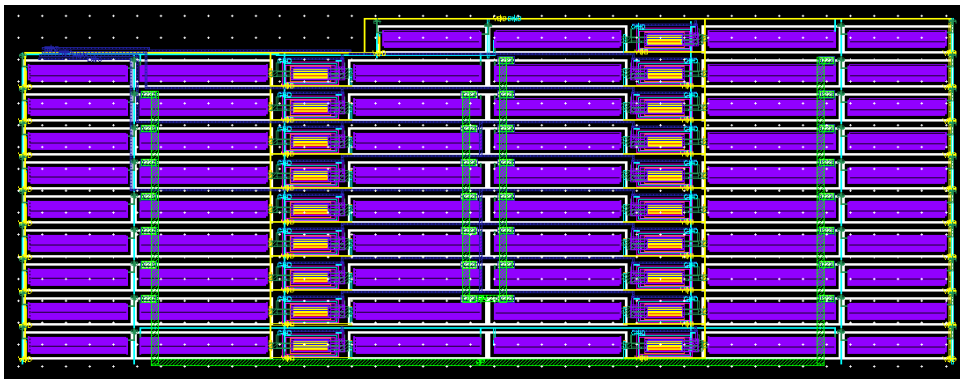

Figure 42 - Coarse bank layout including dummy's.

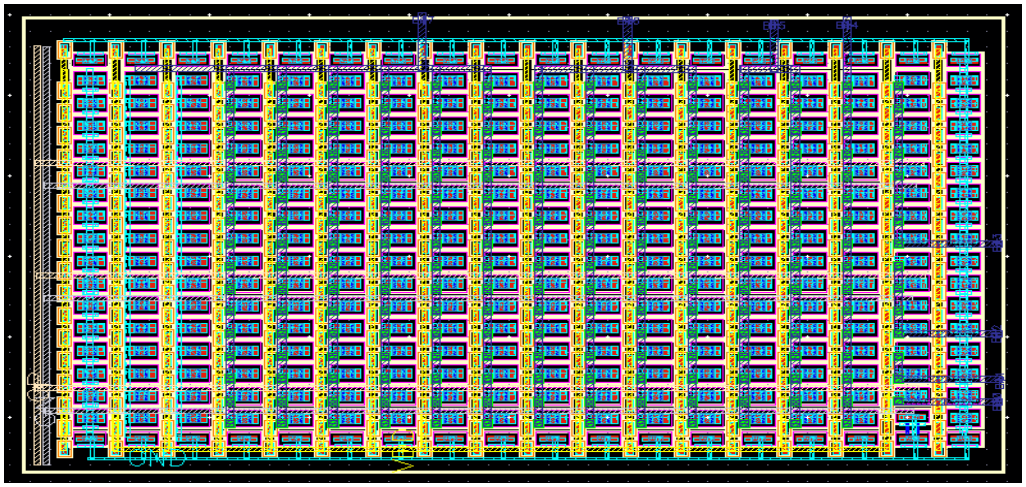

Figure 43 - Fine bank layout including dummy's.

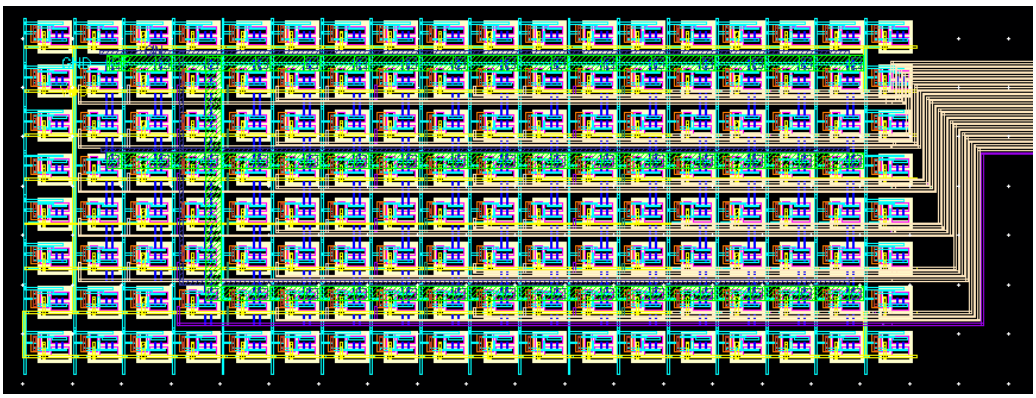

Figure 44 - Thermometer bank layout including dummy's.

5 DCO prototype

As said before, the LC tank alone can't hold an oscillation. In this chapter, it is explained the design of the second part of the DCO, the cross-coupled CMOS, who provides negative resistance to ensure the oscillation condition. A trend for battery operated devices lead to improvements in energy consumption of whole RF systems. Class-C operation allows a power consumption reduction by changing the bias condition when the amplitude is stabilized, reducing the amount of current drawn from the power supply.

Following, it is presented the full DCO implementation, where optimization of power consumption, frequency tuning and phase noise are discussed.

5.1 DCO schematic and layout

5.1.1 Cross-coupled design

Cross-coupled pairs are used to create negative gm to compensate the losses in the LC Tank. The essential condition to fulfill oscillation is

$$|G_{MOS}| \geq 2\ \frac{1}{R_{tank}}, \tag{46}$$

where G_{MOS} is the total transconductance seen at the terminals of the cross-coupled. In industry it's typically three or four times larger than the required minimum to ensure oscillation and reasonable phase noise. Here it's chosen to be two times higher.

There are several possible topologies to implement this part of the circuit, using NMOS, PMOS or both pairs, circuit with or without current source, each having their own trade-offs. In [30,32] is proved that the power consumption of the DCO would be much higher using only PMOS instead of NMOS. Between NMOS and CMOS topology, CMOS is preferable to its reduced transconductance. The equivalent negative conductance for NMOS cross-coupled topology is

$$G_{NMOS} = -\frac{g_{mn}}{2}. \tag{47}$$

Compared with equation (14), for the same current the transconductance can be twice larger. Thus, CMOS differential cross-coupled is the topology chosen. Although, using CMOS adds more devices and consequently increases the parasitic capacitances affecting the frequency tuning characteristics.

Then, the way to bias the DCO should be analyzed. Two different forms of cross-coupled topologies are compared, as shown in Figure 45. From the point of view of the cross-coupled, all parasitic capacitors are in parallel. The first implementation presented, Figure 45 left, without current source, the polarization is made by tension applied to V_{SG} and V_{GS} to respective MOS pair transistors. Here, output amplitude can't be easily controlled because the supply voltage is fixed.

However, the circuit schematic on the right, which allows amplitude swing control using a current source, provides an extra parameter maneuver (I_{tail} current).

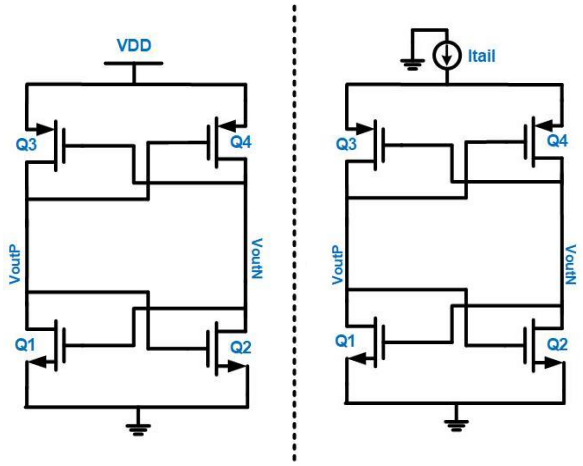

Figure 45 - Different versions of differential cross-coupled regarding bias supply.

Following simulations confirm the flexibility of using a CMOS cross-coupled with current source. To simulate the equivalent conductance and capacitance of the conventional CMOS cross-coupled using a current source, values in Table 14 are used for I_{tail} varying from 100 µA to 400 µA.

Table 14 – Transistors parameters used in the cross-coupled.

Gate finger width PMOS [µm]	Gate finger width NMOS [µm]	Gate finger number	Gate length [nm]
7.2	5	4	120

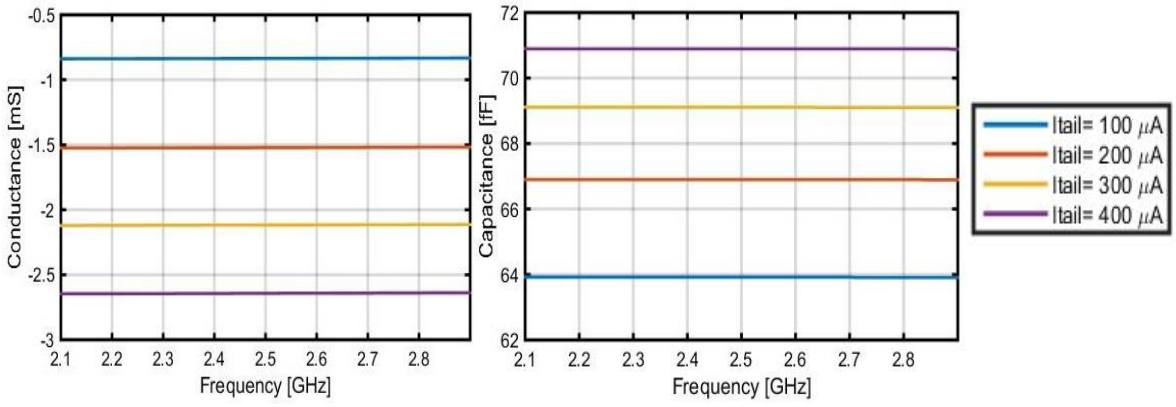

Figure 46 - Simulated results for cross-coupled Conductance (left) and Capacitance (right), for different values of I_{tail}.

From the analysis above is already possible to infer that by increasing I_{tail} one can get more negative conductance, likewise increasing the capacitance imposed by the cross-coupled.

The cross-coupled conductance is directly related with the resonance frequency, thus having an I_{tail} gives some way to compensate in case post-layout tuning range results are deviated.

5.1.2 Class-C differential cross-coupled

The idea of working in Class-C is basically consume less power in the steady-state than during start-up. This design method is not trivial since the conditions to sustain oscillations in the steady-state differ from the required ones during startup period. An extra circuit for changing bias conditions is needed. Please note that, although the oscillator bias can be changed to class-C during steady-state, it won't be able to start with class-C. For that a class-AB is usually required.

The transistors of the cross-coupled pairs are biased to work always in the saturation region. The input impedance of the LC cross-coupled circuit is

$$Z_{IN} = -\frac{2}{G_{mTotal}} || \frac{2}{j\omega C_{total}}, \quad (48)$$

where $G_{mTotal} = g_{mn} + g_{mp}$, and C_{total} represents all parallel equivalent capacitances, inductor included. It was necessary to find a way to reduce the loop gain when the oscillation is sustained to achieved lower power consumption. After the LC cross-coupled source current is chosen, the transconductance (gm) is a fixed value.

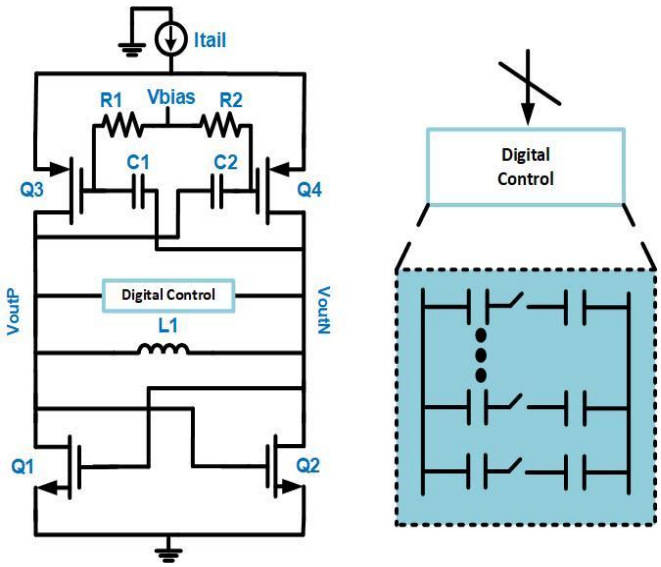

Figure 47 - Simplified schematic of the DCO.

As seen in Figure 47, to achieve Class-C operation, v_{bias} voltage has to be raised when the oscillation is achieved. In a first analysis, the cross-coupled Class-C circuit schematic is implemented with two resistors (R_1= R_2= 20 kΩ) and two capacitors (C_1= C_2= 500 fF) from RF technology, as exemplified in Figure 47. For the same transistor values, presented in Table 14, the conventional cross-coupled is compared with the Class-C. The I_{tail} is fixed to 300 μA and there are different values of v_{bias} in the Class-C case.

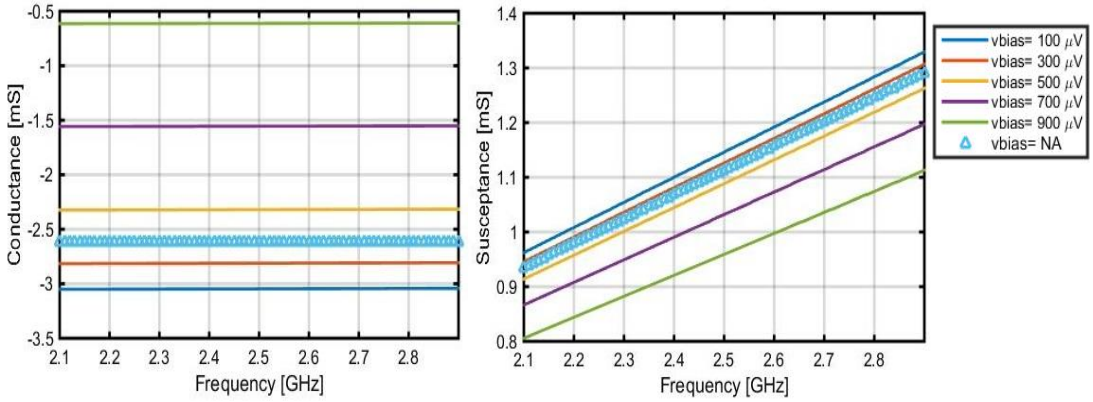

Figure 48 - Simulated results for the conventional cross-coupled and class-C; Conductance (left) and Capacitance (right), for different values of v_{bias} in the case of the class-C; when v_{bias} equals to NA, it refers to the conventional cross-coupled where a v_{bias} doesn't exist.

From the simulation results presented in Figure 48, it's evident that v_{bias} allows to control the loop gain. The susceptance also suffers variation when different values of v_{bias} are used.

To design the class-C cross-coupled, it's necessary to know LC tank losses. In previous Figure 41, it is determined that the maximum post-layout simulated value of the tank conductance, is 2 mS. Using equation (46), the negative conductance is calculated to be at least -4 mS. In order to determine the pairs transistors size according to this information, the following simulation was created, changing NMOS width (w1), PMOS width (w2), and v_{bias}.

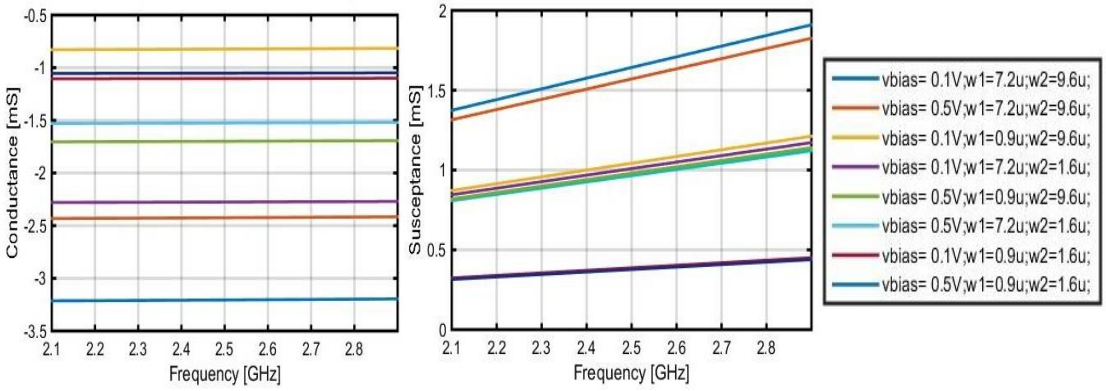

Figure 49 - Schematic simulation results for class-c cross-coupled for different values of gate finger width and v_{bias}; conductance (left) and susceptance (right).

From what it has been seen there are three variables to design the cross-coupled pairs, varying the width, the bias current (I_{tail}) and the transistors bias (v_{bias}). From Figure 49 (left), one can assume that increasing the w1 and w2 of the transistors, one gets higher gm. However, the maximum width is restrained by their parasitic capacitances impact on the LC tank, which already have been provisioned during the capacitor banks design as 70 fF. v_{bias} value have to be chosen in order to create oscillation startup.

The next step consists in examining the post-layout conductance and capacitance of the Class-C cross-coupled. Next post-layout simulation is performed, with the same resistors and

capacitors used before. However, the PMOS width is fixed to maximum width (9,6 µm) and NMOS values are varied between to 1 µm and 5 µm.

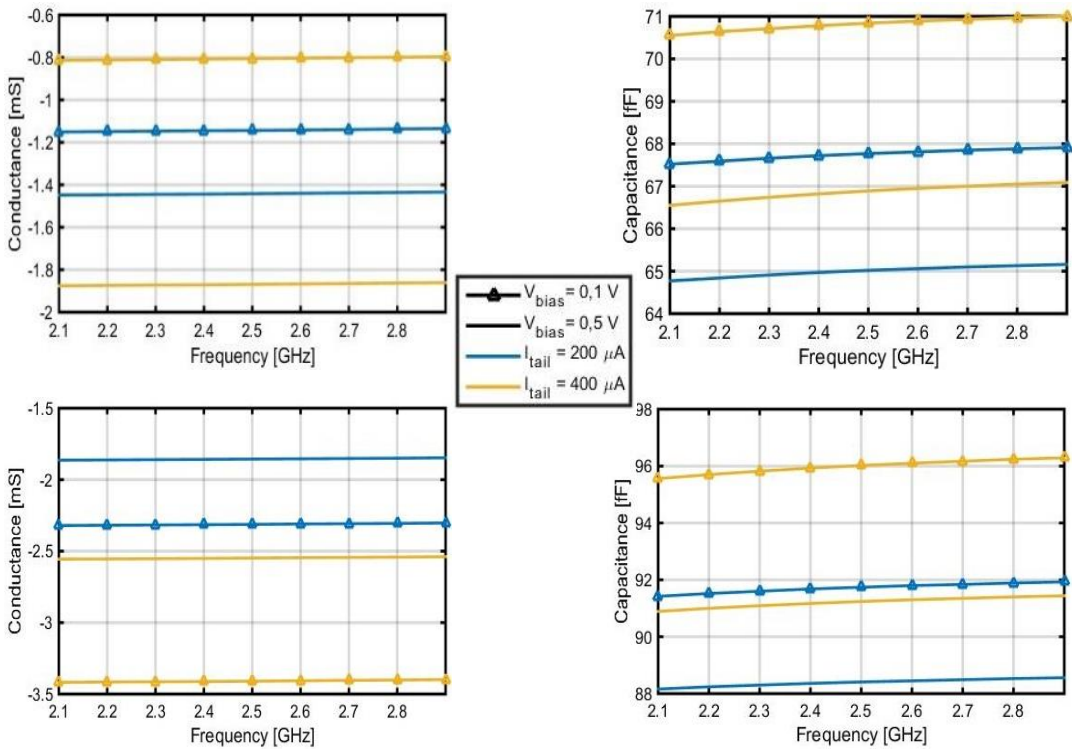

Figure 50 – Extracted simulation results for Class-c cross-coupled, for different values of NMOS gate finger width, I_{tail} and fixed v_{bias} ; Top figures: NMOS width equal to 1um; Down figures: NMOS width equal to 5um; Conductance (left); capacitance (right).

To guarantee the correct PFR, v_{bias} = 0,4 V and I_{Ref} = 400 mA is chosen for startup. Although it creates more capacitance parasitics, it's chosen NMOS width equal to 5 µm to ensure enough negative gm.

Last simulation was obtained using a fixed v_{bias}, but as explained earlier a feedback mechanism is required to dynamic change the transistor bias after steady-state is reached. A time domain simulation can be performed to replicate this behavior even without the feedback circuit. It is possible to explore if it is viable to change the gate bias voltage required to reduce power consumption and, at the same time, secure robust startup oscillation. An ideal source (vpulse) is used, allowing an initial value (V1) to be changed to a final value (V2) after a certain time delay. The values used in the next simulation can be seen in Table 15.

Table 15 - Values used to simulate schematic cross-coupled Class-C operation.

Hypothesis	Voltage 1 [mV]	Voltage 2 [mV]	Delay time [ns]	Itail [µA]
	400	402	1500	537
	400	406	1500	533
	400	410	1500	531
	400	414	1500	527

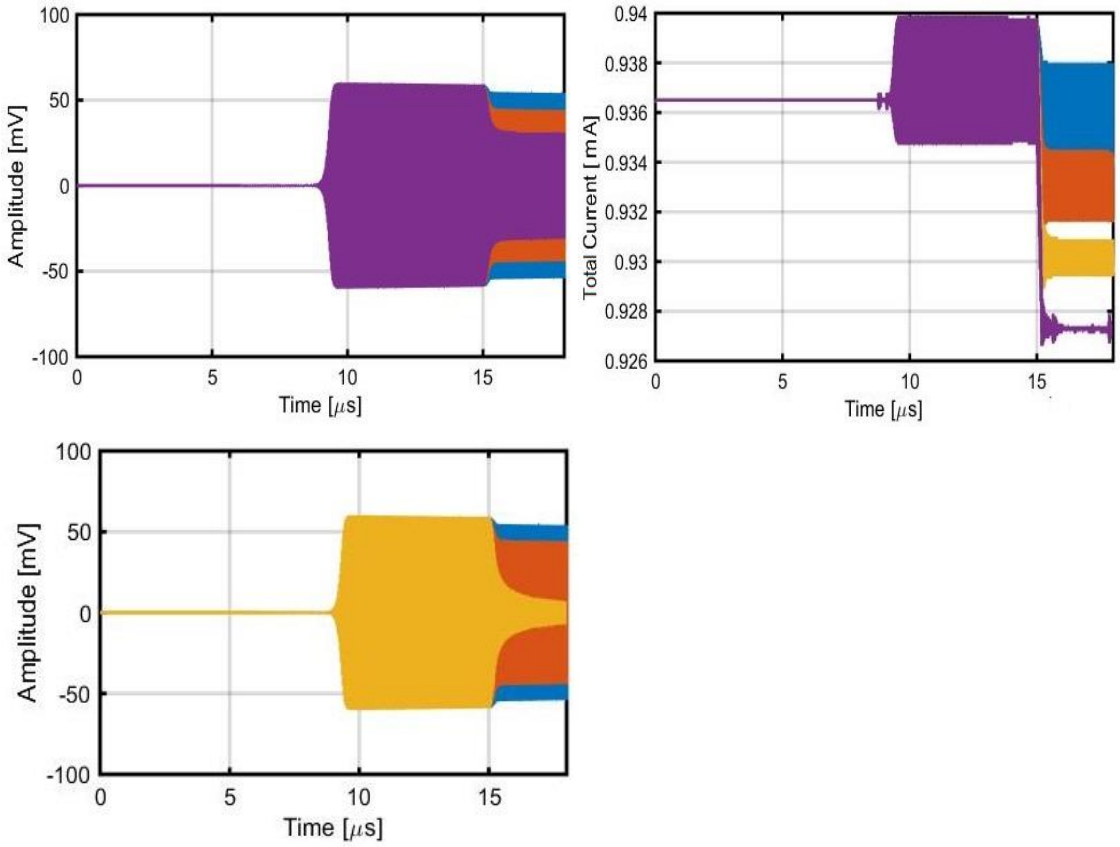

Figure 51 - Schematic class-C transient waveforms; Left- Output voltage; right – Consumed current; Bottom figure is equal to the upper figure, but here option v2=410 m is visible.

In this transient simulation it was used the LC tank circuit schematic dimensioned in the previous chapter. This transient analysis is performed mainly to test the output amplitude as well as the startup time of the oscillation. Initially the circuit stars with a voltage V1 to work in class-AB, after 15 μs the voltage is increased in V2 to work in class-C. When increasing to V2, with a fixed I_{Ref} the V_{SD} tension will decrease, reducing the current, as observed in Figure 51.

Is possible to conclude that less power is consumed to sustain the oscillation than to start. However, the time period to start oscillation with v_{bias} = 0.4 V is superior than conventional cross-coupled which only takes a few ns.

Since between V2 = 410 mV and V2 = 414 mV the output amplitude starts to fade, a value of V2 = 410 mV is chosen to be used in the final DCO circuit. In Figure 52 it's presented the final transistor parameters.

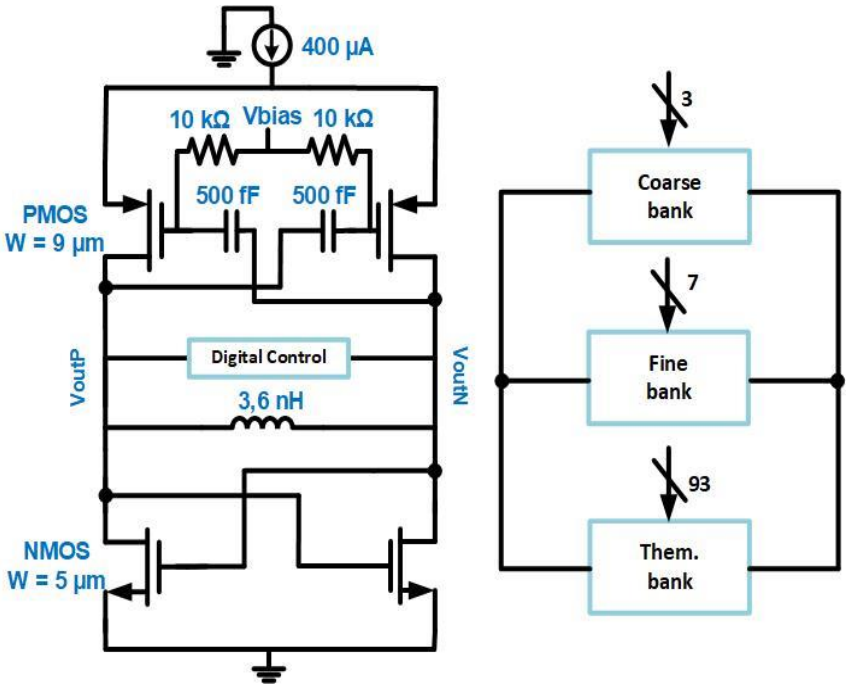

Figure 52 - Final schematic of the oscillator.

5.1.3 Class-C Cross-coupled layout

Regarding the cross-coupled circuit, the four transistors are laid out symmetrically. The principles used in section 4.6 were applied here, minimum metals widths were used to minimize parasitics.

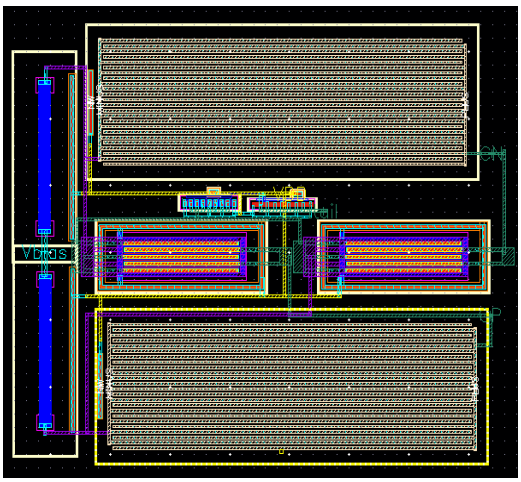

Figure 53 – Layout design for the PMOS cross-coupled pair.

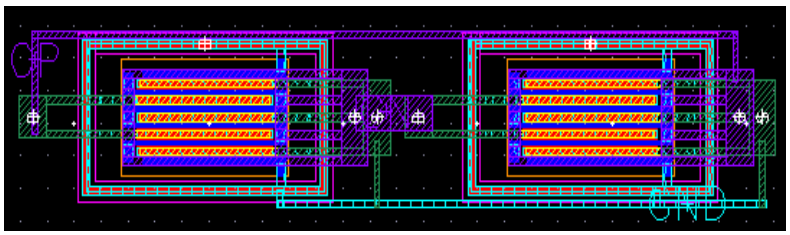

Figure 54 - Layout design for NMOS cross-coupled pair.

5.2.4 Final layout

This section presents the full DCO design layout. The circuit layout is composed of a 3.6 nH inductor, three bank of capacitors and class-C CMOS cross-coupled. The total dimensions of the chip is 352 x 311 μm², an area of 109 μm². Although, all counterparts are presented the interconnections between them were not completed.

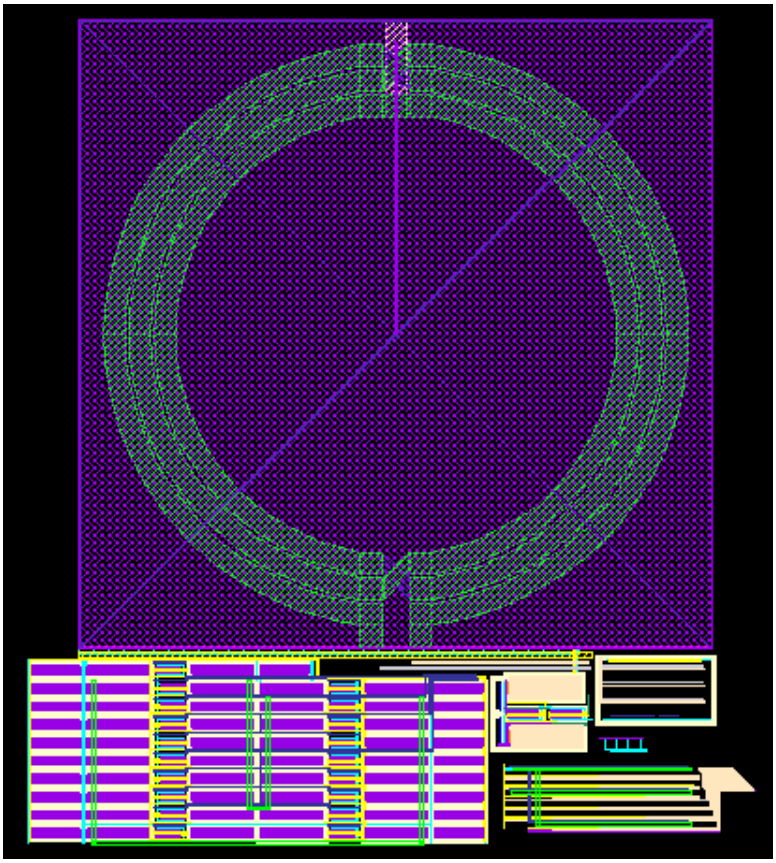

Figure 55 - Layout floorplan of the designed DCO.

5.2 DCO final simulations

In this section the DCO with center frequency of 2.4 GHz is presented. The LC tank was implemented using three banks of capacitors and a differential inductor of 3.6 nH. As was described in Chapter 4, the coarse bank is composed by 3 bits, the fine bank has 7 bits, both binary weighted and the thermometer with 93 bits equally weighted. The cross-coupled pair is biased to operate in Class-C. A final capacitance of 332 fF is added in parallel to the LC tank. All results provided in this section are post-layout simulations.

5.2.1 Oscillation frequency

Observing the simulated tank circuit admittance presented in Figure 56 and looking at the imaginary part zero it is possible to predict that the frequency tuning is comprehended between 2.1 to 2.8 GHz. It is evident that with the class-C cross-coupled capacitance loading effect the

center frequency tends to shift to lower values. A final transient simulation is made to test the functionality of this DCO.

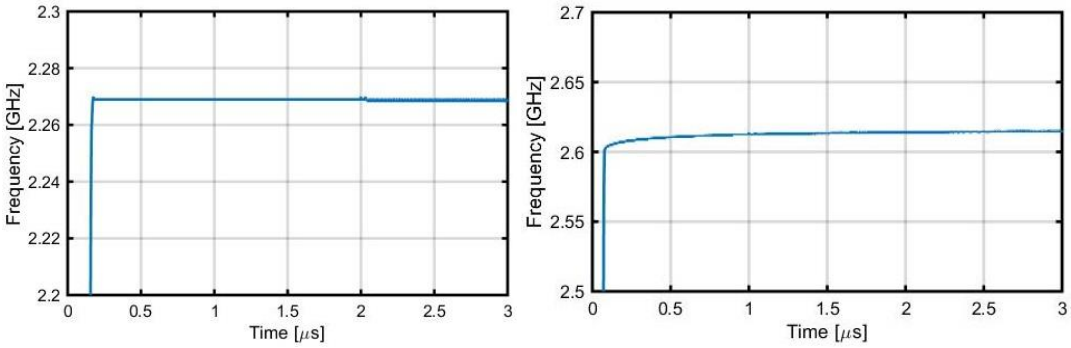

Figure 56 - Extracted simulations of worst case process corners for maximum frequency (left) and minimum frequency (right).

The frequency range varies with different process corners. The nominal values are f_{max}= 2.732 GHz and f_{min}= 2.093 GHz. The worst-case process corner, where inductor, capacitors and transistors have maximum values, for on and off state respectively, is f_{min}= 2.268 Ghz and f_{max}= 2.614 Ghz, comprehending the tuning band pretended (2.4 – 2485 GHz). Comparing to the conventional cross-coupled an oscillation frequency degradation is also observed. The worst-case process corners frequencies for the conventional cross-coupled are f_{max}= 2.63 Ghz and f_{max}= 2.27 Ghz. There is a decrease of frequencies in class-C because extra elements add parasitic capacitances which will influence the oscillation frequency to go down.

The respective resolution for coarse, fine and thermometer bank are 6.4 MHz, 5.8 MHz and 20 kHz, respectively. The fine resolution of 12 kHz was not possible to achieve due to parasitics.

5.2.2 Power consumption and phase noise

The final output amplitude and current consumed is presented in the following figure. Although, the change between V1 and V2 is subtle, it exists. In the case of the current it includes the current provided to the cross-coupled (400 µA).

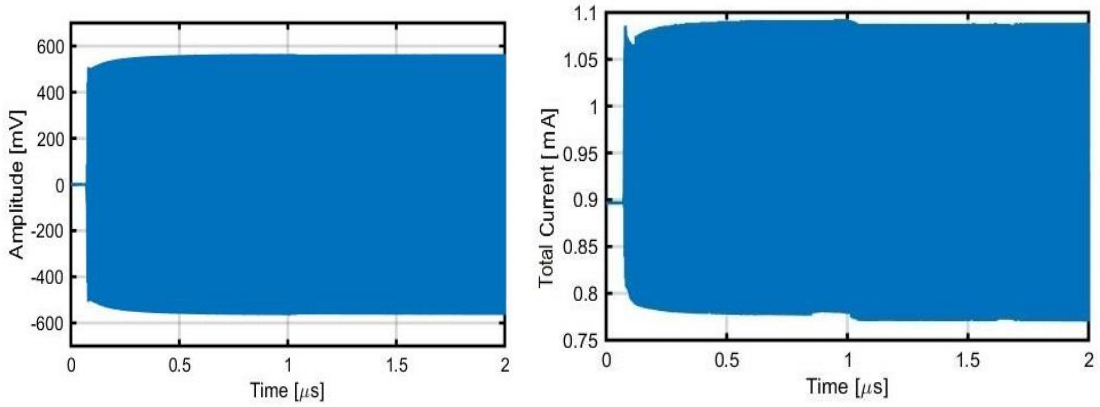

Figure 57 - Extracted Class-C transient waveforms; Left- Output voltage; right – Consumed current.

One can also conclude that is possible to increase V2 to a higher voltage than 410 mV because is likely the oscillation be sustained after V2 and at the same time reduce more the current consumption.

It is also important to visualize the phase noise. Although, it is expected an improvement regarding phase noise characteristics of Class-C cross-coupled in accordance to papers review, more components were added to the circuit, increasing parasitics. Next graphic examines the post layout full DCO phase noise while the oscillation is in steady state.

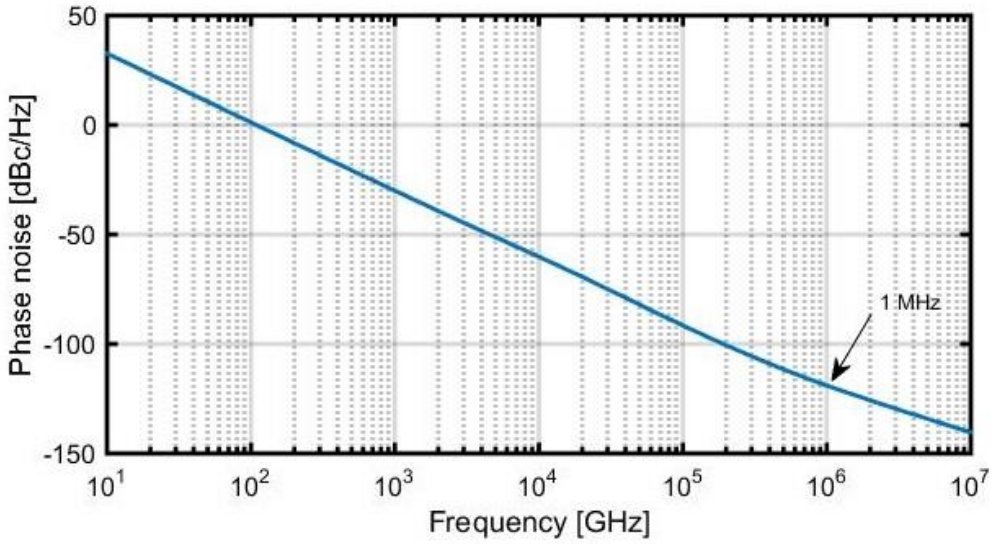

Figure 58 - Phase noise in the steady state.

In steady state the phase noise is -119 dBc/Hz and in startup is -119,2 dBc/Hz. There is a subtle increase in the phase noise performance in the steady state Class-C oscillator, this can be due the reduction of output power.

Table 16 compares measurements results with the DCO previous design, with the same technology and power supply.

Table 16 - Summary results and comparisons with previous DCO.

	Previous work	This work
Center frequency [GHz]	2.4	2.4
Tuning range [GHz]	2.1 – 3.1	2.1 – 2.7
Current consumption [µA]	550	500
Output amplitude [mV]	452	500
FoM [dBc/Hz]	-125	-119
Total area [µm²]	90	109

6 Conclusions

The study of ultra-low power oscillators is forthcoming, but as seen before to improve one characteristics some other requirements are jeopardized. The presented design provides digital control, high frequency resolution, keeping in mind power consumption reduction.

During tuning range planning, three banks of capacitors were dimensioned. The use of several banks helped to cover the desired band with frequency resolution of 12 kHz, under a low power consumption. The main concern about sizing the banks consisted in reducing the occupied area and maximize parallel equivalent resistance in order to reduce losses. Furthermore, the presented design solution allows tuning range adjustment by considering a fixed extra parallel capacitor. Like this in case final extracted parasitic capacitance exceeds expected value, compensation is possible.

Comparing the percentage increase of RC parasitic of each bank, 10%, 90% and 50% for coarse, fine and thermometer, respectively it's certain one could trust MOM corner values. The 15% extra band wasn't necessary to add. On the other hand, fine and thermometer bank ranges an extra margin of 20% and 30% was added.

For improved ultra-low power consumption, Class-C cross-coupled is proposed. Since the goal was reduce power consumption one had relaxed specifications concerning phase noise, quality factor and output amplitude. As the results show there is an evident decrease on the current consumption with Class-C operation. Still there is some degradation in the quality factor performance and phase noise. The oscillation starts with a current consumption of ≈ 9 mA and decreases to 900 µA, subtracting I_{REF}, there is a total current consumption of 500 µA. It's visible an inferior performance concerning phase noise during steady state Class-C oscillator.

After full DCO post layout simulation with parasitic capacitances, a degradation of tuning range was found, therefore, a correction was performed by variations of some circuit parameters, like capacitors values to increase maximum frequency. Final tuning range, 2.093 – 2.732 GHz, comprises the band pretended, between 2.4 – 2.485 GHz with all dispersions and parasitic capacitances taking in count.

The simulation results show that not all the design specifications are met as shown in Table 16. In summary, 109 µm² is the total area occupied with 0.6 mW power consumption, phase noise of -119 dBc/Hz at 1 MHz offset. The finest frequency resolution obtained is about 20 kHz, higher than the one pretended. Cell thermometer parameters must be changed to find lower value of capacitance step.

Comparing with previous DCO design there is an improvement in current consumption but at the cost of the phase noise degradation. The tuning range was optimized but the area increased, probably due to adding dummy's in each bank, not used in the previous one.

As future work, it is needed to design the class-C bias switching circuit to control the bias value to guarantee a startup oscillation. A study is needed to ensure that adding auxiliary circuitries will not negatively influence phase noise and efficiency improvement. Probably with the increase of parasitic capacitances there will be a degradation on the tuning range.

Buffers should be added to isolate the output of the DCO from other circuits with high input impedance. The buffers extra capacitance should be considered in C_{extra}.

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7 References

[1] K. Peng, P. Wu, “High Performance Fractional–N Frequency Synthesizer Using a Two-Point Channel Selection Technique”, in Asia Pacific Microwave Conference, pp. 2320-2323, 2009.

[2] T. Tokairin, M. Okada, M. Kitsunezuka, T. Maeda, M. Fukaishi, “A 2.1-to-2.8-GHz Low-Phase-Noise All-Digital Frequency Synthesizer with a Time-Windowed Time-to-Digital Converter,” in IEEE J. SolidState Circuits, vol.45, no 12, pp. 2582-2590, 2010.

[3] Y. Liu, X. Huang, M. Vidojkovic, K. Imamura, P. Harpe, G. Dolmans, H. De Groot, “A 2.7nJ/b Multi-Standard 2.3/2.4GHz Polar Transmitter for Wireless Sensor Networks”, in ISSCC Dig. Tech. Papers, pp. 448-450, 2012.

[4] V. Chillara, Y. Liu, B. Wang, A. Ba, M. Vidojkovic, K. Philips, H. de Groot, and R. B. Staszewski, “An 860μW 2.1-to-2.7GHz all-digital PLL-based frequency modulator with a DTC-assisted snapshot TDC for WPAN (Bluetooth Smart and ZigBee) applications” in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp. 172-173, 2014.

[5] S. Hong, S. Kim, S. Choi, H. Cho, J. Hong, Y. Seo, B. Kim, H.Park, J. Sim, “A 250μW 2.4GHz Fast-Lock Fractional-N Frequency Generation for Ultra-Low-Power Applications”, in IEEE Transactions on Circuits and Systems II: Express Briefs, 2016.

[6] Microelectronic Circuits, Adel S. Sedra, Kenneth C. Smith, Oxford University Press, 2004.

[7] K. Stadius, “Integrated RF oscillators and LO signal generation circuits”, 2010

8] Andreani, X. Wang, L. Vandi, A. Fard ,“A Study of Phase Noise in Colpitts and LC-Tank CMOS Oscillators”, in IEEE Journal of Solid-State Circuits , Vol. 40,no. 5, pp. 1107-1118, 2005.

[9] A. Mazzanti, P. Andreani, “Class-C harmonic CMOS VCOs, with a general result on phase noise”, in IEEE J. Solid-State Circuits, vol. 43, no. 12, pp. 2716–2729, 2008.

[10] R. Rottava, C. Camara Santes, F. Rangel de Sousa, R. Nunes de Lima, “Ultra-low-power 2.4GHz Colpitts oscillator based on double feedback technique”, in Proc. of 2013 IEEE Int. Sym. on Circuits and Systems, pp. 1785-1788, 2013.

[11] C. Zhang, J. Zhou, “A 2.4GHz Low Power Low Phase Noise Ring VCO”, Taiwan, October 2012.

[12] X. Wang, X. Yang, X. Xu, T. Yoshimasu, “2.4-GHz-Band Ultra-Low-Voltage LC-VCO in 180-nm CMOS”, in Electron Devices and Solid-State Circuits (EDSSC), 2015.

[13] X. Wang, X. Yang, X. Xu, T. Yoshimasu, “2.4-GHz-Band Low-Voltage LC-VCO IC with Simplified Noise Filtering in 180-nm CMOS”, in Wireless Symposium (IWS), 2016 IEEE MTT-S International, 2016.

[14] S. Lee, S. Jang, Y. Chuang, J. Chao, J. Lee, M. Juang, “A Low Power Injection Locked LC-Tank Oscillator with Current Reused Topology”, in IEEE Microwave and wireless components letters, Vol. 17, no. 3, 2007.

[15] L. Hung, H. Hsieh, Y. Liao, “A wide tuning-range CMOS VCO with a differential tunable active inductor”, IEEE Trans on Microwave Theory and Techniques, vol. 54, pp. 3462-3468, 2006.

[16] E. Temporiti, C. Weltin-Wu, Daniele Baldi, R. Tonietto and F. Svelto, “A 3 GHz Fractional all-Digital PLL with a 1.8 MHz bandwidth implementing spur reduction techniques”, in IEEE Journal of Solid-State circuits, Vol. 44, no. 3, 2009.

[17] K. Okada, Y. Nomiyama, R. Murakami, and A. Matsuzawa, “A 0.114-mW dual-conduction class-C CMOS VCO with 0.2-V power supply”, in Symp. VLSI Circuits Dig. Tech. Papers, pp. 228–229, 2009.

[18] M. Tohidian, A. Fotowat-Ahmadi, M. Kamarei, and F. Ndagijimana, “High-swing class-C VCO”, in Proc. ESSCIRC, pp. 495–498, 2011.

[19] Jian Chen, Fredrik Jonsson, Mats Carlsson, Charlotta Hedenäs, and Li-Rong Zheng, “A Low Power, Startup Ensured and Constant Amplitude Class-C VCO in 0.18 CMOS”, in IEEE Microwave and Wireless Components Letters, Vol. 21, no 8, pp. 427-429, 2011

[20] Zhangming Zhu, Member, IEEE, Liang Liang, and Yintang Yang, “A Startup Robust Feedback Class-C VCO With Constant Amplitude Control in 0.18 m CMOS”, in IEEE Microwave and Wireless Components Letters, Vol. 25, no 8, pp. 541-543, 2015.

[21] Jae-Hoon Song, Byung-Sung Kim and Sangwook Nam, “An Adaptively Biased Class-C VCO with a Self-Turn-Off Auxiliary Class-B Pair for Fast and Robust Startup”, in IEEE Microwave and Wireless Components Letters, Vol. 26, no 1, pp. 1531-1309, 2016.

[22] M. B. Vijayanathan, “Design of a DCO for an All Digital PLL for the 60 GHz Band”, 2013.

[23] A. Ba, “Ultra-low-power Digitally-controlled Oscillator for Event-driven Transmitter”, Netherlands, 2011.

[24] L. Xu, S. Lindfords, “A Digitally Controlled 2.4-GHz Oscillator in 65-nm CMOS”, 2007.

[25] R. B. Staszewski, C. Hung, N. Barton, M. Lee, “A Digitally Controlled Oscillator in a 90 nm Digital CMOS Process for Mobile Phones”, in IEEE Journal of Solid-State Circuits, Vol. 40, 2005.

[26] M. Jurgo, R. Navickas, “Design of gigahertz tuning range 5 GHz LC digitally controlld oscillator in 0,18 μm CMOS” , in Journal of Electrical Engineering, Vol. 67, 2016.

[27] B. T. Thiel, A. Neyer, S. Heinen, “Design of a Low Noise, Low Power 3.05–3.45 GHz Digitally Controlled Oscillator in 90 nm CMOS”, in Research in Microelectronics and Electronics, 2009.

[28] A. S. Natarajan, “High-Resolution mm-wave Digitally Controlled Oscillator in CMOS”, Oregan, 2015.

[29] A. Tavakol, “Digitally Controlled Oscillator for WiMAX in 40 nm”, 2012.

[30] A. Nasri, M. Yargholi, “Design of a LC-Tank CMOS Voltage-Controlled Oscillator”, in International Journal of Reaserch in Electrical and Electronics Technology, Vol. 1, no 2, 2014.

[31] O. Palampougioukis, “Inductor Characterization and VCO design in 65nm CMOS”, 2013.

[32] M. A. Saber, “LC VCO tuning with parallel MOS-varactor in FDSM application”, 2006.

[33] C. S. Salimah, “Design of CMOS LC voltage-controlled oscillators”, 2006.

[34] Z. Li, Z. Wang, Z. Li, Q. Li, “Design of 33-40GHz Low Power VCO in 90-nm CMOS, Technology”, in Electrical, Computer and Communication Engineering , China, 2017.

[35] T. M. Hancock, “High Performance 12-24 GHz RF Front-End Components Fabricated in a Commercial SiGe Bipolar Process”, 2005.