Development of an integrated magnetic sensor

in CMOS 0.13µm tecnology

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***Abstract* — This paper is divided into 2 parts: the first part presents the research and study of a magnetic sensor based on a MAGFET device and second part presents the implementation of integrated magnetic sensor. The MAGFET is developed in CMOS 0.13µm technology and this sensor is obtained from a standard NMOS transistor, in which the transistor drain is divided into two drains (split-drain). The MAGFET uses Hall effect to detect the magnetic field and this sensor is intended for low sensibility applications, which means that the MAGFET does higher measurements in relation to earth magnetic field. With no magnetic field the drains current difference (ΔI_d) theoretically is zero. But in presence of magnetic field there is a different current between the two drains and which value (ΔI_d) is proportional to the magnetic field. The development of 4 MAGFETs allowed to see this behavior and the sensibility of the sensor with or without magnetic field. The implementation of integrated magnetic sensor has all circuits (MAGFET sensor and others electronic circuits) that are needed to detect the magnetic field and convert to digital signal (ADC). For the ADC a dual slope ADC was used because it is simpler than others ADC and the main objective is checking the dynamic range of the MAGFET. A differential dual slope ADC topology was used because it has more advantages in relation to single-ended like a higher output excursion and better rejection of noise and common mode disturbances.**

Keywords—MAGFET;Integrated magnetic; sensor;ADC;CMOS;

I. INTRODUCTION

The sensors are elements that allows interaction with the environment and are used in several areas as automotive, computational, aerospace, health and industrial level. The evolution of micro and nanoelectronics was possible development more efficient sensor, with small size and low consumption to measurement and control of a certain physical or chemical phenomenon. There are several physical phenomena to detect the magnetic field in according measurement sensibility of the field (low, medium and high). There are several physical phenomena to the detect the magnetic field but the more common and used are Hall effect, magneto resistive, fluxgate, SQUID and solenoid.

This project allowed study a magnetic sensor based a MAGFET device and then development a fully integrated magnetic sensor in CMOS 0.13µm technology. The Cadence software is used to design the electric circuits and make the simulations in according to the intended specifications.

II. MAGNETIC SENSOR

The magnetic sensors allow measure a magnetic field or from this, measure other parameters, which it has a proportional or inverse relationship with the magnetic field. The sensors are devices that produces a change in output (preferably electric) in function of a stimulus produced on the input [1]. The sensor MAGFET developed in micro and nanoelectronics reacts a magnetic stimulus, therefore the sensor changes the output electric signal according the magnetic field value.

According to the measurement range of magnetic field, the magnetic sensors can be divided in 3 categories: low, medium and high sensibility sensors [2]. The low sensibility sensor can only measure fields of values much higher in relation to the earth magnetic field, the medium can measure fields in order of earth magnetic field and the high can measure fields below of earth magnetic field.

The MAGFET uses Hall effect to detect the magnetic field and this sensor is intended for low sensibility applications, which means that MAGFET does higher measurements in relation to earth magnetic field. The following figure represents the measurement range of field for different common types of magnetic sensors (Hall effect, magneto resistive, fluxgate, SQUID and coil) [2].

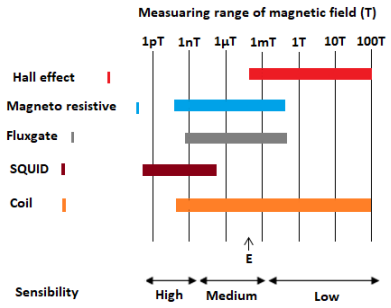

Figure 1 – Measurement range of magnetic field for different types of magnetic sensors

It is to be noted that some sensors have a higher measurement range and so it has more than one sensibility category as the magneto resistive sensor and the coil sensor.

Is to Refer that the only magnetic sensor possible to integrate in CMOS technology is the MAGFET. The MAGFET sensor is destined to application of low sensibility and utilizes the Hall effect technical.

A. MAGFET sensor

The MAGFET is a magnetic sensor developed in CMOS technology. This sensor is obtained from a standard NMOS transistor, which the transistor drain is divided in two drains (split-drain) [3]. The following figure represents the structure of MAGFET in 3 dimension with L, W and d.

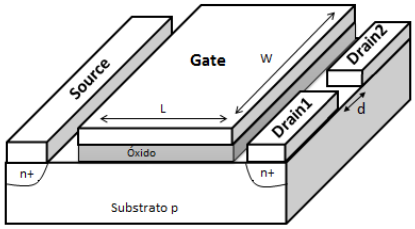

Figure 2 – MAGFET structure in 3 dimensions.

As a MOS transistor, insert a suitable voltage in gate (Vg) allows to create the channel between the drains and the source. Therefore, there is a channel that obtain a source current of MAGFET(Is), which that current is divided by 2 drains, being divided equally in the absence of the magnetic field. The source current is equals with the sum of current of each drain as show the following equation:

$$Is = Id1 + Id2 \quad (1)$$

, being Is is the source current and Id1,2 is the drain current on transistor.

Thus, in absence of magnetic field ideally the current of each drain are equals and the difference is zero (ΔId).

$$Id1 = Id2 = Is/2 \quad (2)$$

$$\Delta Id = Id1 - Id2 = 0 \quad (3)$$

In the presence of magnetic field will exist a current difference (ΔId) proportional to the intensity of the applied field. This operation is due to the Hall effect.

The Hall effect occurs on material conductive when there is an electric current (I) and this material is submitted to one magnetic field. The electric charge is subjected a Lorentz force to create a potential difference therefore, there is a Hall voltage (V_H) in material conductive.

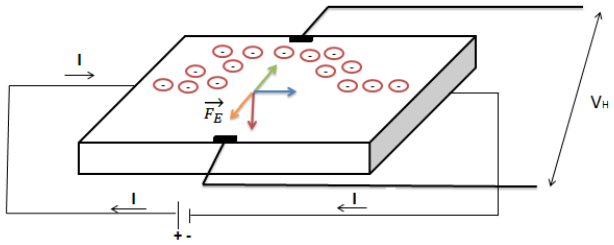

Figure 3 – Hall effect on material conductor.

The following figure shows the current deflection on MAGFET according to the direction of the applied magnetic field. Notice that the deflection only happens when the vector of magnetic field (Bz) is perpendicular to the direction of electric charge (qv).

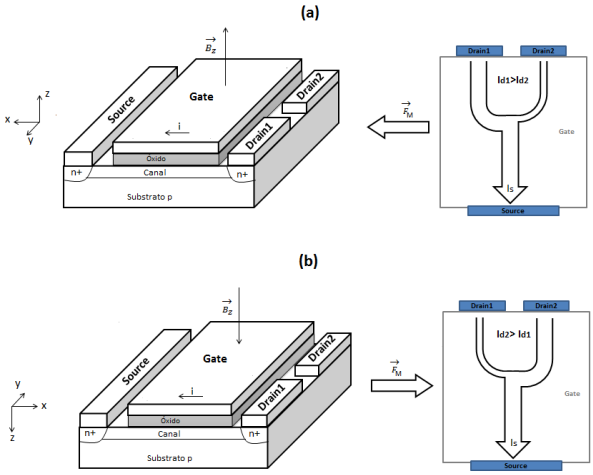

Figure 4 – Current unbalance (ΔId): positive(a) and negative(b).

According the Hall effect and Lorentz force, when applied a magnetic field perpendicular to the MAGFET ($\overrightarrow{B_z}$), a magnetic force is applied on this resulting in current deflection and thus there is an unbalance of the currents.

This unbalance allows to obtain a current difference (ΔI_d) proportional to the applied magnetic field. There is a relation between the unbalance of the currents and the magnetic field, being that the measurement sensibility of a certain value of field depends of created deflection in channel current and consequently of current difference (ΔI_d) [4].

The relative sensibility of MAGFET(S) is defined as a ration between the currents difference in the drains and the product of magnetic field through the total current of sensor (I_T) as show the equation 6 [4].

$$\frac{\Delta I}{I_T\ B} = \frac{|I_{d1} - I_{d2}|}{(I_{d1} + I_{d2})\ B} \quad (4)$$

By the article [4], [5] and [6] it is verified that the difference of the currents depends much of electric propriety of materials and the dimensions of MAGFET, this is, depend of length (L) and the mobility of electrons in the inverting layer of NMOS transistor (µn).

The increased of length and of the sensor mobility (NMOS transistor) allows to a greater deflection and consequently a greater difference of the currents for a magnetic field constant, as shows the following equations [4].

$$Deflection = \Delta I_d = L\ \mu\ B \quad (5)$$

Thus, the deflection increased allows to increase the measurement sensibility of magnetic field in MAGFET.

Behind of L, also it is necessary to consider the dimensioning of W length channel and of the distance d between the drains. In relation to the W, this should not be too big because from a certain value, the sensibility starts to decrease with the increased of W [4]. In relation to the distance between the drains, this must be as low as possible because it is verified that how much greater the distance, less will be the relative sensibility (S) of MAGFET [4].

Also, the polarization of MAGFET (Vgs, Vd1 e Vd2) is very important because the polarization allows to obtain a certain current and it allows increase the relative sensibility of MAGFET [4].

Therefore, the relative sensibility of one MAGFET depends of the following parameters [4]:

- Dimensioning of L, W and d.
- Mobility of electrons (µ).
- Polarization (Vgs, Vd1 e Vd2).

III. EXPERIMENTAL CARACTERIZATION OF MAGFET

From of the study obtained about the sensor MAGFET, it was developed and fabricated four MAGFETs in CMOS 0.13 µm technology, with different dimensions of L, W and d. This fabrication allowed to obtain an experimental characterization of each MAGFET, verifying your behavior in absence and in presence of magnetic field.

A. Developing and implementacion of MAGFET on PCB

From of a NMOS standard transistor was developed four MAGFETs with different sizes. The following figures shows the layout of 4 MAGFETs manufactured. Does it refer that The MAGFET have a distance d equal a 1.4 µ, which it is the minimal value acceptable for the technology.

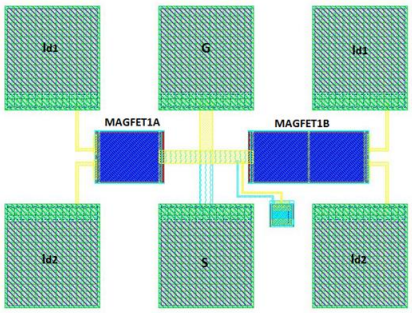

Figure 5 - MAGFET1A with W=38µm e L= 50µm; MAGFET2A with W=38µm; L= 90µm

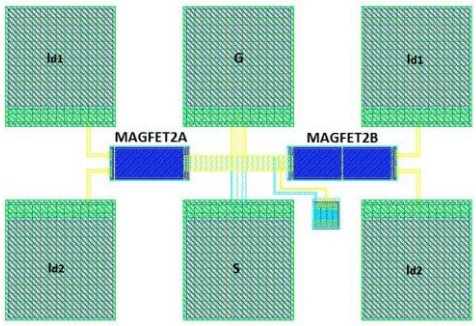

Figure 6 - MAGFET1A with W=20µm e L= 50um; MAGFET2A with W=20µm; L= 70µm.

Then a PCB was developed to put the chips and to realize the necessary measurement for study of each one. The following figure represents the PCB developed where the chips were putted with the chip-on-board (CoB) technical.

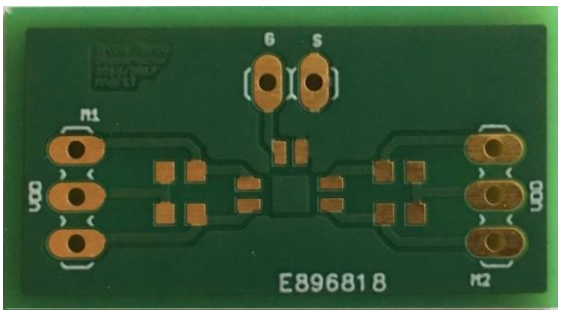

Figure 7 – MAGFET test board (3.1cm by 1.7 cm dimensions).

The following figure represents the MAGFET symbol, it is constituted with 2 drains (V_{D1} e V_{D2}). Being this equal a standard MOS transistor that will be necessary to realize the polarization in the gate(V_g) and in the drains also ($V_{d1,2}$).

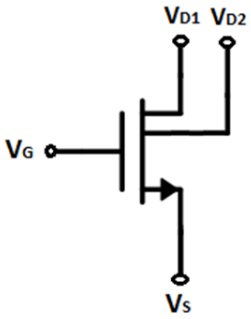

Figure 8 – The MAGFET symbol.

B. MAGFET measurement in the absence of magnetic field

Using a curve plotter equipment to applie several values of Vg (from 0.4 to 1V) and Vds=Vd1=Vd2 (from 0 to 1V), the characteristic curves of currents (drains 1 and 2) in function of Vds and Vg voltage it was obtained. The figure 10 and 11 represents 2 examples (MAGFET 1A and 1B) of the current-voltage characteristic in absence of magnetic field.

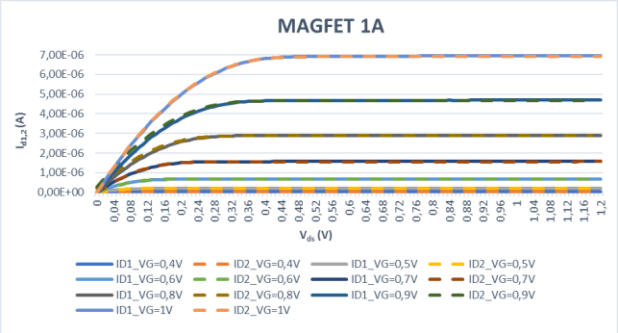

Figure 9- Characteristic curve of MAGFET1B (W=38µm and L= 50µm) in the absence of field.

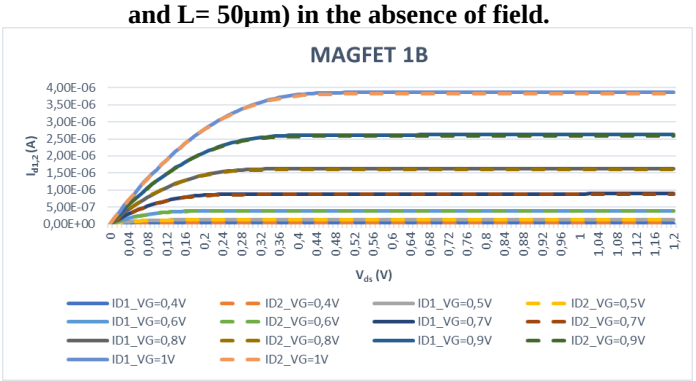

Figure 10 - Characteristic curve of MAGFET1B (W=38µm and L= 90µm) in the presence of field.

Observing the characteristic curves of each MAGFET, it is verified that the current of each drain is in order of microamperes. Ideally these currents should be equals, however there is an offset between the currents (I_{D1}-I_{D2}) in order of nanoamperes.

The offset of the currents can be caused by a systematic error of measure or by the MAGFET sensor (dimensioning of layout and manufactured). But by the research done it was verified that the offset obtained is due to a no symmetry in the drains (layout or manufactured) that will can cause this offset error obtained in each MAGFET.

C. MAGFET measurement in with presence of magnetic field

To apply a magnetic field in MAGFET, it was created two coils with air core and wrapped in an acrylic tube. The first coil has the inductance equal 8,4 mH and the second coil has the inductance equal 2,4 mH. When applying a maximum current possible (1,5A) in the coils, the first coil can only generate a magnetic field equal 1,25 mT and the second coil can only generate a field equal 2,12 mT.

The field generated by coils didn't produce significant changes in the MAGFET current. To produces changes, it is necessary apply fields in order of Tesla to obtain a reasonable response for MAGFET sensor.

To verify the response of sensor to stronger fields (order of Tesla), the solution founded was use a permanent magnet of neodymium. The datasheet of magnet shows that it generate a magnetic field in order of 1,22T.

Figure 11 –Neodymium magnet.

The MAGFET will work in saturation zone and consequently it chose a voltage polarization in gate and drains equal 1V and 0,6V, respectively. The drains voltage value is due to the input common mode chosen for the ADC.

The following table shows the variation of each MAGFET with the magnet presence and respective sensibilities. It is called attention that the current unbalance must be subtracted with the MAGFET to obtain the correct value of currents deflection caused by the magnetic field.

	Negative unbalance				
	Offset (nA)	**I_{d1} (µA)**	**I_{d2} (µA)**	**Unbalance of the currents (nA)**	**Relative sensibility (%)**
MAGFET1A	19,6	6,89	6,93	-55,9	-0,331
MAGFET1B	45,8	3,85	3,83	-28,2	-0,300
MAGFET2A	-42,1	3,65	3,72	-29,5	-0,327
MAGFET2B	-81,5	2,57	2,67	-18,6	-0,290
	Positive unbalance				
	Offset (nA)	**I_{d1} (µA)**	**I_{d2} (µA)**	**Unbalance of the currents (nA)**	**Relative sensibility (%)**
MAGFET1A	19,6	6,95	6,88	48,3	0,286
MAGFET1B	45,8	3,87	3,80	26,3	0,280
MAGFET2A	-42,1	3,67	3,69	27,8	0,310
MAGFET2B	-81,5	2,59	2,65	19,4	0,303

Table 1 – Variation and sensibility of each MAGFET with V_g= 1V and $V_{d1,2}$=0,6V.

By table 1 shows that to a positive unbalance the MAGFET 2A has a greater relative sensibility, and to a negative unbalance the MAGFET 1A has a greater relative sensibility.

The relative sensibility obtained with the magnet is below of 1%, being that to obtain more conclusion it would be necessary to realize measure with different magnetic field and to obtain a relation between the field and the sensibility.

D. MAGFET model

As the MAGFET don't have the provided electric model by the technology manufacturer so, from the experimental characterization we created a model based on the MOS transistor. Then with one MAGFET model will be possible to do an electric simulation in Cadence software.

Initially we tried the first model of MOSFET (level 1) but this model in triode zone had a less curvature in relation to the experimental behavior of MAGFET. Thus, we use the second model of MOSFET (level 2), being this model have in consideration the electrons speed for each mode of MAGFET operation (triode and saturation zone).

The following figure represent the level 2 equations of the MOSFET.

- No operation, $V_{GS} \leq V_T$

$I_d = 0$;

- Operation zone, $V_{GS} > V_T$

$$I_d = \beta * \left\{ \left(V_{gs} * V_{bi} - \frac{\eta * V_{de}}{2} \right) - \frac{2}{3} * Y * \left[(PHI + V_{de} + V_{sb})^{\frac{3}{2}} - (PHI + V_{sb})^{\frac{3}{2}} \right] \right\} * I_{d\lambda};$$

Being that:

$$V_{de} = \min(V_{ds}, V_{dsat});$$

$$V_{bi} = V_T - GAMMA * (PHI)^{\frac{1}{2}} + (\eta - 1) * (PHI + V_{sb});$$

$$V_{sat} = \frac{V_{gs} - V_{bi}}{\eta} + \frac{1}{2} * \left(\frac{Y}{\eta}\right)^2 * \left\{ 1 - \left[1 + 4 * \left(\frac{\eta}{Y}\right)^2 * \left(\frac{V_{gs} - V_{bi}}{\eta} + PHI + V_{sb} \right) \right]^{\frac{1}{2}} \right\};$$

$$V_{dsat} = V_{sat} + V_c - \left({V_{sat}}^2 + {V_c}^2 \right)^{\frac{1}{2}};$$

$$I_{d\lambda} = \frac{1}{1 - \lambda * V_{ds}};$$

Figure 12 – MOSFET level 2.

The followings figures show the experimental characteristic (ID) and the model result to the MAGFET1A and 1B (ID_MODELO).

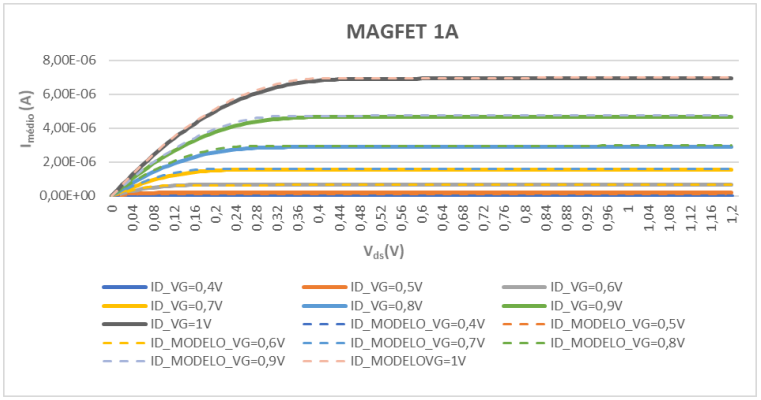

Figure 13 – Model (level 2) of MAGFET1A (W=38µm e L= 50µm).

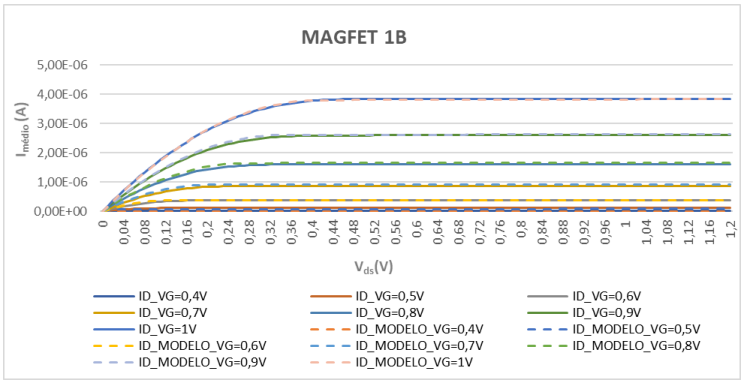

Figure 14 - Model (level 2) of MAGFET1B (W=38µm e L= 90µm).

The level 2 model was implemented to each MAGFET in Verilog A. The following figure represents the symbol and the schematic of MAGFET.

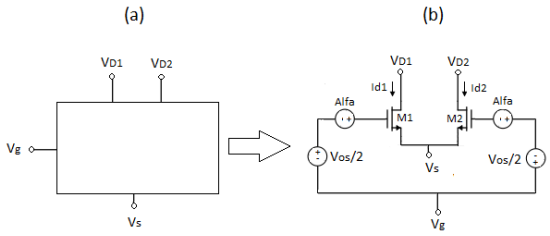

Figure 15 – Symbol (a) and the schematic of MAGFET (b).

The schematic of MAGFET is like a differential pair (two transistor), being this much used as step of amplification in microelectronic. Being V the input voltage in Vg, the equations

(5 and 6) for the input gate of transistor M1 and M2(Vg1 and Vg2) are obtained.

$$V_{g1} = V + \frac{V_{os}}{2} + Alfa \quad (5)$$

$$V_{g2} = V - \frac{V_{os}}{2} - Alfa \quad (6)$$

, being Vos allows to model the offset of MAGFET and Alfa will allow to simulate the variation of current with magnetic field.

With the input definition (Vg1 and Vg2) and from the level 2 equations of MOSFET, the equation to the current in the drain1(I_{d1}) and the drain2(I_{d2}) are obtained as shows the following figure.

$$\begin{cases} I_{d1} = 0 , \quad se \ \ V_{g1} \leq V_T \\ I_{d1} = \beta * \left\{ \left(V_{g1} * V_{bi-} \frac{\eta * V_{de1}}{2} \right) - \frac{2}{3} * Y * \left[(PHI + V_{de1} + V_{sb})^{\frac{3}{2}} - (PHI + V_{sb})^{\frac{3}{2}} \right] \right\} * \ I_{ds\lambda} , se \ \ Vg1 > V_T \end{cases}$$

$$\begin{cases} I_{d2} = 0 , \quad V_{g2} \leq V_T \\ I_{d2} = \beta * \left\{ \left(V_{g2} * V_{bi-} \frac{\eta * V_{de2}}{2} \right) - \frac{2}{3} * Y * \left[(PHI + V_{de2} + V_{sb})^{\frac{3}{2}} - (PHI + V_{sb})^{\frac{3}{2}} \right] \right\} * \ I_{ds\lambda} , \quad Vg2 > V_T \end{cases}$$

Figure 16 – Equation of the current on I_{d1} and I_{d2}

IV. ANALISYS AND IMPLEMENTATION OF INTEGRATED MAGNETIC SENSOR

The implementation of magnetic sensor can be from a topology with an ADC single-ended or differential as shows the following figure.

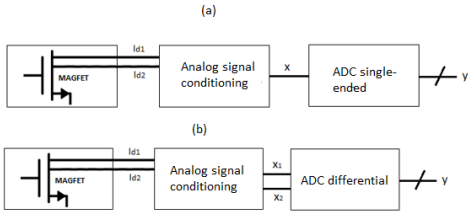

Figure 17 – Implementation in single-ended (a) or in differential (b) to the integrated magnetic sensor.

By the analysis done we conclude that it is better to use the differential topology because this have a higher output excursion and better rejection of noise and common mode disturbances.

The following table represent a comparison between the ADCs most used on the market in relation to the speed, resolution, area and consumption [7]. As focus of the project is based on study of MAGFET and, so it was decided to development an easy ADC to obtain an output digital with low resolution to verify the sensibility of sensor.

ADC type	Speed	Resolution (bits)	Area	Consumption
Flash	High	12	High	High
SAR	Medium - High	16	Low	Low - Medium
Dual ramp	Low	18	Medium	Low - Medium
Sigma Delta	Low	24	Medium	Low

Table 2 -Comparison between the ADCs [7].

The system that the magnetic sensor will be inserted have a low clock frequency (31,25 kHz), it is not needed a higher speed and with this it was used a dual ramp to implement the ADC differential.

The following figure represents the MAGFET and the ADC dual ramp differential with input voltage.

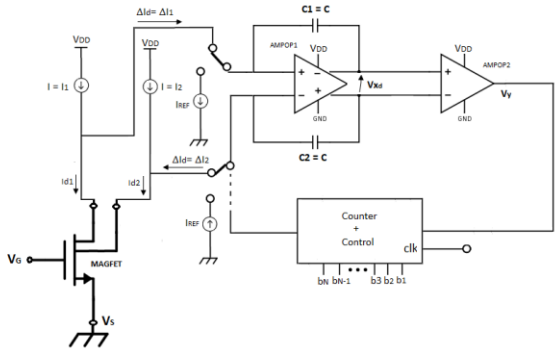

Figure 18 - Schematic of the MAGFET and the ADC dual ramp differential with voltage input.

The operation is like a single-ended topology, that initially the capacitor will be charged by the differential input voltage of MAGFET (V_1-V_2) during the counter maximum time (Tc). Then from the control block there is the reset to the counter and change the switch to the current reference (I_{REF}). Thus, the second time (T_{xd1} or T_{xd2}) will be uncharged the capacitor until the voltage V_{xd} is equal to zero as shows the figure 19. The comparator gives the signal to the control block to stop the counter and shows the binary result.

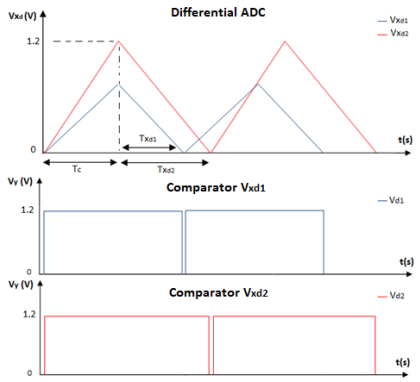

Figure 19 – ADC operation of a differential dual ramp with input voltage.

The following figure represents the full implementation of magnetic sensor, that includes the analog signal conditioning and the differential dual ramp ADC. It was used 4 bits in ADC because the principal objective on this first prototype is verify the dynamic range of the sensor.

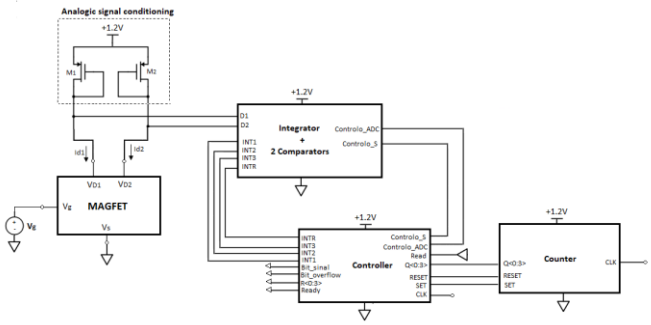

Figure 20 – Implementation of integrated magnetic sensor in 0,13 µm CMOS technology.

The MAGFET will work in saturation zone, being it was used a gate voltage equal 1V(Vg) and in the drains equal 0,6V (V_{D1} and V_{D2}). This chooses of V_{D1} and V_{D2} allows to have the desired value in input common mode ADC. Also, it was used the MAGFET1A to implement and realize simulation to the system.

The following figure shows the implementation of differential integrator with input voltage. It was used V_{REF} to ensure the common mode in reference current source (I_{REF}).

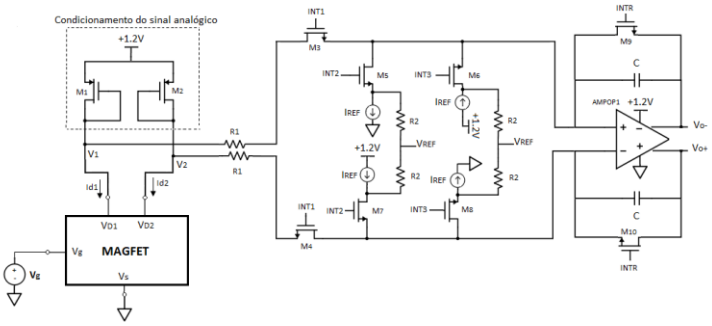

Figure 21 – Implementation of differential integrator with input voltage.

It was used NMOS transistor to work as switch's, that the activation of each transistor (INT1, INT2, INT3 or INTR) is obtained by controller. The activation of INTR on M9 and M10 transistor allows the reset of differential integrator, forcing the capacitors to have the differential voltage equal to 0. When the integrator has a positive excursion is enabled the switch INT2 and when it has a negative excursion is enabled the switch INT3. The controller enables the switch according the value of differential output and this detection of positive and negative unbalance is obtained through a comparator.

The following figure represents the operation of integrator for a maximum negative unbalance on the MAGFET.

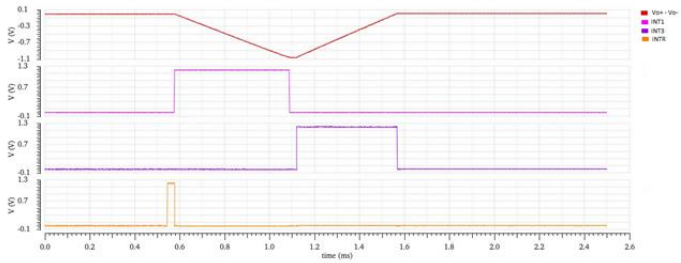

Figure 22- Operation of differential integrator for a maximum negative unbalance on the MAGFET.

The differential excursion in previous figure can get a output equal 1V however the magnetic unbalance (positive and negative) obtained are not symmetric, that the positive unbalance can only get half of the VDD excursion as shows in the following figure.

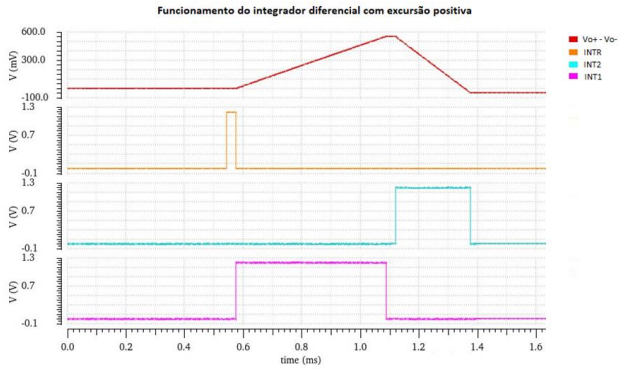

Figure 23 - Operation of differential integrator for a maximum positive unbalance on the MAGFET.

To the system are necessary 2 comparators to generate the signal for controller (Control_ADC and Control_S). The Control_ADC signal allows to control the counter and change of switches in the circuit, whilst the Control_S signal allows to detect if the unbalance of field is positive or negative. This controller allows to change the sense (charge or discharge) of reference current of each input, according the differential value of integrator output.

The following figure shows the 2 comparators, that these signals are sent to the controller and V_{REF} is equal $V_{DD}/2$.

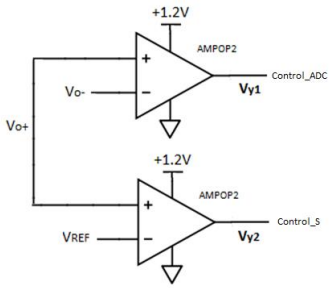

Figure 24 – Signals sent to the controller.

The following figure represents the master-slave JK flip-flip implemented on this project. This is constituted with 2 JK flip-flops, that the flip-flop slave has a clock input inverse to the master flip-flop to allow that the Q and $\bar{Q}$ output change only when the clock changes from low to high (rising edge).

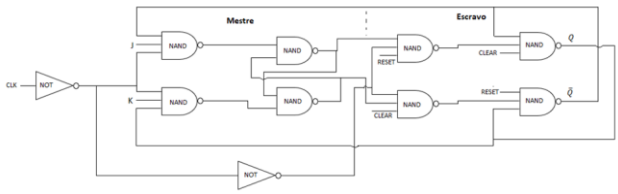

Figure 25 – The master-slave JK flip-flop implemented to the development of the counter.

The following figure represent the counter implemented on system. It is to be noted that the flip-flop works in commutation condition, in that the 2 inputs of the first flip-flop are in high.

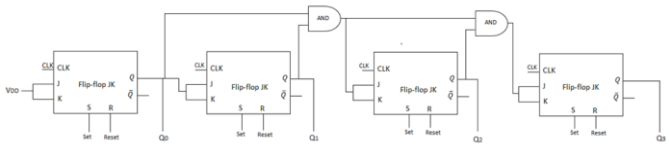

Figure 26 – 4 bits counter developed with JK flip-flops.

The controller is one of the most important parts of the system because this have the controls of ADC switch's, the counter and shows the binary value. Initially this is developed in Verilog code and after the compilation with technology gates we have the final schematic of controller.

The following figure shows an example of different states of controller on the differential integrator. In a differential analysis to the control, phase T1 represents the charging of the capacitor. The T2 phase happens when the counter has the maximum value, on what the switch enabled is turned off and the counter does the reset. The T3 and T4 phase depends the result of phase T2, on what the switch is enabling to discharge the capacitor according the value of input differential.

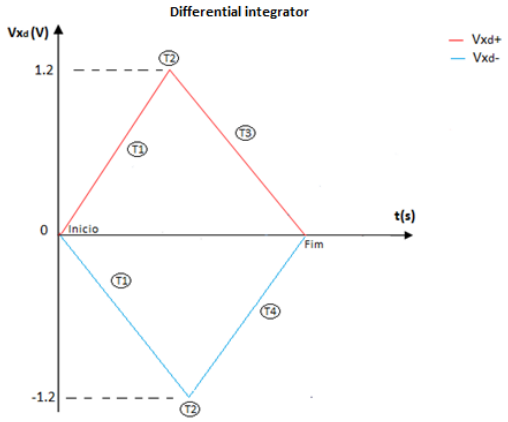

Figure 27 – Differential integrator with different phases of the controller.

If the differential value of integrator is positive the switch 2 is enabled and if the differential is negative the switch is enabled. The following figure represents the schematic of the controller after compiling the Verilog code.

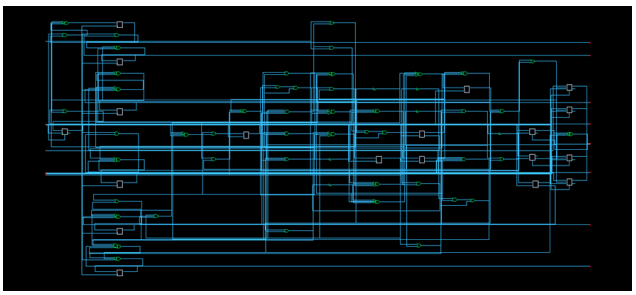

Figure 28 – Schematic with logic gates of the controller.

The following figure represents the block with inputs and outputs of integrated magnetic sensor. It is verified that only the controller was implemented digitally, and the rest were implemented in analogic.

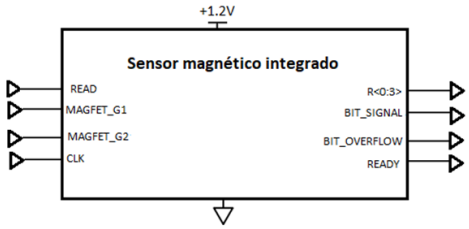

Figure 29 – Block with inputs and outputs of integrated magnetic sensor

To make a reading of a field is necessary enable the read input and the ready output is enabled when the system realizes that reading, showing the result (R<0:3>), the unbalance sense (BIT_SIGNAL) and if there is an overflow enables the correspondent flag (BIT_OVERFLOW).

The following figure represents one example of mix signal simulation to the integrated magnetic sensor. This simulation is accomplished with the obtained value by MAGFET1A in absence of magnetic field.

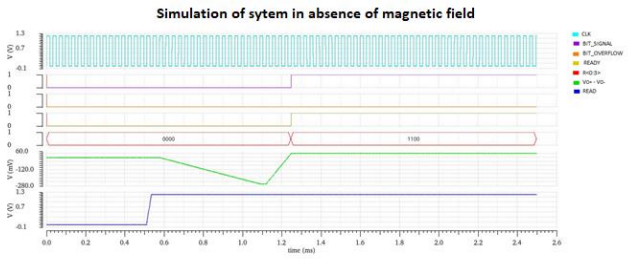

Figure 30 – Simulation of magnetic sensor in absence of magnetic field.

It is to be noted that the MAGFET has an offset and therefore with no field the field reading it was obtained equal to 3 (1100).

The following figure represents the positive unbalance of mix signal simulation to the integrated magnetic sensor. How to see the field reading it was obtained equal to 7 (1110).

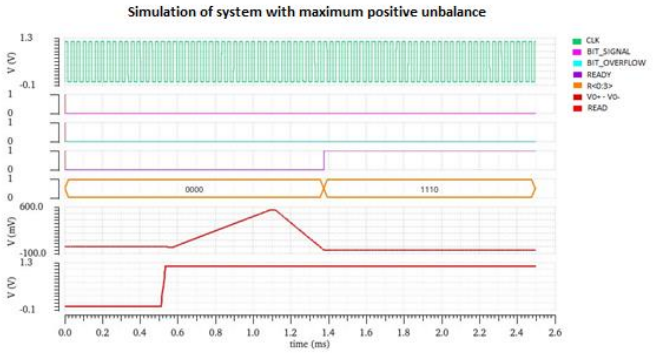

Figure 31 - Simulation of magnetic sensor in presence of magnetic field.

The following table shows the reading done by the implemented system, considering the offset errors of MAGET and differential AMPOP.

Offset/maximum unbalance of field	Read (value decimal)
Offset MAGFET (no field)	3
Offset AMPOP	0
MAGFET (maximum positive unbalance)	7
MAGFET (maximum negative unbalance)	13
MAGFET (maximum positive unbalance) + offset AMPOP	7
MAGFET (maximum negative unbalance) + offset AMPOP	13

Table 3 – Reading done considering the errors.

As the integrator is differential, the offset of AMPOP don't have influence the magnetic field reading, so the reading error is only due to the offset of MAGFET.As the field reading includes the offset error of MAGFET, Therefore the value obtained is necessary to remove the initially error of the system (1100). So, it has a maximum positive and negative unbalance equal to 4 (0010) and 10 (0101), respectively.

The following table shows the power and energy consumed by system to the reading of a magnetic field. The principal objective was implement an integrated magnetic sensor with low consumption.

Integrated magnetic sensor	Current consumption (µA)	Power (µW)	Maximum energy (nJ)
MAGFET	13,82	16,5	16,89
Differential AMPOP	2.695	3,234	3,31
Comparator	0,614	0,73	0,74
Counter	0,009	0,01	0,001
Controller	1,76	2,1	2,15
Total of implemented system	18,898	22,57	23,09

Table 4 - Consumption of integrated magnetic sensor

The system has the current consumption equal to the 18,898 µA, being the large percentage of this consumptions is due to the currents polarization in the drains of the MAGFET.

V. CONCLUSION

The study of the MAGFET sensor allowed to manufacture 4 MAGFETs in CMOS technology and realize an experimental characterization of each of them, showing your behavior with absence and presence of magnetic field. The initial idea for experimental characterization of MAGFET's was developed coils with air core to produce magnetic fields, however the field generated by these was not strong enough to influence the operation of the MAGFET.

The alternative solution was to use a neodymium magnet (field intensity equal to 1.22T), which was able to create small changes in the currents of each MAGFET (in order of Nano Amperes), taking to a relative sensitivity of less than 1%. The result obtained with the magnet did not allow to characterize the MAGFETs for different magnetic field intensities.

To realize the experimental study of the MAGFETs a fully integrated magnetic sensor was implemented. A low-resolution (4bits) differential dual-ramp ADC was used, being that the main objective of this first prototype is verify the sensitivity of the MAGFET sensor.

The obtained limitation in the experimental study of MAGFET'S had influence in the implementation of the system, in which it has an initial error (no field) and the field unbalance are not symmetrical. However, the implemented system is low consumption (18,898µA), being the large percentage of this consumptions is due to the currents polarization in the drains of the MAGFET

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