High Frequency Integrated DC/DC Converter
Digital Control

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Abstract—This work focuses on the power management of electronic circuits that operate with low load currents, in the range of a few hundred mA, with voltage regulated by a DC/DC converter since efficiency requirements don’t allow to consider the application of a linear regulator. Therefore, the use of a buck converter, whose efficiency doesn’t decrease significantly with the decrease of the load current, was studied, as well as the use of high frequency in order to allow the reduction of buck’s filter elements.

After the DC/DC step down converter design was completed, the power stage modular approach was studied. The solution consisted on including in each module a portion of the power transistors and their respective drivers, dynamically enabling just the number of necessary modules, depending on the load current applied, so that the reference voltage was reached. By doing this, the conduction and switching losses are optimized as the load current decreases and, the efficiency of the converter is maintained approximately constant.

Index Terms—Buck Converter, CMOS, High Frequency DC/DC, Modular Project

1. INTRODUCTION

Recently the use of portable devices, with many different features and purposes, has increased substantially. In particular, we have seen a mass use of mobile phones, laptops and more recently of tablet devices. However, all of these devices have one thing in common, they require both autonomy and portability. And, although the size of the equipments have been reduced, the number of different applications that they have to perform has increased.

All these functionalities and applications involve a rise in their energy consumption and a corresponding demand for increasing their battery capacity, but it is intended that they remain portable and with high autonomy. So, we can say that portable device battery capacities hasn’t kept pace with their power consumption. To that end, since the size of the equipment and, consequently its battery has been decreasing, it is necessary that they have a high efficient power management. For this reason, the power management circuits are critical blocks in portable equipment. These aim to reduce power consumption and improve the efficiency of equipment taking into account their different types of possible uses (for example, performing communications or being on standby). This, in addition to increasing the battery life will also improve the system performance.

The purpose of using high switching frequency in this work is to allow buck’s filter elements to be smaller and reach their full integration into System on Chip (SoC), or partially in a System in Package (SiP). However, the increased frequency results in a raise of the switching losses associated with the converter and, as such, can strongly penalize its performance.

The frequency used in this project, $20MHz$, is therefore a compromise between the analysis of the effects that high frequency will arouse in converter’s efficiency and the partial integration of its filter in a SiP (concerning its inductive element).

Another key aspect in the project is the current range used in the output. What is intended with this study is to explore the feasibility of a DC/DC converter operating in a current range of a few hundred mA. That range is low for a DC/DC converter point of view but, sufficiently high to make unfeasible the use of a linear regulator (due to its low efficiency). It should be taken into account that the efficiency of a linear regulator will be given by the ratio between its output and input voltages [1]. Consequently, in this case, we would have an efficiency of approximately 30%.

Linear regulators are a simple alternative in order to obtain a regulated output voltage lower than the input voltage. However, they are always associated with a significant power dissipation and that is the main reason why they are primarily used in applications that require low output current (where the absolute value of the energy associated with these losses is not critical). Nevertheless, with the increasing of load current, not only the power losses increase as well, as there’s a greater difficulty in dissipating the heat associated with such losses. As such, the DC/DC converters have been the primary choice when dealing with applications that require higher output current, due to its better efficiency (over 90%) and lower power dissipation [1].

However, the DC/DC converters have the disadvantage, compared to linear regulators, of requiring an external filter that can be minimized by increasing the switching frequency. Yet, when considering the use of a higher frequency than the usual 1–5$MHz$ in a DC/DC converter, one should pay special attention to their switching losses. These are increasingly significant and penalty in terms of the efficiency obtained, as lower the converter’s operating frequency is.

Thus, the output current to consider can be said to be reduced when considering an application of a DC/DC converter, where it will have a lower efficiency (compared with the efficiencies reached when operating at lower frequencies but with a bulkier filter), although it is high from the point of view of the application of a linear regulator. Nonetheless, even a lower efficiency (around 80%) for a DC/DC converter remains higher than that.
The organization of this paper is as follows.

In section II the concept of the control method proposed is introduced.

The aim of section III is to detail the steps taken on the initial design of the DC/DC converter. This primarily design will be used as a starting point towards the modularization of converter’s power stage.

On section IV is studied how to modularize the converter’s power stage. It contains the several steps that allowed to define the power stage unitary modules, as well as the analysis of the results obtained after the implementation.

For last, section V presents the overall conclusions about the work made and the future steps that could be done towards a final prototype.

II. PROPOSED CONTROL METHOD

As previous mentioned, the use of higher switching frequency will lead to an increase in the energy losses associated with the switching of the transistors, making these the most relevant, compared to the transistor’s conduction losses. Since it is intended that the switching losses are as minimal as possible, it is usual to consider more than one mode of operation for the converters. Usually the workload in mobile equipments is variable over time, alternating between long periods of inactivity (standby) and short time intensive tasks. So the ideal is to have a different treatment to each of the operating modes of the devices.

Typically, we can approach an ideal switched converter (i.e. get a high efficiency regardless of the load conditions) when using a hybrid mode, usually composed by Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM). The mode of operation will thus be chosen according to the load conditions [2] [3] [4]. For a low energy mode, such as sleep, standby or power saving, the usual modulation considered is PFM. In cases where there’s an heavy load, is then frequently used PWM. Thereby providing an alternating way between a lower switching frequency with PFM and a higher switching frequency when changing to PWM.

The buck converter proposed in [5] uses a hybrid mode, using PWM for heavy loads and Switch-On-Demand Modulation (SODM) when the converter’s load is lower. This SODM control method proposed in [5], consists in skipping cycles in which the converter should be on its on-state, thereby decreasing the switching frequency. This will, according to the authors, allow the converter to pass from its Discontinuous Conduction Mode (DCM) to the Continuous Conduction Mode (CCM) in a smooth and automatic way, as the load current increases.

However, this work [5], was also used a technique of Switch Size Control (SSC), which consists in the changing of the power transistors size according to the conditions prevailing in the converter’s load. Thus, the authors divided the power stage into four segments, where only one of it is used when the converter has a low load current.

Thus, SSC technique used in [5] was the influence for the control method developed in this work. Taking into account the concept of dividing the power stage, but using the number of the connected segments as a control method (not only to decrease the power associated with the power transistors and their drivers as in [5])

The control method implemented requires the modularization of the power stage, insofar as it consists of several modules containing a specific number of power transistors and their drivers. This additional modules are added to the power stage when the output voltage of the converter is lower than the reference voltage and, otherwise removed as the output voltage decreases.

The number of modules present in the power stage will be the only mean used for correcting the voltage at the converter’s output, as its duty cycle is fixed. By setting the time in which the converter is in its on-state, it is not necessary to have a pulse modulation, as in PWM, which implies a significant current consumption.

The control method developed to set how the constituent modules of the power stage are connected or disconnected, is done in a simple digital manner, based on the digital word originated from the comparison between the output voltage sampled and the reference voltage.

The fact that the power stage is modular and its control done digitally, allow it to be adapted or changed in the future, depending on the needs or requirements that may be later identified. This adaptability is one of the advantages of using digital control methods.

III. POWER STAGE PROJECT

A. Converter’s Components

The specifications for the buck converter set the frequency at $20MHz$ and the capacitor of its filter to be $1\mu F$. It was also specified that the typical value of the input voltage was $3.3V$ and the reference voltage should be $1V$.

So, the duty cycle of the converter, in its CCM, is approximately $0.3$. Considering a voltage drop in the inductor of $2V$ and its current amplitude to be $300mA$, the inductor was deduced to have $100\pi H$.

B. Power Transistors Drivers

One of the key aspects on buck’s operation is the switching of its power transistors. So, in order to enable the converter to switch between its on-state and off-state, it is necessary that the power transistors are turned on or off, according to the intended operating state.

Preventing the appearance of a shoot-through current, it was necessary to control both power transistors intercalating their conduction with a non-overlap time. This was implemented by placing a driver (that consisted in inverters) for each power transistor, which only allows it to be connected after the cutting off of the other transistor.

C. Converter Active Elements Sizing and Proportions

In choosing the size of transistors, it is necessary to consider the compromise between their conduction losses and the ones related with their switching.

Thus, by increasing power transistors channel width it is possible to decrease the resistance of their channel and minimize their conduction losses. However, increasing the transistor width will also result in a raise of the parasitic
capacity associated with their terminals, including its gate, and so the switching losses are increased too.

Then, the dimensions of the power transistors need to be varied in order to find the optimal solution leading to a higher efficiency. Also, taking into account the current that will flow through the power transistors, these will have dimensions that prevent them of being composed by a single cell. As such, they have been implemented using arrays of smaller transistors with 10 fingers and a width of 30\(\mu\text{m}\).

However, unlike what happens with the length (L), which will vary depending on the considered transistor (pMOS or nMOS, of power transistors or their drivers), the width (W) of the base transistor will always be constant.

The proportions used on the sizing of the transistors and their drivers were:

\[
\left(\frac{W}{L}\right)_{\text{pMOS}} = 3 \left(\frac{W}{L}\right)_{\text{nMOS}}
\]
\[
\left(\frac{W}{L}\right)_{\text{PwrTrans.}} = 20 \left(\frac{W}{L}\right)_{\text{Driver}}
\]

(1)

D. Driver’s Transistors Length (L)

The drivers transmit the control signal that will turn on, or off, the respective power transistor. The ideal would be to have an instantaneous transition between the on and off signal. As such, it is desired for driver’s transistors to be as fast as possible so that the transition of their signal could be closer to the ideal case.

Faster switching implies that the transistor has to have more current flow between its terminals. So, that involves decreasing the transistor’s length, enhancing its speed.

As in the technology used the minimum length for pMOS and nMOS transistors is 300\(\mu\text{m}\) and 340\(\mu\text{m}\), respectively, these were the lengths used for the driver’s transistors.

E. Power Transistors Length (L)

In order to analyze what will be the appropriate length for the power transistors, it will be necessary to assign them a width nearby the one they will have at the end of their sizing.

After their estimated sizing were then determined their associated leakage currents according to the different lengths considered.

Estimated transistor’s width: To be able to vary the length of the power transistors and determine its optimal value, it is initially necessary to provide a realistic width of the power transistors.

So, it was decided to assign a length of 600\(\mu\text{m}\) to the power transistors, consider an output current of 250\(\text{mA}\) and adjusting the duty cycle as necessary to maintain an output voltage of 1V. The iterations were made by changing the number of the base transistors present in the power transistor nMOS, being the other parameters (number of base transistors in the power transistor pMOS and the number of the transistors in the drivers) calculated according to the proportions defined.

Based on the efficiencies obtained, the best condition was achieved with 260 power transistors nMOS, corresponding to an efficiency of 81.62%.

Power Transistor’s Leakage Current: With the approximate size of the power transistors defined, the leakage currents associated with the power transistors were simulated, according to their possible different lengths.

The length has been modified from the lowest value possible (300\(\mu\text{m}\) for the pMOS and 340\(\mu\text{m}\) for the nMOS) up to the 600\(\mu\text{m}\), which had been used initially for estimating the size of the power transistors. To better observe the leakage current effects, the temperature of the simulations was set to 125\(^\circ\text{C}\).

In evaluating the results obtained it is necessary to take into account that the increasing of the channel length translates into lower losses due to leakage currents. But also results in increasing the gate capacitance, with higher switching losses and, in a reduction of power transistors switching speed.

Thus, the analyses focused on the points at which an equal increase of the transistor’s length led to a further reduction in the leakage current. These being the points where the leakage current curve had a higher slope.

The lengths that better suit this condition were the combination of 340\(\mu\text{m}\) for the power transistor pMOS and, 380\(\mu\text{m}\) for the nMOS. But, despite considering this combination as a better compromise between the trade-offs identified, other combinations were taken for comparison (in the next step for the evaluation of what should be the power transistor’s length).

Effect of Power Transistor’s Length: After the identification of the leakage currents associated with the power transistor’s different lengths, their impact was checked out changing also the power transistor’s width. The output current specified for this simulation was approximately 250\(\text{mA}\) and, the duty cycle adjusted so it could be achieved an output voltage of nearly 1V. In these simulations, 12 different combinations were tested and the best result achieved, taking in consideration the reduction of the leakage current, was composed by 698 pMOS power transistors with a length of 340\(\mu\text{m}\), 260 nMOS power transistors with a length of 380\(\mu\text{m}\) (and, their driver implemented by 31 pMOS and 12 nMOS), where the efficiency obtained was 86.65%.

This stage also allowed reducing the number of combinations that should be evaluated. Meaning that it should be considered two different combinations (one of which is that presented before) and the ones correspondent to the border restraints (maximum and minimum lengths tested), in order to compare the results.

Selection of Power Transistor’s Length: To choose which final length should be assigned to the power transistors, was then done an analysis of the results obtained with the four different combinations of lengths identified in the previous step. But in this case, also changing the output current of the converter to: 200\(\text{mA}\), 250\(\text{mA}\), 300\(\text{mA}\) and, 400\(\text{mA}\).

The different efficiencies obtained allowed concluding that the option with lengths 340\(\mu\text{m}\) (for pMOS) and
380nm (for nMOS) were the most regular and independent of the output current on the converter. Furthermore, in all the combinations simulated, the best efficiencies are obtained when the output current is close to 300mA, whose results could be seen in table I and figure 1.

### TABLE I
RESULTS OBTAINED WITH AN OUTPUT CURRENT OF 300mA, FOR DIFFERENT COMBINATIONS OF POWER TRANSISTOR’S LENGTH.

<table>
<thead>
<tr>
<th># pMOS_Pot</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Comb. P1</th>
<th>Comb. P2</th>
</tr>
</thead>
<tbody>
<tr>
<td>W pMOS_Pot</td>
<td>23.4</td>
<td>260</td>
<td>15W</td>
<td>15W</td>
</tr>
<tr>
<td>L pMOS_Pot</td>
<td>600</td>
<td>340</td>
<td>20.9</td>
<td>20.9</td>
</tr>
<tr>
<td>Iin mA</td>
<td>107</td>
<td>107</td>
<td>107</td>
<td>107</td>
</tr>
<tr>
<td>Ton ns</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>pMOS_Pot nm</td>
<td>340</td>
<td>340</td>
<td>340</td>
<td>340</td>
</tr>
<tr>
<td>Iin_ctr mA</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>iLeakP uA</td>
<td>1.7</td>
<td>1.7</td>
<td>1.7</td>
<td>1.7</td>
</tr>
<tr>
<td>Io mW</td>
<td>352</td>
<td>352</td>
<td>352</td>
<td>352</td>
</tr>
<tr>
<td>nMOS_Pot nm</td>
<td>380</td>
<td>380</td>
<td>380</td>
<td>380</td>
</tr>
<tr>
<td>Pin_ctr mW</td>
<td>18</td>
<td>18</td>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td>iLeakN uA</td>
<td>2.1</td>
<td>2.1</td>
<td>2.1</td>
<td>2.1</td>
</tr>
<tr>
<td>Po mW</td>
<td>321</td>
<td>321</td>
<td>321</td>
<td>321</td>
</tr>
<tr>
<td>pMOS_Drv η</td>
<td>86.8</td>
<td>86.8</td>
<td>86.8</td>
<td>86.8</td>
</tr>
<tr>
<td>nMOS_Drv</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
</tr>
</tbody>
</table>

IV. MODULAR IMPLEMENTATION OF THE DC/DC CONVERTER

A. Power Stage Modularization

After the power stage initial project it was studied the possibility of its modularization. As it was perceptible, just by increasing or decreasing the number of basic transistors in the power transistor’s arrays the output voltage obtained varied. However, in the power stage project the intention was to find the perfect design. So, besides changing the transistor’s width and length, the duty cycle was also adjusted to achieve the desired output voltage.

The goal in the power stage modularization is to set the converter’s duty cycle and, achieve the desired output voltage by only dynamically setting the number of active power transistors and their drivers.

The modular structure implemented is depicted in simplified form in figure 2.

As is present in the representation of the modular power stage, the modules required for a particular converter’s configuration are connected in parallel. Thereby adding the number of base transistors needed to each of its active elements.

This modularization will involve compromises on the variation levels of either output voltage and current, when adding each module. Therefor, the less base transistors of each active element that are present on each module, the greater will be the precision obtained on the output voltage. On the contrary, the more base transistors that are present in each module, the higher will be their impact on the variation that they will produce in the output voltage. On the output current range achieved, the impact will be similar. As there are more base transistors in each module, the reference voltage is obtained for less output current values.

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Fig. 1. Comparison of results obtained with an output current of 300mA, for different combinations of power transistor’s length.

As is possible to see in figure 1, while the efficiency in “Comb. P1” is slightly lower than the one obtained for “Minimum”, there is a significant decrease in the power transistor’s leakage current. Being this the main reason why the "Comb. P1" was the one chosen for the power stage initial sizing.

F. Power Stage Initial Design

The converter’s initial project included not only the design of its passive elements, but mostly its power stage.

In the case of power transistor’s drivers, the main feature taken into account was their switching speed, which is why their active elements have been designed with the minimum length allowed by technology.

As regards the power transistors, compromises had been made on its design between what would be their conduction losses, those associated with its switching and their speed in state transitions.

After the study of several possible combinations for the power transistor’s width and length, considering different load currents, the design selected was the one that led to the best efficiency, balancing the different commitments already indicated. In table II is described the configuration chosen and, the simulation results obtained.

### TABLE II
RESULTS FOR THE POWER STAGE INITIAL SIZING.

<table>
<thead>
<tr>
<th># pMOS_Pot</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Comb. P1</th>
<th>Comb. P2</th>
</tr>
</thead>
<tbody>
<tr>
<td>W pMOS_Pot</td>
<td>20.9</td>
<td>260</td>
<td>107</td>
<td>107</td>
</tr>
<tr>
<td>L pMOS_Pot</td>
<td>340</td>
<td>380</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>iLeakP uA</td>
<td>1.7</td>
<td>1.7</td>
<td>312</td>
<td>312</td>
</tr>
<tr>
<td>Po mW</td>
<td>352</td>
<td>352</td>
<td>1.029</td>
<td>1.029</td>
</tr>
<tr>
<td>nMOS_Pot</td>
<td>380</td>
<td>440</td>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td>Pin_ctr mW</td>
<td>321</td>
<td>321</td>
<td>600</td>
<td>600</td>
</tr>
<tr>
<td>iLeakN uA</td>
<td>2.1</td>
<td>2.1</td>
<td>3.0</td>
<td>3.0</td>
</tr>
<tr>
<td>nMOS_Drv η</td>
<td>86.8</td>
<td>86.8</td>
<td>3.56</td>
<td>3.56</td>
</tr>
<tr>
<td>pMOS_Drv</td>
<td>12</td>
<td>12</td>
<td>1.03</td>
<td>1.03</td>
</tr>
</tbody>
</table>

---

As is present in the representation of the modular power stage, the modules required for a particular converter’s configuration are connected in parallel. Thereby adding the number of base transistors needed to each of its active elements.

This modularization will involve compromises on the variation levels of either output voltage and current, when adding each module. Therefor, the less base transistors of each active element that are present on each module, the greater will be the precision obtained on the output voltage. On the contrary, the more base transistors that are present in each module, the higher will be their impact on the variation that they will produce in the output voltage. On the output current range achieved, the impact will be similar. As there are more base transistors in each module, the reference voltage is obtained for less output current values.
This granularity based on how many transistors must be present in each module has to be balanced due to the identified commitments. The target is to increase the modularization of the power stage (which means to have the most possible base transistors in each module) without losing precision in both the output voltage obtained and the current range supported.

In the following parts of this section are described the steps that were taken for the selection of granularity. Trying to increase the modularization of the power stage without prejudice its performance.

The contents of each module are shown in figure 3, also in simplified form. As can be seen, each module has four major components that contain a number of basic transistors corresponding to transistors: power PMOS, power nMOS, driver’s pMOS and driver’s nMOS.

![Module representation](image)

**Fig. 3. Module representation.**

### B. Transistor’s Variation Analysis

As indicated before, there is a need to verify how many base transistors could be allocated in a module, respecting the commitments already identified. After some initial simulations, it was stipulated that it should be observed the changes occurring when incrementing 20 nMOS base transistors at each time. Since for a lower number, the changes in the output voltage were too minimal, leading to a very low granularity and, a numerous of modules in order to allow the reference voltage to be reached.

For each level of output current (400mA, 300mA, 200mA and, 180mA) was then tested the effect that the variation indicated caused, both within the obtained output voltage and in the efficiency reached.

The starting point for the number of nMOS base transistors to be used was 260, since it corresponds to the initial power stage project. The other transistors were then adjusted according to the proportions that needed to be respected. For each different configuration tested was also observed the variation that occurred in terms of the output voltage reached and the efficiency obtained. So, it was possible to check how an addition of each these set of base transistor altered those parameters.

In terms of the output voltage variation was identified that, as the output current decreases, it takes higher absolute values. For example, in conditions adjacent to the

### C. Unitary Module Proportions

Regarding the efficiency obtained, it should be noted that between the maximum value obtained (86.3% for 300mA) and its minimum (86.4% for 180mA) it just varies 0.5%.

<table>
<thead>
<tr>
<th>Base Trans.</th>
<th>400mA</th>
<th>300mA</th>
<th>200mA</th>
<th>180mA</th>
<th>Minimum</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS</td>
<td>16</td>
<td>13</td>
<td>8</td>
<td>7</td>
<td>5</td>
</tr>
<tr>
<td>nMOS</td>
<td>260</td>
<td>290</td>
<td>160</td>
<td>160</td>
<td>120</td>
</tr>
<tr>
<td>pMOS</td>
<td>16</td>
<td>13</td>
<td>8</td>
<td>7</td>
<td>5</td>
</tr>
<tr>
<td>Efficiency [%]</td>
<td>86.1</td>
<td>86.3</td>
<td>86.4</td>
<td>86.4</td>
<td>86.2</td>
</tr>
</tbody>
</table>

In the table III, are presented the results for the configuration chosen in each output current level analyze (400mA, 300mA, 200mA and, 180mA). Also, are presented the “Minimum” configuration that corresponds to the combination with the minimum base transistors with which the converter still operates in the CCM.
stage, and that correspond to the minimum base transistors estimated before to be necessary to maintain the converter on its CCM. And, the “Additional Modules” that will be added only when needed to reach the reference voltage.

D. Proposed Control

The implemented control aims to turn on, or off, the number of necessary “Additional Modules” according to the converter’s output voltage. When the output voltage is lower than the reference voltage, it is necessary to connect “Additional Modules” until it is achieved. On the contrary, when the inverter output voltage exceeds the reference voltage there are “Additional modules” that need to be disconnected.

In order to know if the output voltage is higher, or lower, than the reference voltage, it is necessary to use an Analog-to-Digital Converter (ADC). The ADC allows to translate the analog output voltage to a digital word representative of its value. Since the implementation of the ADC is already outside the scope of this work, certain characteristics were assumed only from a conceptual point of view, adjusted to the modularization of the power stage and not for an ADC in particular. Since it is intended to control 12 “Additional modules”, it was assumed that it would be used an ADC with 24 bits, whose digital word encoding is performed in thermometer code.

The digital word Sel < 0 : 23 > in thermometer code provided from the sampling and comparison done by the ADC is then used by the control in order to turn on, or off, the number of “Additional Modules” necessary. However, it was necessary to divide it into two other distinct arrays: bitH < 1 : 12 > and bitL < 1 : 12 >.

![Fig. 4. Correspondence representation of the digital word and the "Additional Modules".](image)

As it is represented in figure 4, the bits bitHx and bitLx allow controlling one “Module x”. Thus, it is the combination of these two bits which decides whether a module should be turned on or off.

Before describing how the module’s control was implemented, using the arrays bitH < 1 : 12 > and bitL < 1 : 12 >, it is necessary to observe their correspondence with the digital word (in thermometer code) obtained from the ADC.

<table>
<thead>
<tr>
<th>Module</th>
<th>#pMOS_Pwr54</th>
<th>#nMOS_Pwr20</th>
<th>#pMOS_Drv2</th>
<th>#nMOS_Drv1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Module</td>
<td>54</td>
<td>20</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

TABLE IV

Number of base transistors in each module.

As it is perceptible by the condition where is necessary to maintain the previous module state, the control method has to have memory. This way the module’s state assigned in a previous assessment of the output voltage sampled can be maintained if necessary. To implement the control’s memory it was used a NAND latch.

In a state where is intended to increment a specific module, it corresponds to a latch set. Otherwise, when a module needs to be removed, that is accomplished by doing a reset in the latch. However, the latch will be on hold either when it is intended to maintain the previous state attributed to a module and, in the impossible case to occur (given the representation of the digital word in thermometer code).

Regarding the control signals that should be given to the power transistors, it is necessary to identify the situations where they should be enable.

In the case of the pMOS power transistor, it should only be active when the latch is on set state (identifying that a particular module should be connected) and when the converter is in its on-state (that corresponds to the clock’s raising edge).

For the nMOS power transistor, it is also intended to be switched on only when the latch is in set state, but simultaneously with the falling edge of the clock, which corresponds to the converter's off-mode.

After identifying when the power transistors may, or may not, be connected, it is also necessary to ensure that

- \([V_O = V_{ref}]\) That means that \(bitL < 1 : 12 > = 1\) and \(bitH < 1 : 12 >= 0\) once the reference voltage has been reached. So it is intended that the modules remain in the state they were in before. Therefore, the combination of modules (connected or disconnected) which allowed reaching the reference voltage should remain unchanged.

- \([V_O < V_{ref}]\) In this case \(bitH < 1 : 12 >= 0\) but not all bits in the \(bitLx\) array are unitary. So, the reference voltage was not reached and the modules which have \(bitLx = 0\) need to be connected.

- \([V_O > V_{ref}]\) This situation is dual of the previous one. In this case \(bitL < 1 : 12 >= 1\) but not all the \(bitLx\) array is null. So, the output voltage is higher than the reference voltage and the modules which have \(bitHx = 1\) need to be disconnected.

With the three possible scenarios described and identified their correspondence with the arrays \(bitHx\) and \(bitLx\), it is showed on table V how the modules should be controlled.

<table>
<thead>
<tr>
<th>bitLx</th>
<th>bitHx</th>
<th>Actions</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Enable Module x</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Impossible</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Hold</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Disable Module x</td>
</tr>
</tbody>
</table>

TABLE V

Analysis of actions to take for each combination \(bitHx\) and \(bitLx\).
it will not occur an overlap on their conduction.

Thus, it is intended that a power transistor only be turned on after the other one is already turned off. Otherwise, there will be some periods in which both power transistors would be simultaneously conducting in these switching stages (between the converter’s on-state and off-state).

The implemented control may be considered to be divided into three different parts, being these represented in figure 5.

![Control Circuit Representation](image)

The first part "States" corresponds to the analysis of the arrays $bitHx$ and $bitLx$ and, the respective evaluation of which state should be attributed to a "Module $x$" (enable it, disable it or hold its previous state).

The second part "Impulses" is where the control signals for the power transistor’s gates are defined.

And the last one "Non-Overlap" guarantees that the control signals will not cause any simultaneous conduction of the power transistors.

**E. Effects of Including Control**

After the unit module proportions are set and each module’s control defined, it is necessary to check the impact of control’ insertion on the converter’s efficiency.

As expected, the power associated with the converter’s control elements increased slightly, from about 1.6$mW$ a 1.8$mW$. However, it was also observed that either the voltage and current on the converter’s output decreased slightly, when the control proceeded to dictate the signals for the power transistor’s gates.

Regarding the efficiency obtained there is also a reduction, but it doesn’t exceed 0.7%. Being even less significant (only 0.1%) in the best case identified, i.e. for a current of approximately 300$mA$.

Due to the reductions in the voltage and current at the converter’s output, it was decided to adjust the number of base modules present in the power stage.

Thus, the number of base modules was increased to 7 and then observed the consequences that such increase could imply in the number of additional modules used for each output current level.

The results obtained allowed concluding that regarding the output current the raise was minimum but, as far as the output voltage the value obtained is near to the reference value, as it was intended. Thus, it was also confirmed that there was no need to adjust the additional modules, for each output current level, after the inclusion of one more base module (this adjustment was sufficient to guarantee that the reference voltage was achieved).

The results achieved after the control inclusion and, the adjustment of the base modules, are present in table VI

### Table VI

<table>
<thead>
<tr>
<th>7 base modules</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Iin [mA]</strong></td>
</tr>
<tr>
<td><strong>Iin_ctr [mA]</strong></td>
</tr>
<tr>
<td><strong>Io [mA]</strong></td>
</tr>
<tr>
<td><strong>Vo [V]</strong></td>
</tr>
<tr>
<td><strong>Pin_ctr [mW]</strong></td>
</tr>
<tr>
<td><strong>Po [mW]</strong></td>
</tr>
<tr>
<td><strong>η [%]</strong></td>
</tr>
</tbody>
</table>

As the output voltage of this configuration (with 7 base modules) is more close to the reference voltage that it’s aimed to achieve in the converter’s output, without compromising either the efficiency obtained or the output current levels achieved, this was the configuration chosen for the power stage’s modular implementation.

**F. Converter Analysis**

**Steady State Waveforms:** Analyzing the converter’s output current and voltage waveforms when the steady state is reached, their amplitude were: $ΔV_D ≃ 2.24mV$, $ΔI_D ≃ 0.68mA$ and, $ΔI_L ≃ 358mA$.

So, the output voltage and current were considered constant when reached the steady state. Observing the variation indicated, against the end value for which they stabilize, this approximation can be considered valid because: $\frac{ΔV_D}{V_D} ≃ 0.22\%$ and $\frac{ΔI_D}{I_D} ≃ 0.23\%$.

In both cases the variation is quite less than 1%, then both parameters can be considered continuous.

**Fixed Output Current:** Rather than check the efficiency obtained for a certain fixed output current, it is intended to examine the converter’s behavior to a change in its output current. Thus, it was used in the converter’s output an ideal current source with two different current levels and observed how the control corrected the output voltage to compensate it and achieve the desired reference voltage.

![Output Voltage and Current Waveforms](image)

In figure 6 it is possible to see the waveforms of the voltage and current at the converter’s output. This transition corresponds to a simulation of 20$\mu$s where at 10$\mu$s the current output was changed from 200mA to 300mA.

In the output voltage plot is signaled the reference voltage to achieve (1V). After the change in the output current (at 10$\mu$s) it is possible to observe a slight oscillation, where the output voltage has decreased due to the raise...
of the output current. That was promptly compensated by adding more 5 additional modules.

**Fixed Output Voltage:** Fixing the converter’s output voltage at the reference value will allow assessing the output current achieved when adding each additional module.

Thus, keeping the 7 base modules active and an ideal voltage source of 1V at the converter’s output, were included additional modules one by one. The results for each of these 13 conditions, from 0 to 12 additional modules, are present on a graphic presented in figure 7.

Regarding the variation in the output current caused by adding each additional module, it is possible to verify that its value is increasing as more additional modules are added. However, this variation is located between 13.6% between the variation obtained initially (with the addition of the first modules) and the variation obtained with the insertion of the last modules.

As can be seen the increase of the current is approximately linear, which would be expected since the variation of the output current increases slightly, as the number of connected modules are also raised.

As to the efficiency obtained, it remains approximately constant, considering that between the maximum and minimum values reached there is only a difference of 0.19%

![Graph showing efficiency and output current](image)

**Fig. 7.** Efficiency and output current obtained by adding each additional module to the modular power stage, with a fixed output voltage.

**V. CONCLUSIONS AND FUTURE WORK**

The main goal in the modular implementation of the power stage is to use only the required number of transistors in each active element of the converter (power transistors and their drivers). Minimizing the number of transistors present in each active element, reduces conduction and switching losses as the conditions on converter load are changed; because they are optimized for each circumstance and not fixed regardless of the requirements that are imposed on its load.

With this approach it was possible to maintain an approximately constant output with a variation of only 0.19%, for a load current from 185mA to 399mA. Such behaviour runs counter to the downward trend of the converter’s efficiency as its output current is decreased.

The best efficiency obtained was 86.8%, for an output current of 304mA. Although this is lower than the typically efficiency obtained for converters that operate with higher load currents (up to 90%), it is still much higher than what could be achieved by using a linear regulator (about 30%).

The modular implementation also allows to propose a method for controlling the output voltage by partial activate the power stage. Preliminary results show that for a significant current range, it is possible to maintain the duty cycle and make the output voltage regulation only by changing the number of active elements in the power stage.

Regarding the ripple of the output voltage, the value obtained was 2.3mV, much lower than what was specified (30mV). More specifically, the ripple obtained compared to the output voltage value reached was about 0.2%. So it can be considered that the output voltage is regulated and constant.

The next challenge in the design is clearly the integration of a ADC that can provide a digital word to the control and test the solution in a closed loop. The ADC should have 24 levels, so that each additional module has 2 bits of the digital word associated to them.

Afterwords, solutions that enable a full integration of converter’s filter elements in a SiP should be studied, so that a prototype could be manufactured.

**REFERENCES**


