Development and Implementation of a Data Acquisition System for Teaching Purposes

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***Abstract*—A data acquisition (DAQ) system acquires analog data into digital form for storage, processing and analysis. These signals are sampled, converted to digital and stored by a computer or by a standalone device. A DAQ system consists of an analog signal conversion hardware and DAQ measurement hardware. These systems can be standalone or coupled to a computer and can acquire multiple channels of data.**

The aim of this work is to develop, implement and characterise a small-sized, production cost reduced data acquisition system powered and controlled by an USB interface for educational purposes. A computer controls the values of the sampling frequency, range of channels, number of points to acquire and then retrieves the data acquired.

I. Introduction

Every data acquisition task has its own special challenges. Data acquisition test and measurement can be mobile or fixed, can be used on a test cell or under extreme environmental conditions and in laboratory research or for academic purposes. These systems can be used not only for electric signals but also to measure temperature, acceleration, sound, force and pressure, light or position and displacement, with a transducer is required at the input of the DAQs channels. Obtaining proper results from a DAQ system depends on the signal conditioning, the DAQ hardware, the computer and the software.

Signal conditioning assures that the signal about to be measured will not damage the system, protecting against overcurrent and overvoltage and adjusting the input ranges to the ADC input range. The main component composing the DAQ hardware is the analog to digital converter that digitises the conditioned signal with a certain resolution and sampling frequency. It is also composed by a processing unit to transmit the acquired data to the computer to be processed and analysed.

The main criteria to take into account when selecting a data acquisition system are the maximum sampling frequency, number of channels, input ranges, ADC resolution and the possibility of simultaneous acquisition. The cost of the device is also important since the goal is to develop an acquisition system similar to the available systems in the market with a lower production cost. The costs of the currently available devices vary according to the criteria above and some other specific characteristics of each device. In order to reduce costs, the aim of this work is to develop, implement and characterise a small-sized data acquisition device powered and controlled by USB. The computer-DAQ communication bus can drastically affect the maximum speeds at which one is able to continuously acquire data.

The main objective of this dissertation is to develop, implement and characterise a small-sized data acquisition board powered and controlled via USB. In order to achieve this, some key milestones were established:

- Defining the scope of acquiring signals (frequency and amplitude of the signal) and control commands from the DAQ;
- Selection and test(s) of the Integrated circuit(s) responsible for signal acquisition (ADC) and of a processing unit and communication (PIC or dsPIC);
- Development of an analog conditioning circuitry of the input signals of the DAQ and implementation of the complete system in the printed circuit board;
- Development of the PIC firmware and LabVIEW VIs and experimental validation of the designed system;

II. State of the Art

In this section some concepts about the project and characterisation of acquisition systems are introduced. These include the basic building blocks of their constitution, types of existing architectures and typical characteristics. The DAQ acts as the interface between a computer and signals from the outside world. It primarily functions as a device that acquires incoming voltages and converts into digital form so a computer can process, analyse and store them.

The three key components of a DAQ device used for measuring a signal are: the analog signal conditioning circuitry, analog-to-digital converter (ADC) and the microcontroller [1]. The USB bus serves as the communication interface between the DAQ device and computer for transmitting configurations and measured data. DAQ devices are offered on the most common computer buses including USB, PCI [2], PCI Express [3] and Ethernet [4].

A. Signal Conditioning

Signals from sensors or the outside world either can be noisy or, when the amplitude of a signal can harm the human being, it can be too dangerous to measure them directly. One of the key elements of signal conditioning is protecting the circuit from these adverse effects that might occur, such as an unexpected increase in voltage and/or current.

Signal conditioning circuitry adjusts a signal into a form that is suitable for input into an ADC. This circuitry can include amplification, attenuation, filtering and galvanic isolation. Signal conditioning provides distinct enhancements to both the performance and accuracy of data acquisition systems [5].

B. Analog-to-Digital Converter

An ADC is a device that provides a digital representation of an analog signal at an instant in time [1]. In practice, analog signals continuously vary over time and an ADC takes periodic samples of the signal at a predefined sampling rate. These samples are transferred to a computer over a bus where the original signal is reconstructed from the samples in software. The key characteristics of an ADC are the maximum conversion rate, the number of bits, the voltage input range, the output type (series/parallel) and the type of input scale (unipolar/bipolar) [6].

The maximum conversion rate defines the digital bandwidth of the ADC which is the maximum frequency the ADC can sample [7]. However, signals with frequencies above half of the maximum sampling frequency can be sampled through subsampling techniques, if the analog bandwidth of the ADC and signal conditioning circuitry allows [8].

The number of bits in a data acquisition system is the number of bits of the digitiser. Any ADC, has inherent performance limitations so the effective number of bits provided by the system can be useful in determining if the system is right for the application. Every converter has non-linearity, noise from reference voltages and aperture jitter. The effective number of bits (ENOB) is a measure of the dynamic performance of an ADC and its associated circuitry. It is determined by sampling a spectrally pure sinusoidal wave and determining the RMS signal and noise levels recorded by the system. Often, data acquisition system manufacturers specify a SINAD (performance parameter). SINAD is the ratio of the fundamental sinusoidal signal power acquired to the total noise and distortion since this parameter contains noise and distortion. It can be used to calculate effective number of bits (ENOB) [9].

C. Processing Control Unit

In a data acquisition system, the processing control unit controls the analog signal conditioning (amplification chain or attenuation with digitally programmable gains). It is also responsible for collecting the data from the ADC and control the sampling frequency [8]. This controller can be a PIC (Peripheral Interface Controller), a DSP (Digital Signal Processor) or a FPGA (Field Programmable Gate Array).The controllers can communicate with other devices through several protocols. The most commonly used protocols are SPI, I2C, UART and USB. Another protocol is parallel communication that is used to communicate between the processing unit and the other components. All of these protocols can be implemented in software. However, the existence of dedicated hardware modules in the control unit for the implementation of a DAQ system allows more control flexibility of each module.

III. Proposed Architecture

In this section the several blocks of the proposed architecture for the data acquisition system are presented (Figure 1).

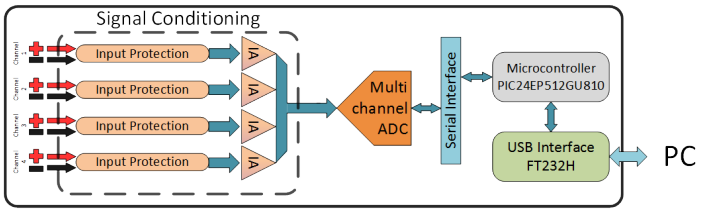

Fig. 1. Block diagram of the proposed data acquisition system.

The proposed architecture is composed by three main blocks. The signal conditioning, the analog to digital converter and the digital control using the USB communication protocol. These proposed system has simultaneous acquisition, where the analog to digital conversion happens with a single four-channel ADC [10]. This solution is cheaper than using four ADCs (one per channel) and can still achieve high acquisition ratios since the data transmission is done by serial interface with two data output lines. To set the sampling frequency, the input range of each channel, the transmission of the acquired data and the clock signal supplied to the ADC a microcontroller (PIC24EP512GU810) [11] is used. The acquired data is sent to a PC through the integrated circuit FT232H [12] from FTDI, which receives the data through 8 bit parallel communication from the PIC microcontroller. This integrated circuit allows the system to send data through the USB *Hi-Speed* communication protocol. The interface between the user and the data acquisition system, allowing the visualisation and data processing, can be done by an application developed in LabVIEW. This way the user can control the sampling frequency, the input range of each channel and the sampling mode (sequential or continuous).

A. Signal Conditioning

The signal conditioning circuit can be separated into two parts, the input protection and the amplification block. In the input, a protection circuit limits the voltage and current that reaches the input of the amplifier block, which in turn amplifies the signal before reaching the ADC. Through various techniques for signal conditioning, including attenuation and signal amplification, the acquisition system allows the measurement of a range of high and low amplitude signals. In Figure 2 the proposed schematic of the signal conditioning is represented.

In the proposed data acquisition system, the maximum voltage is ± 10 V. This system must be protected against higher voltage and electric current values that could damage the circuit and its components.

This overload protection reduces the current entering the circuit by having resistor, $R_1 = 1\ M\Omega$, in series with the input of the circuit. The worst case scenario is at the maximum

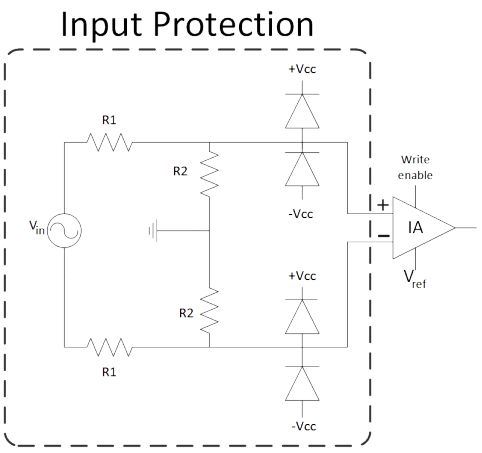

Fig. 2. Proposed signal conditioning circuit schematic.

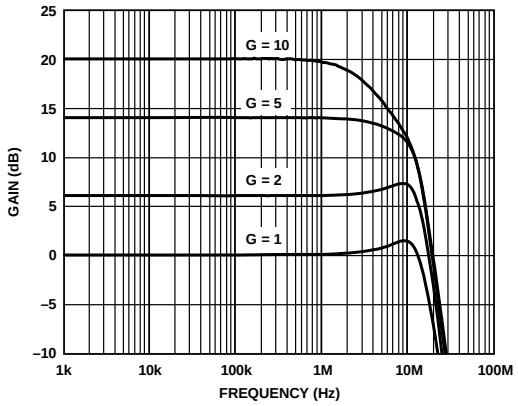

Fig. 3. Frequency response of the AI for the different possible gains [14].

voltage rating, where V_{in} =10 V, using Ohm's law, the maximum current entering the circuit would be 10 µA.

A voltage divider is created using R_1 and R_2 in order to reduce the voltage to half. In that way, the amplification block can receive the input signal without damaging the instrumentation amplifiers. Again, assuming the worst case scenario that only half of the input voltage goes through the divider and, in order to make sure it won't damage the instrumentation amplifier (with $R_2 = 1$ MΩ), a biased diode clipping was inserted to make sure the voltage that goes to the input of the IA is at a maximum 5 V.

The diode clipping (BAS70-07 shotkey diodes [13]) works for the positive input voltage signal when input voltage exceeds voltage (+V). The diode D_1 conducts while diode D_2 is reversed biased and so voltage +V appears across the output. This output voltage +V stays as long as the input signal voltage exceeds +Vcc. On the other hand, and for the negative input voltage signal, the diode D_1 remains reverse biased and diode D_2 conducts only when input voltage exceeds voltage −Vcc in magnitude. Thus, during the negative half cycle, the output stays at −V as long as the input signal voltage is greater than −Vcc. These diodes have a direct voltage of 0,4 V, 70 mA of direct current and 70 V of reverse voltage.

The amplification block aims to adjust, as much as possible, the amplitude of the signal to exploit the dynamic range of the ADC. To make this possible, it must be known at the outset what the maximum range of the signal to be measured is. In that way, the user can use the digitally programmable gain of the amplifier to better suit his needs. The use of instrumentation amplifiers is chosen (AD8250 [14] from Analog Devices) for three reasons: because they have programmable gains (in this case, four digitally programmable gains (1, 2, 5 and 10)); they also have a joint CMRR mode, which amplifies only the difference between the signals at its inputs; and finally because they make differential measurements.

Since the output of the amplification block is a bipolar signal with a voltage reference of 0 V (GND), it is yet required to be in the input range of the ADC, which is between 0 V and 5 V. To adjust the signal to the input range of the ADC and make an offset correction, a level shift circuit for a bipolar input [10] is placed. Using a operational amplifier circuit and four external resistors that assures that the measured voltage is above 0 V and around the the internal reference voltage (2,5 V) of the ADC as displayed in Figure 4. For a bipolar input of ± 5 V, R_1 =2 kΩ and R_2 =10 kΩ.

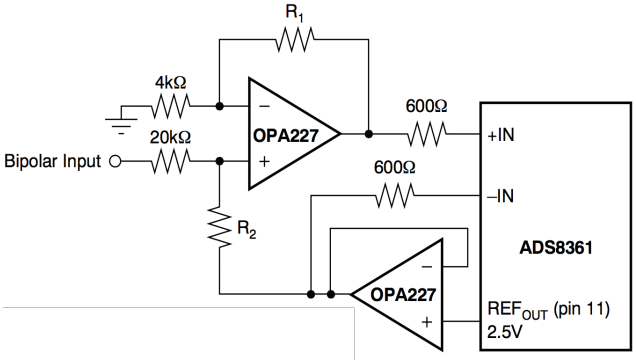

Fig. 4. Level shift circuit for bipolar input for the ADC (ADS8361) [10].

B. Analog to Digital Converter

To choose an analog to digital converter, there are some parameters to take into account, such as the conversion method, the resolution, the maximum sampling rate, the data interface, the number of channels, the type of acquisition and the cost.

The chosen analog to digital converter is the ADS8361 [10] from Texas Instruments. It is a high-speed, low-power, dual, 16-bit A/D converter that operates from +3 V/+5 V supply. It has a 4 µs successive approximation A/D converter, two differential sample-and- hold amplifiers, 16-bit resolution, an internal +2,5 V reference, up to 500 ksamples/s sampling ratio, four fully differential input channels grouped into two pairs for high-speed and simultaneous signal acquisition. Inputs to the sample-and-hold amplifiers are fully differential and are maintained differentially to the input of the A/D converter. The high-speed dual serial interface and control inputs minimise

software overhead. The output data for each channel is available as a 16-bit word. To achieve the maximum throughput rate, the master clock must be set at 10 MHz. A minimum of 20 clock cycles are required for each 16-bit conversion, as the data output format are 20 bits with the first two bits having the channel information (0 or 1, A or B) and the last two bits being zeros.

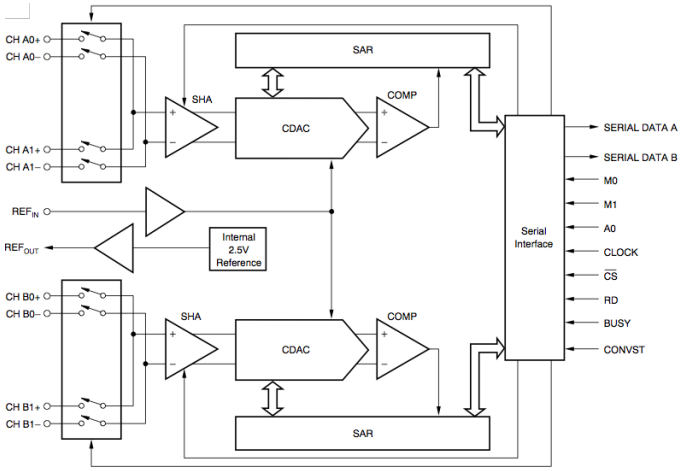

Fig. 5. Block diagram of the ADS8361 analog to digital converter [10].

The ADC has four modes of operation, all depending on the channel selection and on the data output. These modes are selected with M0 and M1. A0 is used to choose which channel to send (0 or 1). The channel selection allows to send information of a single channel of either channels (A and B alternating) or to always send a specific channel that changes the data output as well (from a single output (Serial Data A pin only) or both the data outputs pin).

The conversion method of this ADC from voltage to binary two's complement is made by linear interpolation and has a LSB of 76 µV. Where 0 V is the voltage for the negative full-scale code 8000_{H}, the voltage of 2,5 V is the bipolar zero code of 0000_{H} and the voltage of 5 V for the positive full-scale code is $7FFF_{\mathrm{H}}$. With two of these points, it is possible to determine in the LabVIEW program, the measured ADC voltage.

C. USB Interface

The USB interface is a the FT232H, a single channel USB 2.0 *Hi-Speed* (480Mb/s) to UART/FIFO integrated circuit and can be configured in a variety of serial or parallel interfaces. The proposed mode of operation is the one that allows the use of the PMP module by the microcontroller. Therefore, the asynchronous 245 FIFO mode that has a transfer data rate up to 8 Mbyte/s. When configured in this mode, it has two input pins used to read and write strobes and two output flags (read and write flag) that are active low. When one of them is high, the microcontroller is unable to perform that operation in the FIFO (read or write or both). When low, when there is data available to read from the FIFO or write into the FIFO, the strobes can be used. In this mode, data is written or read on the falling edge of the strobe signals and does not provide a output clock signal (and does not expect one). To enter this mode, the external EEPROM must be set to 245 asynchronous FIFO mode which only needs to be programmed from the computer once.

The two output flags are connected to the microcontroller as two external interrupts and both stop the normal behaviour of the firmware (waiting instructions or acquisition) to deal with one of two situations: either the FIFO is full and the microcontroller is unable to write more data (this is not supposed to ever happen but, if it ever happens, it stops the acquisition); or the user sends instructions from the LabVIEW program, such as start acquisition, stop acquisition or any other generic configurations, before starting to acquire.

D. Processing and Control Unit

The processing unit has an architecture with 16 bits (because of the chosen ADC) is needed. It is also important to know the processing speed, the serial communication protocol speed and the existence of a bidirectional parallel communication module. The PIC24EP512GU810 microcontroller has a 16 bit architecture, a working frequency of 120 MHz, a flash memory of 512 kB, a Random Access Memory (RAM) of 52 kB, 16/32 bit timers and 15 configurable channels DMA.The DMA has priority arbitration and can access the UART, SPI, I_2C, timers, input compare and output compare. The microcontroller has nine 16-bit timers and up to four 32-bit timers that can be remappabled from the peripheral pin select (PPS). The PPS increases the pinout options available on this device, being able to better tailor the microcontroller to the application, rather than trimming the application to fit the device.

E. Current Consumption

The DAQ system is projected to be powered only by the USB port and has a projected current consumption between 232 mA and 447 mA. Even though the USB port supplies 500 mA, the maximum current limit is unachievable since only up to 300 mA are supplied from the DC-DC converter. Therefore, the actual current consumption is between 232 mA and 300 mA and there is a high dependency on the PIC power consumption. If too many PIC modules are powered up, the DAQ system will shut down from lack of current.

F. LabVIEW Software

The virtual instrumentation (VI) that the user can use is exactly as the one in the Figure 6. This layout VI was developed with the resources and drivers supplied by the datasheet [12].

With *Device Index*, the system designator can be chosen and it is possible to know which system the user is controlling at that time. The user can pick which channels wants to receive information from by selecting the respective boolean variable. Also it has a 32-bit variable with the *Number of samples* to be required by the user for the DAQ system and the gains of each instrumentation amplifier.

This VI returns an error if one happened during the acquisition and a cluster of arrays with the acquired samples to the

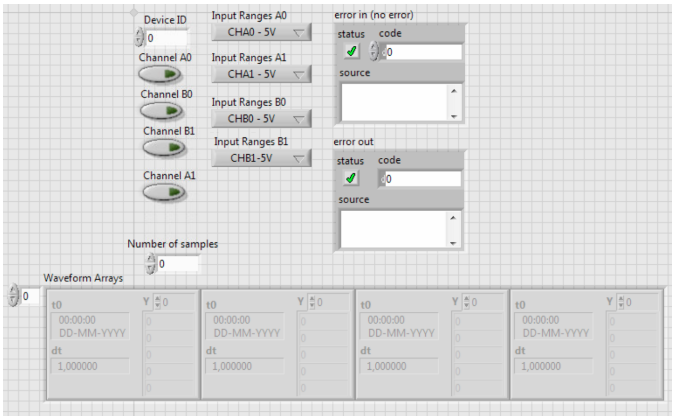

Fig. 6. Virtual instrumentation layout for sequential acquisition.

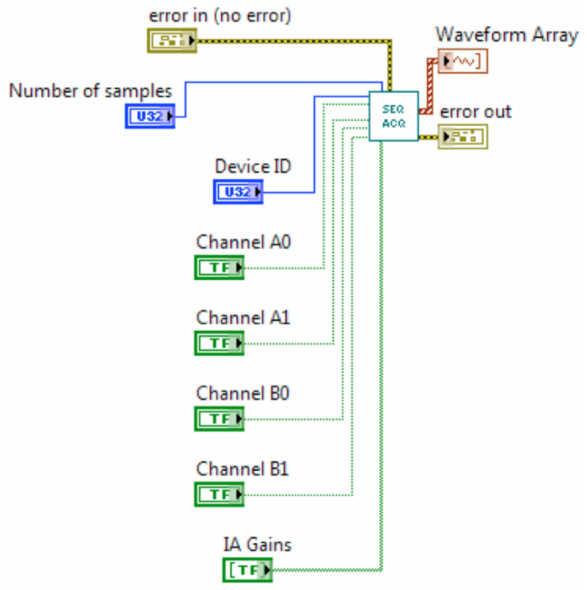

Fig. 7. Virtual instrumentation layout for sequential acquisition.

user. The user then can choose how to process or how display them as seen in Figures 6, 7.

In the continuous acquisition VI (Figure 8) the data that is being constantly read by the VI in a while cycle that will only stop if the user hit the stop button. The reading process starts with a request for how many bytes can be read from the FIFO of the USB Interface, then it proceeds to transfer bytes to the computer. The array of 8-bit values is converted into an array of 16-bit values only to be separated by channel information (0 or 1) and by channel data (A or B). Using the interpolation method mentioned before, it is possible to convert the 16-bit data into a voltage value. These values will be joined into a cluster of arrays to be delivered to the user as it can be seen in Figure 6.

IV. System Characterisation

In this section the tests to develop a characterisation of the system are presented: the analog bandwidth of the system, the

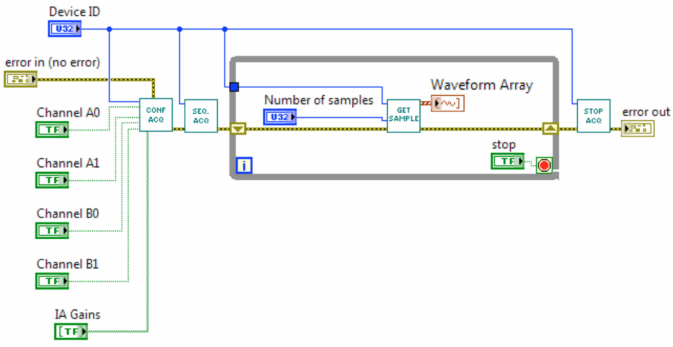

Fig. 8. Virtual instrumentation layout for continuous acquisition.

crosstalk between channels, the delay between channels, the average power spectrum of a sine signal in each channel and an example of continuous acquisition. A specific VI was built to perform each of these tests to taylor the needs and calculations of each test. They are described in detailed bellow.

A. Analog Bandwidth

The analog bandwidth test describes the influence the circuit that precedes the analog to digital converter at the incoming signal.

In order to perform this test to each channel, a VI that uses the developed DAQ system and the function generator TG1010A generates the input signals into the DAQ. The generator is controlled by the VI and is connected to the computer through GPIB communication. This VI controls all the parameters of the DAQ system as well as the amplitude and frequency of the generated input signal. The amplitude is at each of the limit of each configurable gain input range. In each measured frequency, the difference between the output signal and the input signal is calculated. This is done to each sample in the frequency sweep, from 10 Hz to 1,5 MHz, and each sweep was made 20 times.

The average analog bandwidth of each channel are presented in the Figures 9 to 12.

From Figures 9 to 12, it is possible to check that the DAQ system analog bandwidth depends on the smallest scale ($\pm$1 V) where the gain is higher. Above 1 MHz the analog bandwidth is distorted, decreasing the gains to the amplitude input ranges of 1 V and 2 V and the slight increase in the amplitude input ranges of 5 V and 10 V. The device mainly responsible for limiting the analog bandwidth is the instrumentation amplifier of each channel with a slew rate of 20 V/µs and which starts distorting the input signal at 650 kHz. To see changes (effect of the capacitor of the diode) in the figures above we would need to change the IA or do a sweep with strong signals instead of weak signals.

The overall DAQ system analog bandwidth is independent from the gain until approximately 700 kHz. After that, the gain distorts the analog bandwidth.

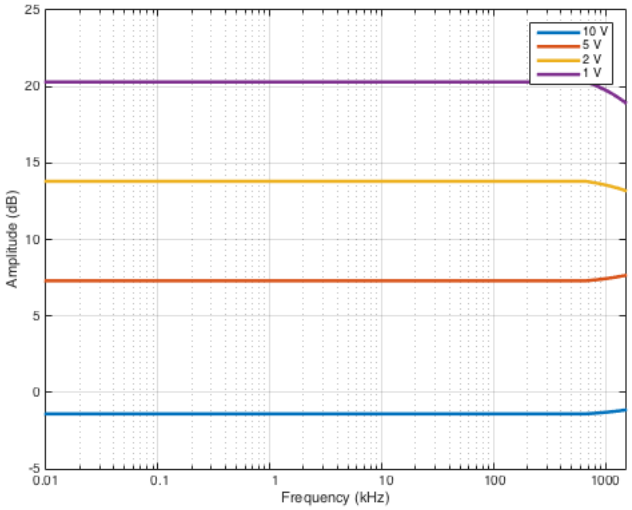

Fig. 9. Channel 1 analog bandwidth for the different input ranges.

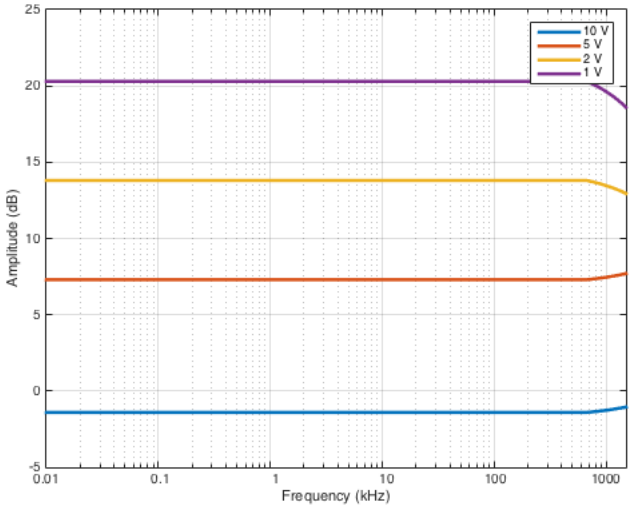

Fig. 10. Channel 2 analog bandwidth for the different input ranges.

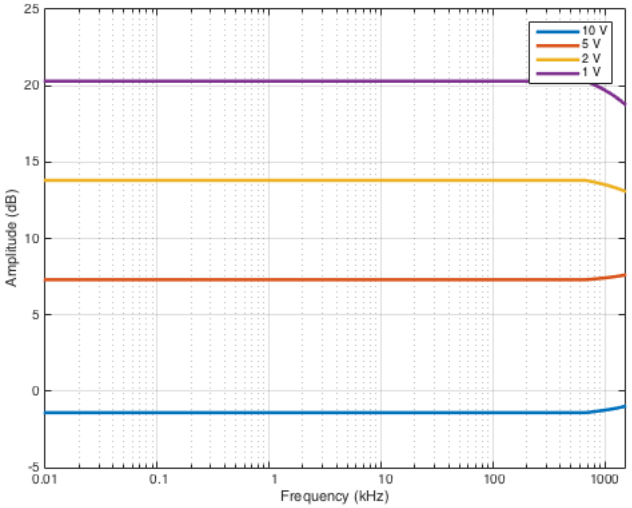

Fig. 11. Channel 3 analog bandwidth for the different input ranges.

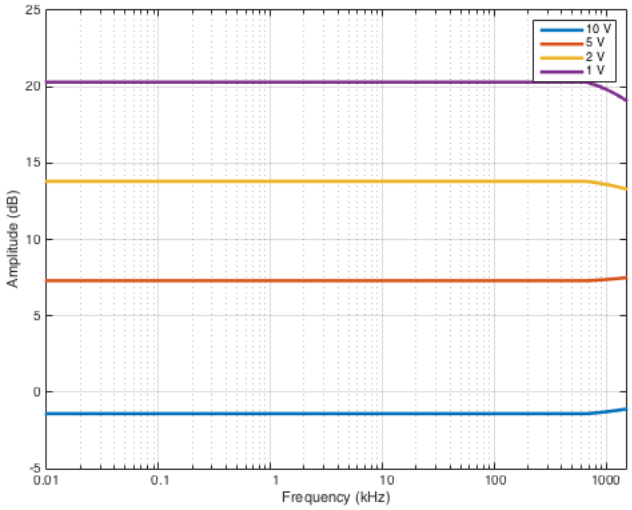

Fig. 12. Channel 4 analog bandwidth for the different input ranges.

B. Crosstalk Between Channels

In order to test the crosstalk between channels, one input signal is placed on one channel with the other three connected to the ground plane. The influence detected on those channels is measured. Crosstalk, in dB, is measured as the difference between the power detected in the channel where the input signal is and the channel being tested,

$$\text{Crosstalk (dB)} = \text{P}_{\text{input signal}}(\text{dB}) - \text{P}_{\text{detected}}(\text{dB}). \quad (1)$$

Each test was performed 20 times to obtain the average power spectrum of each channel. Afterwards, the crosstalk was measured. The FFT was performed to that array then the point by point averages were placed into another array.

The input signal to test the crosstalk requires a high frequency and amplitude in order so that slight changes can be noticed on other channels. The testing signal was a sine signal with 48 kHz and 9,5 V whose spectrum can be seen in Figure 13.

From the results, displayed in the Table I it can be concluded that the crosstalk effect is spread evenly among all the channels. It is also almost independent of the channel distance and higher than the noise floor detected. This is due to a bad design decision in the PCB, since a power supply line in the PCB crosses all channels, causing an even interference along the PCB board. Since the crosstalk values obtained are higher than the noise floor detected ($\pm$90 dB), the floor to be considered is the crosstalk floor as the minimum limit of the signals to measure.

C. Continuous Acquisition

To test the DAQ system and check if continuous acquisition was possible, four different input signals were measured as it can be seen in Figure 14. They have the same amplitude and different frequencies. Also, they were sampled at a frequency

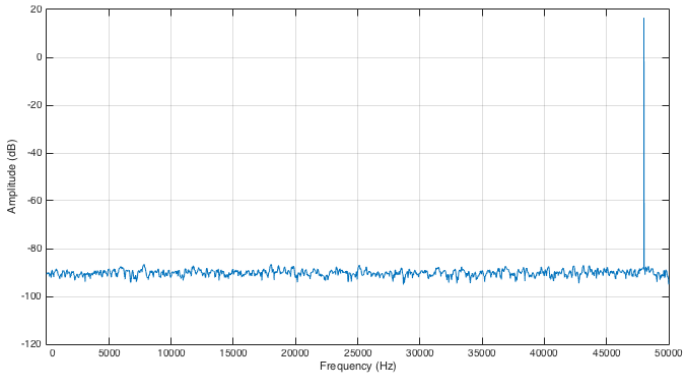

Fig. 13. Average power spectrum of channel 1 for the amplitude range of ±10 V of a sine signal with 48 kHz and 9,5 V.

TABLE I
CROSSTALK VALUES OF THE FOUR CHANNELS OF THE DAQ SYSTEM.

Input signal	Tested channel			
	Channel 1	Channel 2	Channel 3	Channel 4
Channel 1	-	86,11 dB	86,65 dB	86,95 dB
Channel 2	86,37 dB	-	86,38 dB	86,53 dB
Channel 3	86,54 dB	86,09 dB	-	86,23 dB
Channel 4	86,99 dB	86,44 dB	86,27 dB	-

of 100 kSamples/s/ch to assure that less periods of each signal had to be acquired. In channel 1, there is a sine signal with a frequency of 1 kHz. In channel 2, there is a sine signal with a frequency of 750 Hz. In channel 3, there is a square signal with a frequency of 600 Hz and finally channel 4 is a triangular signal with a frequency of 500 Hz.

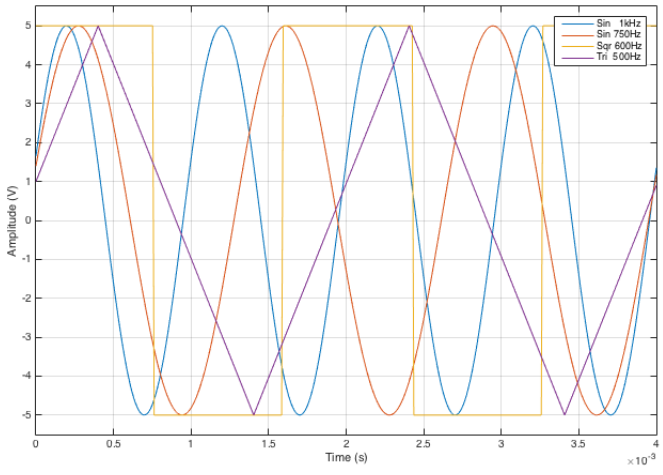

Fig. 14. Simultaneous Acquisition with the four channels of the DAQ system.

Even though each channel has an input signal with different frequencies, there is a measure delay between each channel to measure that a different test was made. The delay between channels was measured and is displayed in Table II.

D. Delay Between Channels

In order to measure the delay between channels, the same input signal was placed in all four channels with the same amplitude and frequency in a continuous and simultaneous acquisition. To measure the delay, it has to be known the period between samples and after that the phase difference between channels can be measured. The time delay is given by,

$$\Delta t = \frac{\Delta\phi x \frac{1}{f_{signal}}}{360^o}, \tag{2}$$

where Δt is the time delay, $\Delta\phi$ is the phase delay in degrees and f_{signal} is the frequency of the signal. To obtain this data, an internal VI was supplied by the software LabVIEW. As input, it has the measured sine signal (as an array) and as outputs, the frequency, amplitude and phase of this array.

The time delay is given related to channel 1 and displayed in Table II.

TABLE II
TIME DELAYS OF THE FOUR CHANNELS OF THE DAQ SYSTEM RELATED TO CHANNEL 1.

	Tested channel			
	Channel 1	Channel 2	Channel 3	Channel 4
Channel 1	-	12,28 ns	-24,30 ns	29,49 ns
Channel 2	-12,31 ns	-	-19,87 ns	25,37 ns
Channel 3	21,23 ns	-9,32 ns	-	14,35 ns
Channel 4	30,05 ns	-18,81 ns	-13,79 ns	-

The time delay does not varies in average between all channels from −24,3 ns to 30,05 ns. The value of the time delay can change depending on the frequency of the input signal tested. Compared to known DAQ systems with no simultaneous acquisition, the time delay is inferior.

E. Average Power Spectrum

A single sweep sample acquisition does not collect enough data to give accurate information about the power spectrum of a signal in a channel. Therefore, using several sweeps over a period of time assures a higher accuracy in the data measured. If it was required an even higher accuracy, it could be achieved by sweeping over a longer period of time (more samples than before), which reduces the variance of the resulting spectrum.

To verify the behaviour of a channel, 300 kSamples at a sampling rate (F_s) of 100 kSamples/s are acquired of several different input signals (sine signal, square signal and triangular signal) with the same amplitude, the same frequency and with 50% duty cycle. The channel is measured 20 times and the 5 kHz frequency is chosen in order that, up to the Nyquist frequency ($\frac{F_s}{2}$), several harmonics of the triangular signal and square signal could be seen.

From the average power spectrums measured, it can be seen, as expected, that the square signal has higher power

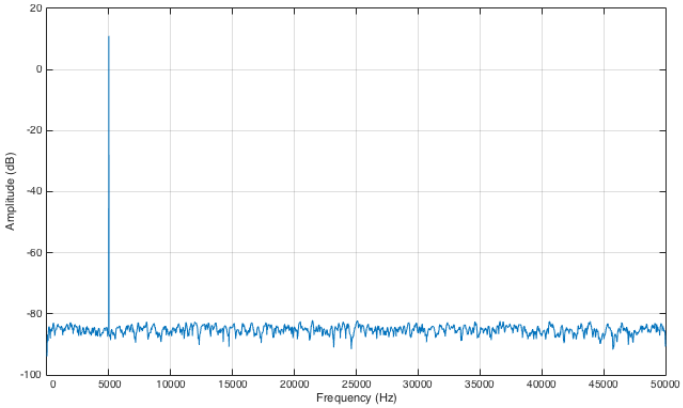

Fig. 15. Average power spectrum of a sine signal with a frequency of 5 kHz.

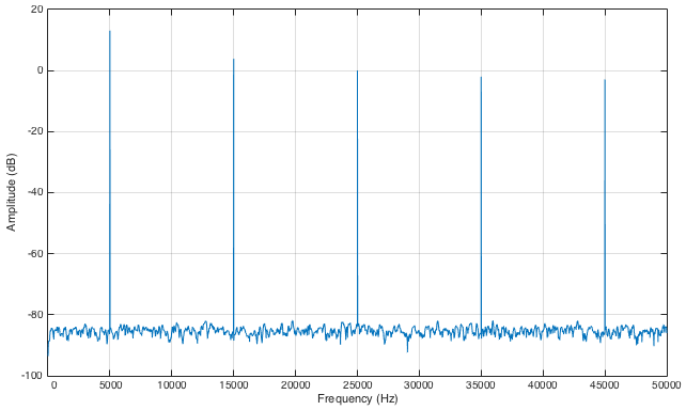

Fig. 16. Average power spectrum of a square signal with a frequency of 5 kHz.

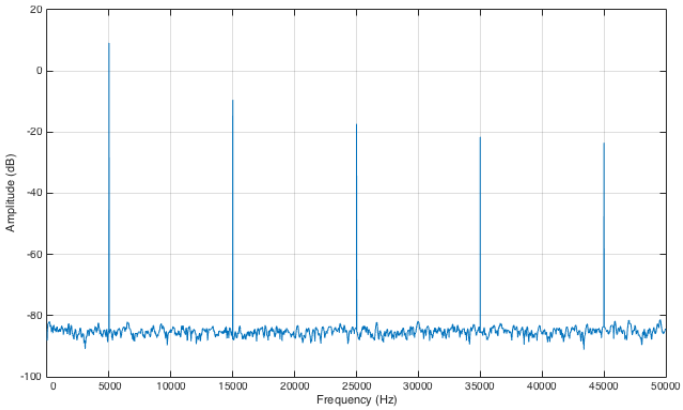

Fig. 17. Average power spectrum of a triangular signal with a frequency of 5 kHz.

in the fundamental frequency and its harmonics than in the triangular signal (as seen in Figures 16 and 17). The average power spectrum in any of the cases tested provides a clearer noise floor, fundamental frequency and harmonics than a single sweep would with the same number of samples at the same sampling rate as seen is Figure 18.

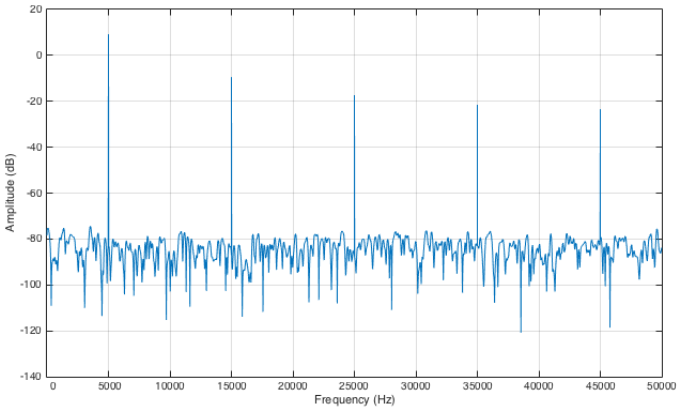

Fig. 18. Power spectrum of a single sampling set triangular signal with a frequency of 5 kHz.

V. Conclusion

Current data acquisition systems like the NI-6008 and NI-6009, commonly used in the courses at IST, already allow, not only for a wide range of academic applications, but also domestic and industrial applications. The usefulness of a data acquisition system is that it allows for the configuration of many of its parameters through a virtual graphic software interface and this is an asset to be taken into consideration. The main advantage of the produced prototype is that the development cost is far lower compared to the others already existent in the market. This is mainly due to the fact that the this DAQ does not have some extra specifications as the ones analysed (higher maximum frequency, number of channels and input ranges). But, contrary to the all-purpose market solutions, this solution focuses on the academic environment and, more specifically, on teaching purposes.

The delevoped prototype has four differential channels, all with simultaneous acquisition and a sampling frequency of 100 kSamples/s/ch, and with input amplitude ranges between ± 1 V and ± 10 V. The prototype is entirely powered by USB. The PIC24EP512GU810 shows the versatility of a microcontroller with peripheral pin selection, specially when implementing communication protocols between the PIC and the the other main devices (ADC and FT232H). USB interfacing was the industry standard USB 2.0 *Hi-Speed* since it allowed to achieve the desired data transmission rates.

This work was able to be cost-efficient by lowering the cost of the signal conditioning of the system. Thanks to this, the cost of the major components of these data acquisition systems were lowered.

As expected from the average power spectrums measured, it can be seen that the square signal has higher power in the fundamental frequency and its harmonics than the triangular signal. The average power spectrum in any of the cases tested provides a clearer noise floor, fundamental frequency and harmonics than a single sweep would with the same number of samples at the same sampling rate.

The analog bandwidth of this data acquisition system is of 700 kHz, which is higher than the sampling rate with a value of 100 kSamples/s, and can be used in applications that need under sampling techniques. The analog bandwidth is higher (1 MHz) for some input amplitude ranges. This happens due to the instrumentation amplifier slew rate distorting the signal. Therefore, the recommended working bandwidth is 700 kHz.

From the crosstalk tests, an even distribution of the crosstalk between channels was measured. In the planning of PCB design, the supply block was to be the furthest away from the signal conditioning as possible in order to avoid a higher crosstalk between adjacent channels. The biggest mistake with impact on the crosstalk between channels is the fact that the power supply is intertwined between all channels and specially the data lines.

The main goal with the simultaneous acquisition test was, first, to know if the system would choke at the total sampling frequency of 100 kSamples/s for all four channels and, second, if it also allowed to verify the existing channel delay between them. It is truly a simultaneous acquisition since the system worked properly with the desired maximum sampling frequency and also demonstrated that the channel delay varies in average between all channels from $-24,3$ ns to $29,4$ ns.

During the development phase of the prototype and during the acquisition tests, it was shown that the prototype system requires only USB power supply and that the current consumption is between 232 mA and 300 mA.

The developed prototype system main goal is to be used for teaching purposes. Therefore, the virtual communication interface with the computer was developed in LabVIEW 2014, although the drivers supplied by the USB interface allowed for virtual communication interfaces with other softwares as well as other operating systems.

Currently the system is fully operational and, even though this prototype is cheaper than the ones currently used in the market, a better DC-DC converter is required since it would allow the PIC to use as much current as it needs. The current solution works by disabling/not using some internal modules, such as the input capture module that would be vital for a better DMA/CPU synergy and better firmware programming.

For future work, changing the DC-DC converter to allow for full usage of the PIC capabilities would be a significant change. Small redesign of the PCB design are desirable to avoid all the power supply lines to cross with data lines at any point in the circuit. Also, the development of a box to protect the prototype could be added.

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