Receiver Front-End for 60 GHz Systems with a SiGe Technology

(Master Thesis Extended Abstract)

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***Abstract* — This paper presents the design of a sliding-IF receiver front-end for 60 GHz systems in 0.25 µm SiGe BiCMOS technology. The designed front-end, without a low noise amplifier (LNA), presents a conversion gain of 7 dB and a noise figure of 24 dB. For a 1.8 V power supply, the receiver has a current consumption of 47 mA, including the voltage controlled oscillator (VCO) with a tuning range of 14.65%, frequency doubler, frequency divider by two and the frequency downconversion. From the designed circuits, more emphasis is given to the VCO design, being used an electromagnetic (EM) simulator to provide accurate results.**

***Index Terms* — Receiver Front-End, 60 GHz systems, Downconversion Mixers, Voltage Controlled Oscillator, Frequency Multiplier, Frequency Divider**

I. Introduction

In the last few years, people are getting more and more addicted to wireless systems, leading to a huge growth in these area. The miniaturization of wireless communication systems has allowed them to have an increasing application in a wide set of industries that spread from computers, tablets and mobile phones, to telemetry, health monitoring and remotely controlled appliances. Moreover, this evolution allows the end-user to have an interconnection between mobile devices and wireless data sources, which are imperative to satisfy its needs. There are many technologies, radio frequency (RF) based, allowing connectivity such as Bluetooth, Wi-Fi and WiMax. These kind of technologies are mainly used in short-range communications and are not well responding to the demanding of faster connectivity and higher data-rate, thereby, there is a market need in fulfill those necessities [1], [2].

The need for higher data-rate leads to an escalate at the frequencies bands, being the 60 GHz frequency band the most probable band to use in private networks since the signals propagation suffers from high attenuation and it is an unlicensed band. Therefore it will be the future band for short-range communications.

The RF receivers are one of the key circuits for wireless communications, allowing the data signals to be received at an end point. The high working frequencies increase the design difficulty due the weak quality factor (Q) of inductors and capacitors and many parasitic effects, which makes it a challenging design. The need for sub-circuits as local oscillators (LO), frequency mixers, frequency multipliers and dividers make the receiver an attractive project by dealing with a huge variety of important circuits in RF design. Furthermore, its importance in communications systems and the use of a SiGe BiCMOS technology are distinctive points in RF design. As an academic thesis, in this work it is intended to verify the technology feasibility to design this high frequency circuits.

This paper presents the design of a receiver front-end for 60 GHz systems. Due to the high complexity of a complete receiver, it is only designed the frequency translation part, including the LO. The VCO is the main focus of this work, being designed with an extended use of EM simulations.

II. Technology Study

Studying the technology is an important step to design every circuit. Knowing the technology and the available components as well as its performance, makes the circuit design easier. It is intended to study the components and their behavior along the main parameters as frequency, voltages and currents. In some cases, electromagnetic simulations are required. To do so, the substrate profile used is the one studied in [3]. The technology in use has available five different metal layers, being the lowers the metal1, metal2 and metal3 whereas the higher layers with better conductivity properties are the topmetal1 and topmetal2.

A. Heterojunction Bipolar Transistor (HBT)

The technology has two types of HBTs, the npn200 and npn201, whose main difference are its maximum allowed collector current, maximum oscillation frequency and current gain. Each type of transistor has eight different sizes available, which are dictated by the number of emitters, going from one to eight. The group npn201 presents higher current gain and higher maximum oscillation frequency, making this group the most adequate for the design.

The DC analysis presented in Figure 1 allows an estimated V_{ce} of 300 mV for the transistor to entering into active region. Furthermore, the breakdown voltage, where the transistor enters the breakdown region, is around 1.9 V.

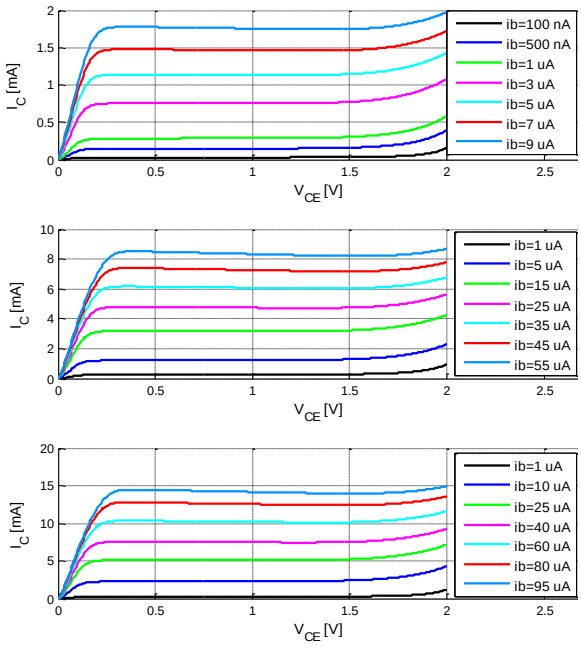

Figure 1 - Simulation results for the HBT's DC characteristics using a current base biasing for the transistor with one (top), four (middle) and eight (bottom) emitters.

B. MIM Capacitors

In the technology in use, there is only MIM capacitor, which is built with the bottom plate at metal2 layer and the top plate at metal3. As a passive element, and mainly due to its working principle based at electric fields, electromagnetic simulations must be used to provide accurate result for high frequencies. Capacitors are not purely capacitive, thus, the Q factor provides a value that relates its capacitance and its resistive part. To study the capacitors and compare the technology models with the EM extracted values, a study for different capacitances as 100 fF, 500 fF, 1 pF, 2 pF and 5 pF was performed. The analysis for the capacitors is presented in Figure 2 for the capacitance and in Figure 3 for the Q.

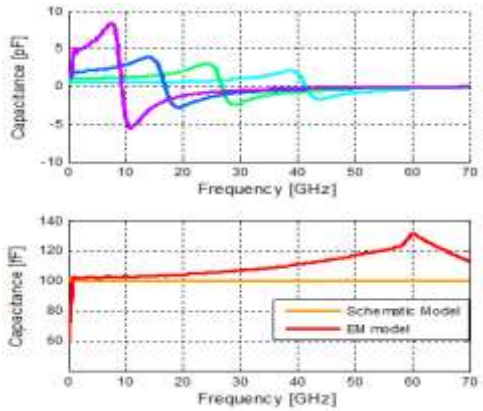

Figure 2 - Simulation results for the capacitors analysis through EM simulation. Effective capacitance (top), Effective capacitance comparison between schematic and EM extracted values (bottom).

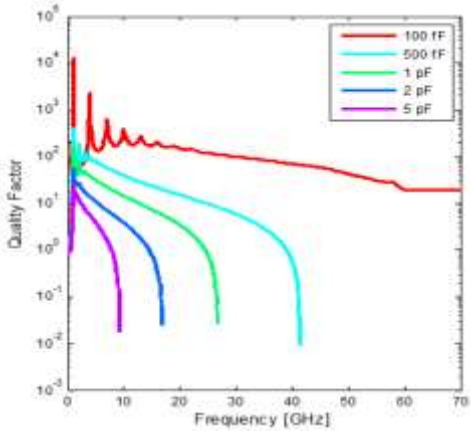

Figure 3 – Simulation results for the capacitors Q, through the EM extracted values.

C. Variable Capacitors- Varicaps

Variable capacitors, also known as varicaps, are active devices whose working principle is different from the passive capacitors. Capacitors are built with parallel metal plates, whereas the varicaps are normally MOS devices. As an active device, its capacitance has a non-linear characteristic, which is dependent on the voltage applied between its well and gate (V_{WG}). The technology in use has two types of varicaps, the symmetrical varicap (SVaricap) and the single-ended varicap. However, the single-ended varicap is inadvisable by the foundry to use in high frequency circuits, thus, only the SVaricap is studied. These have three terminals as presented in Figure 4, two sources where the signal is connected and one well where a tuning voltage is applied.

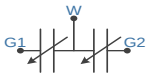

Figure 4 - SVaricap schematic circuit.

The simulated result for the varicaps characteristic is presented in Figure 5, for sizes from one up to six fingers, applying 1.8 V_{DC} to its gates. The results shows that it needs high V_{Tune} voltage to attain the depletion region.

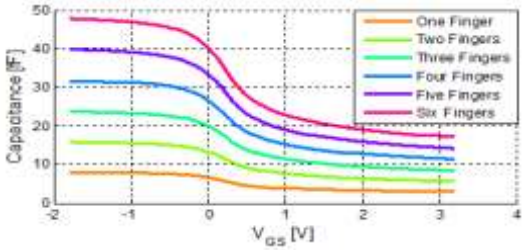

Figure 5 – Simulated results for the smaller varicap characteristic.

D. Inductors

The available inductors in the technology have predefined layouts, which mean that their properties are not adjustable and there is no scalable inductor. However, the technology

offers two different types of inductors, the simple and the one with center tap. The available simple inductors go from 0.94 nH up to 23.8 nH, while the center tap goes from 0.7 nH up to 5.5 nH. Besides the lower inductance, the center tap inductors are smaller, which allows to save space at the layout.

The inductor shielding makes a possible way of achieving better performances from the inductor. There are plenty ways for implementing it, being the most common method the patterned grounded shield. In spite of being the most common method, the work in [4] suggests that for higher frequencies there is a better way to build the shield which consists in a floating shield. In order to improve the inductor performance, EM simulations are used to test three different shields while comparing it to the technology model for the same inductor. Based in the presented study at [4], it was used a floating patterned shield (FPS) consisting in metal1 lines with 0.6 µm width and spaced by 0.6 µm, covering all the inductor. In this same shield, another metal2 layer is used with the same pattern but with orthogonal directions. Based on the first, a floating squared shield (FSS) is simulated by using a simple metal1 plate under the inductor. Since the plate shield makes use of a huge metal1 line, leading to higher capacitive coupling to the substrate, the plate shield is scratched into smaller squares of 30 μm^2, floating small squares shield (FSSS). The referred shielding methods are verified for the 0.7 nH inductor through EM simulation, as presented in Figure 6 for the inductance and in Figure 7 for their Q.

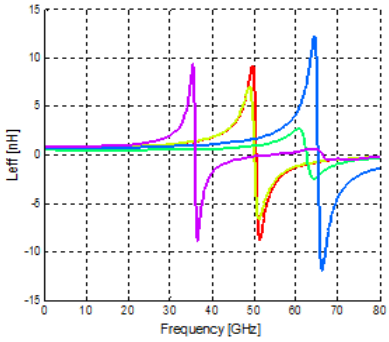

Figure 6 – Simulation results with EM extracted results for the inductance using various shielding methods.

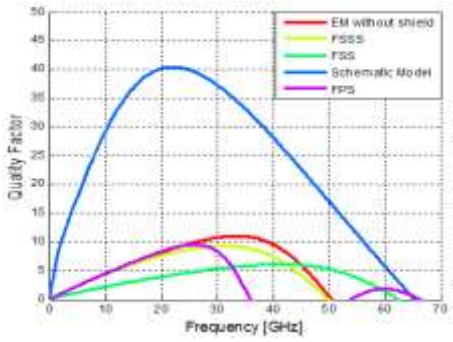

Figure 7 – Simulation results using EM extracted results for the Q using various shielding methods.

III. Architecture

The proposed receiver front-end design is made for sliding-IF architecture, as presented in Figure 8.

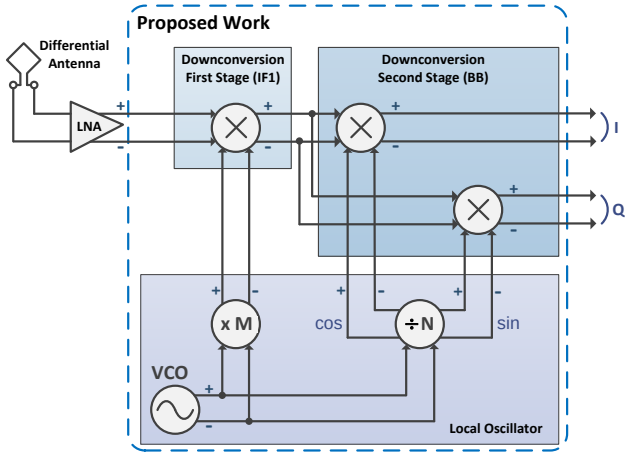

Figure 8 - Block Diagram for the proposed sliding-IF receiver.

High frequency heterodyne receivers for IQ modulation are usually dual-conversion receivers, which require the use of two different LO frequencies. These architectures allow the use of lower frequency VCOs and also high IF. The use of high IF avoids the necessity of image-rejection filters and reduces the LO to RF crosstalk due to its large separation.

The sliding-IF architecture, which is designed in this work, is built with the same principle but instead of using a fixed second LO frequency, it uses a variable one. In a Sliding-IF architecture, both LO frequencies are obtained from the same oscillator. Thus, both frequencies are related and only one frequency synthesizer is required. In this work a sliding-IF is used with a main oscillator for 24 GHz band, which frequency is then multiplied and divided by two, to perform the first and second LO frequencies, respectively.

IV. Local Oscillator

A. Voltage Controlled Oscillator (VCO)

As a fundamental block for the most wireless systems, it is a vastly studied block. However, these block still keeping its interesting difficulties, mainly at high frequencies. Despite the several possible topologies, the most used at high frequencies are the Colpitts in [5], [6] and the LC Tank in [7], [8], and [9]. The Colpitts topology presents a lower phase noise and lower power consumption when comparing to the LC Tank. On the other side, due to its differential output, the LC Tank has a greater common-mode rejection, providing higher output power and also being less susceptible to low Q inductors. Besides, the LC Tank allows a higher tuning range which makes it the most appealing topology for high frequencies VCO's. The voltage variation is commonly achieved through the use of varicaps. However, there are other ways to do it as the use of independent transistors base

biasing [8], switched capacitors [7] and also variable bridge inductors [9].

The oscillator working principle is ruled by Barkhausen's criteria [10]. Based on a feedback system with an input and one output, the criteria can be analyzed as a two-port network, being the system divided into an A and B blocks. However, a more appropriate technique is used for high frequency oscillators, which is the use of a one-port method, through the assumption of both blocks being connected. This method separates the blocks into an active block (A) and a passive block (B).

In order to have a proper work, the oscillator must fulfill its steady-state condition, which is the LC tank resonance. In order to fulfill the start-up conditions, the cross-coupled transconductance must be higher than the LC's. The cross-coupled analysis can be made through its N-Shape characteristic, which in fact, is all that is needed to guarantee the oscillation start-up. In case of symmetry it leads to a unique and stable oscillation [11].

The cross-coupled analysis allows the study of the start-up conditions and also the study of the minimum achievable phase noise, which is -100 dBc/Hz. However, for the required frequency, only the smallest transistor is possible to use, due to the large capacitance of the others. With the smaller transistor, the minimum achievable phase noise increases to -90 dBc/Hz.

In this work, the frequency bands for the system are regulated by the WiGig standard, which has four channels with 2.16 GHz each. The channels are presented in Figure 9, being also presented in the figure the required bands at the VCO, considering the use of a frequency multiplier and divider by two. The WiGig channels are represented by the higher four channels.

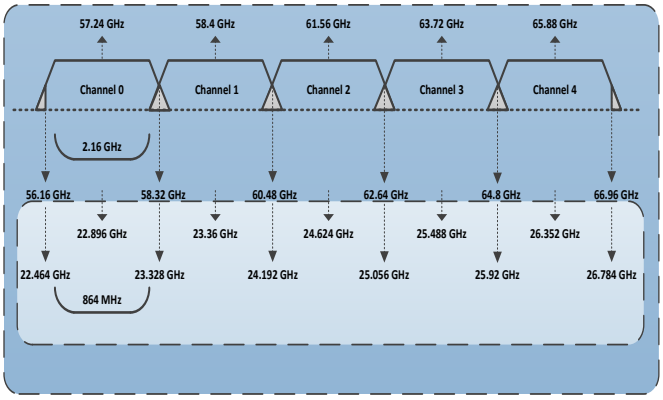

Figure 9 - Frequency channel bands for 60 GHz systems.

The frequency tuning has high concern due to the high frequency VCO susceptibility to a small capacitance variation. Thus, a single varicap is used to provide the fine tuning while it is used binary controlled switched capacitors to provide the channel selection.

However, the technology varicaps are not able to provide the required fine tuning while achieving the highest frequencies. Thus, a non-common method has been used. Using an HBT varicap, the VCO is able to vary its frequency in the entire band. The HBT varicap is designed as presented in Figure 10.

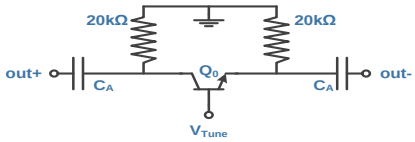

Figure 10 - Schematic circuit for the HBT Varicap.

With a 0 V biasing, the HBT is at the cutoff region, where there is no current. Thus, the capacitances C_A do not load the circuit, being the capacitance seen by the VCO, the equivalent to the HBT's junctions. With the V_{Tune} bias increase, the transistor leaves the cutoff region and it slowly starts to conduct. Therefore, it starts to load the VCO with half the capacitance C_A. The high resistors provide a DC path to ground while avoiding the AC signal suppression.

Although this solution allows the VCO to cover the entire band, it presents a K_{VCO} around -5.2 GHz/V. Therefore, a mathematical function is implemented in order to expand the V_{Tune} voltage for the linear capacitance variation, being able to decrease the K_{VCO} to -1.39 GHz/V.

In order to isolate the VCO from the load capacitances of the other circuits, an output buffer is designed. The output buffer must present the minimum load capacitance to the VCO, in order to preserve its frequency bands. Thus, the final circuit for the designed VCO is presented in Figure 11.

At the VCO design, the passive components as capacitors and inductors are electromagnetically simulated as well as the long metal lines connecting the blocks. Although slower due to the EM simulations, this method provides more accurate results. In Figure 12 is presented a simplified diagram block in order to show which blocks are electromagnetically simulated or extracted from the layout.

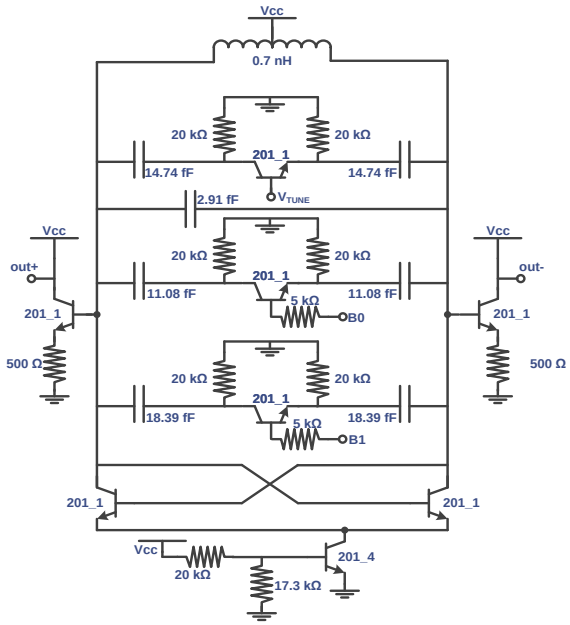

Figure 11 – Schematic circuit for the designed VCO.

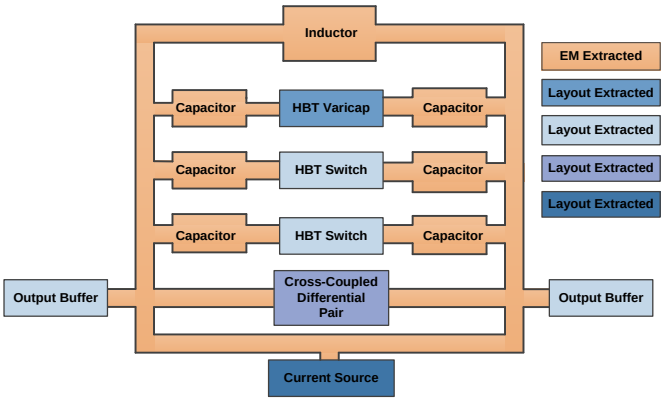

Figure 12 - Block Diagram presenting which blocks are extracted from layout and which are simulated EM.

The designed VCO, including the output buffers, present a current consumption going from 4.86 mA up to 5.11 mA, considering all the FTR. With a central frequency at 24.99 GHz, it has a 14.65 % FTR going from 23.16 GHz up to 26.82 GHz, tunable into four channels.

B. Frequency Divider by Two

The motivation in using frequency dividers in RF circuits is not only to produce lower frequencies but also to provide a quadrature separation for the output. In a frequency synthesizer, the divider can also be used as a prescaler. Its common implementation is a D flip-flop which is composed by two latches in a master-slave configuration as stated in [12], [13] and [14]. This frequency divider architecture is also denominated as static dividers in contrast to the dynamic divider also implemented in [13].

Besides the static and dynamic dividers by two, also an injection locked frequency divider (ILFD) can be used to the purpose as in [15]. This solution uses two crossed oscillators, each locked by one of the differential input terminals that have a phase difference of 180º. The ILO is able to produce quadrature outputs and is locked at half the input frequency.

The designed divider presents a static divider built with type-D Latches. Each D-Latch is built based on a core stage (Q3, Q4) and a transconductance amplifier stage (Q1, Q2), being the circuit for each latch presented in Figure 13.

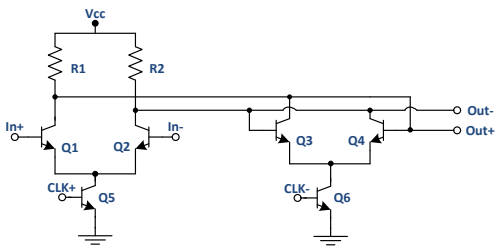

Figure 13 - Schematic circuit for a D-Latch.

In order to properly design the frequency divider, a sweep at the load resistors is made while varying the DC biasing for the different transistors. The solution that has the maximum conversion gain uses transistors with a single emitter at the core stage and transistors with two emitters at the transconductance stage, for a 400 Ω load resistors.

The conversion gain, as presented in Figure 14, for the post-layout is almost the same along the input voltage. However, in frequency, the post-layout simulation results are much below the schematic results, mainly for frequencies beyond 30 GHz. The current consumption goes from a minimum value of 7.18 mA up to 9.07 mA.

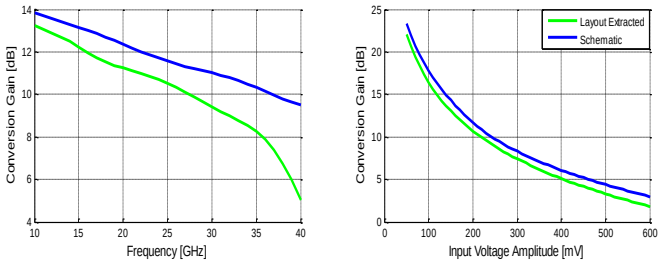

Figure 14 – Simulated results for conversion gain along the frequency (left) and along the input voltage amplitude (right), using the schematic and layout with extracted parasitic designs.

Besides the high conversion gain, the designed divider also has a high fundamental rejection.

C. Frequency Multiplier by Two (Doubler)

Frequency multipliers are commonly used for factors of two or three. In this work a doubler is used. The typical implementations use the higher harmonics of the signals, which are naturally or intentionally generated.

Doublers can be built using a circuit that allows intermodulation products generation, known as mixer. In this case the signal is mixed whit himself, being a self-mixing circuit. Other circuits to achieve frequency multiplications can be built through the injection-lock phenomena or by taking advantage of the active devices non-linearity.

In this work, the topology used for the doubler design is the double balanced mixer, also known as Gilbert cell, presented in Figure 15.

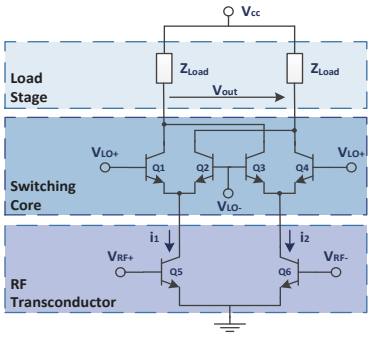

Figure 15 - Schematic circuit for the double balanced mixer, Gilbert cell.

The Gilbert cell is built with a switching core stage controlled by the LO signal and a transconductance stage controlled by the RF signal. Since for this application it is a self-mixing mixer, both signals are strong and with the same frequency. A first approach to its design is analyzing the DC

operating point, regarding that both stages must work in the active region. The biasing voltage for the LO port imposes the V_{CE} at the transconductance stage. Thus, it must be enough to provide a proper V_{CE} for the other stage while working at the active region.

The use of a resistive load does not allow the necessary headroom voltage and it is necessary to use an inductive load. As in the VCO, the smaller center tap inductor is suitable for this circuit. Sweeping the biasing voltages and testing the multiple transistors combinations, it is possible to obtain the circuit which provides higher conversion gain.

The better inductor shield to be used at these frequencies is the FSS. However, both FSS and FSSS shields are simulated at the doubler, using their EM extracted values along with the doubler core schematic and post-layout circuits. The FSS does not only improve the conversion gain (left) as presented in Figure 16 but it also improves the port-to-port isolation (right).

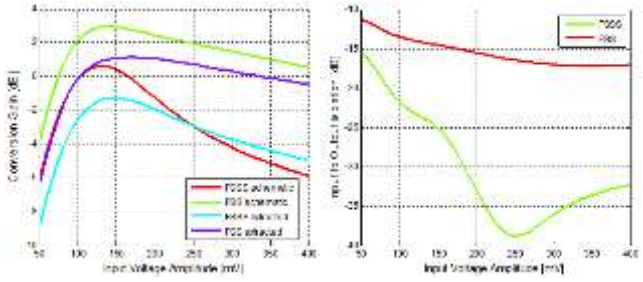

Figure 16 - Simulation results for the conversion gain (left) and the input to output isolation (right) using two types of inductor shielding.

In summary, the transconductance stage (Q5, Q6) is built with eight emitters transistors and has a voltage biasing of 900 mV while the switching core stage (Q1 - Q4) is built with five emitter's transistor and has a bias of 1.6 V. The frequency doubler presents a current consumption from 14 mA up to 16.86 mA while providing a conversion gain up to 3 dB. The layout design has been made trying to keep the Gilbert cell symmetry in order to avoid different path capacitances which could unbalance the mixer.

D. Local Oscillator

The local oscillator output bands are presented in Figure 17 in order to show the correct work of the VCO, the multiplier and divider.

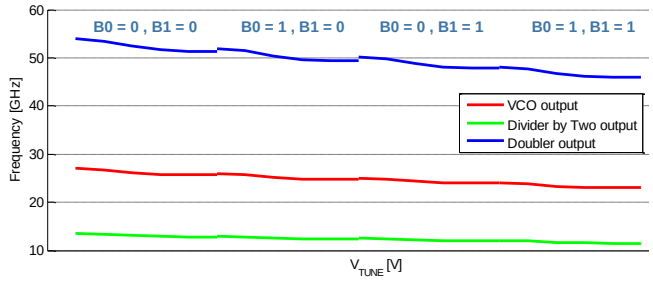

Figure 17 - Simulation results for the frequency bands at the LO outputs and at the VCO.

IV. Frequency Downconversion

One of the receiver building blocks is the downconversion mixer. This block allows the frequency conversion from an RF frequency to an intermediate frequency or baseband. As already referred, the receiver architecture used in this work is a sliding-IF. Thus, two downconversion mixers are required. The first mixing stage converts the RF at 60 GHz band into an IF at a 12 GHz band whereas the second mixing stage converts the IF to baseband. Both stages are designed using a double balanced mixer, the Gilbert cell circuit topology.

A. Gilbert cell mixer

Both stages must work in the active region. The switching core transistors shall have a V_{CE} in the middle of the active region to allow a voltage swing into the active region. Although the transconductance stage does not need to be biased for the same V_{CE} due to the lower voltage swing, it might be in order to increase its transconductance [16].

In Gilbert cell designs it is common the use of a bias current source bellow the transconductance stage. However, with a low supply voltage it becomes hard to meet the headroom due to the necessity of another V_{CE} voltage (at the current source). The DC operating points can be estimated through the analysis of one Gilbert cell branch, as presented in Figure 18.

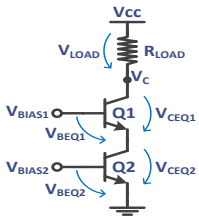

Figure 18 - Schematic circuit of a Gilbert cell branch.

In mixers design there is a trade-off between gain, linearity and noise. Therefore, the transistors and R_{LOAD} sizing must be carefully chosen by taking into account the variables which affects the circuit performance. The switching-core stage must perform a good switch whereas the lower stage must present higher transconductance in order to compensate the noise, mainly generated by the switches.

B. Second Mixing Stage

The second mixing stage is the one that shall be designed in first place, because its input impedance is required to design the first mixing stage. The second downconversion stage works at lower frequencies, being its aim the conversion from an IF to a baseband signal. The circuit after the second downconversion stage is typically a Gm-C filter, which input impedance is assumed to have high value, given by a parallel equivalent circuit with a 100 kΩ resistance and a 50 fF capacitance, at 100 MHz. The mixer design is made for a 100 MHz IF, which is close to the desired baseband. The conversion gain for the designed mixer is presented in

Figure 19, in function of input power (left) and input frequency (right).

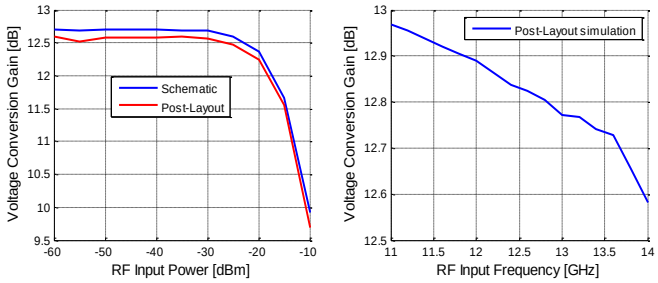

Figure 19 – Simulation results for the second mixing stage conversion gain function of the input power (left) and function of the input frequency (right).

The RF-to-IF, LO-to-RF and the LO-to-IF isolations are high, as presented in Figure 20.

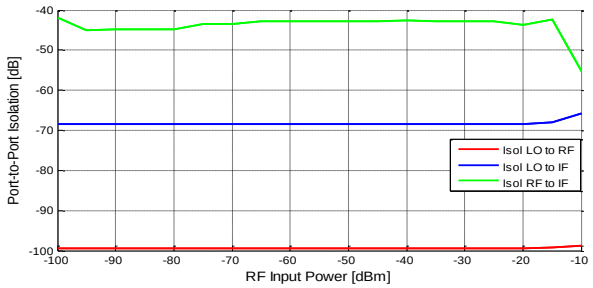

Figure 20 – Simulation results for the port-to-port isolation at the first mixing stage, presenting the isolation for the LO to RF and LO to IF.

For a -40 dBm input power at 12.1 GHz, the noise figure (NF) is 14.91 dB. The circuit has a current consumption of 1.59 mA until the input $P_{1dB,}$ where it starts to increase up to 1.95 mA (at -10 dBm input power). The circuit input impedance, as already referred, is important for the first mixing stage design. The designed mixer presents an input impedance of 933 Ω, which equivalent RC parallel is represented by a 221.45 Ω resistance and a 14.58 fF capacitor at 12 GHz.

C. First Mixing Stage

The first stage downconversion mixer aims the frequency conversion from a 60 GHz band to an IF in a 12 GHz band. The load impedance is already known from the second downconversion stage. However, it is necessary to regard that the load is composed by two second mixing stages due to the receiver quadrature output. The mixer design is made for a LO with 170 mV, which is the amplitude observed at the frequency doubler design.

Following the same process as in the second stage design, the DC operating points are established to V_{CEQ1} = 537.5 mV and V_{CEQ2} = 557.8 mV. Although in the second stage high load impedance has been considered, the first stage is loaded by low impedance. Thus, the R_{LOAD} in this mixer has to be smaller, settled to R_{LOAD} = 250 Ω. The eight emitters transistor are chosen to build both stages, being this circuit whose provide higher conversion gain without much noise or linearity degradation. The simulated results for the conversion gain, in function of input power (left) as well as in function of the RF frequency, are depicted in Figure 21.

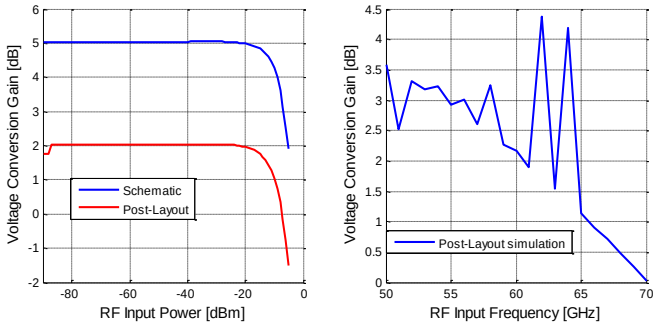

Figure 21 - Simulation results for the first mixing stage conversion gain in function of the input power (left) and in function of the input frequency (right).

The designed mixer provide a conversion gain of 3.4 dB while having an input P_{1dB} = -9.33 dBm. For a -60 dBm input power at 60 GHz, the circuit presents a NF of 12.5 dB. The current consumption is 5.84 mA at the linear region and starts to grow up to 6.96 mA (at -5 dBm). As in the second stage, it provides high port-to-port isolation.

D. Frequency Downconversion Block

In order to verify the proper functionality of the circuit, it was simulated using an RF input frequency of 60 GHz and two LOs which frequencies are 48 GHz and 11 GHz. Thus, an IF at 1 GHz is produced at the circuit output. The simulation results for the first and second mixing stages output are presented in Figure 22.

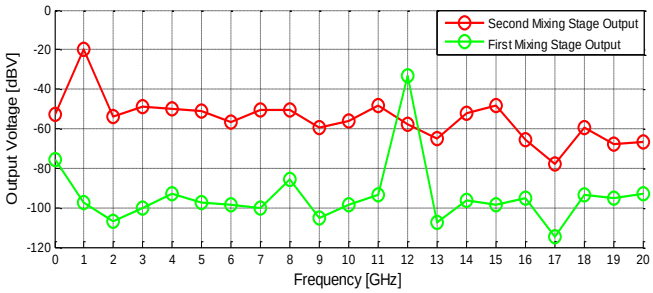

Figure 22 – Simulation Results for both mixing stages outputs.

The simulation results for the voltage conversion gain in function of RF input frequency (left) and in function of the RF input power (right) are presented in Figure 23. The frequency downconversion circuit presents an input P_{1dB} = -14 dBm and it shows a NF of 25.52 dB. For an RF input signal with -40 dBm at 60 GHz, the conversion gain is around 14.7 dB while drawing 10.13 mA from the power supply.

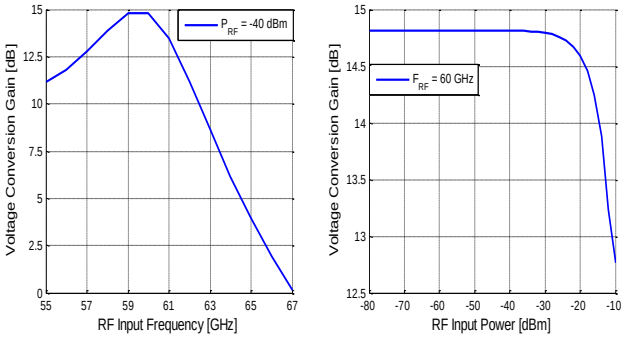

Figure 23 – Simulation results for the conversion gain in function of the RF input frequency (left) and RF input power (right).

V. Receiver Front-End

During the layout design, each individual circuit was built taking in account its position in relation to the others. The circuit arrangement was previously studied in order to shorten the connection metal lines between blocks. Although the frequency synthesizer and LNA were not designed in this work, their presence in the layout has been regarded in order to preserve space for an eventual future implementation. The final layout for the developed receiver front-end is presented in Figure 24, where the chip area eventually reserved for the frequency synthesizer and LNA are also represented.

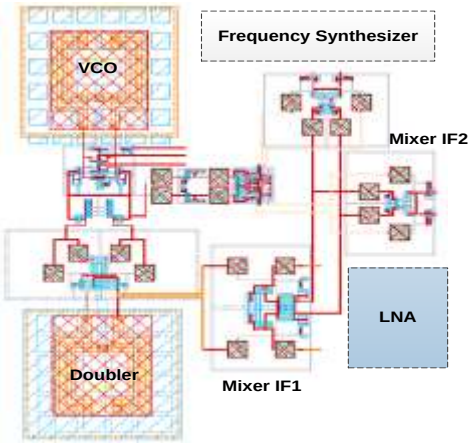

Figure 24 – Receiver Front-End layout, presenting a relative position for the LNA and frequency synthesizer.

Without having the LNA design, most of the receiver parameters do not have any meaning. However, in order to verify the circuit proper role, a simple analysis is made to the receiver. The output waveforms at the LO are presented in Figure 25. In this figure the results are simulated for the lower VCO frequency (around 23 GHz), using an RF signal with -30 dB at 58 GHz.

The aim of the receiver is to convert the RF frequency to a baseband signal. With the same conditions as referred above, the simulation results for the first and second mixing stage are presented in Figure 26. The RF frequency is used as 58 GHz in order to generate a signal around 1 GHz at the receiver's output.

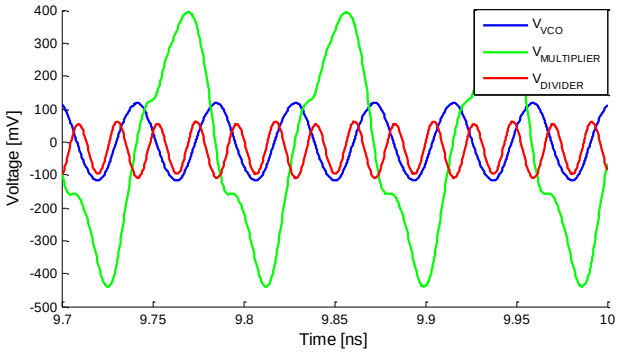

Figure 25 – Transient Simulation results for the LO waveforms, presenting the VCO output (blue), the doubler output (green) and the divider by two output (green).

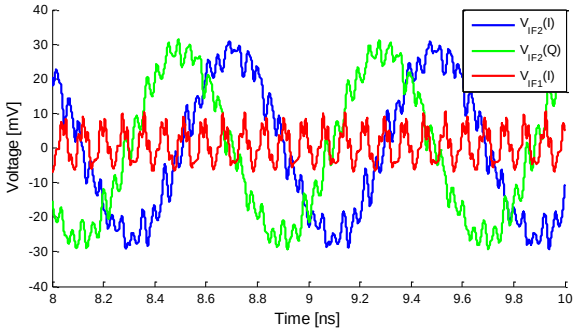

Figure 26 – Transient simulation results for the downconversion circuit, presenting the first stage output (red) and the quadrature output at the second stage (blue and green).

From the transient analysis, the designed receiver front-end is calculated to draw 47 mA from the supply voltage. The presented results prove that the receiver is working properly, converting the RF frequency to baseband. However, as already referred, periodic signal analysis are also necessary to characterize the receiver. For the same conditions that the transient simulations were made, a PSS analysis was made along with a periodic s-parameter (PSP) analyze. The PSP analysis only allows the variation of a port frequency. Thus, the analysis is made through a RF frequency variation between the 55 GHz and 67 GHz, being the voltage conversion gain represented in Figure 27.

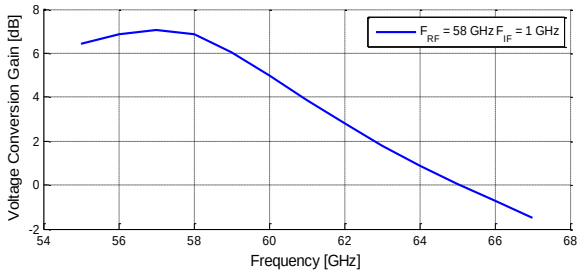

Figure 27 – Simulation results for the receiver voltage conversion gain in function of input frequency, obtained through a PSP analysis.

The NF obtained for the receiver front-end at 58 GHz, is 23.29 dB. However, the obtained value has no meaning for

the receiver front-end characterization, due to the inexistence of an LNA. The LNA not only would increase the conversion gain as it would improve the receiver overall NF value.

VI. Conclusions and Future Work

The 60 GHz systems are a promising technology for the future of short range communications. Receiver front-end is an important part of these systems, allowing the received signals to be converted to a lower frequency where the signal demodulation is possible, without losing the signal information.

The proposed architecture in this work is a sliding-IF receiver front-end for 60 GHz systems. Due to the large and complex system that a receiver represents, it was only developed the frequency translation part, including the local oscillator. Thus, except for the LNA, all the other front-end building blocks have been designed. In order to ease the circuits design, it has been made a technology study, which has provided the recognition of its capabilities and limitations.

The major focus of this work was the VCO development, whose circuit has its passive components and metal lines extracted through EM simulation. It was designed using an LC topology, achieving a phase noise better than -75.5 dBc/Hz. Although the phase noise has high value, the use of a frequency synthesizer would certainly improve it. The tuning range of 14.65% is attained by using an HBT varicap for the fine tuning and binary controlled switched capacitors for the channel selection. Drawing less than 5.11 mA, the designed VCO has a FoM of -157.18 dBc/Hz, which is low when compared to the other state of the art VCOs.

In order to accomplish the sliding-IF architecture, a frequency doubler and a frequency divider by two have been designed. The doubler has been implemented using a Gilbert cell mixer, having a conversion gain up to 3 dB while drawing less than 16.86 mA from the power supply. The designed divider is a type-D latch based, providing a gain up to 22 dB while drawing less than 9.45 mA.

The frequency downconversion stage has been designed separately, with a first and second mixing stage. The second stage, working at lower frequencies, provides a higher gain than the first. Both together provide a gain higher than 14 dB while drawing less than 10.16 mA. Furthermore, the circuit presents a noise figure of 25.16 dB.

The complete receiver front-end has a current consumption of 47 mA from a 1.8 V power supply. However, this consumption would increase with the LNA design that is the circuit with higher power consumption. The receiver presents a conversion gain higher than 5 dB and NF of 24 dB at 58 GHz. Withal, the NF value does not mean too much since the LNA has not been designed and it is the circuit which basically imposes the NF at the receiver.

Although the receiver front-end has been designed with success, the employed technology presents some limitations for circuits at so higher frequencies. Besides the weak performance of the components at high frequencies, also their schematic models were proven to be inaccurate, at least for the passive components.

Whilst the receiver front-end has been designed with success, there still exists the need of complete the receiver through the LNA and frequency synthesizer designs. The design for these blocks would not only complete the front-end receiver but it would also improve the performance of the overall receiver.

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