TÉCNICO LISBOA

Impact of Emitter Dopant Gradient on Amorphous/Crystalline Silicon HIT Cell Performance

MISHAEL EBERE STANLEY

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Supervisors : Prof. Ana Maria Heleno Branquinho de Amaral
Engr. Igor Sobkowicz

Examination Commitee

Chairperson: Prof. José Alberto Caiado Falcão de Campos
Supervisor: Prof. Ana Maria Heleno Branquinho de Amaral
Members of the Committee: Prof. Guilherme António Rodrigues Lavareda

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Resumo

Palavras Chave: Passivação, Degradação, gradiente da camada p, fotocondutância, recozimento

As células HIT consistem numa camada muito fina de a-Si:H intrínseco entre a camada de a-Si:H tipo p e o substrato de c-Si tipo n. Esta estrutura foi inicialmente investigada para aplicação no fabrico de uma junção a baixa temperatura para uma célula solar baseada em silício policristalino ou monocristalino. O emissor é composto por uma camada muito fina de silício amorfo intrínseco coberta por uma camada de silício amorfo tipo p. A zona de absorção óptica é composta pela bolacha de silício cristalino tipo n e a camada BSF é constituída por um filme fino de a-Si:H intrínseco coberto por uma camada de silício amorfo tipo n. O ITO é depositado por pulverização catódica em ambas as faces da célula e actua simultâneamente como camada anti-reflectora e como óxido transparente e condutor para aumentar a recolha de portadores. O objectivo desta tese é investigar a influência de alguns processos de fabrico de células na passivação, na degradação e no desempenho da célula solar. As células são fabricadas usando o método de deposição de PECVD; a célula padrão é fabricada sem gradiente de concentração na camada p enquanto na célula optimizada é introduzida na sua estrutura uma camada p com gradiente. A passivação é caracterizada por medidas de tempo de vida dos portadores fotogerados. Após a finalização do processo de fabrico as células obtidas são recozidas e caracterizadas para avaliar a sua eficiência e desempenho global sendo feita a comparação entre as células com e sem gradiente. As células são então optimizadas introduzindo um material que melhora a sua passivação e recozimentos posteriores provaram ser benéficos para as propriedades da célula. Um resultado interessante é o elevado valor de Voc e de eficiência conseguidos na célula optimizada, recozida e com gradiente quando comparada com a célula padrão que não tem gradiente na camada p. Os resultados provam que a presença de uma camada emissora com gradiente é benéfica para a célula solar de heterojunção a-Si:H/c-Si

Abstract

Keywords : Passivation, Degradation, p-layer gradient, photoconductance, annealing

The HIT (Heterojunction with Intrinsic layer) cell features a very thin layer of intrinsic a-Si:H inserted between p-type a-Si:H and n-type c-Si. This structure was originally investigated for a low temperature junction fabrication technique for a thin film poly-Si or nc-Si solar cell. The emitter is composed of a very thin intrinsic a-Si:H layer capped by p-type a-Si:H. The absorber is thick n-type c-Si wafer and the BSF is made of a thin undoped a-Si:H capped by n-type a-Si. ITO is sputtered on the front and back sides of the cell and it acts as both an anti-reflection coating and a transparent conducting electrode to enhance the collection of carriers. The objective of this thesis is to investigate the influence of cell recipes on the passivation, degradation and performance of the cell. The cell was fabricated using the PECVD deposition method; the standard cell has no p-layer gradient while in the optimized cell a p-layer gradient is introduced in the cell structure. The passivation is characterized by photoconductance lifetime measurements. The finished cells are annealed and characterized to evaluate their efficiency and overall performance and a comparison is made between cells with a p-layer gradient and without a p-later gradient. The cells are then enhanced by introducing some material which improves its passivation, further annealing steps proved beneficial to the cell properties. An interesting outcome is the high V_{OC} and efficiency achieved in the enhanced, annealed p-layer gradient cells as compared to the standard, no p-layer gradient cell. The results prove that the presence of an emitter layer gradient is beneficial for a-Si:H/c-Si heterojunction solar cells.

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List of abbreviations

a-Si:H - Hydrogenated amorphous Silicon
BSF - Back Surface Field
c-Si - Crystalline Silicon
E_C - Conduction Band
E_V - Valence band
FF - Fill Factor
Grad – Gradient
noGrad – no Gradient
HIT – Heterojunction with Intrinsic Thin Layer
ITO – Indium Tin Oxide
LED - Light Emitting Diode
PECVD – Plasma Enhanced Chemical Vapor Deposition
PCD – PhotoConductance Decay
PVD – Physical Vapor Deposition
SHJ – Silicon Heterojunction
TCO - Transparent Conducting Oxide
V_{OC} - Open Circuit Voltage
I_{SC} - Short Circuit Current

Chapter 1
An Introduction to Photovoltaics

1.1 Basic Principles of Photovoltaic Power Generation

1.1.1 The Photovoltaic effect

The Photoelectric effect is the generation of charge carrier when particles called photon is incident on a material. In photovoltaics, the incident photons induce the creation of an electron-hole pair which can flow through an external circuit thereby producing electricity. Alexandre-Edmond Becquerel is credited with the discovery of the photovoltaic effect and the operating principle of the solar cell, in 1839 [1][2]. To describe this mechanism more formally, it is best to think of light in terms of a stream of photons where each photon carries one quantum of energy. Each photon is associated with just one wavelength or frequency. High-frequency photons have more energy than the ones with low frequency. The solar cell is composed of a *p-n junction* which formed by a p-doped semiconductor and an n-doped semiconductor. (See figure 1.1).

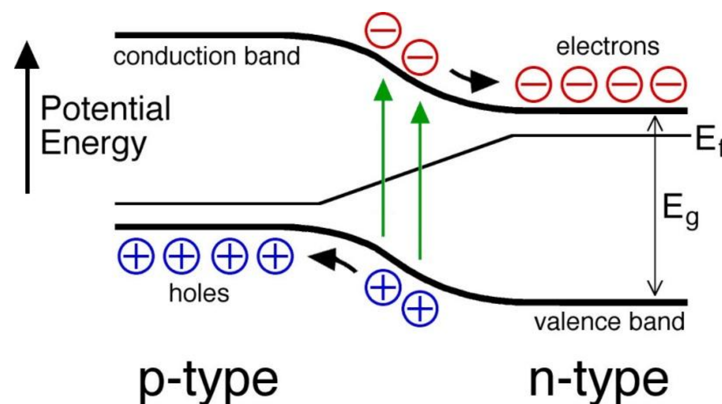


Figure 1.1 A typical p-n Junction band diagram

When the cell is illuminated by light, a number of physical processes occur:

- Absorption of photons with energy $h\nu \geq E_g$ (where E_g is the energy gap of the cell)
- Generation of charge carrier pairs (Electrons and Holes)
- Migration of charge carriers (Diffusion) and
- Separation of charge carriers induced by the built-in electric field. This separation results in a voltage across the electrodes of the cell.

1.1.2 Photovoltaic Conversion efficiency

The efficiency of a PV cell can be analyzed on the basis of the current-voltage (I-V) light characteristics illustrated in figure 1.2.

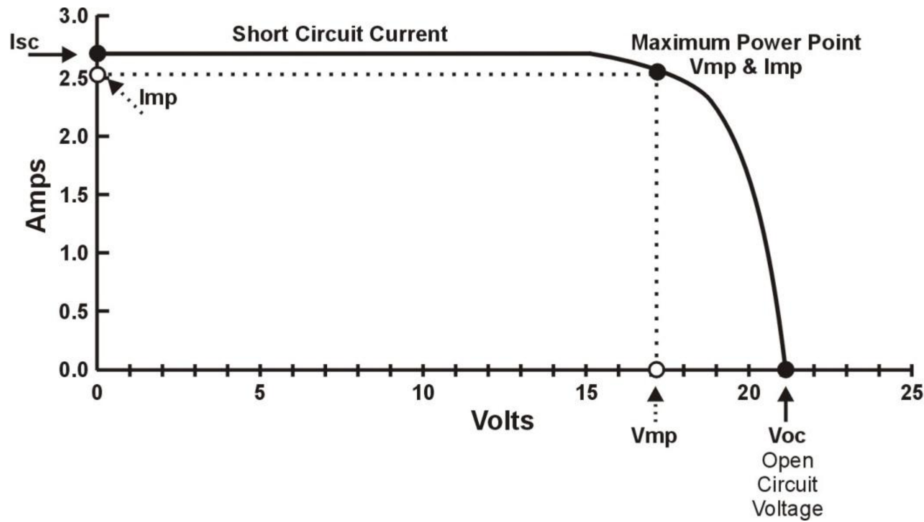


Figure 1.2 I-V characteristics of a solar cell under illumination

The efficiency of the solar cell is described as:

$$\eta = \frac{P_m}{P_{in}} \qquad 1.1$$

Where P_m is the maximal power developed in the cell and P_{in} is the surface power density of the incident light. [3]

$$P_m = J_m V_m \qquad 1.2$$

Where J_m and V_m are the maximum current and voltage obtained in the cell respectively. The Fill Factor (FF) is now introduced and is defined in very simple terms as the degree of "squareness" of the J-V characteristic curve of the solar cell. It is expressed as:

$$FF = \frac{J_m V_m}{J_{SC} V_{OC}} \qquad 1.3$$

Hence, the efficiency, η can be expressed as:

$$\eta = \frac{J_{SC} V_{OC} FF}{P_{in}} \qquad 1.4$$

The short circuit current, I_{sc}, open circuit voltage, V_{oc}, fill factor, FF and the solar cell efficiency, η are macroscopic quantities characterizing the cell and can be determined by appropriate measurements.

1.2 World Record PV Cells

Since the emergence of photovoltaic technology and its potential for energy production, global R&D effort has been aimed at developing new types of PV cells and at the same time trying to increase the conversion efficiencies of existing solar cells. Indeed, a lot of progress has been made in this regard and more resources are being dedicated to further research in this field. The National Renewable Laboratory (NREL) in the United States releases periodically a detailed chart featuring the best cell efficiencies obtained at research level.

The record efficiency for crystalline silicon heterostructures which is the focus of this report is 25.6%. The most efficient cells in the chart are the four-junction (or more) concentrator cells. A major drawback facing the utilization of these cells is often the complex mounting and sun tracking mechanisms required for its operation.

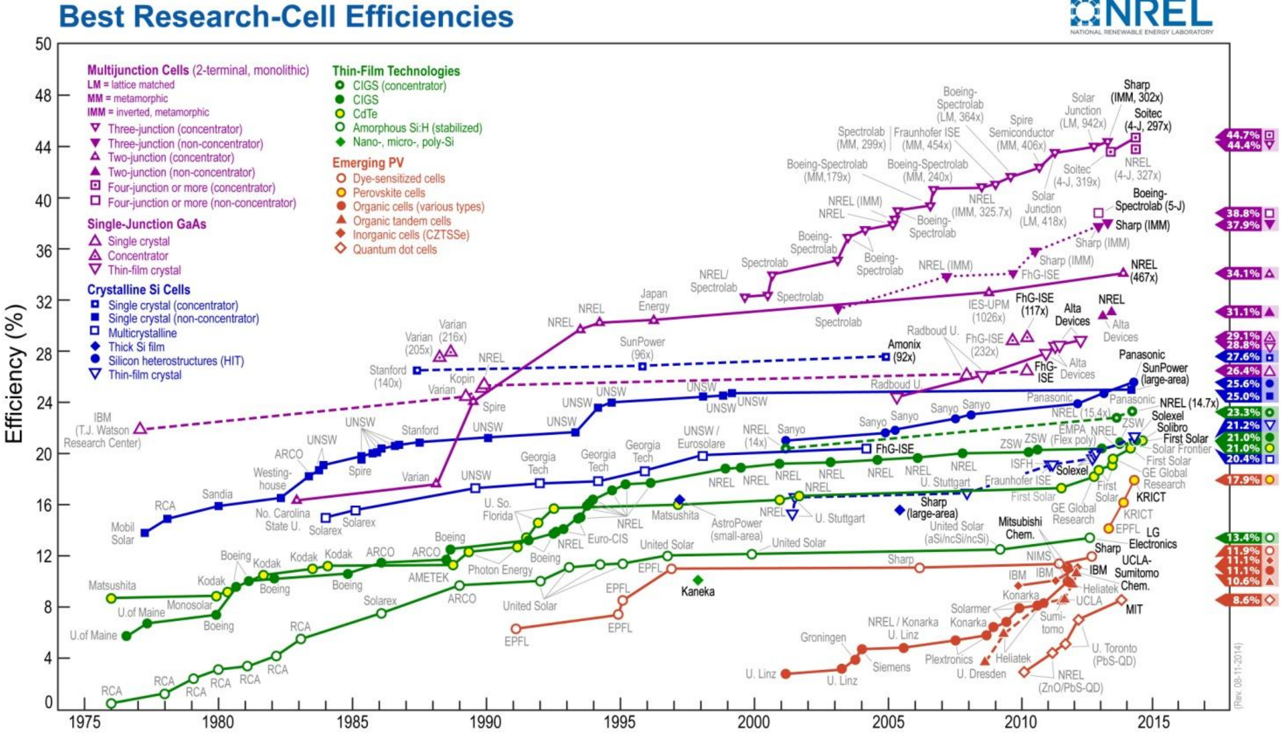


Figure 1.3 Best cell efficiencies chart compiled by the National Renewable laboratory (Source: NREL) [4]

1.3 Solar Energy Market

Solar electric energy demand has grown by an average 30% per annum over the past 20 years against a backdrop of rapidly declining costs and prices. This decline in cost has been driven by economies of manufacturing scale, manufacturing technology improvements, and the increasing efficiency of solar cells [5]. PV installations worldwide grew to 7.3 GW in 2009, up 20% from the prior year. Expected to reach 8.4-13.1 GW in 2010, the various forecast scenarios predict demand rising to 15.4-37 GW in 2014, more than five times the size of the 2009 market. The worldwide on-grid segment grew by 20% in 2009, and the off-grid market grew 23% in 2009, faster than on-grid for the first time in 15 years but on a much smaller base [5]. Global solar photovoltaic (PV) markets will finally begin to stabilize in 2013, according to Navigant Research's "Solar PV Market Forecasts"[6] and will reach grid parity by 2020 as demand reorients toward both developing countries and maturing markets.

Figure 1.4 show the current and forecasted installed capacity of solar PV and it is expected that by the end of 2020, solar PV is expected to be cost-competitive with retail electricity prices, without subsidies, in a significant portion of the world. [6].

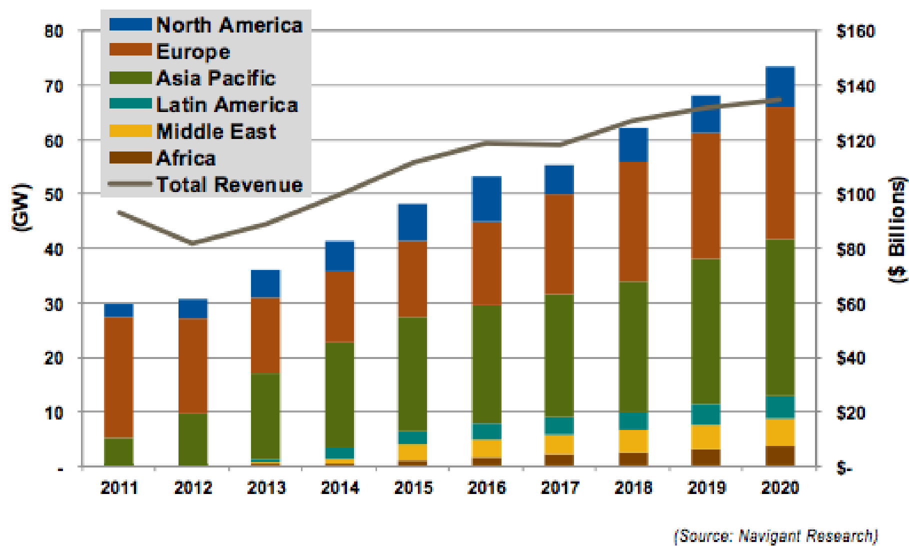


Figure 1.4 Annual Solar PV installed capacity and Revenue by Region (Source: Navigant research) [6]

With a year-on-year increase of 65.5% from 2011 to 2012 [7], solar power (photovoltaic and CSP) leads the pack of renewables. It hence suffices to conclude that the PV market and worldwide installed capacity would continue to increase in the next exciting years to come in spite of the challenges being faced.

As regards crystalline silicon (c-Si) PV modules, it is forecasted that production costs will fall from 50 cents per watt in the fourth quarter of 2012 to 36 cents per watt by the end of 2017 [8]. The report also predicts that the majority of these cost declines will derive from technology innovations such as diamond wire sawing for PV wafers, advanced metallization solutions, and increased automation in place of manual labor.

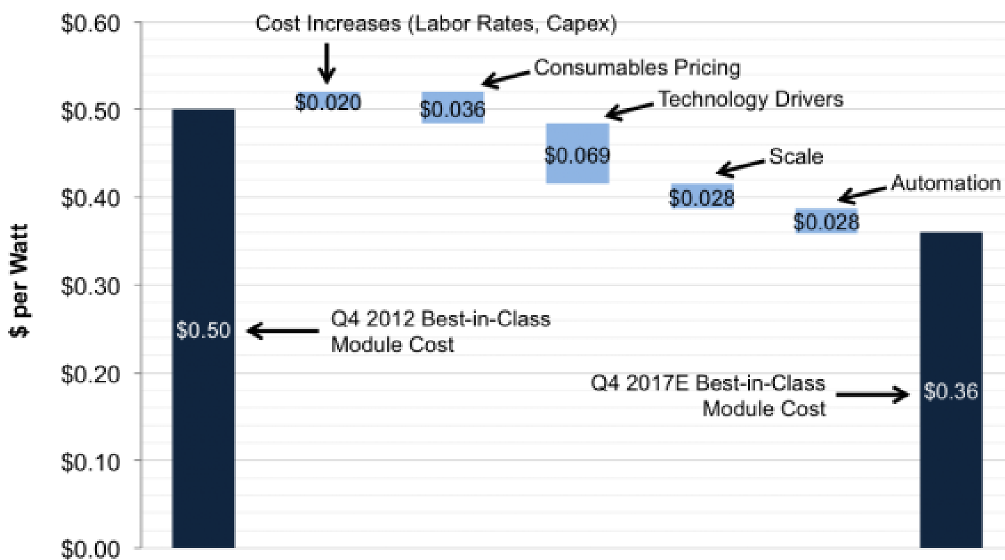


Figure 1.5 Contribution of Key Drivers Toward All-In Module Cost Reduction, Best-in-Class China Producer, Q4 2012-Q4 2017E (source: PV Technology and Cost Outlook, 2013-2017) [8]

The infographic in figure 1.5 shows a breakdown of costs of key drivers contributing to the production cost of c-Si modules. It is interesting to note that back in 2009/2010; industry roadmaps were targeting $1.00/W module costs as a medium-term goal, however, with best-in-class Chinese producers already approaching costs of $0.50/W in 2013, yesterday's goals are no longer relevant today.

Chapter 2
The a-Si:H/c-Si Heterojunction Solar Cell

2.1 Amorphous/Crystalline Silicon Heterojunction cell

A simple heterojunction cell is one that is made of two semiconductors of different bandgaps forming the p-n junction. In this report, the heterojunction solar cell under consideration is made up of amorphous p-type silicon and crystalline n-type silicon wafer.

2.1.1 Structure of an a-Si: H/c-Si HIT cell

The HIT (Heterojunction with Intrinsic layer) cell features a very thin layer of intrinsic a-Si:H inserted between p-type a-Si:H and n-type c-Si. This structure was originally investigated for a low temperature junction fabrication technique for a thin film poly-Si or nc-Si solar cell[9]. In this report, the emitter is composed of a very thin intrinsic a-Si:H layer capped by p-type a-Si:H. The absorber is thick n-type c-Si wafer and the BSF is made of a thin undoped a-Si:H capped by n-type a-Si. ITO is sputtered on the front and back sides of the cell and it acts as both an anti-reflection coating and a transparent conducting electrode to enhance the collection of carriers. Metals contacts are deposited on the front side forming a grid to allow light into the cell, however, since light enters the cell through the front side only, the metal contact covers the entire back side of the cell for maximum collection of carriers.

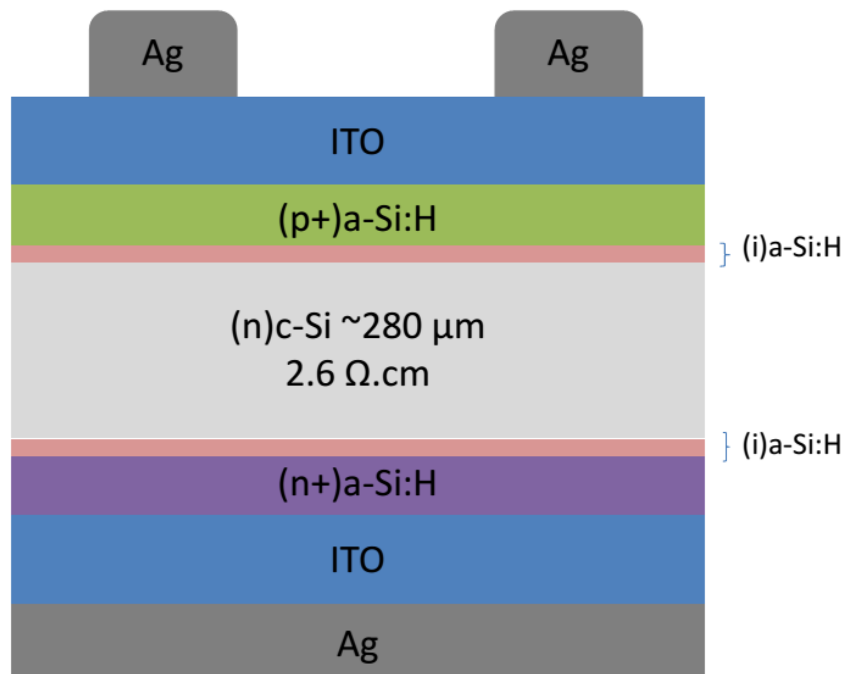


Figure 2.1 Structure of a standard heterojunction solar cell

2.1.2 Band Diagram of the a-Si:H/c-Si cell

As aforementioned, a heterojunction solar cell is made of two materials with different bandgaps. A consequence of this is a bandgap mismatch hence making it impossible to have the conduction and valence band edge levels continuous through the junction. Figure 2.2 demonstrates the band structure of a heterojunction a-Si:H/c-Si solar cell as is generally accepted [10][11].

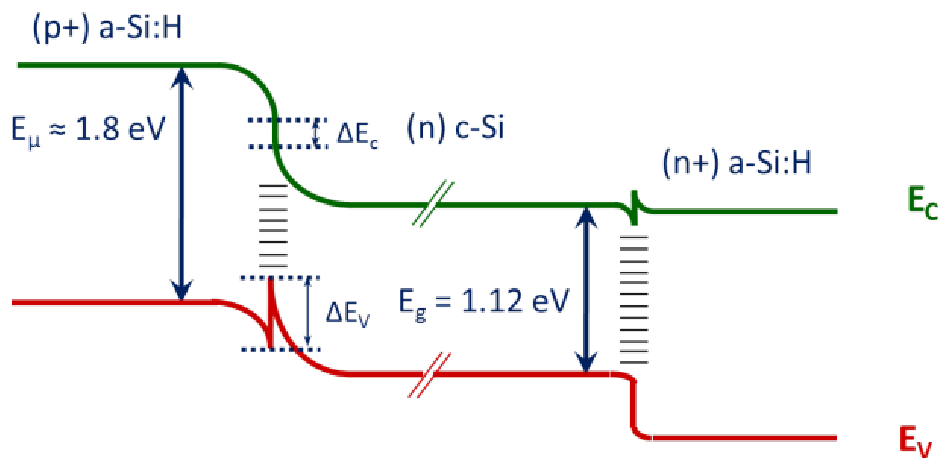


Figure 2.2 Band diagram of a (p+) a-Si:H/(n) c-Si/(n+) a-Si:H heterojunction solar cell

ΔE_C and ΔE_V represents the conduction and valence band offsets respectively. Considering the back side of the cell, the large valence band offset at the (n^+) a-Si:H interface provides a very good mirror and serves as a barrier to the flow of minority holes whereas, the flow of majority electrons from the (n) c-Si to the (n^+) a-Si:H is relatively unhindered as the conduction band offset is quite small. Thus the (i/n^+)a-Si:H provides an excellent back surface field (BSF) with adequate majority carrier electron transport and good passivation repelling minority holes from the back contact. The ohmic contact on the back side of the BSF does not hinder electron collection, hence is not a problem [12].

On the front side of the cell, we have a large valence band offset which represents a barrier which holes generated in the (n) c-Si absorber would have to cross in order to get to the (p^+) a-Si:H and be collected. This barrier is undesirable as an effective minority hole transport is required in this region. Pure thermionic emission is unlikely to provide enough transport for the holes due to the high barrier. However, the trapped holes may be able to tunnel across the thin a-Si:H(i) layer into the a-Si(p) layer, possibly with some thermal and trap assistance [12].

2.2 Passivation of HIT Cells

The goal of passivation is to decrease the number of defect states at the surface of the c-Si which otherwise would serve as recombination sites for minority carriers hence reducing the open circuit voltage and the overall efficiency of the cell. All crystalline silicon cell designs include passivation schemes meaning that the c-Si is always capped by a film whose goal is

to provide a surface passivation of the c-Si. The passivation types can be broadly classed into two:

- Chemical passivation where we aim to reduce the defect density at the interface which would in effect reduce the surface recombination velocities of the electrons and holes
- Field-Effect passivation where we aim to decrease the concentration of minority carriers at the highly doped surfaces.

Indeed, the chemical passivation results in an increase in the effective lifetime of carriers on the entire injection level range while the field effect passivation will mostly increase the lifetime in the low injection range[13]. It generally accepted and proven that a pre-cleaning process of the wafer by dipping in HF results in very good passivation of the dangling bonds on the surface. Very good field effect is further achieved at the back side of the cell by using a highly doped a-Si:H which acts as a Back Surface Field (BSF) and repels minority carriers. It then follows that the best configuration would be to achieve a low interface defect density otherwise known as dangling bonds and to achieve a strong field effect.

2.2.1 The Intrinsic Layer

The current major application of the a-Si:H passivation scheme on c-Si for photovoltaic applications consists of a double-layer stack composed of an intrinsic plus a doped a-Si:H layer. The effectiveness of the intrinsic a-Si:H in providing adequate passivation was shown in Sanyo's cell where the presence of a thin undoped layer inserted between the c-Si absorber and the doped a-Si:H resulted in a decrease in the dark saturation current of the diode as compared to a heterojunction without this buffer layer [14]. Based on the scheme of passivation, Sanyo has reached an efficiency of 23%. This buffer layer is beneficial because intrinsic a-Si:H has a far lower density of defects than a doped a-Si:H layer[15]. A lower density of mid-gap trap states reduces the trap-assisted inter-band tunneling-recombination rate across the a-Si/c-Si interface, thereby suppressing parasitic dark saturation current. On the other hand, if there is unintentional Si epitaxy rather than a-Si:H deposition, the epitaxy may be defective and the interface rough, resulting in unpassivated silicon dangling bonds or other defects [16]. Labrune further showed the negative impact of epitaxial growth during the deposition of the intrinsic a-Si:H layer [17]. In figure 2.3, Labrune demonstrates the impact of growing an epitaxial buffer layer between the (i)a-Si:H and (n) c-Si wafer. A very thin layer of a-SiC:H is introduced as it has been proven to impede epitaxy. An interesting result seen in the graph is that increasing the thickness of the epitaxial layer leads to a loss in passivation

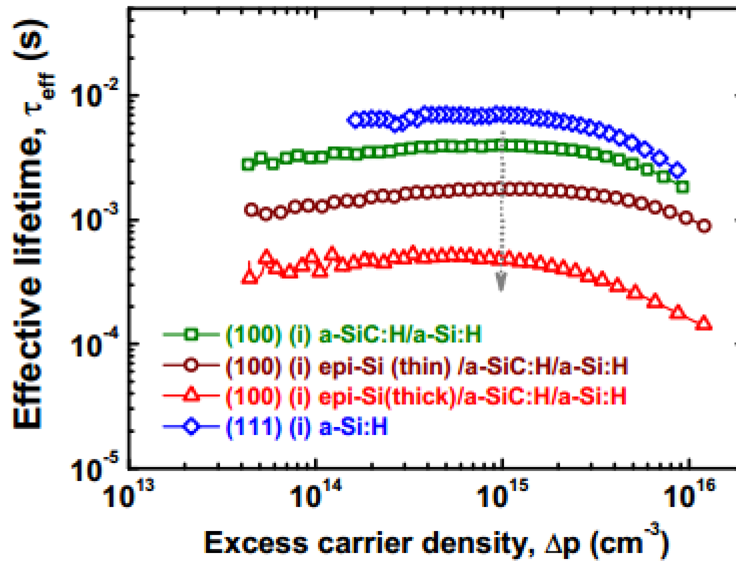


Figure 2.3 Effective lifetimes of (n) c-Si passivated by an (i) a-Si:H layer with a buffer epitaxial layer of varying thickness (source: Labrune PhD thesis)[17]

Thus, in the absence of any epitaxy, a thin buffer layer of undoped a-Si:H would yield a very good passivation hence reducing trap-assisted recombination in the defect states.

2.3 Fabrication of a-Si:H/c-Si cells

Here we review the basic fabrication steps involved in preparing the cell precursors and subsequently the finished cells. The a-Si:H of all the cells studied in this work were deposited by the Plasma Enhanced Chemical Vapor Deposition (PECVD) method. We briefly review this method of deposition

2.3.1 a-Si:H Deposition by PECVD

PECVD uses electrical energy to generate a glow discharge (plasma) in which the energy is transferred into a gas mixture. This transforms the gas mixture into reactive radicals, ions, neutral atoms and molecules, and other highly excited species. These atomic and molecular fragments interact with a substrate and, deposition processes occur at the substrate. Since the formation of the reactive and energetic species in the gas phase occurs by collision in the gas phase, the substrate can be maintained at a low temperature. Hence, film formation can occur on substrates at a lower temperature than is possible in the conventional CVD process, which is a major advantage of PECVD. The ionization of the neutral gas molecules occurs when electrons are accelerated in an oscillating electric field caused by a sinusoidal voltage applied to the RF electrode (Cathode). As the plasma acts as a variable load, a matching box is inserted between the RF voltage source and the Plasma with the goal of adapting the impedance of the plasma to that of a 50Ω load for the generator that will minimize the reflected power (see figure 2.4).

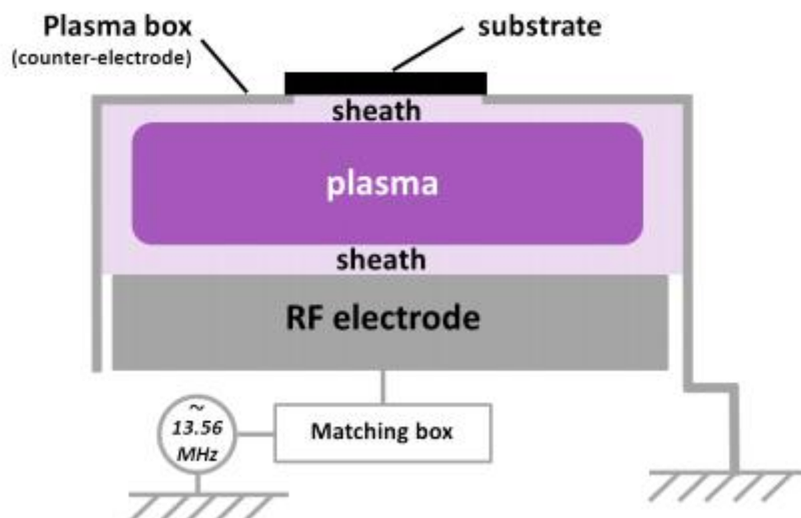


Figure 2.4 Schematic of the plasma box used in the ARCAM reactor in LPICM (Source: Labrune PhD thesis) [17]

2.3.2 Fabrication parameters for a-Si:H/c-Si cell

The fabrication of the solar cells involved the deposition of intrinsic and doped a-Si:H by low-temperature PECVD, the deposition of ITO by PVD at 180°C and the evaporation of silver as metal contacts. The fabrication steps consist of:

- A standard intrinsic amorphous silicon layer with a thickness of 5nm
- A standard n-doped amorphous silicon layer deposited at 200°C. Its conductivity reaches 2.42E-02 Ω-1·cm-1, This layer yields an optical energy bandgap of 1.65 eV. The deposition parameter for this layer is summarized in table 2.1 below

SiH4 [sccm]	PH3 (1% in H2) [sccm]	Time [s]	Pressure [mTorr]	Power [W]	Thickness [nm]
50	1	360	60	1	15

Table 2.1

- A standard p-doped amorphous silicon layer with a conductivity of 1.54E-04 Ω-1·cm-1 with deposition parameters summarized in table 2.2

SiH4 [sccm]	Trimethyl Borane (TMB) (1% in H2) [sccm]	Time [s]	Pressure [mTorr]	Power [W]	Thickness [nm]
50	20	200	110	1	16

Table 2.2

- An ITO layer of approximately 82 nm deposited by sputtering on both sides of solar cell precursor. The n-side was fully covered by the TCO whereas for the p-side, the wafer was cleaved to obtain a quarter of wafer, and a 2x2 cm^2 mask was used to avoid any measurement inaccuracy that could occur due to lateral transport beyond the cell limits.

- A silver contact evaporated on both side of the solar cell precursor, on top of the ITO. On the n-side again, a deposition was made on the whole ITO surface, whereas on the p-side, a grid was used such that it fitted the 2x2 cm² ITO cell limits. The grid containing a tapered busbar is as shown in figure 2.5

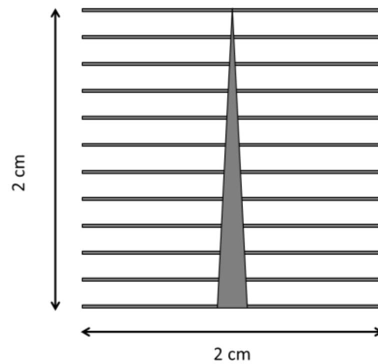


Figure 2.5 Schematic showing the 2x2 cm^2 grid used for the ITO and Silver contact deposition

The above mentioned steps is summarized in figure 2.6 which shows the fabrication chain from a-Si:H deposition to Silver contact evaporation.

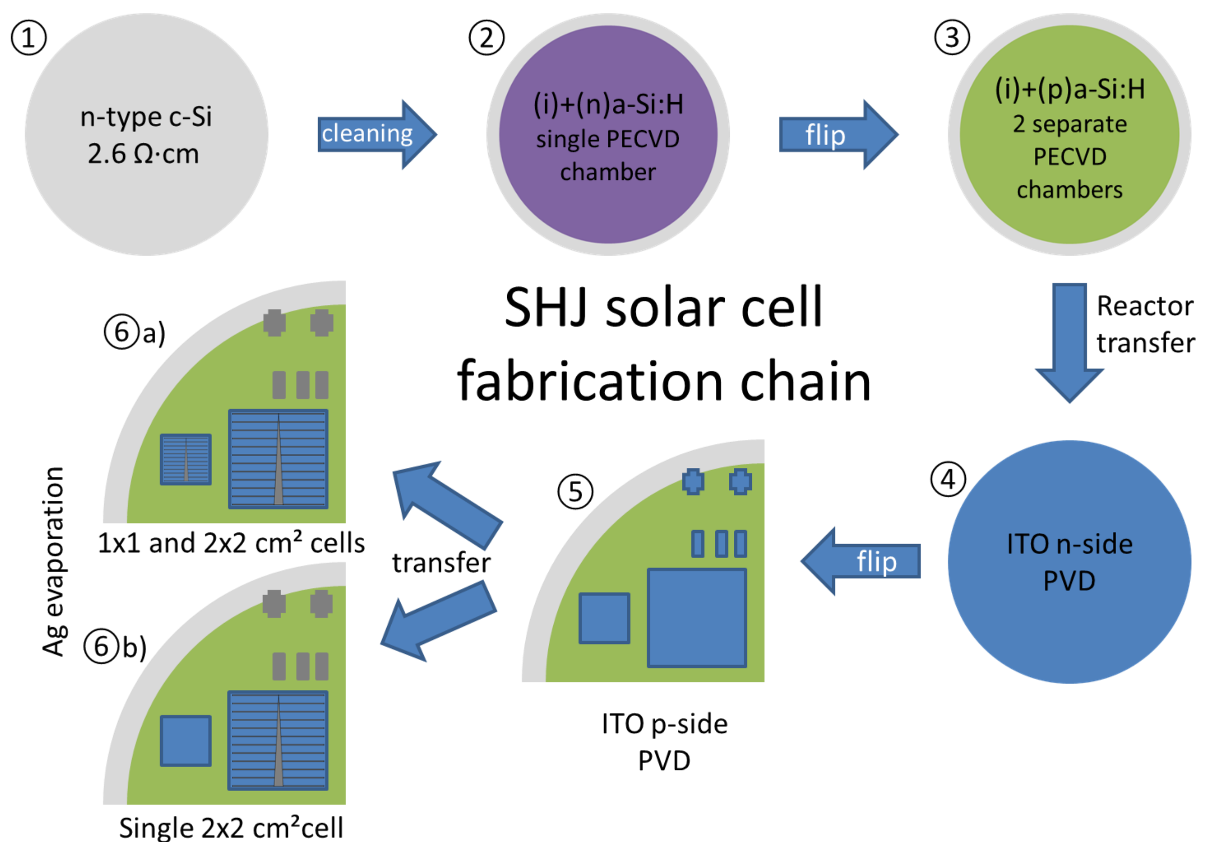


Figure 2.6 HIT solar cell fabrication chain at LPICM

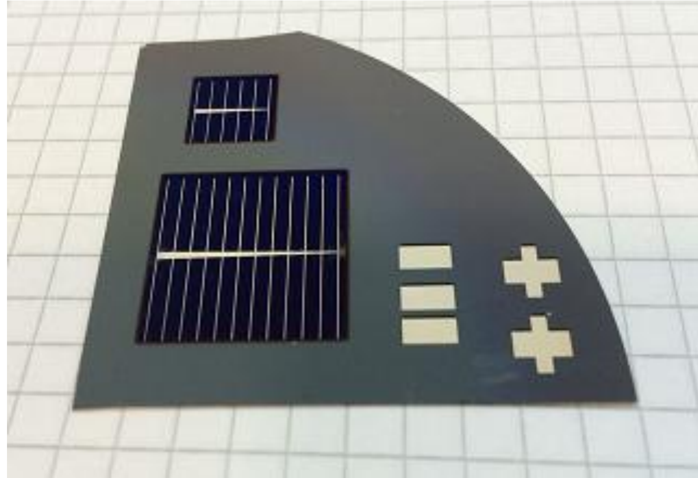


Figure 2.7 Photograph of a finished cell on a wafer quarter holding a 2x2cm^2 and 1x1cm^2 cells

Using this chain fabrication procedure, a record cell efficiency of 17.6% was achieved in LPICM in 2011[17]. A photograph of the finished cell can be seen in figure 2.7 above. This is the standard procedure adopted in this internship.

Chapter 3
Degradation Study by PCD

3.1 Photoconductance Decay

The main applications of photoconductance measurements of silicon wafers include the determination of implicit device V_{OC} and bulk minority carrier lifetimes. The Sinton PCD lifetime tester is shown below in figure 3.1

Figure 3.1. WCT-120 Sinton Lifetime tester (source: www.sintoninstruments.com)

It is a contactless method which is extremely valuable in measuring the carrier lifetimes in silicon wafers and HIT structures. Photoconductance decay is a commonly used method based on analyzing the decay of photo generated carriers after a very short light pulse from a laser, flash lamp, LED array or laser diode is shone upon a sample.

Figure 3.2 shows the photoconductance of a silicon wafer as a function of time in response to a pulse of light. Both the rise and fall of the photoconductance follow an exponential dependence with the minority carrier lifetime of the material τ. Classically, the decay rate is used to determine the lifetime.

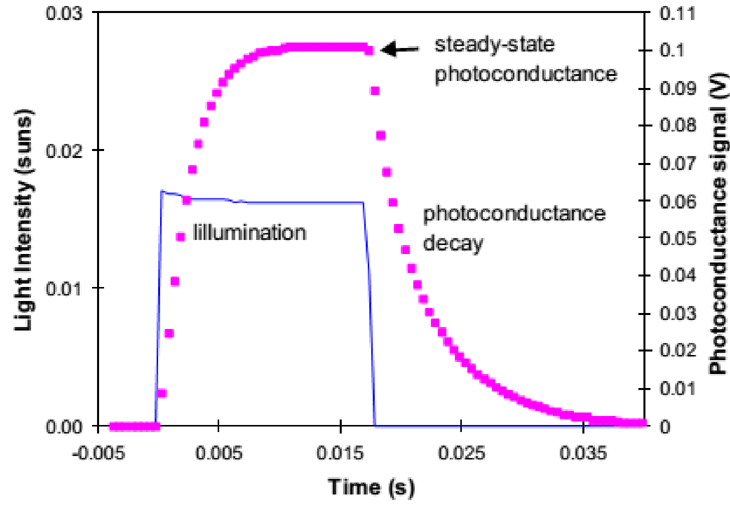


Figure 3.2 Response of a high resistivity FZ wafer to a square pulse of light. (source: Andrés Cuevas et. al)[18]

3.2 Transient PCD

The PCD technique used in this report is the Transient Photoconductance decay technique. The transient method is an adequate way of measuring the effective lifetimes of our samples since the lifetimes are greater than 200µs [19]. The transient approach to measuring the carrier lifetime can be summarized in a number of steps [19];

- The sample is subjected to a short pulse of light that peaks and decays rapidly
- The slower decay of the sheet conductance is measured as a function of time after the flash has finished
- The sheet conductance is then converted into an average excess carrier density Δn for each moment in time and finally
- The derivative of the conductivity is taken with respect to time, the carrier lifetime at each excess carrier density Δn is then determined using the equation;

$$\tau_{eff} = \frac{\Delta n}{d(\Delta n)/_{dt}} \qquad 3.1$$

Proper analysis of transient photoconductance decay requires use of the continuity equation for the excess minority carriers[20]:

$$\frac{\partial \Delta n}{\partial t} = G_b(t,x) - U_b(t,x) + \frac{1}{q}\frac{dJ_n}{dx} \qquad 3.2$$

Where $G_b(t,x)$ and $U_b(t,x)$ are the photogeneration rate and recombination rate in the bulk, Δn the excess minority carrier density, and J_n the electron current density. For the transient regime, $G_b(t,x) = 0$. Nagel *et. al*[21] realized a generalized form for expressing the lifetime by introducing the classical relationship $U \equiv \frac{\Delta n}{\tau_b}$ where U is the recombination rate and τ_b is the bulk carrier lifetime, setting $\tau_{eff} = \tau_b$ and inserting this in equation 3.2 yields;

$$\tau_{eff}(\Delta n) = \frac{\Delta n(t)}{G(t) - \frac{d\Delta n(t)}{dt}} \quad 3.3$$

Again, in the case of transient PCD, setting $G_b(t,) = 0$ and inserting this in equation 3.3 would lead back to equation 3.1. Characterizing the lifetime of the samples is a very improtant procedure as it gives information on the level of passivation of the sample. A loss in passivation of a sample would be seen as a drop in its lifetime, this is usually also seen as an increase in the surface recombination velocity which is inversely proportional to the lifetime.

$$S_b = \frac{W}{2}\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}\right) \quad 3.4$$

Where S_b is the surface recombination velocity, W is the wafer thickness and τ_{eff} and τ_{bulk} are the effective and bulk lifetimes respectively. The lifetimes of the samples are hence monitored at each step of the fabrication in order to understand how the cell degrades.

3.3 Passivation in Standard cell Precursor

The standard cell precursor features a typical HIT stack as developed by Sanyo [9]. The diode junction is formed of p-type a-Si:H and an n-type c-Si respectively. In between the junction is an intrinsic layer of a-Si. The BSF is added by depositing a highly doped n-type a-Si on the (n) c-Si absorber layer. Again, an intrinsic layer of (i) a-Si is sandwiched between the absorber and the BSF to lower the interface defect density. A transparent conducting layer of ITO is deposited on both sides of the precursor. The layer of ITO is essential as it improves the collection of charges to the electrodes. Sputtering which is a PVD technique is used to deposit ITO; however this induces degradation in the cell precursor.

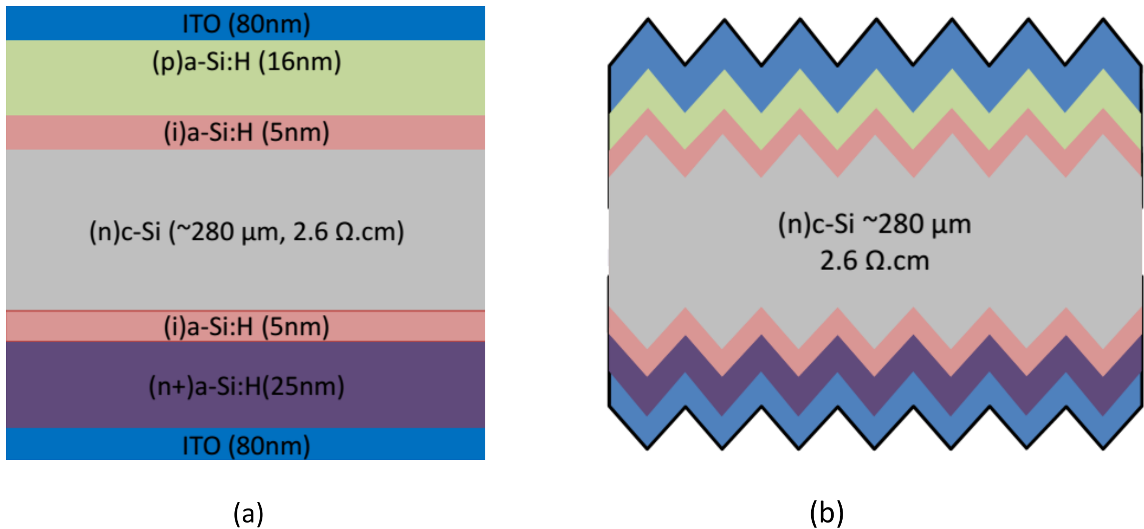


Figure 3.3 Standard HIT cell precursor structure of (a) flat and (b) textured

Figure 3.3 shows the HIT scheme for a flat cell precursor. The configuration of the BSF is kept constant while optimization is carried out only on the p/emitter layer. The thickness of the (n) c-Si absorber layer is 280µm, the (i) a-Si is 5nm while the (n) a-Si BSF is 25nm. To study

the degradation, we have used three types of substrates; the DSP 111 flat substrate, KIno and RTno textured substrates. Several thicknesses of the i-layer are made on the DSP111 substrates and the degree of degradation experienced by each thickness series is evaluated. The thickness of the emitter is also varied and the extent of degradation in the lifetime of the precursor after ITO sputtering will be measured.

3.3.1 ITO sputtering induced degradation in the i-layer

Using the DSP111 substrates, we made four precursors with varying i-layer thicknesses; 5nm, 10nm, 20nm and 50nm. This is done to study the impact of the i-layer thickness on the degradation after ITO is deposited by sputtering. Figure 3.4 shows the loss in passivation experienced by each thickness series characterized by a drop in its effective lifetime. We normalized the lifetimes and have shown the percentage drop in lifetime for each thickness series after ITO deposition.

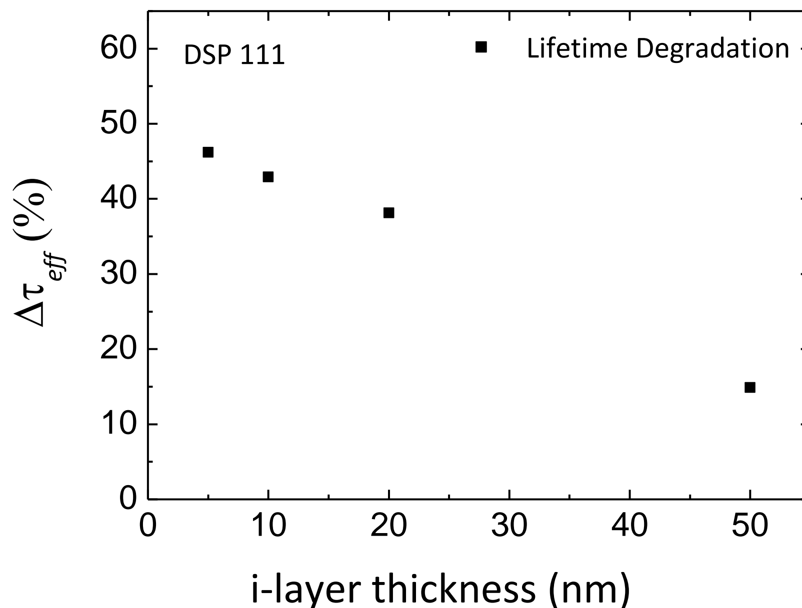


Figure 3.4 Influence of i-layer thickness on degradation after ITO sputtering

It is obvious from the results that increasing the thickness of the i-layer gives a better passivation at the interface as the 50nm thick i-layer experienced the least degradation after ITO was deposited. Its lifetime dropped by only 14.9% while the sample with a 5nm thin i-layer had the most degradation of 46% after ITO was sputtered. We can conclude that the the i-layer plays an important role in protecting the interface from the damaging effects of the ITO over layer sputtering. The protection provided by the i-layer also increases as the thickness is increased. M. Labrune reported in his thesis that increasing the i-layer thickness was beneficial for the V_{OC} of the completed cell[17]. It asserts that the increase in the i-layer thickness reduces the defect density at the interface hence resulting in a smaller recombination rate and thus a higher V_{OC}.

3.3.2 ITO sputtering induced degradation in cell precursor

Several experiments have been conducted to explain the degradation experienced during ITO sputtering. Indeed, more than one factor is implicated in this phenomenon. Zhang *et al.* reports that the elevated temperatures used in ITO deposition can cause passivation degradation when the temperature is over a threshold, it is speculated that the degradation is due to hydrogen effusion from thin a-Si:H at elevated temperatures hence degrading the passivation quality [22]. In a separate study, the degradation during ITO sputtering was attributed to ion bombardment during the sputtering process[23]. It then follows that energetic ions released during the sputtering process can induce Si atoms displacement, through ion-Si atoms collisions, which accounts for the defects generation along the ion penetration path in the film[24]. By intuition, it would be expected that a higher ion kinetic energy would induce more damage leading to a loss in passivation; however, this is not the case. Instead, the level of degradation was shown to depend on the ion flux which creates metastable defects on the c-Si surface[23]. It is noteworthy to state that the damage caused to the passivation is also observed when ZnO is sputtered. By contrast however, boron-doped ZnO TCO layers deposited by metal-organic chemical vapor deposition do not lead to passivation losses hence suggesting that the observed degradation is linked to the sputtering process rather than the specific used TCO material [25].

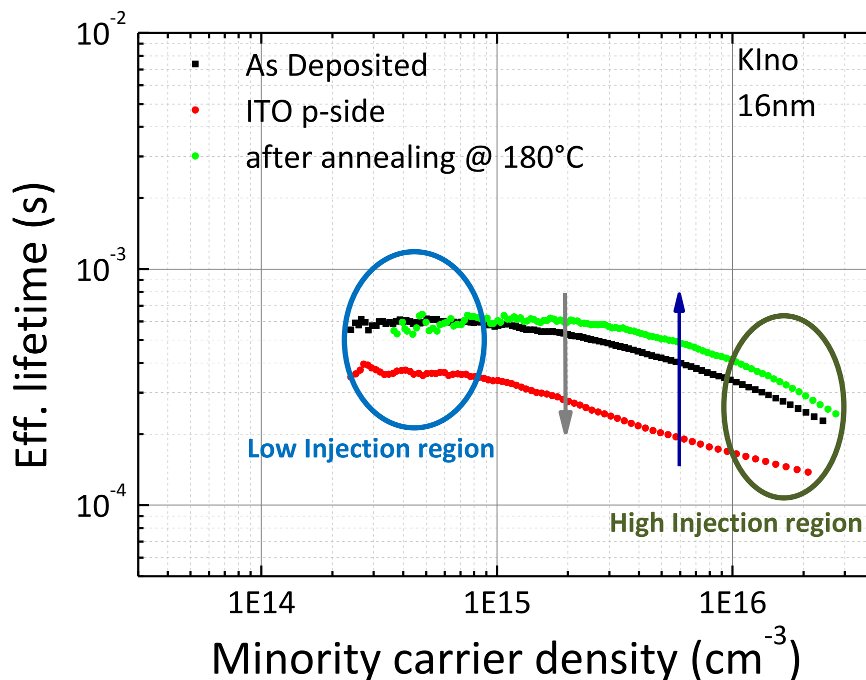


Figure 3.5 *Effective lifetime curve of a-Si:H film on c-Si wafers showing degradation by sputtering and recovery by annealing*

Figure 3.5 shows the loss in passivation after ITO sputtering. There are two regions that are important to take note of; the high injection region which is dominated by defect

recombination and hence depends wholly on the interface defect density and the low injection region where the “field effect passivation” becomes more dominant.

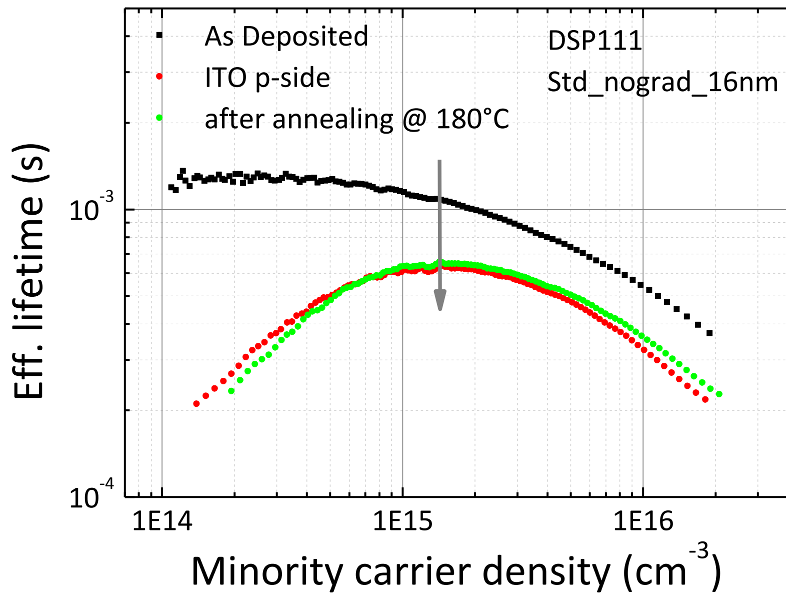
Effect of Annealing

The creation of metastable defects has been linked to the degradation of the precursor samples. Since these defects are metastable, there exists a possibility to recover the passivation by a post-deposition heat treatment step, otherwise called annealing. Results from this procedure indicate that during the annealing, hydrogen bonds with the Si dangling bonds reducing the interface trap density [26]. Zhang *et al.* [22] also showed the beneficial effect of annealing in the samples sputtered with ITO at room temperature. Referring again to figure 3.5, it is observed that the decrease in the level of surface passivation can be recovered fully by annealing. After annealing, we observe that the lifetime in the high injection region is more fully recoverable than that in the low injection region. Hence, annealing effectively reduced the interface defect density giving rise to a lower recombination and higher $V_{OC.}$ This result further indicates that the deterioration of surface passivation is due to the creation of metastable defects at the a-Si:H/c-Si interface[23].

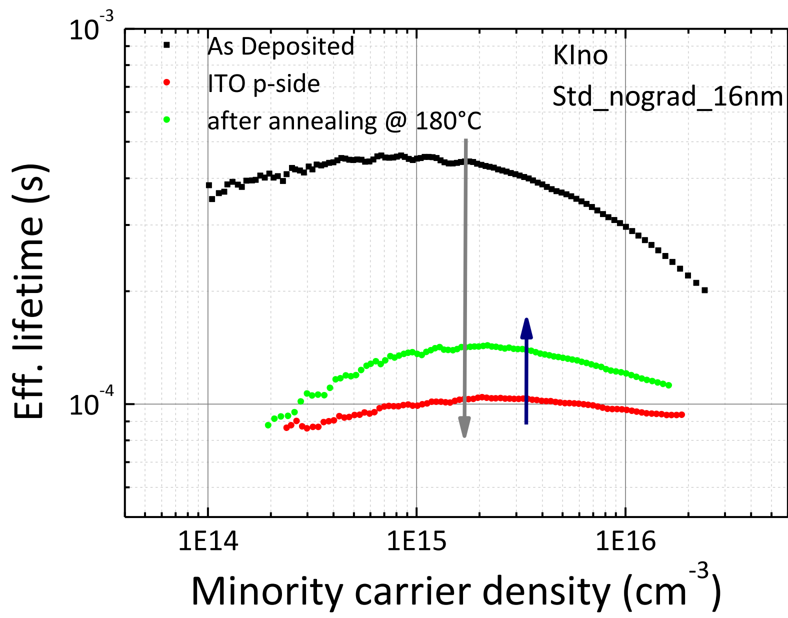
3.3.3 Degradation in the Flat and textured cell precursors

The extent of degradation becomes obvious after obtaining the post-ITO sputtering lifetimes measurements for standard cell precursors. In this report, ‘grad’ refers to ‘p-layer gradient’ while ‘nograd’ refers to ‘no p-layer gradient’. These measurements were taken for both flat and textured substrates with emitter thickness of 16nm. Figure 3.6a depicts the degradation experienced by a flat standard ‘nograd’ cell after ITO is sputtered on the p-side of the cell. The lifetime drops from 1005µs to 615µs which corresponds to 62% its original ‘as deposited’ value. The same trend is observed in figure 3.6b and 3.6c both of which are textured standard ‘nograd’ substrates. In the KIno textured substrates, the lifetime drops from 434µs to 103µs corresponding to 24% of the original value while the lifetime is reduced from 529µs to 100µs (19% of the original value) in the case of the RTno textured susbtrate.

The degraded precursors were subjected to an annealing step to observe any improvement in passivation. The samples were annealed in an N_2/H_2 atmosphere at 180°C which is below the deposition temperature of the a-Si:H in order to reduce the chances of Hydrogen effusion from the samples. For the DSP111 substrate, the results after the ITO sputtering and after annealing are identical. In the case of the KIno and RTno textured substrates, the lifetime improves by a very small amount; 103µs to 142µs for Kino and 100µs to 129µs for RTno respectively.



(a)



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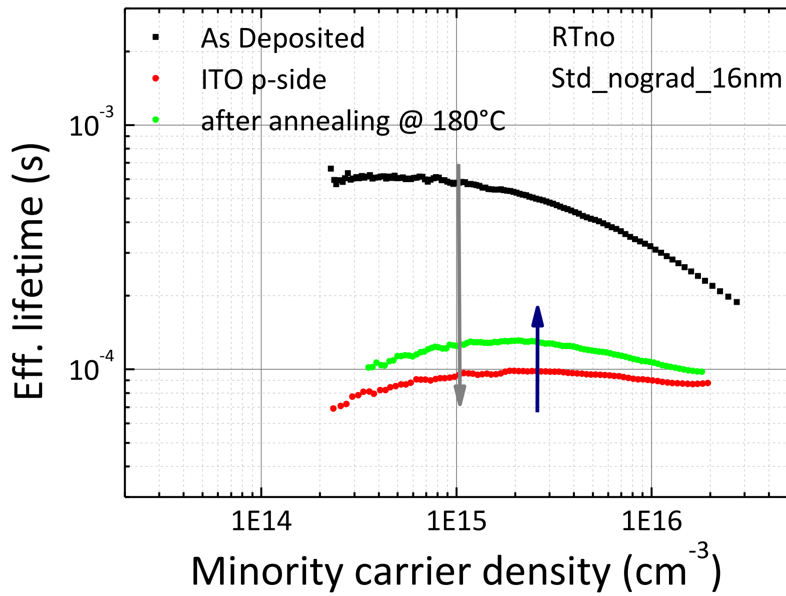


(c)

Figure 3.6 Effective lifetime measurements of standard 'nograd' cell precursors (a) a flat DSP111 (b) KIno textured (c) RTno textured after annealing at 180°C

This seemingly unexpected result could be explained by the growth of epitaxial layers during the deposition of a-Si:H on the c-Si wafer. De Wolf et al[27] studied a sample of films deposited at 205°C which showed a crystalline signature suggesting that that the films gave been grown epitaxially. For these films, annealing does not give rise anymore to an improvement, and for even higher values of T_{depo}, the passivation quality actually drastically goes down as characterized by the measured lifetimes. In our case, we suspect that there has been some epitaxy which prevents an improvement in the passivation of the precursors after annealing. This assertion however, needs further investigation.

3.4 p/emitter side degradation

We now take a step further to optimize the p-layer of the precursors. First, we refer again to the HIT structure shown in figure 3.3a and 3.3b, we have observed after numerous experiments that during ITO sputtering on the (n) and (p) a-Si:H, we experience a very high degradation after sputtering on the p-side as compared to the n-side. Indeed, the damage done after sputtering on the n-side is quite insignificant as lifetime measurements reveal. Hence, we assert that sputtering on the p/emitter side of the precursor induces more damage to the passivation. To demonstrate this, we took a textured cell precursor and characterized the lifetime before ITO sputtering, after ITO sputtering on the n-side (BSF) and after ITO sputtering on the p-side (emitter). The result is shown in figure 3.7 where we experience a greater loss in passivation after sputtering on the p-side. The lifetime degrades by a mere 10% after the n-side deposition of ITO as compared to 40% for the p-side. We have been able to record consistent results in other trials on substrates of varying

thicknesses and also on flat substrates. The reason for this behavior is unknown and needs to be investigated.

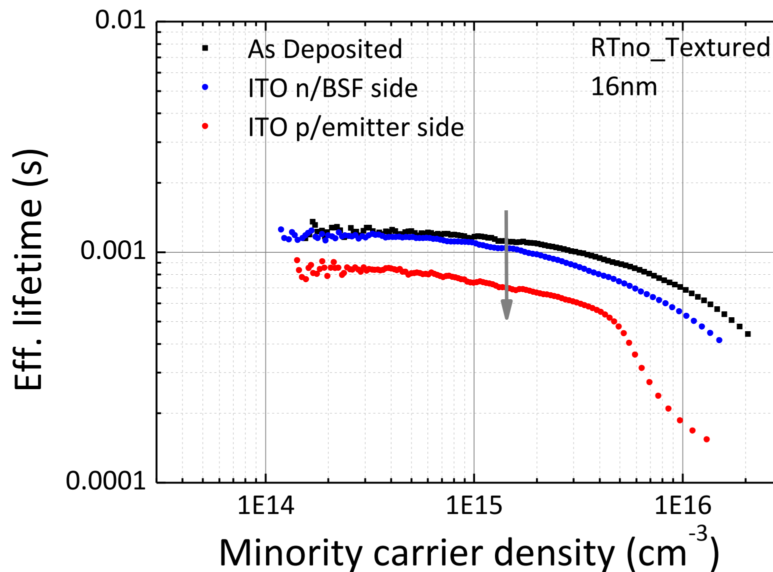


Figure 3.7 Comparison in degradation after ITO sputtering on n/BSF and p/emitter side of a textured cell precursor

Another observed phenomenon is degradation induced by the presence of p-doped a-Si:H in a silicon heterostructure. In a study of the nature of the doped a -Si : H / c -Si interface recombination, De Wolf *et al.*[28] links the dependency of the electronic surface passivation on the a-Si:H film doping to Fermi energy E_F dependent Si–H bond rupture in the films. The study showed the result obtained after depositing a purely intrinsic (i), n-doped (n^+), p-doped (p^+), i/n^+ and i/p^+ stack and then annealing and characterizing them by virtue of their lifetimes. Figure 3.8 shows the change in surface passivation quality, expressed by τ_{eff}, as a function of the described step-wise annealing treatment for, respectively, a few nanometer thin intrinsic, n^+- and p^+-doped single film a-Si:H/c-Si heterostructures. It also shows how for the a-Si:H p^+ case the presence of an intrinsic buffer layer initially results in an improving passivation quality, although at about 220 °C degradation sets in. It is asserted that doped a-Si:H/c-Si interface recombination may result from Fermi energy dependent defect generation in the passivating layer, counteracting the intentional doping. For a-Si:H films, for both types of doping, this defect is likely the amphoteric Si dangling bond, created by Si–H rupture. The effect of n^+-type doping appears to be less detrimental on the passivation properties, compared to that of p^+-type doping. Nevertheless, the study of equally thin phosphorous doped a-Si:H (n^+) films has led to even more direct proof that also for a few nanometer thin films increased doping leads to increasing defect densities. [29]

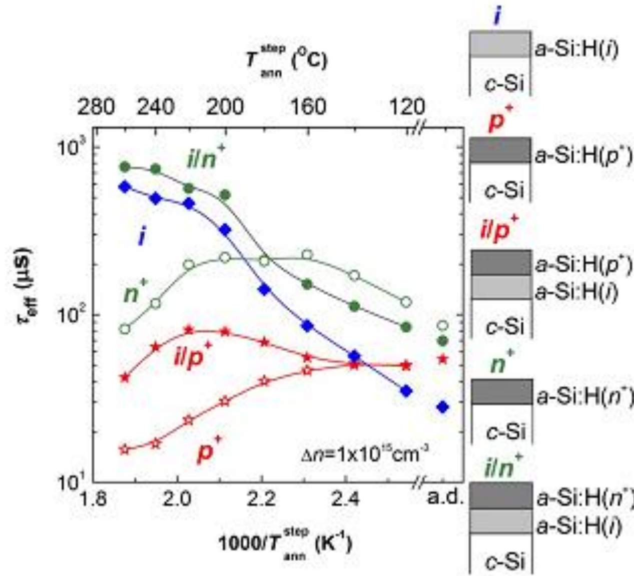
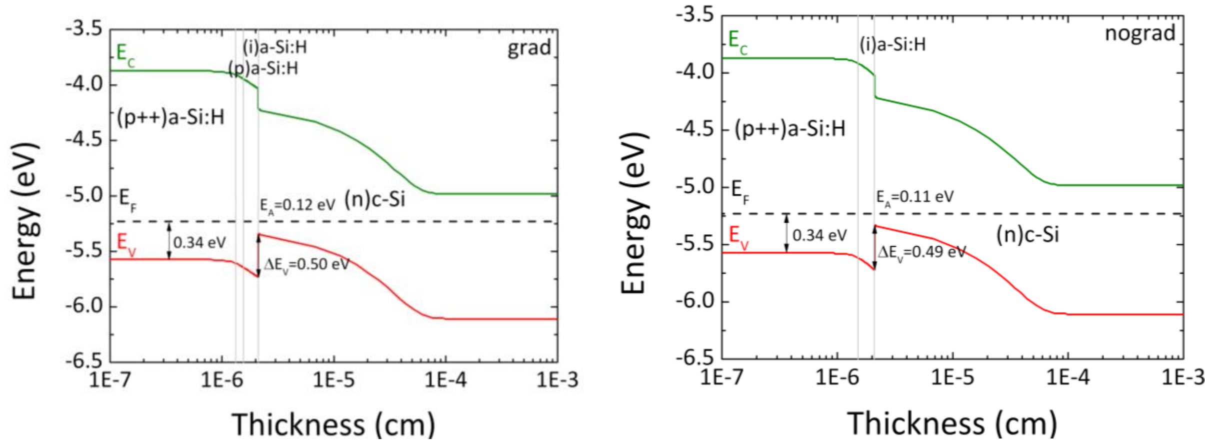
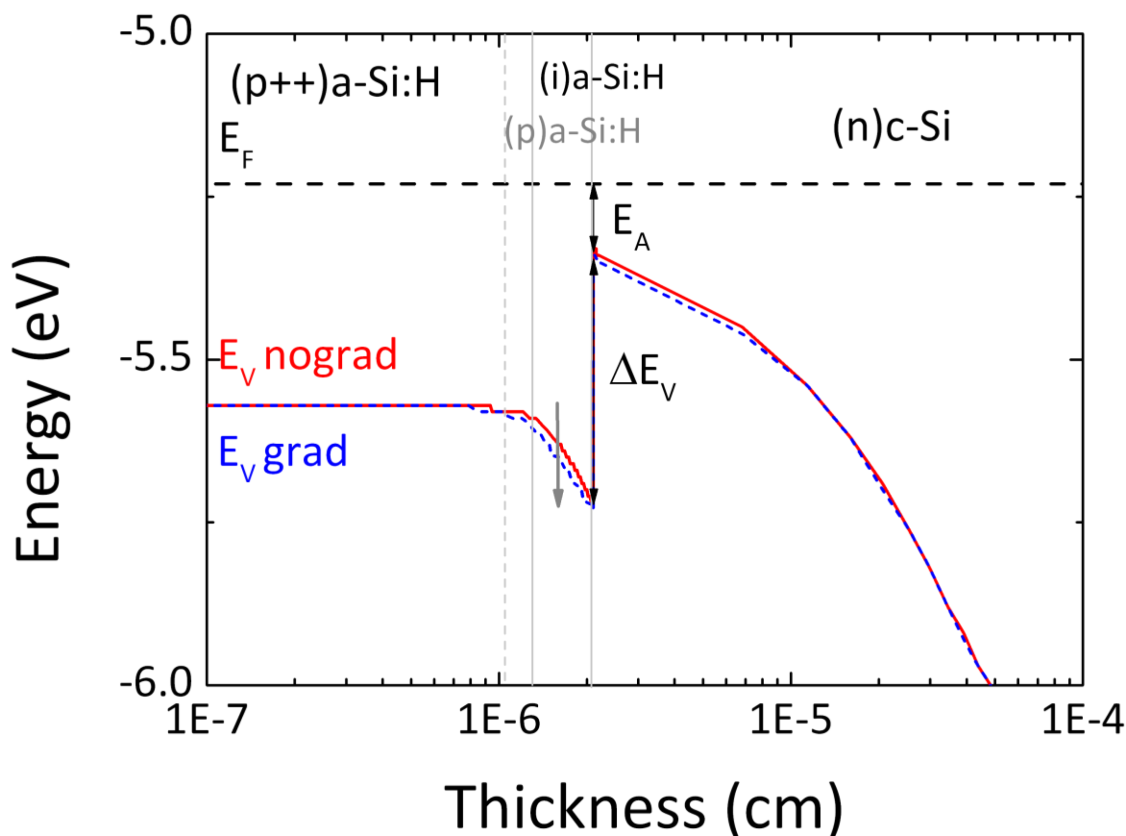


Figure 3.8 Influence of stepwise annealing treatment on the c-Si surface passivation quality, expressed by τ_{eff} (evaluated at $\Delta n=\Delta p=1.0x10^{15}$ cm^{-3}), for doped a-Si:H stacks as shown in the inset sketches. Open symbols represent doped single films, closed symbols represent stacks, featuring an intrinsic buffer layer. Results for as deposited material are indicated in the abscissa by the label a.d.- Extracted from De Wolf et al. [28]

An explanation of this observed trend can also be given using the band diagram. As already described, in the HIT cells, an intrinsic passivating layer is inserted between the (p)a-Si:H and the (n)c-Si. The presence of this thin undoped layer helps to reduce the surface defects as intrinsic a-Si:H has fewer defects states than doped a-Si:H. However, when capping the structure with a doped layer on top, defects can emerge within the bulk of the intrinsic layer. This defect creation can be understood via the band diagram of the junction formed between the (p)a-Si :H and (n)c-Si. At equilibrium, the Fermi levels of the (p) a-Si:H and (n)c-Si must align, this creates a band bending effect and also an inversion layer due to the difference in band gaps of these two materials. However, since an intrinsic layer lies between the a-Si:H/c-Si interface, for the Fermi levels to align properly, the Fermi level of the intrinsic a-si:H would appear to be shifted towards the valence band instead of crossing it at mid gap as it usually happens. Its position corresponds actually more to that of a (p)a-Si:H layer. Indeed, as can be seen in the band diagram below, E_F lies very close to the valence band, even in the intrinsic region. This shift in the Fermi level of the (i)a-Si:H causes the creation of some defects [28].



(a)



(b)

Figure 3.9 AFORS-HET simulation of a heterojunction showing (a) band diagram of a 'grad' cell and band diagram or a 'nograd' cell (b) a superimposition of 'grad' and 'nograd' showing the shift in the band level towards the valence band when a p-layer gradient is introduced

Figures 3.9a is the result of a simulation done in AFORS-HET and it shows the band diagrams for a 'nograd' and 'grad' p^+/i/n interface. After the introduction of the gradient, the height of the barrier is shifted from 0.50eV to 0.49eV, although small, we believe that this difference shifts the Fermi level of the intrinsic layer further away from the valence band. This effect

can be observed more closely in figure 3.9b where shift in the band diagram pushes the Fermi level of the i-layer closer to the center and farther away from E_V. This shift would result in less defect creation due to a highly doped p-layer hence suggesting that using a (p) a-Si:H gradient on the (i) layer is beneficial in reducing interface defects.

Keeping in mind this observation of a more severe degradation on the p-side, we optimized the precursor structure by introducing a dopant gradient in the p-layer. What this means is that the dopant concentration of the p-layer is gradually increased as it is grown over the intrinsic layer resulting in a less doped layer directing in contact with the intrinsic layer. This is done to lower the E_F related degradation just described in the intrinsic layer and it was achieved by increasing the flow rate of the dopant gas at different stages of deposition.

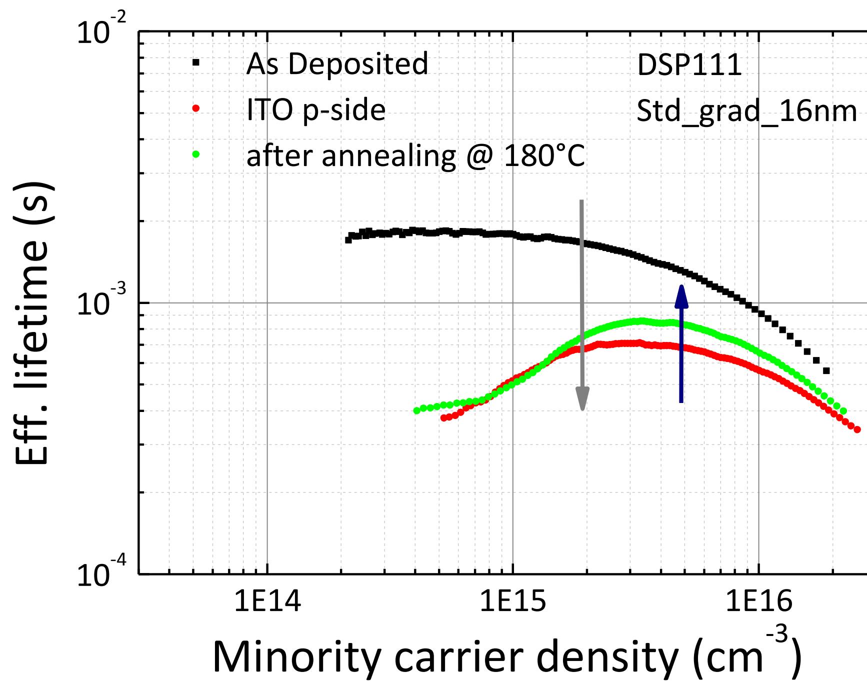
Figure 3.10 Structure of optimized standard cell precursor showing the dopant gradient

To achieve a dopant gradient in the p-layers, a Trimethylborane (TMB) flow rate of 5sccm (P_5) and 20sccm (P_{20}) were used respectively for the two regions of varying doping levels. The resulting conductivity was found to be σ_{p5}=9.52x10$^{-6}\Omega^{-1}$.m^{-1} and σ_{p20}=1.54x10$^{-4}\Omega^{-1}$.m^{-1}. The final structure of the optimized precursor is shown in figure 3.10. Theoretically, we believe that introducing this gradient in the cell structure might lead not only to a higher passivation by reducing the defect density in the intrinsic layer but also that it will lead to a lesser degradation. This needs to be validated by repeating the tests done on the standard "no gradient" precursor.

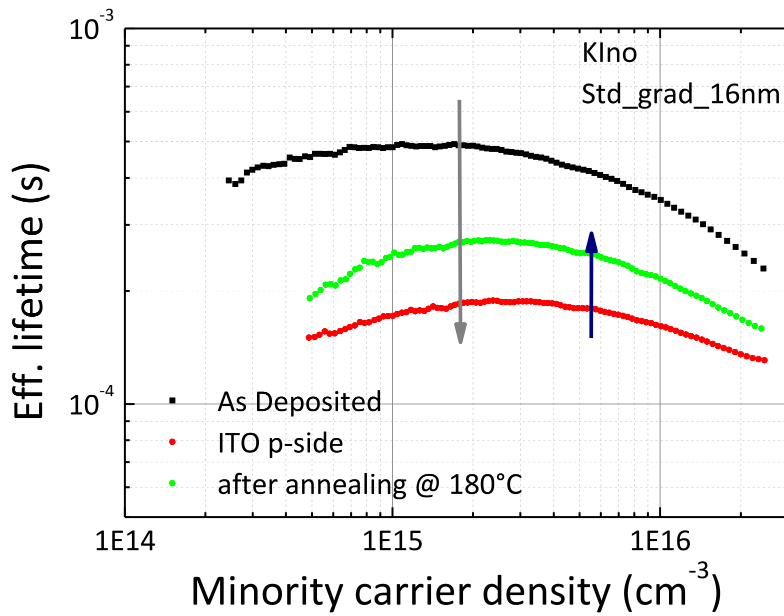
3.4.1 ITO Induced Degradation on Optimized 'Grad' Precursors

3.4.1.1 Optimized Standard Precursor

The extent of degradation induced by the sputtering of ITO over the precursor is evaluated using the lifetime measurements as before. The precursors were subjected to a heat treatment process by annealing at 180°C in N_2/H_2. As aforementioned, this annealing step is done in an attempt to recover some of the passivation lost during the sputtering of ITO on the precursor. The annealing of the samples can help to reduce the interface traps at the amorphous-silicon/crystalline-silicon[26][27]. We expect that the optimized cell precursors with a dopant gradient would exhibit a better response to the heat treatment step than its "nograd" counterpart based on the fact that the p-type doping is chiefly responsible for degradation in the cells (see section 3.4)[29].



(a)



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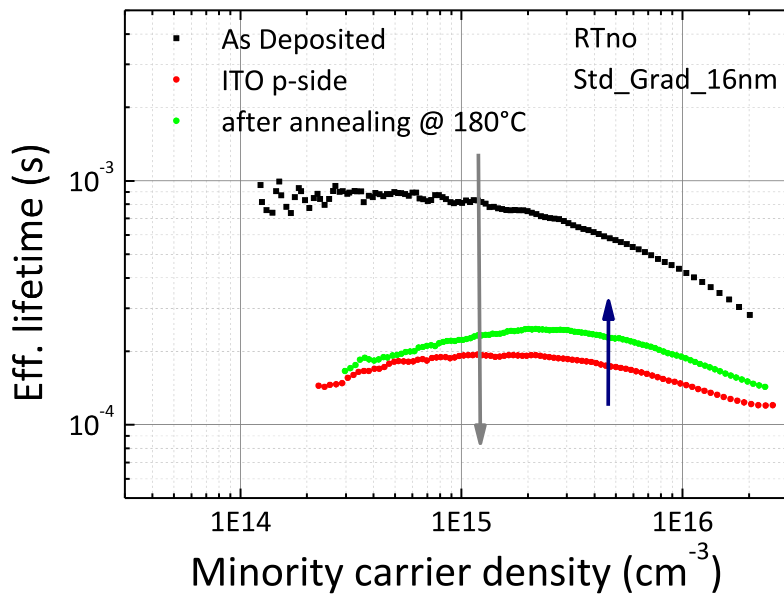
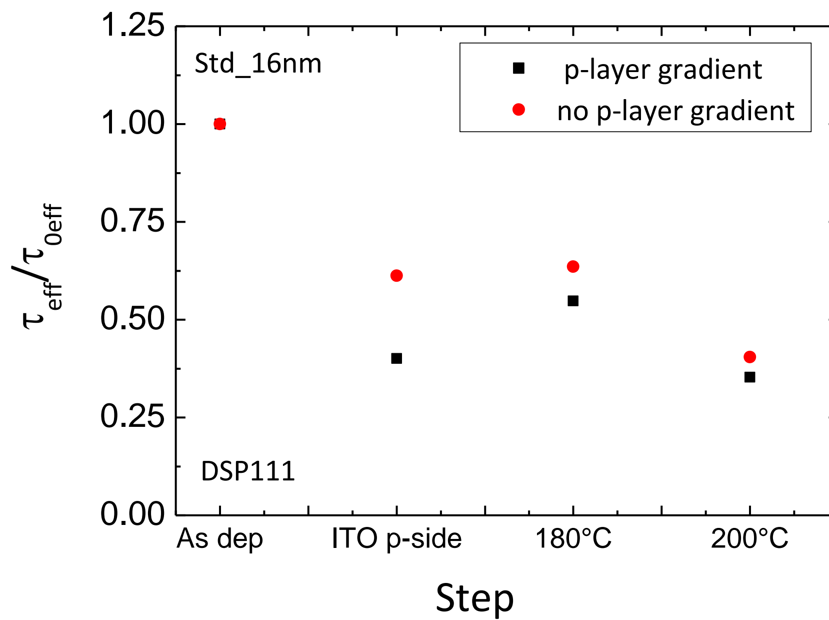


(c)

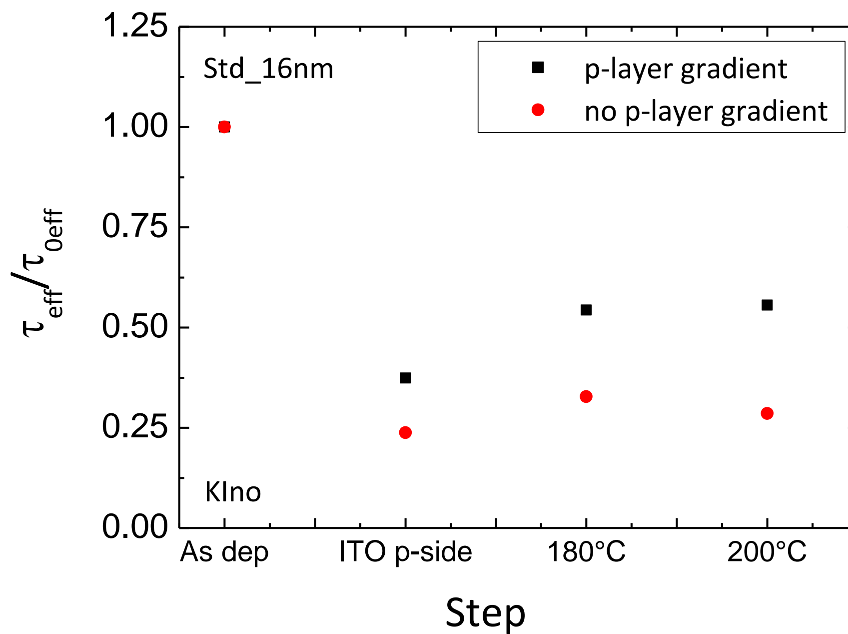
Figure 3.11 Effective lifetime measurements of optimized p-layer gradient cell precursors (a) a flat DSP111 (b) KIno textured (c) RTno textured after annealing at 180°C

A careful observation of the curves in figure 3.11 showed a measureable degree of improvement in the lifetimes of the cell precursor after annealing at 180°C for 30 minutes which points to a recovery of the passivation lost after ITO was sputtered on the precursors. The lifetime for the flat cell increases from 697µs after degradation to 850µs after annealing.

The textured samples also showed some improvements with the KIno textured substrate increasing from 185µs to 270µs and the RTno sample increasing from 191µs to 244µs after annealing. The values of the lifetimes were measured at a minority carrier density of 2.0x10^{16} cm^{-3}. It is evident that introducing a dopant gradient in the cell precursors yields some beneficial characteristics in the samples which make it more responsive to heat treatment as compared to its standard “nograd” counterpart.



(a)



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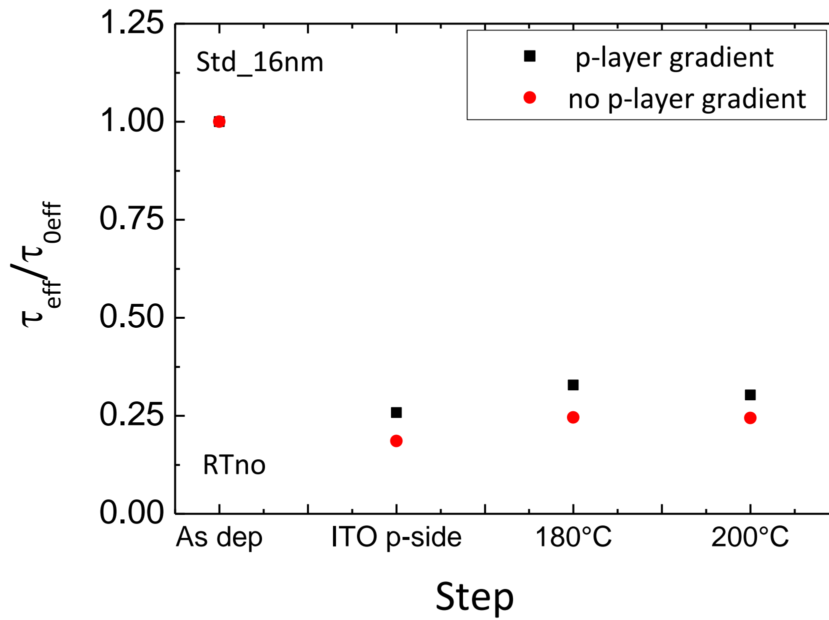


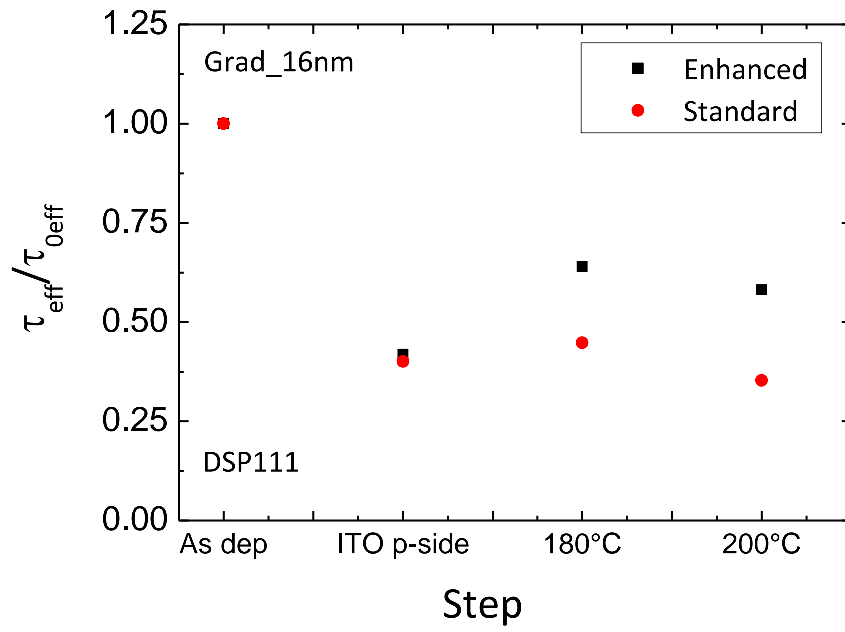
(c)

Figure 3.12 Normalized lifetime plots comparing "Grad" and "noGrad" precursors (a) a flat DSP111 (b) KIno textured (c) RTno textured after annealing at 180°C

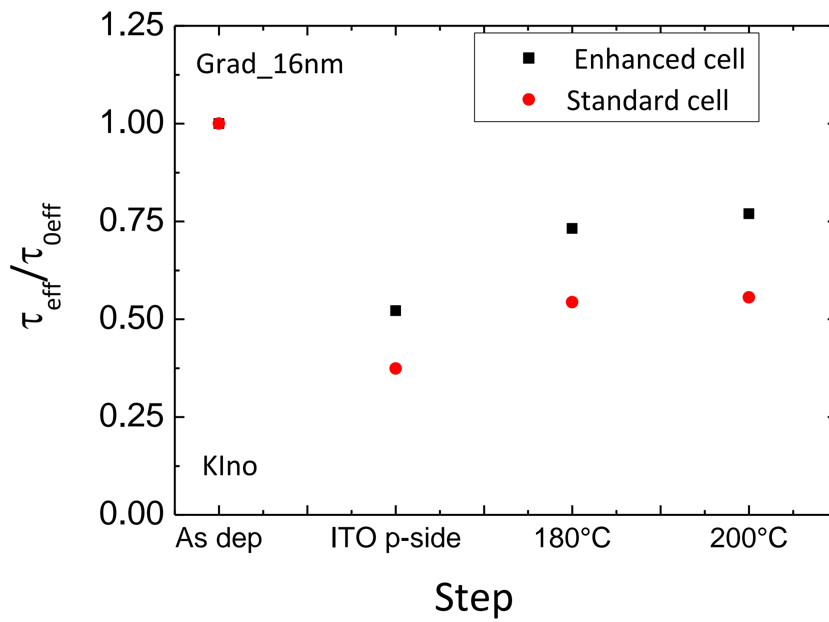
Figures 3.12a, b and c gives a visual representation of the degree of damage and recovery experienced by both types of precursors (nograd vs grad), where we show a normalized plot of the lifetimes before ITO sputtering, after ITO and after annealing at 180°C. In the case of the DSP111 Flat cell precursor, although the lifetime of the 'Grad' sample is lower than the 'noGrad', the 'Grad' sample showed an improvement in its lifetime after annealing which is in contrast to the 'nograd' sample. The RTno and KIno textured 'Grad' samples on the other hand showed better improvement margins as compared to the 'nograd' samples. The RTno precursor with a p-layer gradient rose to 32% as compared to only 24% for that without a p-layer gradient while in the KIno precursor, the 'grad' sample rose to 54% as compared to 33% for the 'nograd' sample. This points to the benefit of introducing a p-layer gradient.

3.4.1.2 Enhanced Precursor

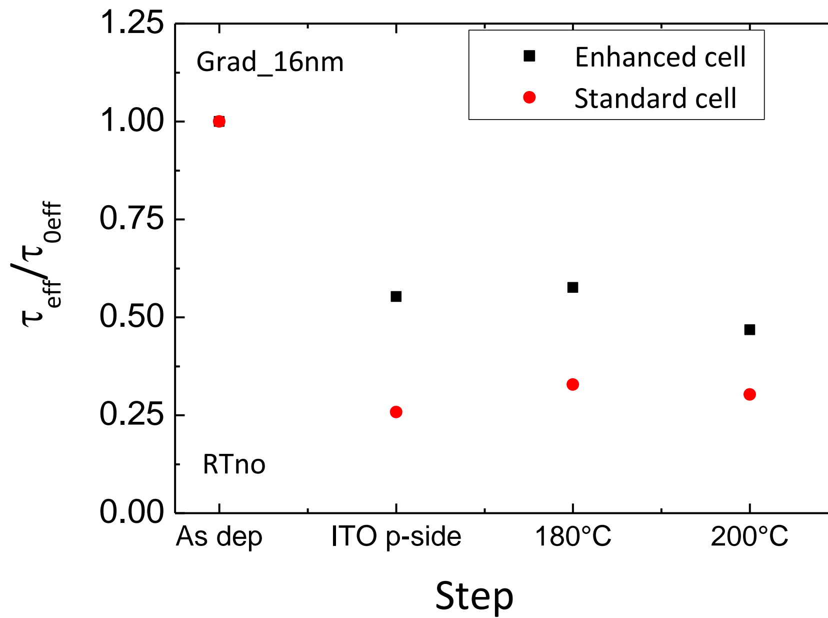
Taking our experiments a notch further, we attempt to introduce some enhancements in the precursor recipe. The intent of this enhancement is to reduce the surface imperfections that arise upon wet-etching process and can affect the passivation level of the precursors. Details of this enhancement cannot be included in this report at the moment because it is a pending patent.



(a)



(b)



(c)

Figure 3.13 Normalized lifetime plots comparing Enhanced and standard precursors (a) a flat DSP111 (b) KIno textured (c) RTno textured after annealing at 180°C

Notwithstanding, we show the results obtained from comparing the enhanced “Grad” precursors with the standard “Grad” represented by their normalized lifetime plots. The stats show that enhanced “Grad” flat (DSP111) precursor improved to 64% of its initial “as dep” value while compared to 44% for the standard optimized (grad) precursor after being annealed at 180°C. The same trend is observed in the RTno textured sample with the enhanced “grad” precursor reaching 57% as compared to 32% for the standard “grad” precursor in the RTno sample while in the KIno sample, the enhanced precursor reached 73% of its original value as against 54% for the standard precursor after annealing at 180°C. All the samples showed no further improvements in passivation when annealed at 200°C. An exception is the KIno enhanced precursor which improved from 73% to 77% after annealing at 200°C. It appears that the temperature threshold at which we can expect to see improvements after annealing lies around 180°C.

So far, we have demonstrated within the limits of our experiments that introducing a dopant gradient to the structure of the cell precursors can play a role in mitigating the damage done by ITO sputtering during the fabrication process of the precursors. We have also shown that altering the composition of the precursors by adding some enhancement can yield further beneficial properties which we have demonstrated to lead some recovery of the passivation lost during sputtering. It would be good to see the impact of the optimization and enhancement on finished solar cells. This will be discussed in the next Chapter.

Chapter 4
Performance of finished HIT solar cells

In the preceding chapter, we established from the outcomes of the lifetime measurements of cell precursors that introducing a p-layer gradient in the structure of the precursor had some beneficial effects. These effects include a higher resilience to degradation after ITO sputtering and a better passivation recovery after annealing as compared to its "nograd" counterpart. In this chapter, we study the effects of these tweaks on the properties exhibited by full HIT cells. The J-V curves were generated at an illumination of 1 sun, AM 1.5 using the Oriel solar Simulator equipment. The cells were kept at a constant temperature of 25°C using a temperature controlled measuring platform. It is important to state at this point that the measurement of the J-V curves was done with a 2cmx2cm opaque mask corresponding to the size of the cell (4cm²) in order to avoid lateral collection of current. The cell area, defined by the ITO is 4cm² but since the cell is made on a wafer with an area large than 4cm², carriers could be generated in the areas not covered by the ITO and outside the cell region. These extra carriers could lead to an over-estimation of the current and an underestimation of the Fill Factor(FF)[30] as seen in figure 4.1.

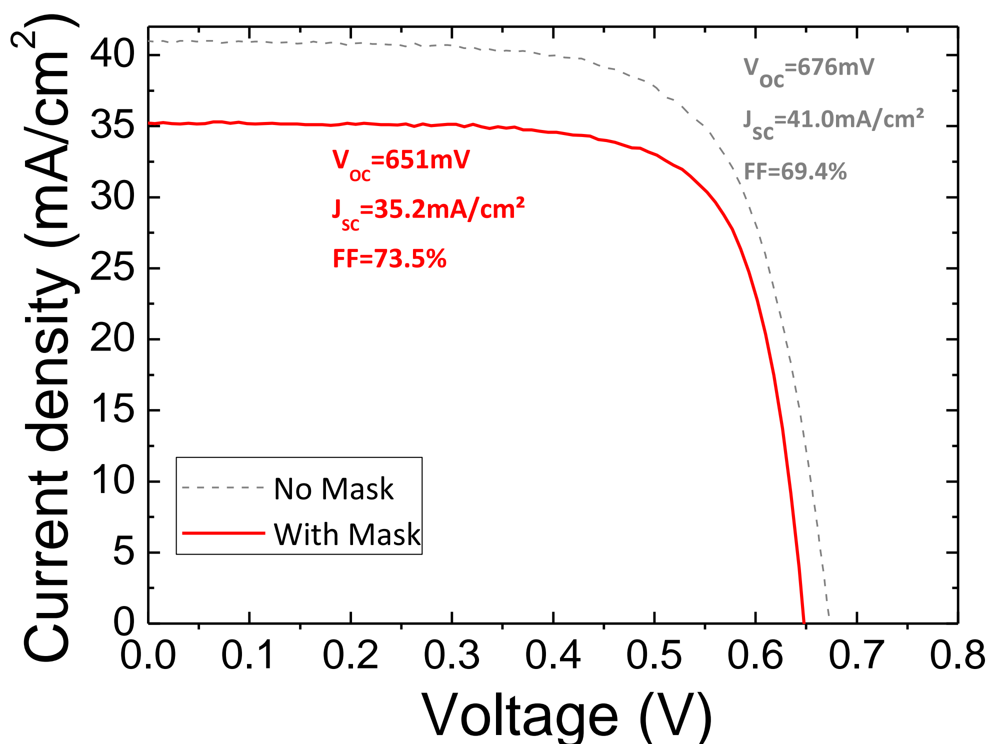


Figure 4.1 J-V characteristic curve of a 4cm2 solar cell measured with and without a mask

4.1 Impact of p-layer Gradient on the Performance of Standard DSP111 Cells

Our goal now is to study the effect on the cell properties when we optimize our standard DSP 111 cell by introducing a p-layer gradient as we did in chapter 3. Table 4.1 describes the cell architecture of all cells discussed herein.

Contact	TCO	Emitter (a-Si:H)	Absorber (c-Si)	BSF (a-Si:H)
Ag	ITO	(i) / 5nm	(n)	(i) / 5nm
800nm	80nm	(p+) / 16nm (grad or nograd)	280µm	(n+) / 25nm

Table 4.1Summary of cell architecture

It should be noted that only the p-layer is varied (grad or nograd), all the other components are kept constant throughout the experiments.

4.1.1 Cell properties in the 'as dep' state

We study these properties by characterizing the illuminated and dark J-V properties of the cell. The cells have been completed by evaporating the metallic silver contacts on both sides. To compare the effect of the p-layer gradient, we chose a 16nm flat DSP111 cell which has a very good passivation and lifetime values of 1.7ms with an implied V_{OC} of 705mV and 1.0ms with an implied V_{OC} of 687mV for the grad and nograd cells respectively as seen in figure 4.2

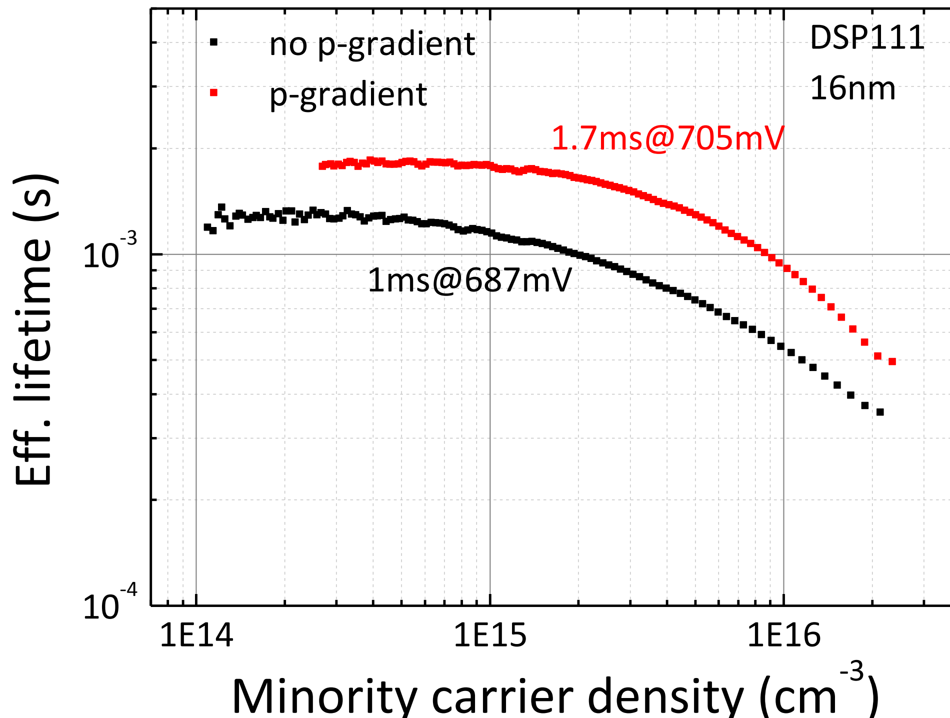


Figure 4.2 Lifetime curves of a well passivated flat DSP111 precursor

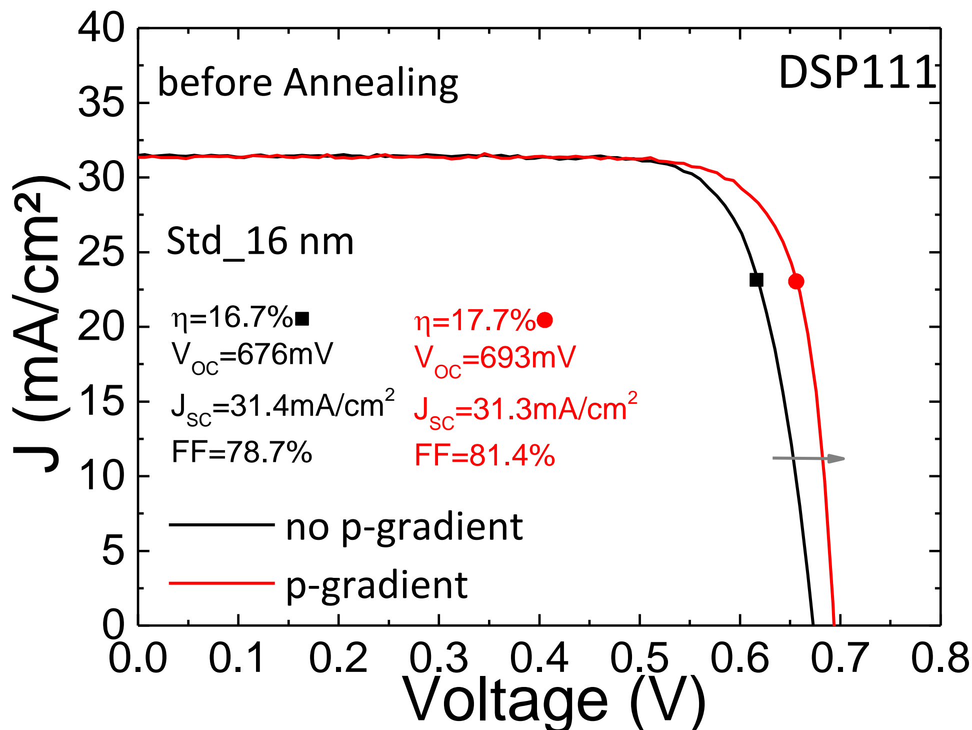


Figure 4.3 J-V characteristic curves comparing a p-layer 'grad' cell with a 'nograd' cell before annealing

Figure 4.3 shows a plot of the light J-V characteristics of the grad and nograd standard cells. As expected, the grad cell which has a better passivation displayed a higher V_{OC} of 693mV as compared to 676mV for the nograd cell. The higher V_{OC} in the grad cell is attributed to a reduced interface defect density caused by introducing a p-layer dopant gradient to effectively decrease the damage caused by p-type doping as described in section 3.4. At the same time, this reduced defect density allows for an improved collection of generated charges and thus we obtain a very high fill factor of 81.4% in the grad cell and 78.7% for the nograd cell. The short circuit current for both cells is similar with a value of 31.4mA/cm^2 and 31.3mA/cm^2 for the nograd and grad cells respectively. These properties ultimately lead to a higher conversion efficiency of the grad cell which stands at 17.7% before being annealed. The nograd cell comes in second place with an efficiency of 16.7%.

4.1.2 Cell properties after annealing

Figure 4.4 illustrates the J-V curve of standard grad and nograd cells after they have been annealed in an N_2/H_2 at a temperature of 180°C. A close observation would reveal a spike in the FF of the grad cell from 81.4% to 82.1%. This increase in the FF points to an improved transport across the interface and a better collection of charges, indeed, it has been shown that a significant decrease in the interface trap density leads to higher fill factors and V_{OC} [31]. We also note that the V_{OC} remained constant for both cells after annealing but the grad cell gained 0.3mA/cm^2 after annealing while its nograd counterpart added only 0.1mA/cm^2 in the J_{SC}. Overall, the increase in the FF and J_{SC} of the grad cell resulted in an efficiency of

18.0% which is higher than the nograd cell which stayed constant at 16.7% even after annealing.

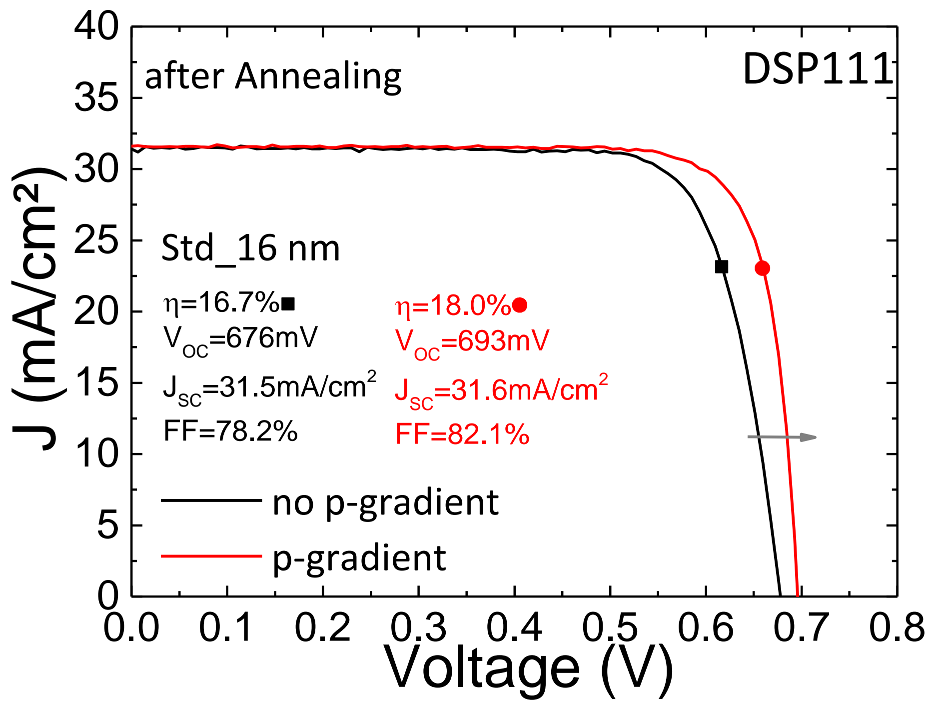
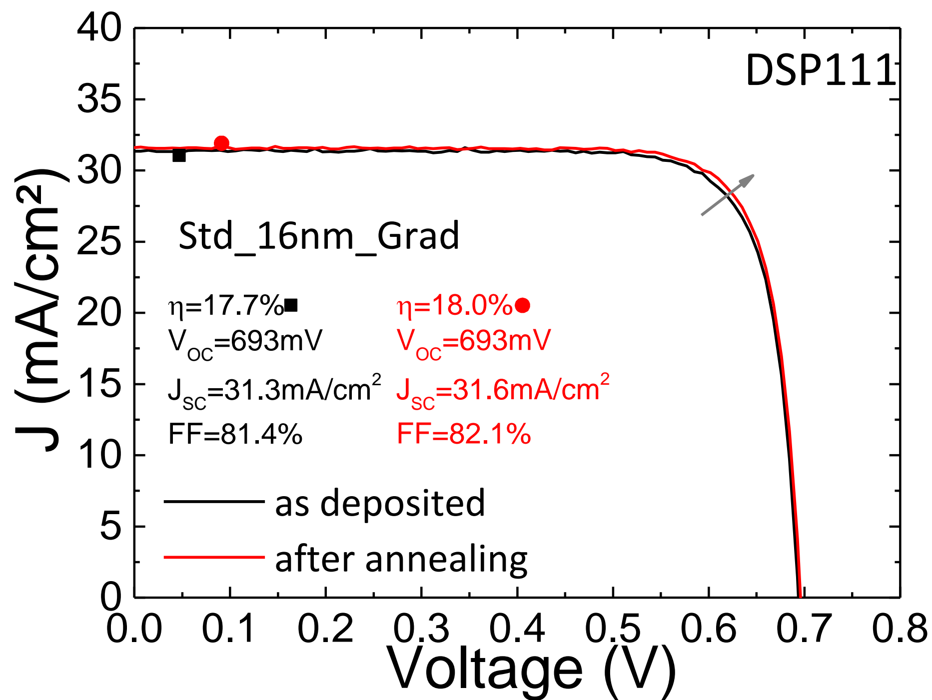
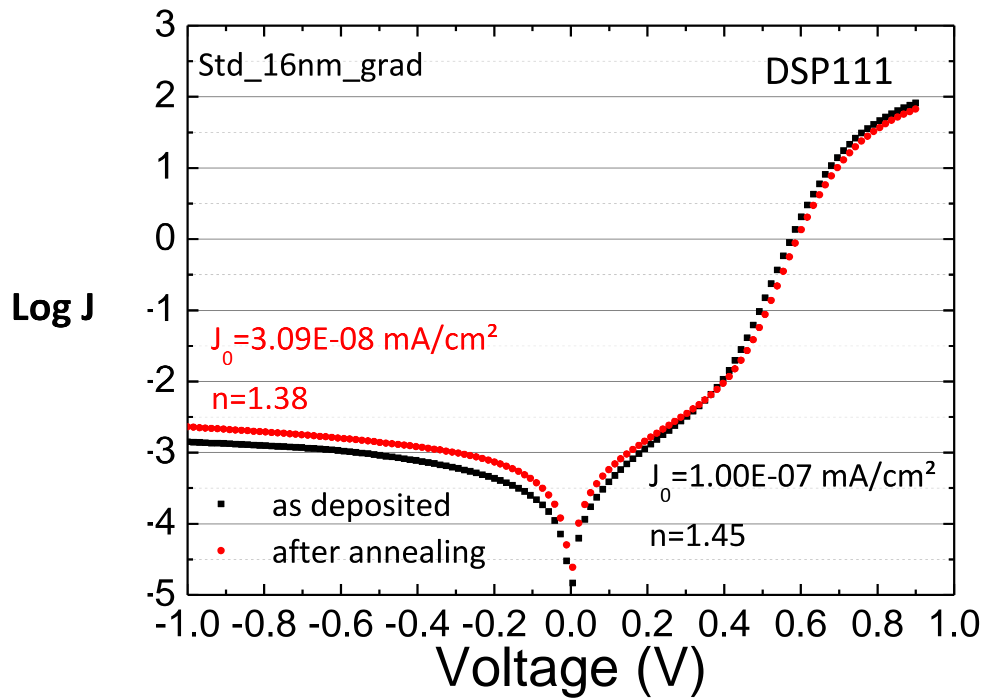


Figure 4.4 J-V characteristic curves comparing a p-layer 'grad' cell with a 'nograd' cell after annealing



(a)



(b)

Figure 4.5 Cell characteristics showing (a)light J-V curve before and after annealing (b)dark J-V before and after annealing for the 'grad' cell

The above results show that the p-layer gradient is beneficial to the properties of the cell. In the as deposited cells, the cell that had a p-layer gradient displayed superior qualities. After annealing, the cell with the gradient again showed a better response to the heat treatment step. Figures 4.5a and 4.5b show how the grad cell responds to annealing. The dark J-V curve reveals that the dark saturation current drops from 1.00E-7mA/cm² to 3.09E-08mA/cm² after annealing and its ideality factor also improved from n=1.45 to n=1.38. The fill factor also improves as well as the efficiency which reaches 18.0%, however, there was no increase in the V_{oc} of the cell. A summary of these values can be seen in table 4.1 below. So it appears that introducing a gradient improved the quality of the cell and makes it more responsive to the heat treatment step.

Cell	J_{SC} (mA/cm^2)	V_{OC} (V)	FF (%)	Efficiency (%)
Std_nograd_bA	31.4	676	78.7	16.7
Std_nograd_aA	31.5	676	78.2	16.7
Std_grad_bA	31.3	693	81.4	17.7
Std_grad_aA	31.6	693	82.1	18.0

Table 4.2 Summary of cell properties of the 'grad' and 'nograd' cells before and after annealing

4.2 Impact of p-layer Gradient on the Performance of an enhanced textured solar cell

4.2.1 Cell properties in the 'as dep 'state

The enhanced cell precursor, introduced in chapter 3 is also characterized to evaluate it impact on the cell properties and whether it is beneficial or not. Due to IP rights, the composition of this cell will not be described in detail, however, we note that the goal of this enhancement step is to provide a better passivation and reduction in the interface defect densities. It is hoped that this enhanced will yield higher V_{OC} and better cell efficiencies. In section 4.1, the p-layer gradient proved beneficial to the overall cell properties with the experiments done on the flat DSP111 substrates. Bearing this in mind, we make enhanced cells also with this p-layer gradient. But for this, we use RTno textured substrates as we have observed that we can get higher I_{SC} on textured substrate than on flat substrates primarily due to the light-trapping properties of textured substrates. High quality intrinsic a-Si:H along with this enhancement provides the needed passivation.

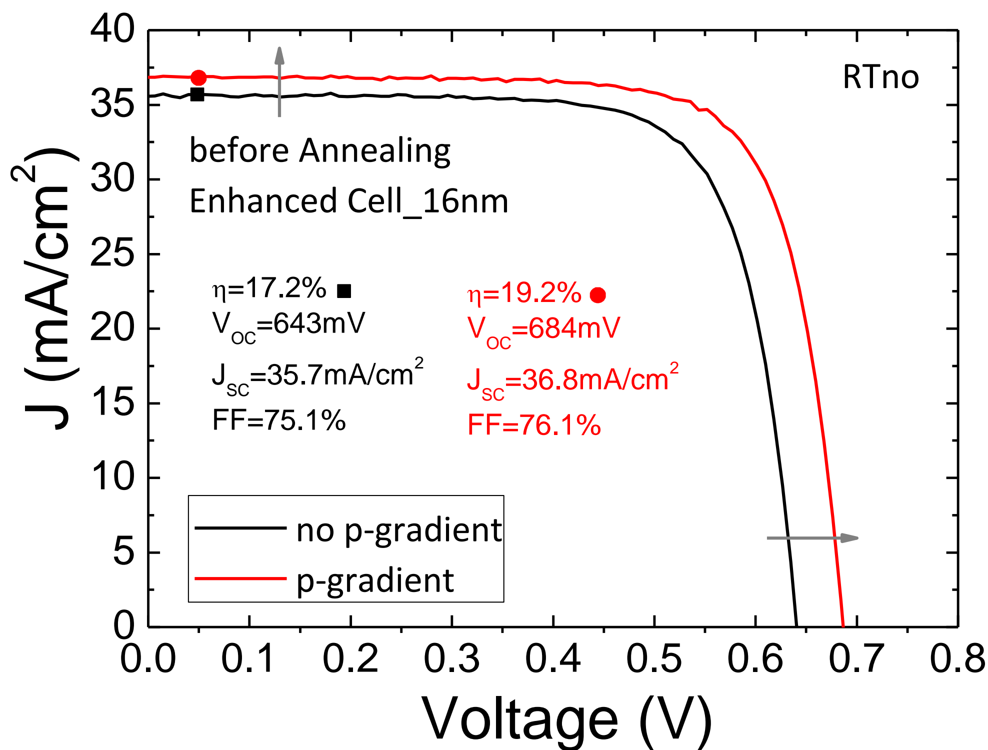


Figure 4.6 J-V characteristic curves comparing the enhanced 'grad' and 'nograd' cell before annealing

The J-V curve in figure 4.6 shows the sharp contrast and superior properties of the 'grad' cell over the 'nograd' cell. The enhanced 'grad' cell has a V_{oc} of 684mV compared to 643mV for the 'nograd' cell before annealing pointing a reduced recombination at the interface and hence a good passivation in the enhanced cell. The 'grad' cell exhibits a higher short circuit

current of 36.8mA/cm² and fill factor of 76.1%. This further strengthens our argument of the advantage of a p-layer gradient.

4.2.2 Cell properties after annealing

To further improve the measured properties of the cell, we anneal both cells and compare their properties once again. The improvement by each cell before and after annealing is evaluated to see the effect of heat treatment on the cell performance.

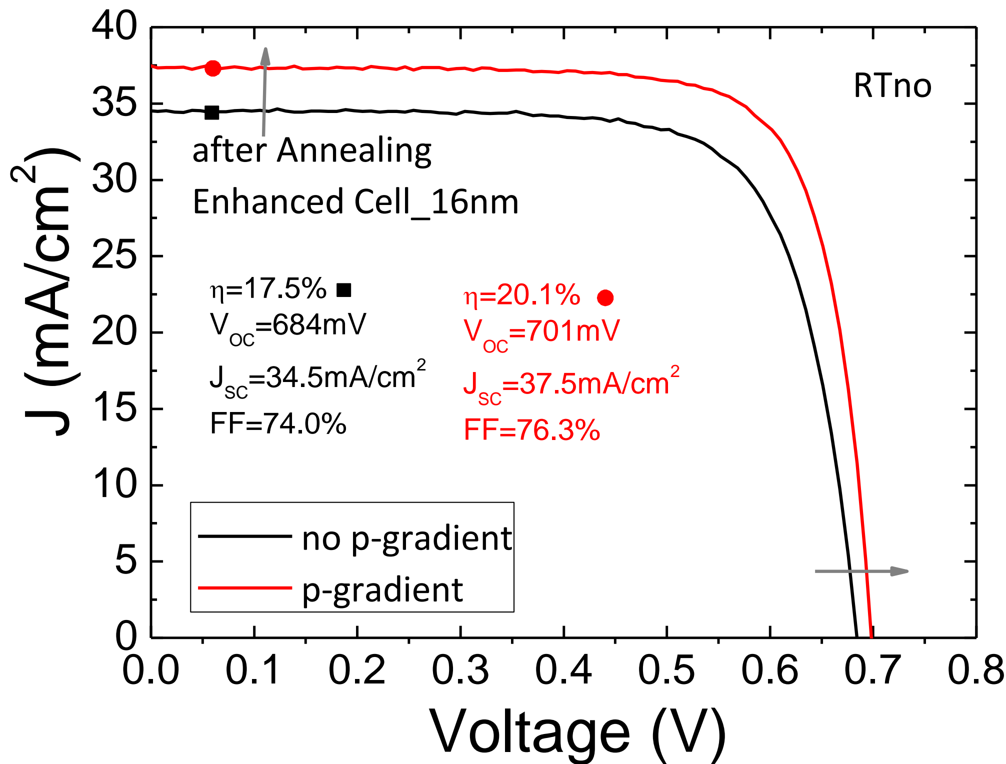


Figure 4.7 J-V characteristic curves comparing the enhanced 'grad' cell and the standard 'grad' cell after annealing

After annealing the cells, we notice an increase in the V_{OC}, efficiency and J_{SC} of the enhanced cell as seen in figure 4.7. It is noteworthy to state that this is the highest efficiency encountered in the course of this work. The 'grad' cell broke the 20% efficiency barrier to reach 20.1% after annealing along with a high V_{OC} of 701mV. It appears that this annealing step healed some defects within the heterostructure leading to an even better passivation. The current also increases to reach 37.5mA/cm². This increase in the current could be attributed due to an increased transparency and conductivity of the ITO layer[22]. The properties displayed by this 'grad' cell far outweigh any improvement seen in the 'nograd' cell although the annealing step also brought some improvements in the latter especially in the V_{oc}. The V_{oc} increases from 643mV to 684mV while the efficiency reached 17.5%. The current drops from 35.7mA/cm² to 34.5mA/cm², this drop is balanced by the increase in the V_{oc} which ultimately led to a little increase in the efficiency. Table 4.2 summarizes the

properties stated above and gives a highlight of the individual properties of the cells under examination.

Cell	J_{SC} (mA/cm^2)	V_{OC} (V)	FF (%)	Efficiency (%)
Enhanced_nograd_bA	35.7	643	75.1	17.2
Enhanced_nograd_aA	34.5	684	74.0	17.5
Enhanced_grad_bA	36.8	684	76.1	19.2
Enhanced_grad_aA	37.5	701	76.3	20.1

Table 4.3 Summary of cell properties of the enhanced and standard 'grad' cells before and after annealing

It is interesting to see the difference in V_{oc} for both cells, the grad cell leads with a V_{oc} of 701mV which is about 100mV more than the 'nograd' cell.

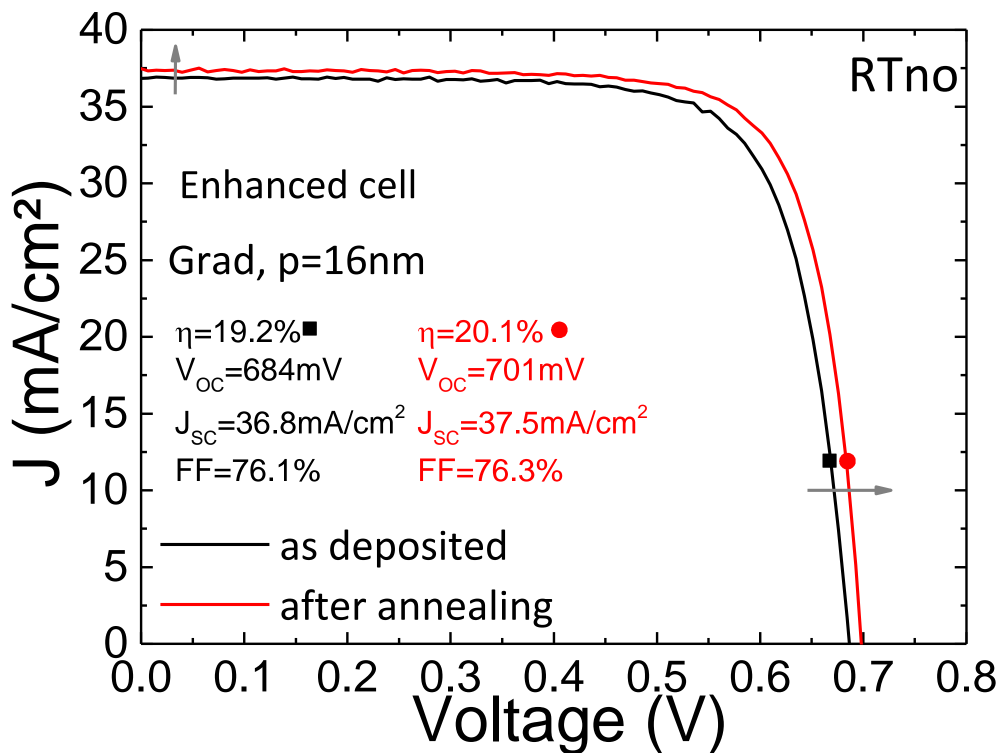


Figure 4.8 J-V characteristic curves showing improvements in the properties of the enhanced 'grad'

Figure 4.8 is a comparison of the enhanced grad cell in its annealed state to its as deposited state showing the improvements experienced after the heat treatment step.

The results obtained so far from the analysis of the 'grad' and 'nograd' are consistent with the results obtained in chapter 3 which further buttresses our argument that introducing a p-layer gradient is beneficial for the cell properties. With an enhanced recipe featuring a p-layer gradient emitter, we were able to reach an efficiency of 20.1% with a V_{OC} of 701mV. We believe that we can reach higher efficiencies by introducing further optimizations in the fabrication process and/or recipe of the precursors.

Conclusion

a-Si:H/c-Si solar cells have been successfully fabricated using the chain process described in chapter 2. This procedure took into consideration the wet-etching and cleaning processes that were done to ensure very good chemical passivation of the (n) c-Si wafer surfaces. PECVD is the method of choice for the deposition of the amorphous layers while the ITO and silver contacts were deposited using the sputtering and evaporation processes respectively.

The effective lifetimes as measured by the WCT-120 Sinton lifetime tester was used to characterize the passivation levels in the cell precursors. It has been shown that the p-type dopant induces a higher degradation as compared to the n-type dopant. To effectively reduce the effect of this phenomenon, a p-layer gradient was introduced in the cell precursor structure. The results showed that the grad was beneficial for both the flat and textured precursors.

Since the optimization done on the cell precursor gave positive results, we sought to study the impact on finished cells. The illuminated J-V properties were measured using the Oriel solar simulator at 1 sun, AM 1.5. Using the optimized chain fabrication procedure and incorporating a p-layer gradient enhanced recipe in our champion cell, we were able to reach a cell efficiency of 20.1% at a V_{OC} of 701mV, I_{SC} of 37.5mA/cm² and FF of 76.3% after annealing the cell in N_2/H_2 at 180°C for 30 minutes. This result was realized for a textured substrate which point to a high level of passivation of the dangling bonds at the surface of the c-Si.

We also conclude from the outcomes of our experiments that annealing is beneficial for passivation if done below a temperature threshold. Above this temperature threshold, further heat treatment would prove detrimental to the passivation of the cell precursor.

Research work on the passivation and optimization of HIT cell recipes and/or fabrication is far from over. The next step which we propose is to investigate new materials and deposition techniques that possess the potential to realize even better passivated precursors which ultimately would lead to higher cell efficiencies.

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