Impact of Emitter Dopant Gradient on Amorphous/Crystalline Silicon Heterjunction Cell Performance

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Abstract

The HIT (Heterojunction with Intrinsic layer) cell features a very thin layer of intrinsic a-Si:H inserted between p-type a-Si:H and n-type c-Si. This structure was originally investigated for a low temperature junction fabrication technique for a thin film poly-Si or nc-Si solar cell. The emitter is composed of a very thin intrinsic a-Si:H layer capped by p-type a-Si:H. The absorber is thick n-type c-Si wafer and the BSF is made of a thin undoped a-Si:H capped by n-type a-Si. ITO is sputtered on the front and back sides of the cell and it acts as both an anti-reflection coating and a transparent conducting electrode to enhance the collection of carriers. The objective of this thesis is to investigate the influence of cell recipes on the passivation, degradation and performance of the cell. The cell was fabricated using the PECVD deposition method; the standard cell has no p-layer gradient while in the optimized cell a p-layer gradient is introduced in the cell structure. The passivation is characterized by photoconductance lifetime measurements. The finished cells are annealed and characterized to evaluate their efficiency and overall performance and a comparison is made between cells with a p-layer gradient and without a p-layerr gradient. The cells are then enhanced by introducing some material which improves its passivation, further annealing steps proved beneficial to the cell properties. An interesting outcome is the high V_{OC} and efficiency achieved in the enhanced, annealed p-layer gradient cells as compared to the standard, no p-layer gradient cell. The results prove that the presence of an emitter layer gradient is beneficial for a-Si:H/c-Si heterojunction solar cells.

1. Introduction

Since the emergence of photovoltaic technology and its potential for energy production, global R&D effort has been aimed at developing new types of PV cells and at the same time trying to increase the conversion efficiencies of existing solar cells. The National Renewable Laboratory (NREL) in the United States releases periodically a detailed chart featuring the best cell efficiencies obtained at research level. The record efficiency for crystalline silicon heterostructures which is the focus of this report is 25.6%. The Solar electric energy demand has grown by an average 30% per annum over the past 20 years against a backdrop of rapidly declining costs and prices. This decline in cost has been driven by economies of manufacturing scale, manufacturing technology improvements, and the increasing efficiency of solar cells[1]. PV installations worldwide grew to 7.3 GW in 2009, up 20% from the prior year. Expected to reach 8.4-13.1 GW in 2010, the various forecast scenarios predict demand rising to 15.4-37 GW in 2014, more than five times the size of the 2009 market.

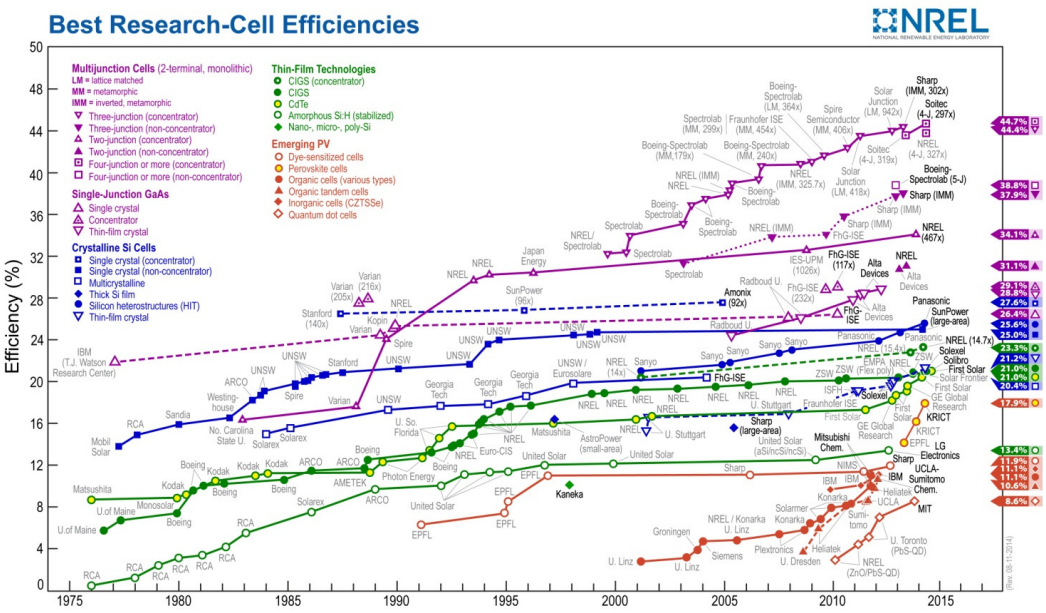


Figure 1 Best cell efficiencies chart compiled by the National Renewable laboratory (Source: NREL)[2]

The Photoelectric effect is the generation of charge carrier when particles called photon is incident on a material. In photovoltaics, the incident photons induce the creation of an electron-hole pair which can flow through an external circuit thereby producing electricity. To describe this mechanism more formally, it is best to think of light in terms of a stream of photons where each photon carries one quantum of energy. Each photon is associated with just one wavelength or frequency. High-frequency photons have more energy than the ones with low frequency. As mentioned before, a heterojunction solar cell is made of two materials with different bandgaps. A consequence of this is a bandgap mismatch hence making it impossible to have the conduction and valence band edge levels continuous through the junction. Figure 2 demonstrates the band structure of a heterojunction a-Si:H/c-Si solar cell as is generally accepted [3][4]. ΔE_C and ΔE_V represents the conduction and valence band offsets respectively. Considering the back side of the cell, the large valence band offset at the (n^+) a-Si:H interface provides a very good mirror and serves as a barrier to the flow of minority holes whereas, the flow of majority electrons from the (n) c-Si to the (n^+) a-Si:H is relatively unhindered as the conduction band offset is quite small. Thus the (i/n^+)a-Si:H provides an excellent back surface field (BSF) with adequate majority carrier electron transport/good passivation repelling minority holes from the back contact. The ohmic contact on the back side of the BSF does not hinder electron collection, hence is not a problem

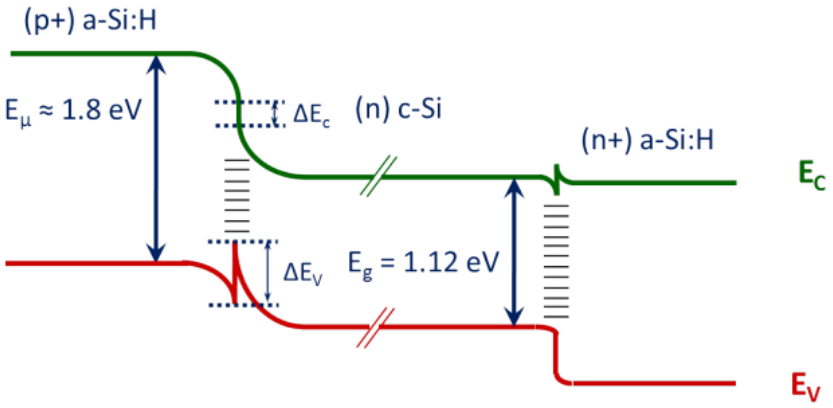


Figure 2 Band diagram of a (p+) a-Si:H/(n) c-Si/(n+) a-Si:H heterojunction solar cell

On the front side of the cell, we have a large valence band offset which represents a barrier which holes generated in the (n) c-Si absorber would have to cross in order to get to the (p^+) a-Si:H and be collected. This barrier is undesirable as an effective minority hole transport is required in this region. Pure thermionic emission is unlikely to provide enough transport for the holes due to the high barrier. However, the trapped holes may be able to tunnel across the thin a-Si:H(i) layer into the a-Si(p) layer, possibly with some thermal and trap assistance [5].

2. Experimental

The amorphous layers of the cell were deposited by low-temperature PECVD, the deposition of ITO was done by sputtering which is a Physical Vapor Deposition (PVD) process at 180°C and the silver contacts were added by the evaporation method. The fabrication steps consist of:

- A standard intrinsic amorphous silicon layer with a thickness of 5nm
- A standard n-doped amorphous silicon layer deposited at 200°C. Its conductivity reaches 2.42E-02 Ω-1·cm-1. The deposition parameter for this layer is summarized in table 1 below

SiH4 [sccm]	PH3 (1% in H2) [sccm]	Time [s]	Pressure [mTorr]	Power [W]	Thickness [nm]
50	1	360	60	1	15

Table 1

- A standard p-doped amorphous silicon layer with a conductivity of 1.54E-04 Ω-1·cm-1 with deposition parameters summarized in table 2

SiH4 [sccm]	TMB (1% in H2) [sccm]	Time [s]	Pressure [mTorr]	Power [W]	Thickness [nm]
50	20	200	110	1	16

Table 2

- An ITO layer of approximately 82 nm deposited by sputtering on both sides of solar cell precursor. The n-side was fully covered by the TCO whereas for the p-side, the wafer was cleaved to obtain a quarter of wafer, and a 2x2 cm² mask was used to avoid any measurement inaccuracy that could occur due to lateral transport beyond the cell limits.

- A silver contact evaporated on both sides of the solar cell precursor, on top of the ITO. On the n-side again, a deposition was made on the whole ITO surface, whereas on the p-side, a grid was used such that it fitted the 2x2 cm² ITO cell limits. The grid containing a tapered busbar is as shown in figure 2.5

Figure 3 summarizes the processes involved in the fabrication of the cells

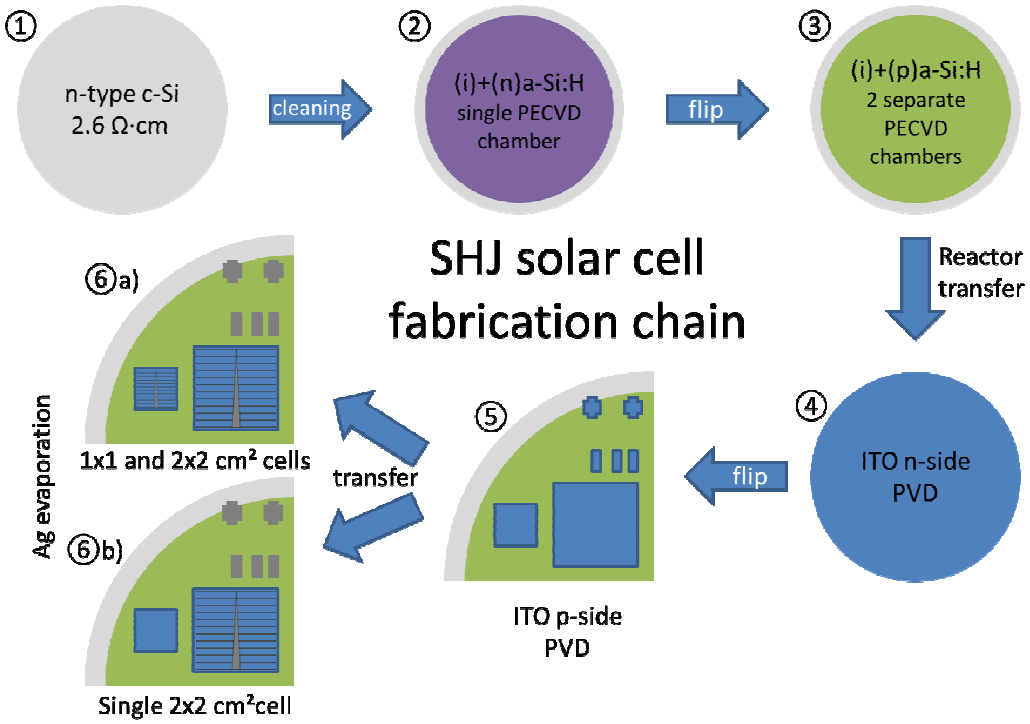


Figure 3 HIT solar cell fabrication chain at LPICM

Using this chain fabrication procedure, a record cell efficiency of 17.6% was achieved in LPICM in 2011 [6].

After fabrication, the passivation of the cell precursors was characterized by their minority carrier lifetimes using the photoconductance decay method (PCD). The cell efficiencies were evaluated by Oriel solar simulator under an illumination of 1 sun.

3. Results and Discussion

3.1 Passivation of cell precursors

Figure 4a and 4b shows the HIT scheme for a flat and textured cell precursor

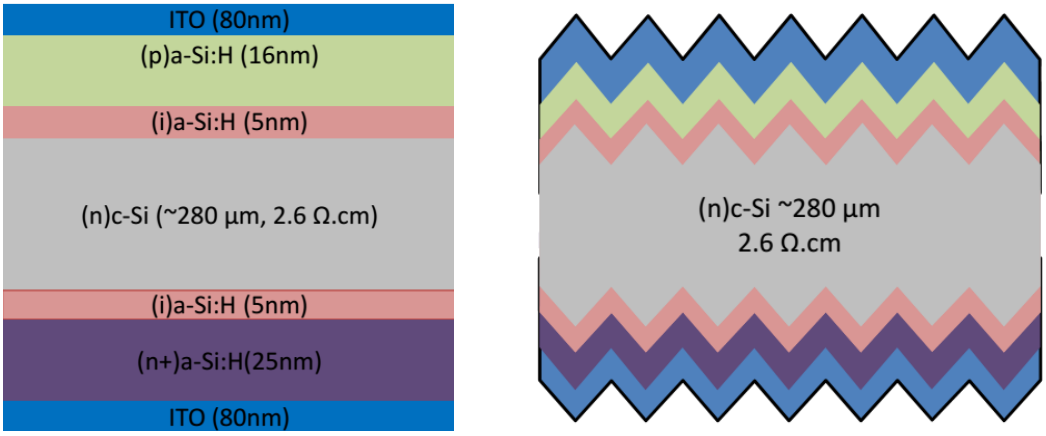


Figure 4 Standard HIT cell precursor structure of (a) flat and (b) textured precursors

3.1.1 ITO sputtering induced degradation in the i-layer

Using the DSP111 substrates, we made four precursors with varying i-layer thicknesses; 5nm, 10nm, 20nm and 50nm. This is done to study the impact of the i-layer thickness on the degradation after ITO is deposited by sputtering. Figure 3.4 shows the loss in passivation experienced by each thickness series characterized by a drop in its effective lifetime.

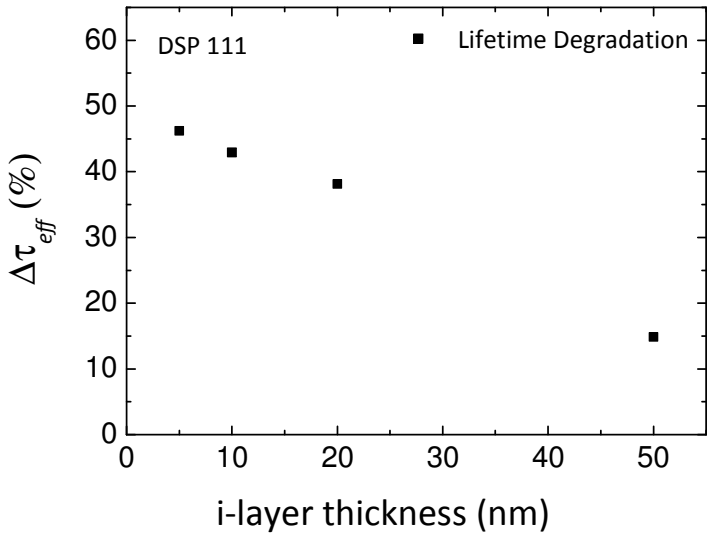


Figure 5 Influence of i-layer thickness on degradation after ITO sputtering

We normalized the lifetimes and have shown the percentage drop in lifetime for each thickness series after ITO deposition. It is obvious from the results that increasing the thickness of the i-layer gives a better passivation at the interface as the 50nm thick i-layer experienced the least degradation after ITO was deposited. Its lifetime dropped by only 14.9% while the sample with a 5nm thin i-layer had the most degradation of 46% after ITO was sputtered. We can conclude that the the i-layer plays an important role in protecting the interface from the damaging effects of the ITO over layer sputtering. It has been reported that increasing the i-layer thickness was beneficial for the V_{OC} of the completed cell[6]. It asserts that the increase in the i-layer thickness reduces the defect density at the interface hence resulting in a smaller recombination rate and thus a higher $V_{OC.}$

3.1.2 ITO sputtering induced degradation in cell precursor

In figure 6, we note that the decrease in the level of surface passivation can be recovered fully by annealing. After annealing, we observe that the lifetime in the high injection region is more fully recoverable than that in the low injection region. Hence, annealing effectively reduced the interface defect density giving rise to a lower recombination and higher $V_{OC.}$ This result further indicates that the deterioration of surface passivation is due to the creation of metastable defects at the a-Si:H/c-Si interface.

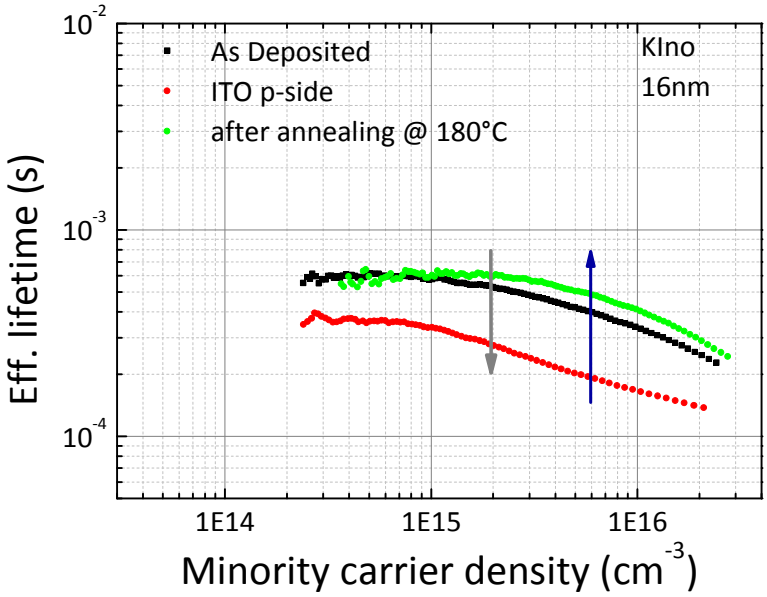


Figure 6 *Effective lifetime curve of a-Si:H film on c-Si wafers showing degradation by sputtering*

3.1.3 p/emitter side degradation

We observe after numerous experiments that during ITO sputtering on the (n) and (p) a-Si:H, we experience a very high degradation after sputtering on the p-side as compared to the n-side. Indeed, the damage done after sputtering on the n-side is quite insignificant as lifetime measurements reveal. Hence, we assert that sputtering on the p/emitter side of the precursor induces more damage to the passivation.

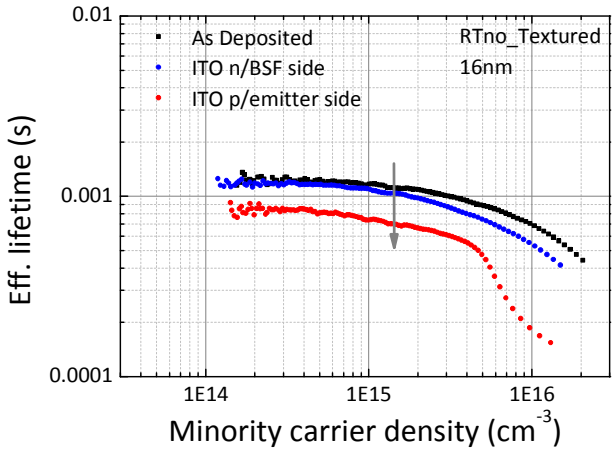


Figure 7 Comparison in degradation after ITO sputtering on n/BSF and p/emitter side

This is demonstrated in in figure 7 where we experience a greater loss in passivation after sputtering on the p-side. The lifetime degrades by a mere 10% after the n-side deposition of ITO as compared to 40% for the p-side. We have been able to record consistent results in other trials on substrates of varying thicknesses and also on flat substrates. The reason for this behavior is unknown and needs to be investigated. Another observed phenomenon is degradation induced by the presence of p-doped a-Si:H in a silicon heterostructure. Keeping in mind this observation of a more severe degradation on the p-side, we optimized the precursor structure by introducing a dopant gradient in the p-layer. What this means is that the dopant concentration of the p-layer is gradually increased as it is grown over the intrinsic layer resulting in a less doped layer directing in contact with the intrinsic layer.

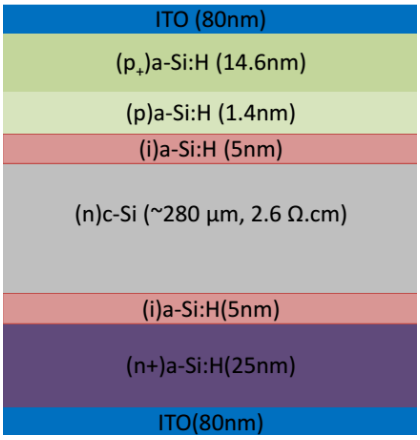
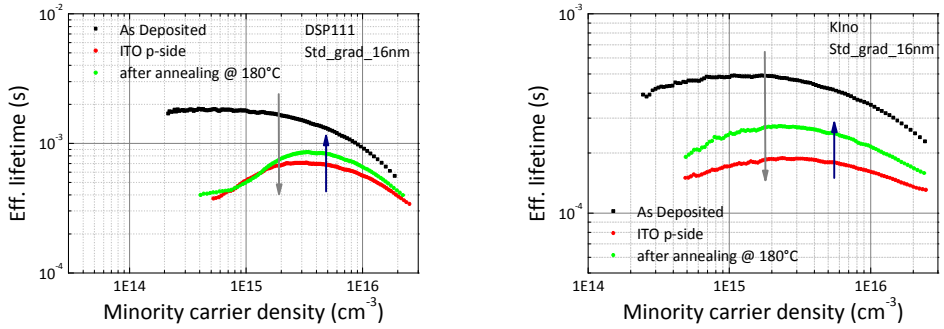


Figure 8 Structure of optimized standard cell precursor showing the dopant gradient

3.1.4 ITO Induced Degradation on Optimized 'Grad' Precursors

We refer to the cell with a gradient as 'grad' and the cell without a gradient as 'nograd'. A careful observation of the curves in figure 9a and b showed a measureable degree of improvement in the lifetimes of the cell precursor after annealing at 180°C for 30 minutes which points to a recovery of the passivation lost after ITO was sputtered on the precursors. The lifetime for the flat cell increases

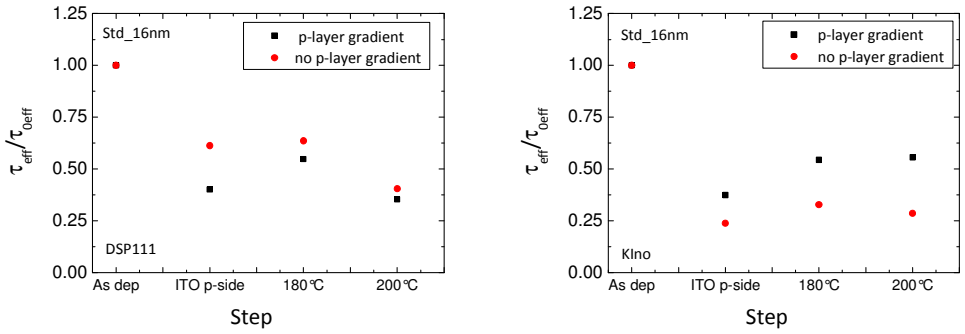
from 697µs after degradation to 1064µs after annealing. The textured sample also showed some improvements increasing from 185µs to 270µs.



(a) (b)

Figure 9 Effective lifetime measurements of optimized p-layer gradient cell precursors (a) a flat DSP111 (b) textured after annealing at 180°C

Figures 10a and b gives a visual representation of the degree of damage and recovery experienced by both types of precursors (nograd vs grad), where we show a normalized plot of the lifetimes before ITO sputtering, after ITO and after annealing at 180°C. In the case of the DSP111 Flat cell precursor, although the lifetime of the 'Grad' sample is lower than the 'noGrad', the 'Grad' sample showed an improvement in its lifetime after annealing which is in contrast to the 'nograd' sample. In the textured precursor, the 'grad' sample rose to 54% as compared to 33% for the 'nograd' sample.



(a) *(b)*

Figure 10 Normalized lifetime plots comparing "Grad" and "noGrad" precursors (a) a flat DSP111 (b)textured

We then attempt to introduce some enhancements in the precursor recipe. The intent of this enhancement is to reduce the surface imperfections that arise upon wet-etching process and can affect the passivation level of the precursors. Details of this enhancement cannot be included in this report at the moment because it is a pending patent.

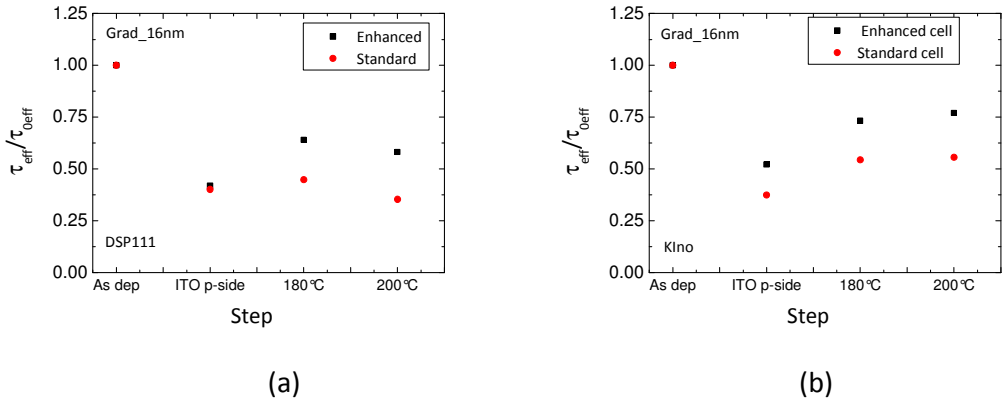


Figure 11 Normalized lifetime plots comparing enhanced and standard precursors (a) a flat DSP111 (b) textured

The stats show that enhanced "Grad" flat (DSP111) precursor improved to 64% of its initial "as dep" value while compared to 44% for the standard optimized (grad) precursor after being annealed at 180°C, while in the KIno sample, the enhanced precursor reached 73% of its original value as against 54% for the standard precursor after annealing at 180°C. The samples showed little or no improvements in passivation when annealed at 200°C. With this, we have demonstrated within the limits of our experiments that introducing a dopant gradient to the structure of the cell precursors can play a role in mitigating the damage done by ITO sputtering during the fabrication process of the precursors. We have also shown that altering the composition of the precursors by adding some enhancement can yield further beneficial properties which we have demonstrated to lead some recovery of the passivation lost during sputtering.

3.2 Performance of finished HIT solar cells

3.2.1 Impact of p-layer Gradient on the Performance of Standard Flat Cells

Our goal here is to investigate and check if the benefits of optimizing our cell precursor can be experienced in the finished cells also. We study these properties by characterizing the illuminated J-V properties of the cell. Figure 12 shows a plot of the light J-V characteristics of the grad and nograd standard flat cells. As expected, the grad cell which has a better passivation displayed a higher VOC of 693mV as compared to 676mV for the nograd cell. The higher VOC in the grad cell is attributed to a reduced interface defect density caused by introducing a p-layer dopant gradient to effectively decrease the damage caused by p-type doping. At the same time, this reduced defect density allows for an improved collection of generated charges and thus we obtain a very high fill factor of 81.4% in the grad cell and 78.7% for the nograd cell. The short circuit current for both cells is similar with a value of 31.4mA/cm^2 and 31.3mA/cm^2 for the nograd and grad cells respectively. These properties ultimately lead to a higher conversion efficiency of the grad cell which stands at 17.7% before being annealed. The nograd cell comes in second place with an efficiency of 16.7%.

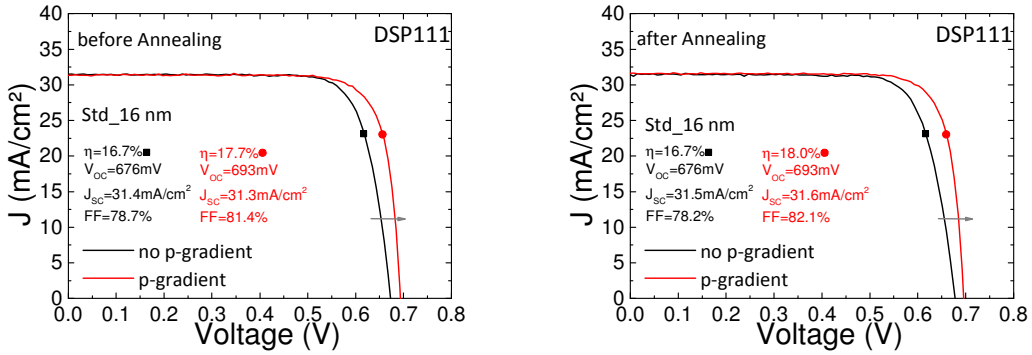


Figure 12 Cell characteristics showing light J-V curve before and after annealing for a flat cell

The above results show that the p-layer gradient is beneficial to the properties of the cell. In the as deposited cells, the cell that had a p-layer gradient displayed superior qualities. After annealing, the cell with the gradient again showed a better response to the heat treatment step.

3.2.2 Impact of p-layer Gradient on the Performance of an enhanced textured solar cell

For this study, we select a textured cell because we are able to get higher short circuit current and hence better cell efficiency primarily due to the light-trapping properties of textured substrates.

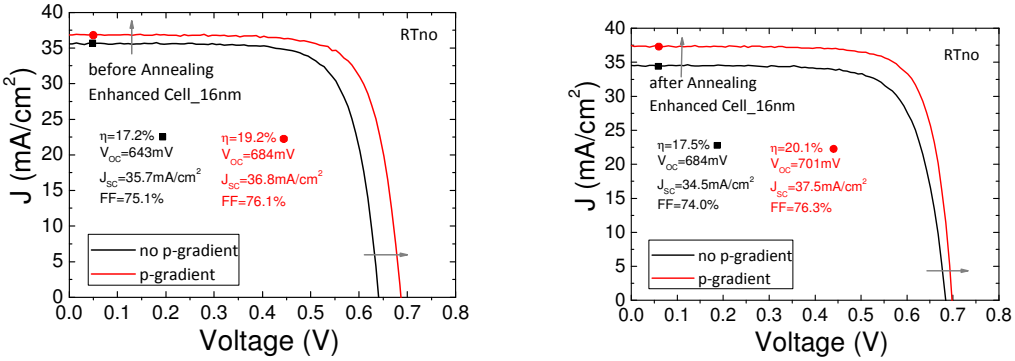


Figure 13 J-V characteristic curves comparing the enhanced 'grad' cell and 'nograd' cell before and after annealing

The J-V curve in figure 13 shows the sharp contrast and superior properties of the 'grad' cell over the 'nograd' cell. The enhanced 'grad' cell has a V_{oc} of 684mV compared to 643mV for the 'nograd' cell before annealing pointing a reduced recombination at the interface and hence a good passivation in the enhanced cell. The 'grad' cell exhibits a higher short circuit current of 36.8mA/cm² and fill factor of 76.1%. This further strengthens our argument of the advantage of a p-layer gradient. After annealing the cells, we notice an increase in the V_{OC}, efficiency and J_{SC} of the enhanced cell. It is noteworthy to state that this is the highest efficiency encountered in the course of this work. The 'grad' cell broke the 20% efficiency barrier to reach 20.1% after annealing along with a high V_{OC} of 701mV. It appears that this annealing step healed some defects within the heterostructure leading to an even better passivation. The current also increases to reach 37.5mA/cm². This increase in the current could be attributed due to an increased transparency and conductivity of the ITO layer [7]. The properties displayed by this 'grad' cell far outweigh any improvement seen in the 'nograd' cell

although the annealing step also brought some improvements in the latter especially in the V_{oc}. The V_{oc} increases from 643mV to 684mV while the efficiency reached 17.5%. The current drops from 35.7mA/cm² to 34.5mA/cm², this drop is balanced by the increase in the V_{oc} which ultimately led to a little increase in the efficiency.

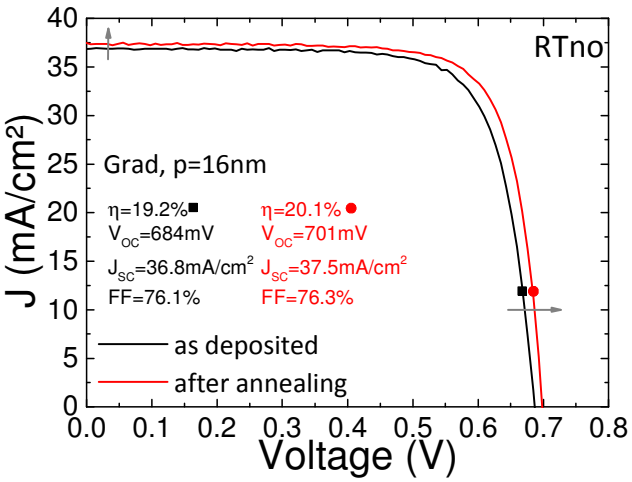


Figure 14 J-V characteristic curves showing improvements in the properties of the enhanced 'grad'cell

Figure 4.8 is a comparison of the enhanced grad cell in its 'annealed state' to its 'as deposited state' showing the improvements experienced after the heat treatment step. The results obtained so far from the analysis of the 'grad' and 'nograd' are consistent with the results obtained in passivation experiments which further buttresses our argument that introducing a p-layer gradient is beneficial for the cell properties. With an enhanced recipe featuring a p-layer gradient emitter, we were able to reach an efficiency of 20.1% with a V_{OC} of 701mV.

4 Conclusion

a-Si:H/c-Si heterojunction solar cells have been successfully fabricated using the chain process described in chapter 2. This procedure took into consideration the wet-etching and cleaning processes that were done to ensure very good chemical passivation of the (n) c-Si wafer surfaces. PECVD is the method of choice for the deposition of the amorphous layers while the ITO and silver contacts were deposited using the sputtering and evaporation processes respectively.The effective lifetimes as measured by the WCT-120 Sinton lifetime tester was used to characterize the passivation levels in the cell precursors. It has been shown that the p-type dopant induces a higher degradation as compared to the n-type dopant. To effectively reduce the effect of this phenomenon, a p-layer gradient was introduced in the cell precursor structure. The results showed that the grad was beneficial for both the flat and textured precursors. Since the optimization done on the cell precursor gave positive results, we sought to study the impact on finished cells. The illuminated J-V properties were measured using the Oriel solar simulator at 1 sun, AM 1.5. Using the optimized chain fabrication procedure and incorporating a p-layer gradient enhanced recipe in our champion cell, we were able to reach a cell efficiency of 20.1% at a V_{OC} of 701mV, J_{SC} of 37.5mA/cm² and FF of 76.3% after annealing the cell in N_2 at 180°C for 30 minutes. This result was realized for a textured substrate which point to a high level of passivation of the dangling bonds at the surface of the c-Si.

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