DC-DC Converter for Aerospace Industry

Rad-Hard Control Integrated Circuit Implant

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Abstract - The electrical potential conversion is nowadays a widespread feature, almost every electronic device have it. Depending on their application, they may have different characteristics. Aerospace converters are a specific case, which has to be able to deal with radiation and higher temperature ranges. There are few aerospace converter suppliers and typically they are available only for the defense industry.

In this dissertation is discussed the design of a converter and its controller for the Aerospace Industries as claimed by ESA. To achieve this objective, in this dissertation it is first discussed the effects of outer space and then what tools and or techniques exist to mitigate this problem. In a second phase, it will be revealed the development. The controller was designed using the Cadence with the design kit of Austriamicrosystems (AMS 0.35u) with a special kind of transistors (ELT - "Enclosed Layout Transistor"). Finally the results of the tests are presented in either simulation or a test plate built for this purpose.

This work exposes a converter working with the specifications required by ESA, a converter controller integrated circuit, and finally the proof that all functionalities of the chip are working as expected.

Keywords - Aerospatiale, Forward, Control, PWM, PFM, SMPS

I. Introduction

Space Environment is an adverse space for an electronic circuit. Special technics are need to strength and extend the life cycle as we will present later on this paper. These circuits with this technics are known as Rad-Hard circuits.

European Space Agency (ESA) suffers from a lack of European supplier of Rad-Hard circuits. Each time an application is sent to US provider we have to wait longer, pay more and have to be controlled by US federal approval.

ESA challenged the European scientific community to design and produce a solution for a DC/DC converter and its controller.

On this paper we will start to espouse the radiation issues and how to mitigate them. Then we will present our decisions to accomplish the ESA goal. Decisions like converter topology, control method and layout technics to mitigate radiation effects.

And finally we present the designed results and then some results of our silicone implemented controller.

II. State of Art

Observing the market and searching for Rad-Hard converters we found some solutions [*1*] [*2*] [*3*] [*4*] [*5*] [*6*].

They have some drawbacks in common; all of them are US providers and none of them accomplishes all the ESA specifications.

III. Radiation

We will focus only ionization radiation, the only one witch has sufficient energy to ionize atoms.

When radiation collides with an electric circuit can have two kind effects: a cumulative effect or a single event effect. Single event effects can be subdivide into two other groups: soft errors and hard errors.

Cumulative effects are relative to gradual changes in the crystalline structure, which tends to degrade the characteristics of the semiconductors.

Single event effects are relative to changes in the electrical potential due to ionization particle strike. This change in the electrical potential could be so high that can cause a hard error or soft error if this potential change for example is only able to change bit value.

In order to improve the life-cycle and mitigate these effects should be used the following technics:

- Use insulation subtracts instead of the common wafers.
- Use vertical BJT instead of horizontal ones
- Use shielding with Boron-11.
- Use a subtract with a wider band-gap
- Use CMOS with enclosed layout for analog circuits.

In specific way and in order to prevent soft errors should be used the following technics:

- Use more parity bits
- Use redundancy and voting logic
- Use watch dog timers

At this paper will be focused the usage of CMOS Enclosed Layout Transistors (ELT), an already made library of ELT will be used.

ELT have a shape in a way that minimizes the cumulative effects, being enclosed by them self prevents the accumulation of ionic matter in the edges of the gates and eliminates the path where currents can flow uncontrolled between source and drain.

IV. Converters

There are lots of different configurations and topologies for power converters. The goal is to design an efficient converter with the following requirements: three outputs with 10 watts

each, isolated, efficient for lower loads, with less than 10% of ripple and at least a margin phase of 60 deg.

The selected topologie is the forward converter, because it can easely have three outputs, it has galvanic isolation, a simple implementation,.low output noise, easy to stabilize and one of the best choices for the desired power output. [*7*] [*8*] [*9*].

V. CONTROL

The control scheme is a key factor for this converter. To reach an efficient converter for all range loads we can do so mixing two different control technics, Pulse Frequency Modulation (PFM) control for lower loads and Pulse Width Modulation (PWM) control for other cases.

This work only uses PWM. The PFM scheme has not been implemented due time restrictions.

The PWM control scheme divides itself in two types: those who have dependency on the output voltage and those who have dependency on the output current and also on the output voltage.

This second type is called current control. The current dependency implements an augmented stability control, this provides a better transient response and grants more audio-susceptibility.

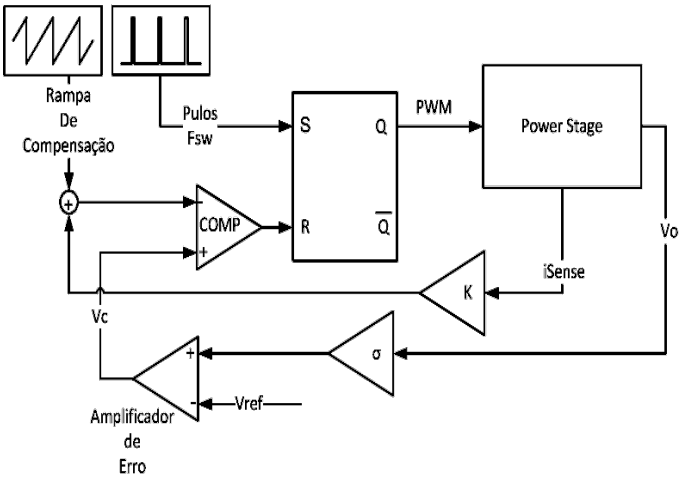

Fig. 1 - Current mode control scheme.

A. PWM Switch Model

According with Basso the power switch working under PWM control model for large signals and for small signals can be modeled as follows [*7*]:

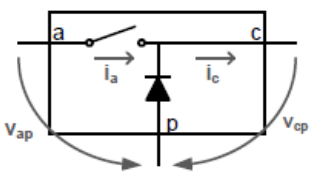

Fig. 2 - PWM Switch model, a is the active port, p is the passive port and c is the common port [*7*].

The state variables are:

$$i_A = I_A + i_a \quad (1)$$

$$i_C = I_C + i_c \quad (2)$$

$$v_{CP} = V_{CP} + v_{cp} \quad (3)$$

$$v_{AP} = V_{AP} + v_{ap} \quad (4)$$

$$v_C = V_C + v_c \quad (5)$$

$$D = D_0 + d \quad (6)$$

The large signal model of Basso is obtained by taking the important state variables and averaging them over a switching cycle (D_0 – duty cycle, R_{Sense} – current sense resistance, T_{sw} – switching period, V_C – control voltage, S_a – compensation slope).

Large signal model:

$$I_A = D_0 I_C \quad (7)$$

$$V_{CP} = D_0 V_{AP} \quad (8)$$

$$I_C = \frac{V_C}{R_{sense}} - \frac{S_a}{R_{sense}} D_0 T_{sw} - V_{CP}(1 - D_0)\frac{T_{sw}}{2L} \quad (9)$$

Small signal model is obtained from perturbed large signal model neglecting the cross alternating products.

Small signal model:

$$i_a = g_i v_{ap} + g_r v_{cp} + k_i v_c \quad (10)$$

$$i_c = g_f v_{ap} + g_0 v_{cp} + k_o v_c \quad (11)$$

$$g_i = D_0\left(g_f - \frac{I_C}{V_{AP}}\right) \quad (12)$$

$$g_r = \frac{I_C}{V_{AP}} - g_0 D_0 \quad (13)$$

$$k_i = \frac{D_0}{R_i} \quad (14)$$

$$g_f = D_0 g_o - \frac{D_0(1 - D_0)T_{sw}}{2L} \quad (15)$$

$$g_0 = \frac{T_{sw}}{L}\left[(1 - D_0)\frac{S_a}{S_1} + \frac{1}{2} - D_0\right] \quad (16)$$

$$k_o = \frac{1}{R_i} \quad (17)$$

$$f_n = \frac{f_{sw}}{2} \quad (18)$$

$$\frac{f_{sw}}{2} = \frac{1}{2\pi\sqrt{LC_s}} \quad (19)$$

$$C_s = \frac{1}{f_{sw}^2 \pi^2 L} \quad (20)$$

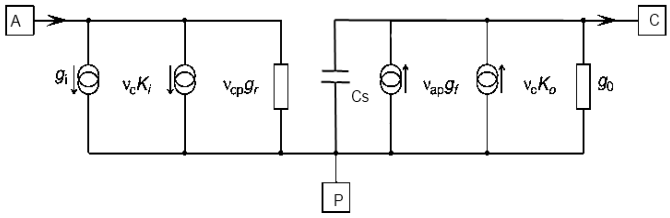

Fig. 3 – PWM switch small signal model for current-mode control [*7*].

B. Compensation

The main goal of the compensation is to stabilize the converter. Other constrains that can be controlled by the

compensation network are the dumping factor the cutoff frequency.

This way this compensator bode plot should have the aspect of Fig. 4. Compensator should have a high static gain to reduce the static error and a phase boost at the cutoff frequency to ensure a correct dumping factor.

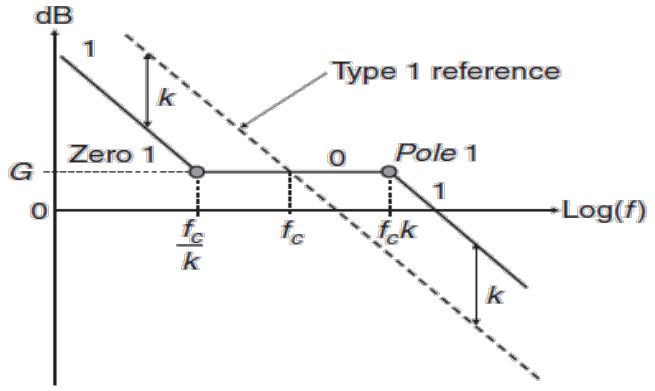

Fig. 4 - Type 2 compensator bode plot [7].

Basso proposed a simple procedure to ensure that the correct phase margin and the desired cutoff is obtained. To reach this is only needed to know the gain of the open loop at cutoff frequency and the phase margin.

$$\varphi_{boost} = \varphi_{PM} - \varphi_{P(s)}\big|_{f=f_c} - 90° \quad (21)$$

$$\varphi_{boost} = \tan^{-1}(k) - \tan^{-1}\left(\frac{1}{k}\right) \quad (22)$$

$$k = \tan\left(\frac{\varphi_{boost}}{2} + 45°\right) \quad (23)$$

$$G_{f_c} = 10^{\frac{\left|G_{P(s)}\right|_{f=f_c}\big|}{20}} \quad (24)$$

$$C_2 = \frac{1}{2\pi f_c G_{f_c} k R_1} \quad (25)$$

$$C_1 = C_2(k-1) \quad (26)$$

$$R_3 = \frac{k}{2\pi f_c C_1} \quad (27)$$

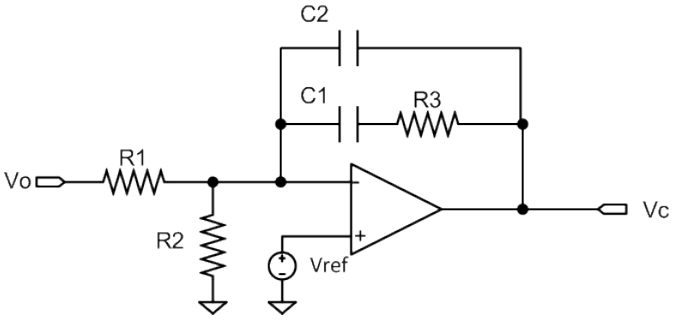

Fig. 5 - Compensator circuit diagram.

$$C(s) = \frac{V_c(s)}{V_{err}(s)} = \frac{1}{R_1(C_1+C_2)} \frac{1 + sC_1R_3}{s\left(1 + s\frac{C_1C_2R_3}{C_1+C_2}\right)} \quad (28)$$

C. System Model

A model for the switch is already presented, a model for the compensator is also already presented, now can be figured the converter system.

The converter can be modeled as follows:

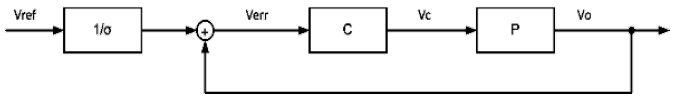

Fig. 6 – Control system model.

Where C is the compensation model and P is the switch model.

$$\frac{V_o(s)}{V_c(s)} = P(s) \quad (29)$$

$$P(s) = \left(\frac{R}{R_i}\right)\left(\frac{1}{1 + \frac{RT_{sw}}{L}K_p}\right)\left(\frac{1 + \frac{s}{\omega_{z1}}}{1 + \frac{s}{\omega_{p1}}}\right) \times \left(\frac{1}{1 + \frac{s}{\left(\frac{\pi}{T_{sw}}\right)\left(\frac{1}{\pi K_p}\right)} + \frac{s^2}{\left(\frac{\pi}{T_{sw}}\right)^2}}\right) \quad (30)$$

$$K_p = \left(1 + \frac{S_a}{S_1}\right)(1-D) - \frac{1}{2} \quad (31)$$

$$\omega_{z1} = \frac{1}{R_C C} \quad (32)$$

$$\omega_{p1} = \frac{1}{RC} + \frac{T_{sw}}{LC}K_p \quad (33)$$

$$\omega_{p2,3} = -\frac{\pi^2 K_p}{2T_{sw}} \pm \frac{\pi K_p}{2}\sqrt{1 - \left(\frac{2}{\pi K_p}\right)^2} \quad (34)$$

D. Topology

This work has a set of background works [*10*] [*11*] [*12*] in which the topology illustrated in Fig. 7 is already studied and suggested to be suitable for this work.

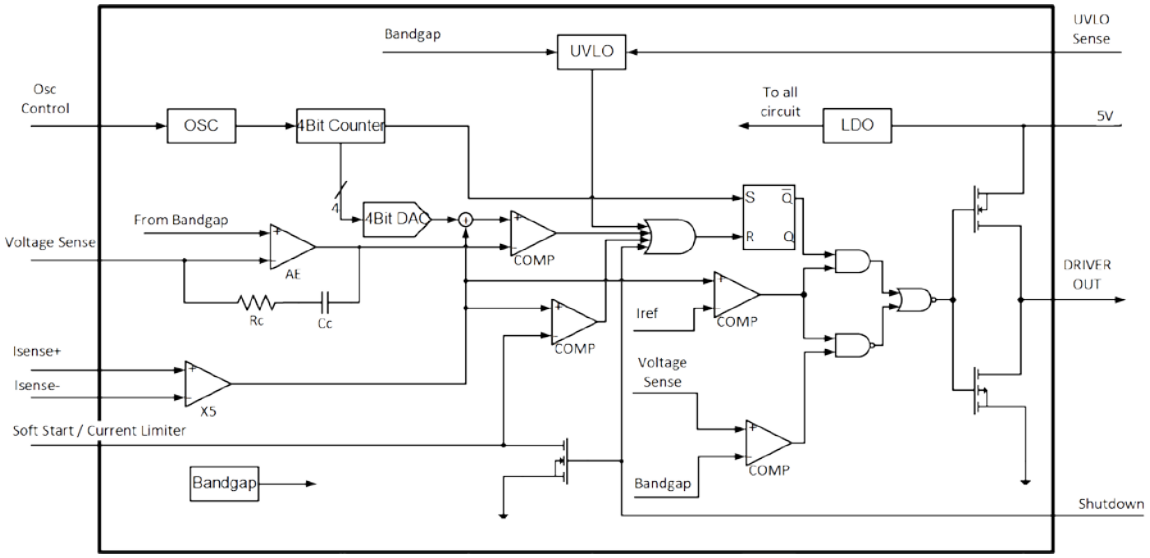

Fig. 7 - Topology of the control circuit.

The implemented circuit has some cuts, not all of the components were implemented and some has been implemented outside of the circuit to make this controller circuit as much as possible converter topology independent.

The error amplifier feedback path is to be implemented outside of the circuit. This way it is easier to compensate any converter.

On the other hand there are some components that were not implemented due to lack of time, these components has to be implemented outside and connected to the control circuit.

The components that has to be outside implemented are: compensation slope, PFM control and LDO.

VI. Top Simulations

The simulations were made upon the following parameters. These parameters were calculated based presented models.

TABLE 1 - SIMULATIONS PARAMETERS.

Transformer [*13*] [*14*]	
Winding Area	12 mm^2
Effective Area	5 mm^2
Primary windings	10
Secondary windings	10
Demagnetization windings	10
Material	3F4
Wire diameter	0.8 mm
Duty Cycle	
Max	0.14
Min	0.26
Output Filter	
Capacitance	22µF
Capacitance resistance	0.01Ω
Inductance	10µH
Load	
Impedance	2.5Ω
Integrated Circuit	
External Slope Ratio	$1250\frac{kV}{s}$
Current Sensing Resistance	0.05Ω
Compensator	
C1	17pF
C2	51fF
R1	2.5MΩ
R3	1.7MΩ
Converter	
Cutoff Frequency	100KHz
Switching Frequency	1MHz
Output Voltage	5V
Phase Margin	80°
Voltage Ripple	±0.05V
Voltage Step Response Peak	±0.3V
Input Voltage	
Max Voltage	37V
Min Voltage	19V
Nominal Voltage	28V

Based on the models already presented here and the parameters list above we archived some results that we show as follows:

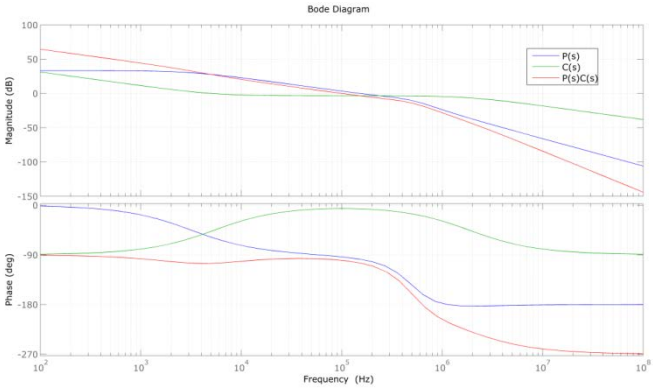

Fig. 8 - Bode plots, red line - closed loop, green line - compensator and blue line - open loop.

The following figures (Fig. 9 and Fig. 10) are related to the Continuous Current Mode (CCM) of the output inductance. The Discontinuous Current Mode (DCM) is neglected in this paper because is not supposed this converter to function in this mode. For this low loads the converter should be in PFM mode not in PWM with DCM.

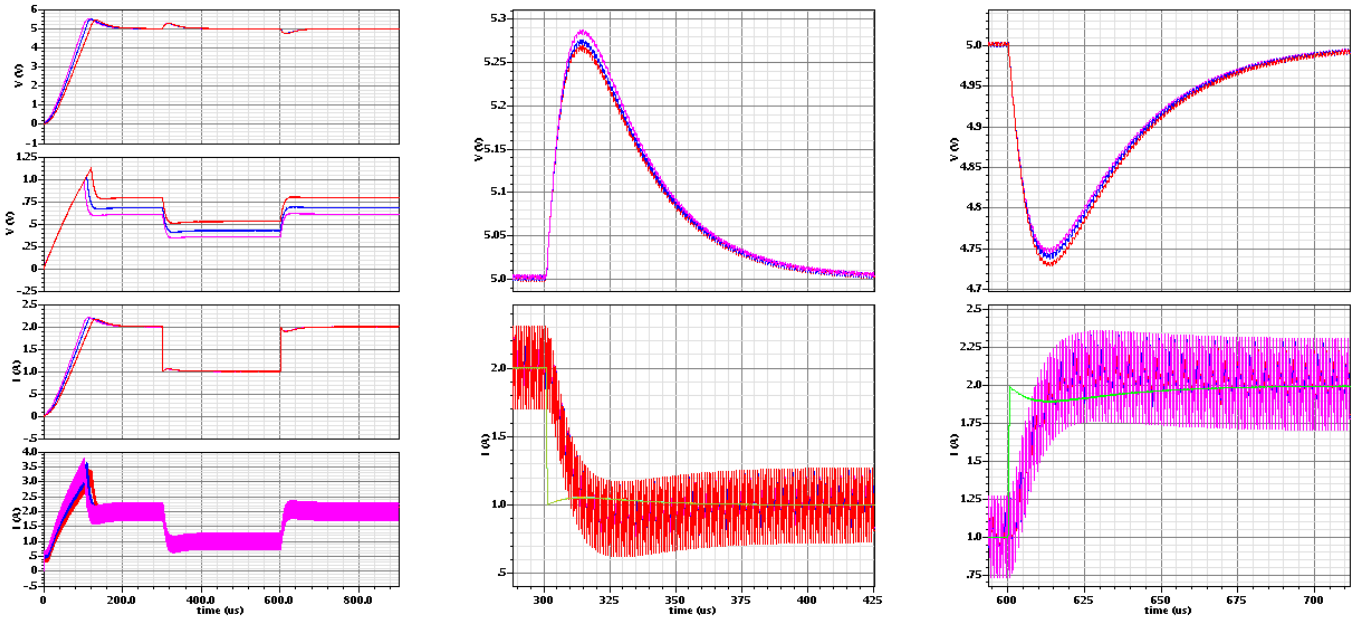

Fig. 9 - Load step response of the proposed converter for the three different input voltage

In Fig. 9 there are a set of plots, those at left are the main plots and those at center and right are zoomed plots of the main plots.

From top to bottom the main plots are: output voltage, control voltage, output current and finally output inductor current. At the center we have the falling step output voltage and current response. At right the rising step output voltage and current response.

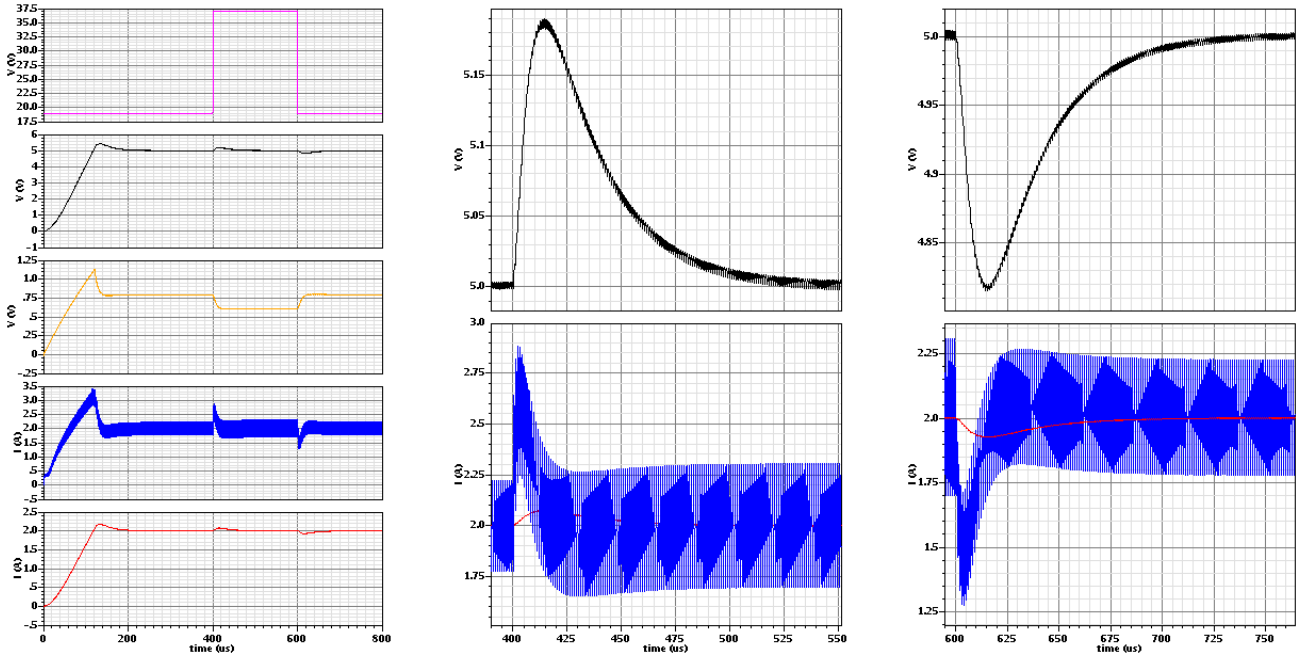

Fig. 10 - Input voltage step response of the proposed converter.

In Fig. 10 there are a set of plots, those at left are the main plots and those at center and right are zoomed plots of the main plots.

From top to bottom the main plots are: input voltage, output voltage, control voltage, output inductor current and finally output current. At the center we have the rising step

output voltage and current response. At right the falling step output voltage and current response.

VII. Silicon Implant

The circuit was implemented in silicone under the AMS 0.35µ technology and using special CMOS transistors (Fig. 11).

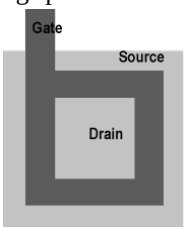

Fig. 11 - ELT transistor example.

In the following Fig. 12 we can observe the implemented circuit. Surrounded in yellow we have the analog parts, in red the mixed signal parts, in blue the digital parts and in orange the power stage.

All the analog transistor or set of analog transistors are surrounded with guard rings to reduce latch-up, reduce noise and capture leakage currents.

The analog parts are separated as far as possible from the noisy digital parts. Between them the mixed signal components.

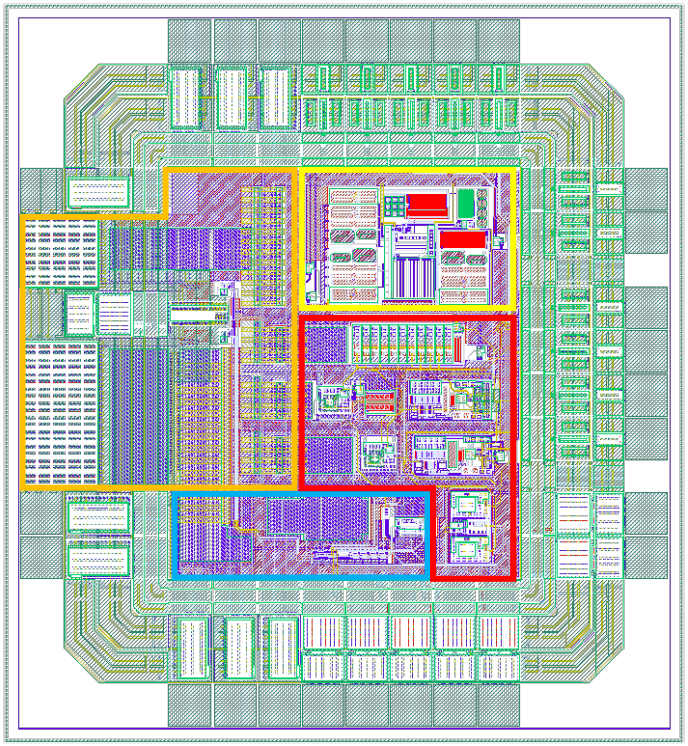

Fig. 12- Silicone implant of the control circuit.

VIII. Test on a Chip

To test the chip effectively we have to construct a converter, in this case because some components have to be implemented outside of the integrated circuit the test board doesn't implement the converter. The board presented in Fig. 13 is able to expose all port signals, feed the circuit and set some bias voltages.

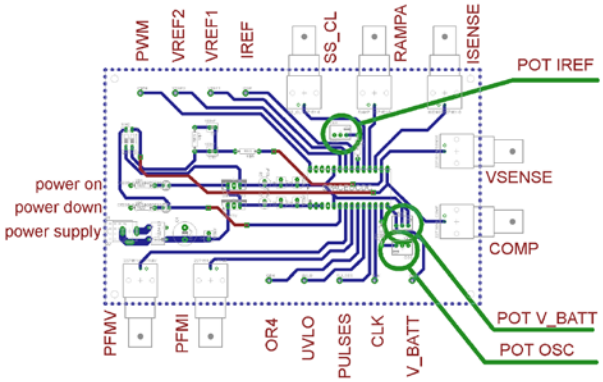

Fig. 13 - Test board to do the "Test On A Chip".

A. Oscillator and Pulses generator

Selecting the correct resistance value to the potentiometer POT OSC we set the bias current of the oscillator and thus the frequency. In Fig. 14 can observe that for an external resistance value of 84 KΩ the output frequency of the square wave is about 16 MHz, and 1 Mhz for the pulses.

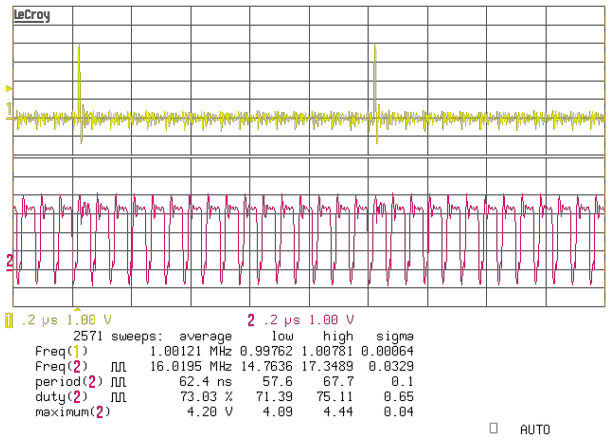

Fig. 14 - Oscillator and pulse generator output.

B. Under Voltage Lockout

Sweeping the potentiometer POT V_BATT in both directions and plotting it in order to UVLO port signal we obtain the signal of the Fig. 15.

$$V_{UVLO_{max}} = 1.34\,V \quad (35)$$

$$V_{UVLO_{min}} = 1.13\,V \quad (36)$$

Collecting some values and using the following equations we are able to calculate and translate these values to the real scenario.

$$V_{BATT} = V_{UVLO} + RI \quad (37)$$

$$I = \frac{V_{BATT}}{R + R_1 + R_2} \quad (38)$$

$$V_{BATT} = \frac{V_{UVLO}}{1 - \left(\frac{R}{R + R_1 + R_2}\right)} \quad (39)$$

TABLE 2 - UVLO RESULTS.

V_{UVLO}	R	V_{BATT}
1.34	1.41MΩ	22.6
1.13		19.0

We set the set the lower voltage to 19 V, then we find the external resistance and finally the upper voltage of the hysteresis, which is 22.6 V. This value is a little bit higher than it was dimensioned; the expected value was 20 V.

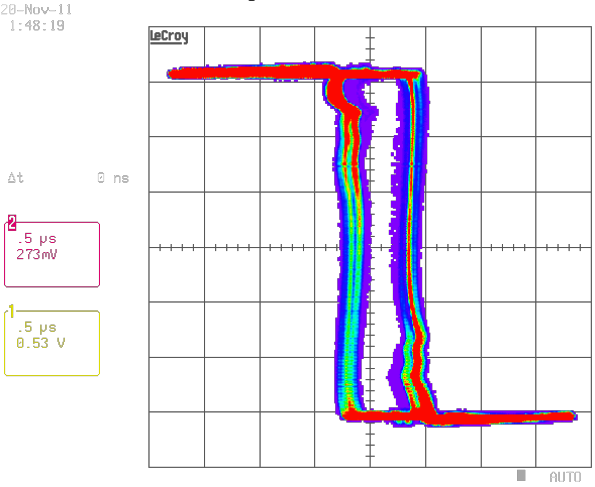

Fig. 15 - Under Voltage Lockout hysteretic output.

C. Comparator

The controller circuit doesn't expose any port with direct access to one of the existing comparators. So we arranged a combination of controller port signals that shows if the comparator is working or not and were we can measure the comparator delay (Fig. 16).

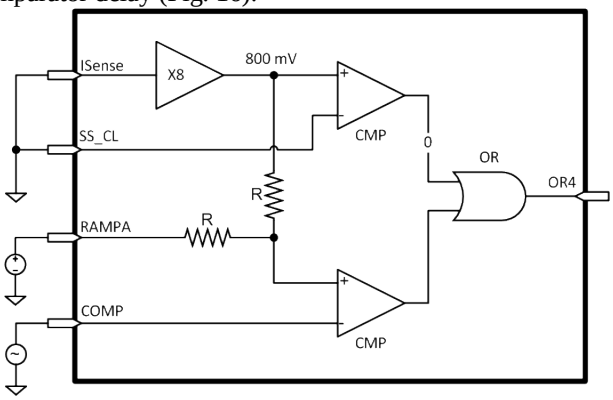

Fig. 16- Schematic of the circuit used to test the comparator.

We observed (Fig. 17) that delay is about 8 ns and the comparator is working as expected.

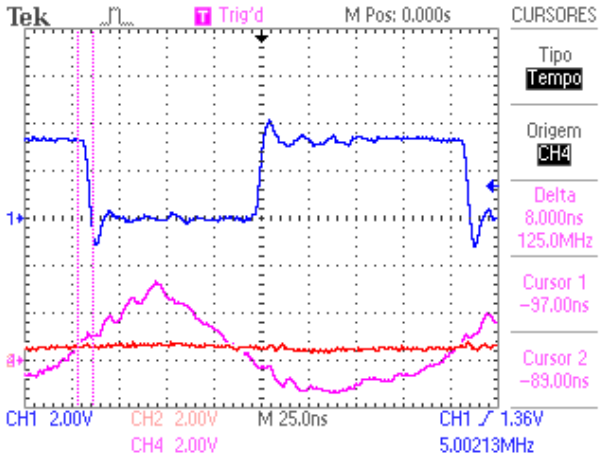

Fig. 17 - Comparator results.

This archived delay time is the sum of comparator delay plus the delay of the big OR4.

D. Non Overlapping Output Power Stage

As we can observe in Fig. 18 we has a delay of 18 ns, and that the non-overlapping system is working according with signal shapes on the transitions.

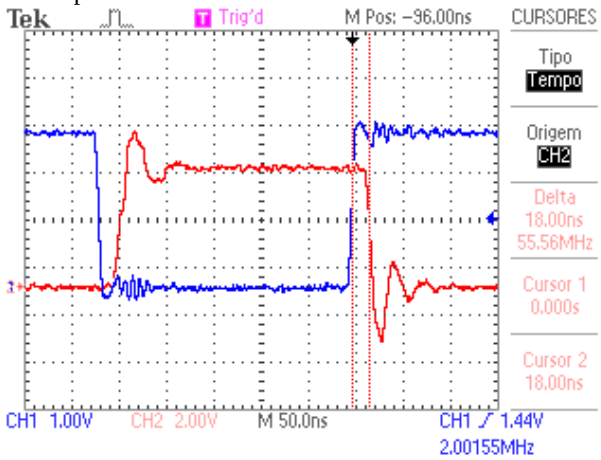

Fig. 18 - Non-Overlapping and Power Stage output.

E. Band Gap Voltage Reference

The voltage reference is working as expected and it has a startup time of about 10 µs and the two output voltages are the expected voltages also (the values of the voltages can be observed in Fig. 19).

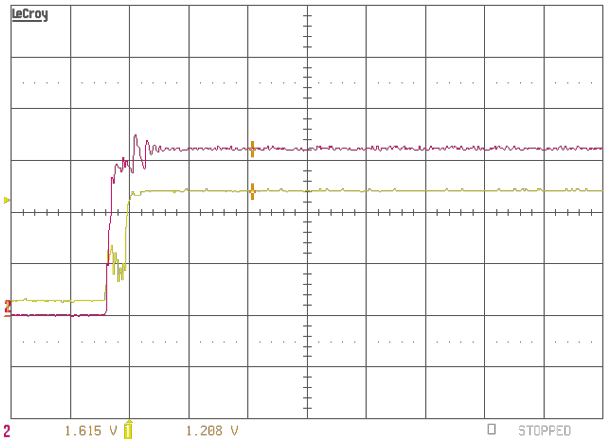

Fig. 19 – Transient response of band gap voltage reference.

F. Error Amplifier

The error amplifier was tested with network analyzer. The montage circuit is shown in Fig. 20.

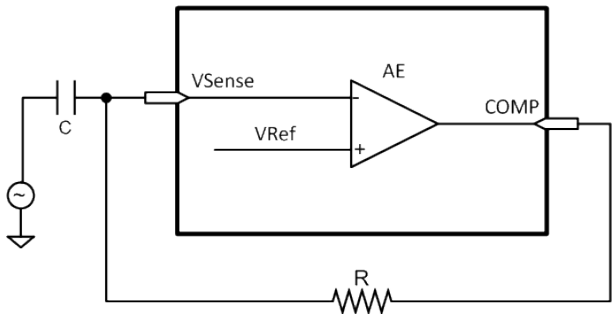

Fig. 20 - Schematic of the error amplifier test circuit.

From the analysis and comparing results with the design results it is possible to infer that the band width is about 7.8 GHz and phase margin is about 45° (Fig. 22).

It is also noticeable that the system singularities has some deviation from what was expected to be. This should be caused by components not presented in the design results, like bonding wires, cross talk in the wires of the test board and impedance calibration in the network analyzer montage.

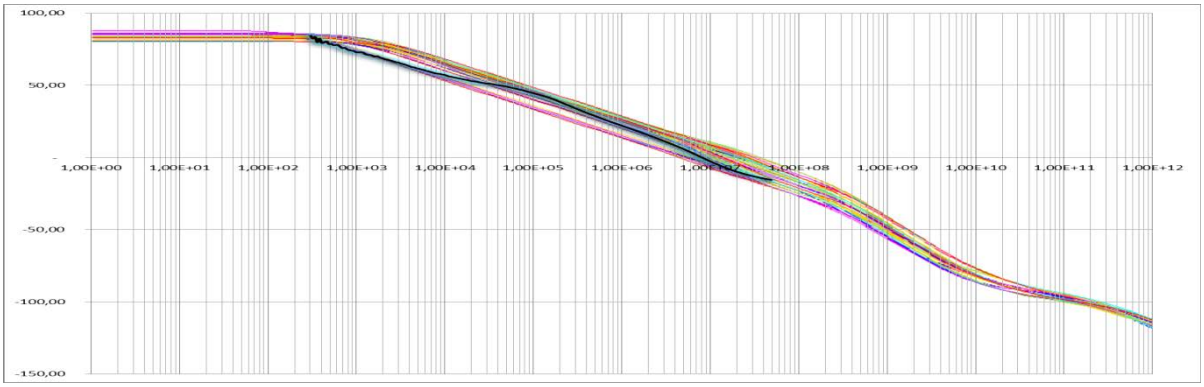

Fig. 21 - Bode plot gain result.

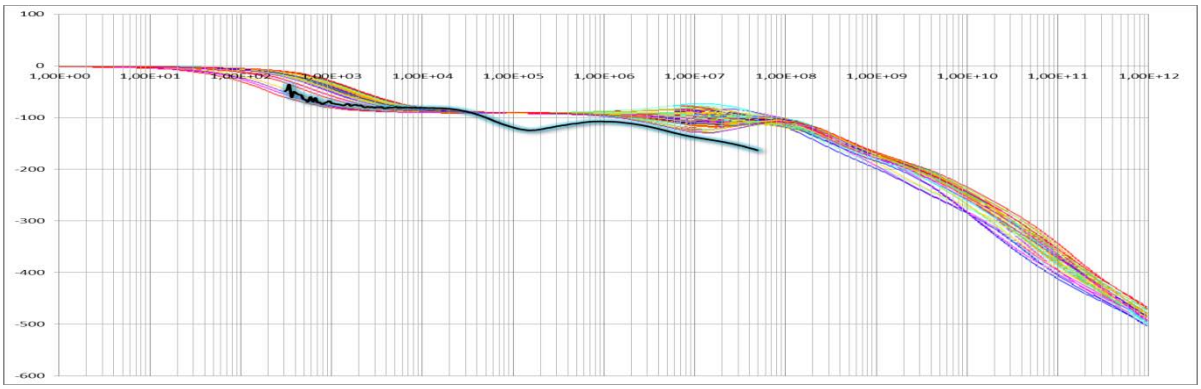

Fig. 22 - Bode plot phase result.

IX. Conclusion

A DC/DC converter for Aerospace environments was studied in this paper. The solution presented have some restrictions, the main cause were time restrictions. The project budget to do the silicone implant has a deadline; this deadline forced us to do some project cuts. We hasn´t implemented the PFM control and the internal compensation slope. Thus, this two systems have to live outside of the integrated circuit.

We have done simulations to the converter and tested on a chip some functionalities of the implemented circuit.

The simulations where not done against all the ESA requirements, on the simulations scenario the converter only have one output. We assumed that if the converter is able to

handle one output, it is also able to handle n cross regulated outputs.

From the simulations we could state that the projected converter accomplishes the specifications for one of the outputs.

After that we have done one test board to test de converter control integrated circuit. Here we could validate that all of the control circuits cells were working like it was predicted.

For future works we suggest to implement the PFM control, and add more isolation from input source (like the current sense path). We also suggest to do a better test board, a board that implements the forward converter and thus would be possible to fully test the converter control integrated circuit.

X. References

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