Prototype of an Inverter for Application in Renewable Energy Systems

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Abstract—The main objective of this work is to present the project and construction of a monophasic inverter. It covers all the stages from the sizing of the controller to the scaling and mounting of the components on two printed circuit boards (PCB). The complete simulation of the system was projected and executed in computational environment. This had as main purpose to assess the general functioning of the system, as well as, serving as a basis for comparison with the real built system.

Index Terms—Inverter, Single phase inverter, Three level PWM, Proportional Integral, Current Control, Voltage control, IGBT, renewable energy.

I. INTRODUCTION

The monophasic inverter, also known as DC-AC converter, it is responsible for transforming direct current (DC) into alternating current (AC). It is a device of power semiconductors operated to conduction and to cut, with the purpose of connecting the direct current source to the network AC voltage, thereby, ensuring the transmission of energy.

The monophasic inverter consists of two arms. In each arm it has two IGBTs and respective freewheel diodes.

The use of a monophasic inverter has as main advantages the use of a few number of semiconductors, the simplicity of the control, the reduced dimensions of the device, the low cost and high reliability and performance.

At the level of disadvantages, it can be mentioned that the monophasic inverter requires a source of DC voltage with a considerably higher value than the desired output voltage, the majority of the modules provided by industry are triphasic and the monophasic inverter has a lower power density when compared with the three-phase inverter.

Lately, the demand for monophasic inverters recorded a sharp increase, originated mainly by the positive growth of micro-generation, using photovoltaic technologies. This type of device is mainly used in residences or small industries for applications that range from UPS (Uninterruptible Power Supplies), to autonomous photovoltaic systems "off grid" or connected to the network (micro-generation).

With this article it is intended to explain the different steps followed in the design of this monophasic inverter. Those steps are the sizing of both inverter and components of the electrical circuit, the design of PCI regarding each circuit and finally, the assembly of the components and laboratory testing. The ultimate goal is to build a versatile and compact prototype of single-phase inverter.

The general scheme is composed by several components. These components are the power circuit to the IGBT, the trigger circuit, the control circuit and the acquisition of signals. The control circuit includes the logic required for control of the drive arms and the acquisition of signals consists of current and voltage transducers circuits.

The general scheme is shown in Fig. 1.

Figure 1 is formed by four main circuits, which are:
- The power circuit encompassing the semiconductor power devices (IGBT) and its free-wheeling diodes, circuits protection, filter and heatsink;
- The trigger circuit containing the optocouplers and the switched sources;
• The control circuit including all the necessary logic to the command of the arms of the IGBT;
• The signal acquisition circuit comprising the current and the voltage transducers.

II. DIMENSIONING OF THE POWER CIRCUIT

It is intended that the inverter has a maximum power of 3 kVA. Knowing that the output voltage is defined by the grid and the current is in phase with the voltage, the current calculation is carried out by (1) obtaining the current output by (2):

\[
S = V_{\text{Rede}} \times I_{\text{Rede}}
\]

\[
I_{\text{Rede}} = \frac{S}{V_{\text{Rede}}} = \frac{3000 \text{ } \text{W}}{230 \text{ } \text{V}} \approx 13.05 \text{A}
\]

The current to be supplied by the DC source can be calculated knowing \( I_{\text{In}} \), for a PWM command of two or three levels, the input voltage must be at least 42% higher than the output (in this case imposed by the mains voltage) and the reference current it is in phase with the mains voltage, defining \( U_{\text{DC}} = 400 \text{V} \). Thus the equation to compute \( I_{\text{In}} \):

\[
V_{\text{Rede}} \times I_{\text{Rede}} = U_{\text{DC}} \times I_{\text{In}}
\]

\[
I_{\text{In}} = \frac{V_{\text{Rede}}}{U_{\text{DC}}} \times I_{\text{Rede}} = \frac{230 \text{ } \text{V}}{400 \text{ } \text{V}} \times 13.05 \text{A} \approx 7.5 \text{A}
\]

The results will be important for choosing the semiconductors, the protections and to determine the width and the spacing of the tracks on the printed circuit board.

A. Input filter

The characteristics of the input filter, comprising a set of capacitors whose minimum capacity is defined by \( C_{\text{min}} \), it is given by the expression (5) using the data (6). It was also introduced a resistor (47 k\( \Omega \), 7 W) in parallel, to ensure that the capacitors of the input filter were safely discharged, when the circuit was not in use.

\[
C_{\text{min}} = \frac{P_{\text{out}} \times \Delta t}{(V_{\text{cc}} \times (1 + \Delta V))^2 - (V_{\text{cc}} \times (1 - \Delta V))^2}
\]

Where:

\[
\begin{cases}
P_{\text{out}} = 3000 \text{ kW} \\
\Delta t = \frac{1}{50} \text{ s} \\
U_{\text{DC}} = 400 \text{ V} \\
\Delta V = 9 \% 
\end{cases}
\]

Resulting:

\[
C_{\text{min}} = 1.04 \text{ mF}
\]

In order to guarantee the specifications described above, it was used a set of three capacitors with total capacity of \( C_{\text{DC}} = 1.122 \text{2 mF} \). Two of them are electrolytic with 560 \( \mu \text{F} \) each, and the third, polyester, with a capacity of 2.2 \( \mu \text{F} \). It was selected to use more than one capacitor to minimize the non-idealities of the capacitors.

B. Power Semiconductor

In this work the four IGBT modules used are from INFINEON - IGBT+ DIODE, 1200 [V] /25 [A], each being composed of the IGBT semiconductor and respective free-wheeling diode in anti-parallel, as illustrated in Fig. 2.

![Figure 2 - Illustration of IGBT power semiconductor.](image)

1) Surge Protection Circuits

\( a) \) Varistors

To ensure the protection of the IGBT’s against voltage surges, that may occur in the IGBT’s terminals, a type MOV varistor was placed between the collector and emitter of each IGBT. Those surges are originated when inductive loads are interrupted, more precisely, by the action of the output fuse or accidental opening of the circuit.

The varistors chosen are from LITTELFUSE, with reference V420LA20AP. They have a maximum clamping voltage of 1120 V and allow to dissipate 90 J of energy, [1]:

\( b) \) Zener’s Gate-Emmitter

To avoid possible disturbances of the trigger signal, which can lead to damage to the semiconductor (IGBT), Zener diodes (with \( V_z = 18 \text{ V} \) and maximum power of 1.3 W)) were used. Those diodes allow limiting the maximum voltage applied between the gate and the emitter, keeping the voltage within the limits defined by the manufacturer. This is presented in Fig. 3.

![Figure 3 – Zener Diode schematic.](image)

2) Aid Switching Circuits

\( a) \) Gate Resistor

The gate resistor (\( R_{\text{gc}} \)) serves to circumvent the non-idealities of the IGBT circuit. This resistor minimizes
oscillations caused by the parasitic inductances of the switching circuit and the input capacity of the IGBT, which together form an LC circuit. [2]

In order to obtain the dumping resistor it was necessary to compute the parasitic inductance. The parasitic inductance is given by (8), where $\mu_0$ represents the magnetic permeability of the air $4\pi \times 10^{-9}$ T cm, $d = 0.2$ cm, it is the distance between tracks (15 V Top layer - Bottom layer 0 V), $l = 6$ cm, it is the length of the track (including return) and $w = 0.1$ cm, it is the width of the track.

$$L_s = \frac{\mu_0 \times d}{2w}$$

Replacing the variables (8) by their values, it is computed (9):

$$L_s = \frac{4\pi \times 10^{-9} \times 0.2}{2 \times 0.1} = 12.57 \text{ nH/cm}$$

As the distance $l_{\text{Max}} \approx 6$ cm, then, inductance $L_s \approx 75.54$ nH.

The value of the input capacity $C_{\text{ies}}$ comes from the manufacturer's data and it has the value of (10):

$$C_{\text{ies}} = 1.43 \text{ nF}$$

The calculation of the resistor $R_G$ is done using the set of equations (11), which relate the input capacities and inductances with the quality factor $Q$, the angular frequency $\omega$ and the damping factor $\xi$. Equations (11) comes from analysis of RLC circuit.

$$Q = \frac{\omega L_s}{R_G}$$

Knowing that the damping factor takes the optimal value for $\xi = \frac{3\pi}{2}$, and relating it to the quality factor $Q$, results:

$$\xi = \frac{R_G}{2} \sqrt{\frac{C_{\text{ies}}}{L_s}} = \frac{1}{2Q}$$

With expressions (11) and (12) it is possible to obtain a minimum resistance of the gate, which is given by (13):

$$R_G \geq 1.44 \times \frac{L_s}{\sqrt{C_{\text{ies}}}} \geq 10.47 \Omega$$

The gate resistor to be used must have a value greater than the result computed in (13). In this work it has been selected the typical value of $R_G = 33 \Omega$.

b) Gate-Emitter Resistor

To prevent errors in the switching process (transition from ON to OFF state), which may lead to the destruction of the power circuit (i.e., short circuit), it is of utmost importance to ensure the proper discharge of input capacity. The discharge is guaranteed by introduction of a resistor $R_{\text{GE}}$ as illustrated in Fig. 5.

![Figure 5 - The input capacity discharge circuit.](image)

The calculation of the minimum value for $R_{\text{GE}}$ resistor is done using the relation that resistor and capacitor $C_{\text{ies}}$ have with the time constant $\tau$. Defining $\tau = 40$ ms - so that in case of a short circuit does not exist destructive consequences - the value for resistor $R_{\text{GE}}$ is:

$$\tau = R_{\text{GE}}C_{\text{ies}} \Rightarrow R_{\text{GE}} = \frac{\tau}{C_{\text{ies}}}$$

$$R_{\text{GE}} \geq \frac{40 \times 10^{-6}}{1.43 \times 10^{-9}} \geq 27.97 \text{ k\Omega}$$

In this work it was used a $R_{\text{GE}} = 29.4 \text{ k\Omega}$.

3) Power Loss

The most significant losses are caused by conduction and switching of IGBTs. The calculation is made using (16) and (17).

$$P_C = V_{\text{CEsat}} \cdot I_{\text{sat}} + R_{\text{on}} \cdot I_{\text{sat}}^2$$

$$P_{\text{COM}} = U_{\text{DC}} \cdot I_0 \left(\frac{\text{Tr} + \text{Tf}}{2T}\right) \cdot 1.3$$

Calculating and adding the losses in IGBT it is obtained the total power dissipated by the inverter, given by (18):

$$P_{\text{Total}} = 4(\, P_C + P_{\text{COM}}) = 106,36 \text{W}$$

C. Heatsink

The correct sizing of the heatsink is crucial for the proper
operation of the inverter, allowing IGBTs to operate within temperature limits defined by the manufacturer. The calculation is made using the heatsink analogy with an electrical circuit. In each surface, the heat flow that must flow across the surface, it is represented by an equivalent resistor. Using the characteristics of semiconductors, atmospheric conditions and the result obtained in (18) and equation (19), it is possible to compute the maximum thermal resistance. In this case the value of (20) is:

\[
T_j - T_A = (R_{th,L,C} + R_{th,C,S} + R_{th,S,A})B_d \tag{19}
\]

\[
R_{th,S,A} = \frac{T_j - T_A}{P_{D,tot}} - R_{th,C} - R_{th,C} = 0.29 \frac{\circ C}{W} \tag{20}
\]

D. Trigger Circuit

The trigger circuit is composed by the optocouplers, DC / DC converters and the delay circuit.

1) DC / DC Converters

The need to supply power to the optocouplers in order they operate correctly and ensure isolation between feedings, requires the use of DC / DC Converters.

2) Optocouplers

The use of this type of semiconductor lies in the fact that it is necessary to ensure the isolation of two circuits operating at different voltages, which are referenced to different grounds (trigger circuit and the IGBT circuit). Also, to prevent the circuit of IGBT to interfere (electromagnetic interference) with the operation of the trigger circuit, causing erratic switching. These semiconductors are powered by DC / DC converters.

3) Buffers and Delay Circuit

The buffers are used to make restitution of signal from the control PCB and isolate impedances. Between two buffers is located the RCD circuit responsible for creating the delay between the “ON” and “OFF” state, to ensure that in an arm does not exist two IGBT’s with “ON” state at the same time. Thus, it avoids short circuit of the direct current source with destructive consequences.

E. Complete Electric Scheme

\[\text{Figure 6 - Electrical schematic of the Power PCB.}\]

Modules description:
A. Buffers and Delay Circuit;
B. Trigger Circuit;
C. IGBT Modules;
D. Input Filter.

III. MODULATION AND CONTROLLING CIRCUIT

A. Modulation

In this work it was used Pulse Width Modulation (PWM) with three levels. Theoretically this type of modulation uses a modulating \(X_m\) with an average value of zero, and two triangular carriers \(X_p\) [2]. However, in practice it is difficult to ensure the timing of the two carriers, so it was chosen to use a variant of this type of modulation. So, the modulating instead of having an average value of zero, it is rectified and compared with a carrier as shown in Fig. 7 [3]. If the modulating is lower than the carrier, logic output takes the value zero, if the modulating is greater than the carrier output logic is one.

\[\text{Figure 7 - Modulation with one carrier \(X_p\) and one modulating \(X_m\).}\]

The output states of the IGBT are shown in Table 1, as a function of the output voltage and the polarity of the modulating. So, it is required to set (21):

\[
S_{ij}\begin{cases} 
"ON" & \rightarrow 1 \\
"OFF" & \rightarrow 0 
\end{cases}
\tag{21}
\]
Table 1 - Table with the states of the IGBTs.

<table>
<thead>
<tr>
<th>Positive alternation</th>
<th>Negative alternation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$X_n &gt; X_p$</td>
<td>$X_n &lt; X_p$</td>
</tr>
<tr>
<td>$</td>
<td>X_m</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output voltage $U_{DC}$</th>
<th>$0$</th>
<th>$0$</th>
<th>$-U_{DC}$</th>
<th>$0$</th>
<th>$0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{11}$</td>
<td>$1$</td>
<td>$1$</td>
<td>$0$</td>
<td>$0$</td>
<td>$1$</td>
</tr>
<tr>
<td>$S_{12}$</td>
<td>$0$</td>
<td>$0$</td>
<td>$1$</td>
<td>$1$</td>
<td>$0$</td>
</tr>
<tr>
<td>$S_{21}$</td>
<td>$0$</td>
<td>$1$</td>
<td>$0$</td>
<td>$1$</td>
<td>$1$</td>
</tr>
<tr>
<td>$S_{22}$</td>
<td>$1$</td>
<td>$0$</td>
<td>$1$</td>
<td>$0$</td>
<td>$0$</td>
</tr>
</tbody>
</table>

Table 2 shows the trigger logic of the arms of the converter obtained by comparing with the modulating with the carrier. Where, $\gamma_1 = 1$ represents $S_{11}$ on “ON” stage and $S_{12}$ on “OFF” stage, $\gamma_1 = 0$ represents $S_{11}$ on “OFF” stage and $S_{12}$ on stage “ON”, analogously, $\gamma_2 = 1$ represents $S_{21}$ on “ON”, state and $S_{22}$ on “OFF” state, $\gamma_1 = 0$ represents $S_{21}$ on “OFF” stage and $S_{22}$ on “ON” stage.

<table>
<thead>
<tr>
<th>Positive alternation</th>
<th>Negative alternation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$X_n &gt; X_p$</td>
<td>$X_n &lt; X_p$</td>
</tr>
<tr>
<td>$</td>
<td>X_m</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Logic output $X_m - X_p$</th>
<th>$1$</th>
<th>$0$</th>
<th>$1$</th>
<th>$0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage $U_{DC}$</td>
<td>$0$</td>
<td>$0$</td>
<td>$-U_{DC}$</td>
<td>$0$</td>
</tr>
<tr>
<td>$Y_1$</td>
<td>$1$</td>
<td>$1$</td>
<td>$0$</td>
<td>$1$</td>
</tr>
<tr>
<td>$Y_2$</td>
<td>$0$</td>
<td>$1$</td>
<td>$1$</td>
<td>$1$</td>
</tr>
</tbody>
</table>

Table 2 - Converter arms logic.

Comparing the previous table with Table 3, which is the truth table of a NAND logic gate type, it is easy to find that, from the comparison of modulating with the carrier, the signals $\gamma_1$ e $\gamma_2$ are obtained using a type NAND logic.

NAND logic gates used are from the manufacturer NXP with HEF4011BP reference.

**NAND gate**

Input$_{A}$ Input$_{B}$ Output

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0$</td>
<td>$0$</td>
<td>$1$</td>
</tr>
<tr>
<td>$0$</td>
<td>$1$</td>
<td>$1$</td>
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<td>$1$</td>
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</tr>
<tr>
<td>$1$</td>
<td>$1$</td>
<td>$0$</td>
</tr>
</tbody>
</table>

Table 3 – Logic of NAND gate.

$\gamma_1$, was obtained by applying to A (Input$_{A}$) the inverted, non-rectified modulant, and on B (Input$_{B}$), was used the logical result for $\gamma_1$, already presented in Table 2 (difference between $X_m - X_p$).

$\gamma_2$, was obtained by applying to A (Input$_{A}$) the inverted, non-rectified modulant and in B (Input$_{B}$), it was used the logic result for $\gamma_2$, already presented in Table 2 (difference between $X_m - X_p$).

**B. Controllers**

This work intended to control the supplied current provided by the inverter and the control of the input voltage. [4], [5], [6] [7], [8]

To make the current control and to ensure a quick response and zero steady state error, it was used a proportional integral compensator (PI) for the control of current, represented by (22).

$$C(s) = \frac{1+s\tau_z}{sT_p}$$

To the input voltage control it was also intended the annulment of the static error, leading again to the use of a proportional integral controller.

In order to apply the sized controllers, in both cases, it was used the schematic shown in Fig. 8.

**C. Signal acquisition circuit**

In the developed work there was the need to measure the different external data to the inverter itself so it was used a set of current transducers and voltage. Two voltage transducers were required: one for obtaining an image of the mains voltage and other, to give a measure of the value of the voltage at the input capacitor. It was also used a transducer current to determine the value of the current injected by the inverter in the network.

As an auxiliary to future applications it was allowed in the printed circuit board, drills for another current transducer. Direct connections of the signals measured by the transducers to the outside through BNC connectors, allowing connection to a DSP, where also included.

**D. Timing**

In order to ensure that the injected current is in phase with the voltage, it was necessary to include a circuit responsible for ensuring that synchronization. For that purpose it was used a multiplier that receives the signal (with 1 V of amplitude)
from the voltage supply transducer multiplying it by the reference given by the voltage compensator of the input voltage.

E. Complete Electric Scheme

![Electric schematic of control PCB.](image)

Modules description:
- A. Modulation;
- B. Current Control;
- C. DC Voltage Control;
- D. Timing;
- E. Network Voltage Transducer;
- F. Input Voltage Transducer;
- G. Injected Current Transducer.

IV. The project of Printed Circuit Boards

For the design of the printed circuit boards, the standards of good practice of IPC, compiled in "Association Connecting Electronics Industries", [9] were followed as a guide. The IPC-2221A "Generic Standard on Printed Board Design and the IPC-9592 "Performance Parameters for Power Conversion Devices", [10] have been used. It should be noted that the use of those standards is not mandatory, but rather a decision tool / guide that is based on a set of specifications that come from experience.

A. Spacing

The computation of the spacing of the copper power tracks was based on the good practice standards referred in IPC-2221A and IPC-9592. The standard IPC-2221A sets a minimum for spacing and IPC-9592 sets up the maximum for the track spacing. To ensure that the isolation between tracks is as effective as possible, it was defined a rule of design (DRC) that ensures, whenever possible, a minimum spacing of 3mm. However, this spacing should never be less than 0.8mm for voltages of 400V.

To the signals tracks (0 – 5 V or ±15V), both in the control circuit and in the trigger circuit, it was defined as minimum spacing d = 1mm, guaranteeing with this, a higher degree of insulation than needed.

B. Width of the tracks

Besides being relevant to determine the minimum spacing between conductors, it is also important to determine the minimum width recommended for the tracks, which can be obtained using the good practice guide IPC-2221A.

The width obtained for the tracks that deal with current intensities of 7.5A, is 5.3mm.

For tracks that support current intensities 13.05A the width is 8mm.

C. Design of the Printed Circuit Boards

The design of the printed circuit boards was carried out using the program ALTIUM DESIGNER, version 13.1. It was taken into account all the principles of good practice set out in the previous paragraph, as well as, help manuals; [11]; [12]; [13].

In order to minimize the effects that could jeopardize the operation of the system, there were considered a number of measures described below:
- It was used ground and power plans and eliminated the use of curves and connections between tracks with angles 90°, favored the use of 45°;
- On the top PCB - Control - it was used a ground plan 0V, both in the upper and lower layers, using a technique called "Via Stitching". This technique, besides helping in the reduction of parasitic impedances, increases the plate's immunity to noise. In the lower PCB – power - a ground plan 0V (Bottom Layer) and a plan of 5V (Top Layer) were used to facilitate the supply of semiconductors (delay, trigger and DC / DC converters);
- To reduce the high frequency interference in supply voltages of semiconductors, a set of capacitors (ceramic and tantalum), were placed at the entrance of the components and at the output of the power supplies;
- In order to facilitate the proper placement of components and to allow a good welding areas, it was attempted to maintain a relationship between hole and pad of 1.8 times. It was also guaranteed that this ratio means, at least 0.5mm, that relationship between the track / hole is less than 2.5 times and that the hole can not be less than the diameter of the component connection plus 0.1mm.
- Whenever advantageous, it was sought to overcome tracks of signals in different layers, in order to assist in the reduction of parasitic inductance;
- The inverter was divided into two plates: a control consisting of the transducers and controllers, and power
circuits with delay circuit, trigger circuit and power circuit. This division allowed the separation of signals with different reference grounds, different currents and voltages.

The implementation of the design involved the following steps:

- Design of the components footprint based on manufacturer information;
- Drawing of an electrical symbol for each footprint created;
- Design of electrical diagram of each PCI;
- Validation and compilation of the wiring diagram drawn;
- Creation of the design module for designing the layout of the PCB;
- Define a set of rules to help the placing and connection of components, in which are the spacing and width presented;
- Transfer the wiring diagram for the layout of the PCB;
- Placement of the footprint of the components at the desired location;
- Connecting the components following the links defined in the schematic, and validation of DRC (Design Rule Check);
- Confirmation of the component's footprint;
- Generation and extraction of the production files (Greber and NC Drill).

V. LABORATORIAL AND COMPUTER SIMULATION

A. Computer simulation

It was performed the computer simulation of control, triggering and power circuits. The simulation allowed to hit the responses of controllers and to verify correct operation of each circuit. Additionally, it allowed the comparison and validation of the results obtained in laboratory.

In Fig. 10 it is possible to see the result of the system simulation, where has been registered the follow-up phase of the injected current with the mains voltage.

In Fig. 11, it is recorded the evolution of the input voltage that confirms the proper operation of the input voltage controller. In Figure 12, it is shown the output voltage of the inverter ($V_{\text{PWM}}$).
B. Laboratory Tests to Single Phase Inverter

All this work led to the prototype shown in Fig. 13.

![Figure 13 – Built prototype](image)

To perform the testing of the prototype of the single phase inverter, the DC side was fed with rectified DC voltage. The output was connected to a charge that serves as a connection point to the network.

The following images were taken during the testing of the prototype:

![Figure 14 - mains voltage reference and the injected current.](image)

![Figure 15 - DC voltage](image)

By comparing the data obtain in the laboratory testing with the data obtained by computer simulation, it is possible to confirm the proper functioning of the proposed system.

In order to demonstrate the correct work of the controllers, the following figures were taken. In this figures it is possible to observe the error of the current controller (Yellow), and the voltage controller (Blue) for different variations of the DC side voltage (Purple).

![Figure 16 - Inverter output voltage ($V_{out}$).](image)

![Figure 17- Positive variation of the DC voltage. Current controller error (yellow); Voltage controller (Blue); DC voltage (Purple) and the injected current (Green).](image)
VI. CONCLUSION

This study aimed to design and construct of a single-phase inverter, which had as main characteristic the ability to provide power up to 3 kVA, being compact and versatile. The work involved the design and dimensioning of the different parts and their assembly. In parallel with the design and construction of the inverter was also performed a simulation of the overall layout as a way to measure several parameters simultaneously and as a comparison of the built prototype. As a conclusion, it can be said that these objectives were achieved.

In order to validate the work done, several tests were performed aiming to check the perfect functioning of the different constituent parts of the inverter as well as the global assembly. The results were, in turn, compared with those of the simulation, confirming in this way the correct functioning of the inverter.

REFERENCES