Abstract—This work is focused on the implementation of an integrated smart temperature sensor in CMOS technology. The most accurate existent temperature sensors consist of an analog frontend, used for temperature sensing, followed by a $\Sigma\Delta$ analog-to-digital converter. The main objective of this work is to propose an alternative technique of implementing the $\Sigma\Delta$ ADC. This technique avoids the design of an operational amplifier, as well as the offset voltage compensation circuit usually implemented to reduce measurement errors. This alternative technique presents a comparator-based circuit, consisting of a dynamic comparator followed by a current source, which replaces the operational amplifier (OpAmp). As this comparator-based circuit is only turned on during short periods of time, it presents no static power consumption, thus lowering power consumption when compared to an OpAmp-based topology. The circuit is first studied at a high-level, in order to confirm the validity of this solution. The transistor level circuit is designed as well as its respective layout. Simulation results show a non-linearity at the digital output of the smart temperature sensor, which result from undesired charge injection at its input. Nevertheless, the proposed topology proves to be a good alternative for these types of circuits when low power consumption is preferred to accuracy.

Keywords – Smart temperature sensor, $\Delta \Sigma$ ADC, Comparator-based circuit, Low-power

I. INTRODUCTION

Temperature sensors are nowadays used in a wide range of applications, from regular thermometers to the most advanced monitoring systems. As analog sensors (thermistors, mercury thermometers, or bimetallic thermometers) make sense in some cases, like thermostats, digital temperature sensors are more suited to applications with digital processing. Temperature sensors are, hence, widely applied in measurement, instrumentation and control systems. Thus, it is fundamental to fabricate sensors in integrated circuit technology with a digital output. An integrated digital temperature sensor can easily communicate with a microprocessor, allowing it to collect data and to make decisions providing different types of outputs.

Being temperature an analog physical quantity, the sensor is usually combined with an analog interface which reflects its variation into the system. If this input is translated into a digital format (e.g. by means of an analog-to-digital converter), the system is classified as a smart temperature sensor.

The implemented sensor is based on a bipolar junction frontend, which is the key element for sensing the temperature variation, followed by a first-order $\Sigma\Delta$ analog-to-digital converter (ADC) that produces a digital bitstream which is, then, converted into a digital word by a digital backend. The circuit is developed in UMC 130nm CMOS technology, which allows the temperature sensor to be integrated into VLSI chips, reducing fabrication cost and measuring on-chip temperature directly.

In this paper, the study and development of a high accuracy smart temperature sensor, using a comparator-based switched capacitor (CBSC) circuit is performed. The goal is to implement a low-power circuit by eliminating static power consumption commonly absorbed by the OpAmp used in $\Sigma\Delta$ A/D converters. This reduces the circuit overall power consumption, area and, therefore, cost. Also, reducing the supply voltage affects directly the swing and gain of amplifiers. Avoiding its use also prevents the design of a high-gain amplifier with a low supply voltage.

II. TEMPERATURE SENSOR DESIGN

The architecture of the implemented smart temperature sensor is shown in Figure 1.

![Smart temperature sensor architecture](image)

Figure 1 - Smart temperature sensor architecture

A. Sensor frontend:

In this work the analog sensor front-end of the circuit is based on a single $n$-$p$-$n$ bipolar transistor, biased alternately with two different bias currents. Therefore, two different $V_{BE}$ voltages are created and a PTAT voltage ($\Delta V_{BE}$) is originated at the input of the $\Sigma\Delta$ modulator. This voltage is given by

$$\Delta V_{BE} = \frac{kT}{q} \ln(p) = \frac{kT}{q} \ln\left(\frac{I_{C2}}{I_{C1}}\right) \quad (1)$$

The use of a single BJT transistor eliminates errors due to process spread variations. Also, as the current source with
higher value is constantly switched on and off, there is no static current flow in one of the biasing branches. This reduces significantly the overall power consumption of the circuit.

### B. OpAmp-Based Modulator:

A typical OpAmp-based switched capacitor ΣΔ modulator is represented in Figure 2.

![Figure 2 - OpAmp-based modulator](image)

The collector of the bipolar junction transistor is connected to the sampling capacitor of the modulator. In this topology, the ΣΔ modulator consists of an OpAmp working as an integrator followed by a latch comparator. The output of the modulator, $bs$, is determined by the comparator and the feedback action is performed by a 1-bit DAC which controls the system stability through at the feedback capacitor $C_F$.

The charge transfer from the input of the OpAmp to its output is promoted by the virtual ground condition at its input node, $V_x$. As the voltage reaches $V_{REF}$, the charge that was stored in $C_I$ is entirely transferred onto $C_F$. During the charge transfer the output voltage, $V_o$, settles exponentially to its steady-state value as shown in Figure 3.

![Figure 3 - Evolution of $V_o$ during the charge transfer phase](image)

The settling time of the system is determined by the time-constant of the circuit during the charge transfer phase. The accuracy of the output depends on the accuracy of the OpAmp to force the virtual ground condition during the charge transfer phase.

OpAmp-based modulators require high gain amplifiers to improve the accuracy of the system output [11]. However, the tendency of CMOS technologies to reduce dimensions and power consumption results on a reduction of the intrinsic device gain and signal swing. This affects the design of operational amplifiers and, although different topologies and techniques have been developed to contour these issues (multiple stage, cascoding, gain-boost), these designs also face several tradeoffs (e.g. higher power consumption) and are not always simple to implement.

### C. CBSC-Based Modulator

Figure 4 presents a ΣΔ modulator implemented with a single-ended comparator-based circuit (CBC).

![Figure 4 - Comparator-Based switched-capacitor ΣΔ Modulator](image)

The comparator-based circuit consists of a continuous-time comparator controlling a current source at its output. This module replaces the operational amplifier on the modulator. The behavior of the circuit during the sampling phase is the same as when using the OpAmp. Figure 5 depicts the modulator behavior during the charge-transfer phase, $\Phi_2$.

![Figure 5 - Operation of the Comparator-Based Circuit during the charge-transfer phase](image)

At the beginning of the charge-transfer phase $\Phi_2$, a short preset to the output voltage $V_O$ is performed. This phase is identified with $\Phi_{2p}$, and lasts only long enough to set the output node of the comparator to $GND$. This preset is performed to ensure that $V_x$, at the input of the comparator, is set below the reference voltage $V_{REF}$. When $\Phi_{2p}$ ends, the output node is disconnected from $GND$ and starts to be charged linearly by the current $I_o$. This voltage ramp is reflected in the input node $V_x$, through the capacitor $C_I$. Hence, $V_x$ also rises linearly due to the increase of charge on $V_O$. When $V_x$ crosses $V_{REF}$, the comparator output turns to high, switching off the current source. This causes the charge at the input and output nodes to maintain their current voltages. Assuming a negligible comparator time response, the voltage $V_{OF}$ is defined by the capacitances used in the
circuit and the output voltage is the same as when using an OpAmp in the modulator.

The response time of the dynamic comparator causes a delay between the instant that $V_s$ crosses $V_{REF}$ and the instant when the current source is shut down. This leads to an error at the output node, which does not settle exactly at $V_{OF}$ voltage. The response time of the dynamic comparator causes a delay between the instant that $V_s$ crosses $V_{REF}$ and the instant when the current source is shut down. This leads to an error at the output node, which does not settle exactly at $V_{OF}$ voltage. Although this overshoot effect is unavoidable, in circuits working at lower frequencies, low currents can be used and still guarantee that the input voltage reaches $V_{REF}$ before the charge-transfer period ends. A lower current generates slower slopes on both $V_O$ and $V_s$, which reduces the overshoot effect, minimizing the voltage error due to the comparator delay.

In this comparator-based modulator design, the instant when the input node $V_s$ crosses $V_{REF}$ is detected by the comparator, instead of forcing the virtual ground condition ($V_s = V_{REF}$) with an OpAmp. As the output voltage is, in both designs, defined by the capacitances of the modulator, this comparator-based circuit can be a more power efficient solution than the OpAmp. The dynamic comparator is only turned on during a short period of the charge-transfer phase. This is the period during which the output current source is also on (period between the start of $\Phi_2$ and the moment when $V_s$ crosses $V_{REF}$). Hence, both the comparator and its output current source only dissipate power during the time required, enhancing the power efficiency of the circuit.

D. Digital backend

At the back-end of the sensor, the digital block converts the output of the modulator into a digital word. The serial sequence of ones and zeroes that results from the $\Sigma\Delta$ modulation is, then, converted into a parallel combination of ones and zeroes that represents the digital word at the output of the smart temperature sensor. To perform such conversion, the implementation of a binary synchronous counter is mandatory.

For an $n$-bit resolution, the circuit requires $2^n$ sampling periods to perform one entire conversion. Therefore, the best achievable resolution is $1$ part of $2^n$.

<table>
<thead>
<tr>
<th>Resolution</th>
<th>10 bit</th>
<th>12 bit</th>
<th>16 bit</th>
<th>18 bit</th>
<th>19 bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Periods</td>
<td>1024</td>
<td>4096</td>
<td>65536</td>
<td>282144</td>
<td>524288</td>
</tr>
</tbody>
</table>

Table 1 - Sampling periods and conversion time for different resolutions and sampling frequencies

The different conversion times reflect that it is possible to perform temperature measurements with sampling frequencies from 500 kHz up to 1 MHz, with resolutions up to 19 bit. Although a converter operating at $F_S = 500$ kHz presents acceptable conversion times, the lower frequency leads to an increase of current leakage on the switches, which affects the linearity of the converter. A frequency of 1 MHz reduces this effect. Using this frequency, a 12-bit converter promotes a good relation between conversion time, resolution and power consumption.

III. CIRCUIT IMPLEMENTATION

The circuit is based on an analog frontend creating the input voltage for the $\Sigma\Delta$ modulator, which is implemented with a comparator-based circuit. The back-end of the circuit is a 12-bit binary counter, presenting a temperature-dependent digital word at its output.

A. Bipolar Frontend

The analog frontend of the proposed circuit consists of a single bipolar junction transistor biased alternately by two different currents. The implemented frontend is represented in Figure 6 and requires two external biasing currents.

Figure 6 - Implemented analog sensor frontend

In this figure, $C_{Load}$ represents the input of the $\Sigma\Delta$ ADC. Different currents produce different base-emitter voltages. Simulations with different currents were performed in order to analyze not only $\Delta V_{BE}$ linearity with temperature, but also its power consumption. Currents of 30µ and 1µA were chosen, producing a current ratio of $p=31$ and a non-linearity below 0.2% throughout the temperature range. All transistors are implemented with a 1µm channel-length. Transistors from $M_1$ to $M_4$ use 5µm and $M_5$ uses 20µm channel-width.

B. Comparator-Based Circuit

The schematic of the dynamic comparator used in this work is shown in Figure 7.
This comparator is based on two NMOS transistors ($M_1$ and $M_2$) working as a pre-amplifier and a positive feedback PMOS circuit. Transistor $M_3$ works as a latch, switching off the comparator during the sampling phase in order to reduce power consumption. Given the sensitivity of this circuit to parasitic charges, minimum length transistors are used at the input stage as well as on the feedback circuit to minimize parasitic capacitances. To obtain an accurate result, symmetry and transistor matching here are mandatory. Transistors $M_1$ and $M_2$ use a 10\,μm channel-width. Transistors $M_3$, $M_4$ and $M_5$ use 5\,μm and $M_6$ and $M_7$ use 1\,μm channel-width.

In order to amplify the output signal of the comparator to a rail-to-rail signal a sequence of buffers is connected to the output of the comparator, as shown in Figure 8.

The current source, controlled by the output of the comparator is implemented by a simple current mirror, as shown in Figure 9.

An external current source of 10\,μA is used to set the integration current during the charge-transfer phase. The current mirror is implemented by $M_1$ and $M_2$, which are turned on and off by transistor $M_{PD}$. This power-down transistor is connected to the output of the comparator block, so that the current source is shut-down when $V_{in,p}$ crosses $V_{REF}$. All transistors use a channel length of 1\,μm and channel width of 5\,μm.

**C. Output Latch-Comparators:**

As depicted in Figure 1, the ΣΔ modulator requires a comparator at its output. The goal of this comparator is to decide whether the output of the integrator is higher than $V_{REF}$ after each integration. Figure 10 illustrates the implemented latch comparator.

While the comparator used in the comparator-based integrator operates dynamically – its output varies during the time the comparator is on - this circuit compares the inputs at the instant that the Latch input is set to “1”. All transistors used in this block are implemented with minimum channel length (120nm) and a width of 1\,µm.

This comparator, however, has the disadvantage that its output is only valid when the comparator is on. As the Latch input is set to “low”, the comparator is disabled and $V_{out,N}$ is connected to GND. To eliminate this problem, a flip-flop is required at the comparator output.
D. Switches:

There are three types of switches implemented in the presented circuit. For increased performance, NMOS switches were used to connect nodes to GND (Pull-Down) and PMOS switches to implement connections to V\text{DD} (Pull-Up). Connections to intermediate voltages (e.g. \text{V}_{\text{REF}}) were implemented with CMOS transmission gates in order to decrease the effective resistance when the switch is conducting. To compensate charge injection at the sources and gates of the switches, two dummy transistors are introduced at the input and output of the switch. Figure 11 depicts this implementation for a NMOS switch.

![Figure 11 - NMOS Switch](image)

The source of each dummy transistor is connected to its drain. The transistors are, then, in the cutoff region having no impact on the operation of the switch. However, each dummy transistor introduces two extra capacities (C_{\text{GS}} and C_{\text{GD}}). As the gates of these transistors are connected to a complementary phase, a current will flow in the opposite direction through the capacitances of the dummy transistors. Each of these transistors must have half the size of the main switch transistor. This ensures that the current injected in the drain of M\textsubscript{1} is absorbed in transistor Dummy\textsubscript{1} and the current injected in the source of M\textsubscript{1} is absorbed in transistor Dummy\textsubscript{2}.

E. 12-bit Binary Counter:

The backend of the presented circuit consists of a 1 MHz 12-bit binary counter, to convert the bitstream into a final digital word. This block consists of three 4-bit binary counters connected in series. The design of the 4-bit counter is shown in Figure 12.

![Figure 12 – A 4-bit synchronous counter](image)

All transistors used to implement this counter use minimum channel length of 120nm. The NMOS transistors use a channel width of 160nm and the PMOS transistors a 480nm width.

F. Multi-Phase Generator

This block is based on a typical non-overlapping phase generator followed by two additional delay equalizer circuits. This delay equalizer circuit is re-used in this block, in order to create two complementary phases (\Phi_{1,N} and \Phi_{2,N}), required for additional control of the switched capacitor circuit. Figure 13 shows the implemented phase generator.

![Figure 13 - Multi-Phase Generator](image)

All PMOS transistors are implemented width and the NMOS transistors with 1µm channel width. Inverters I\textsubscript{4} and I\textsubscript{5} use 360nm channel length, which is higher than the 240nm used in the remaining components. This is done in order to promote better load driving into the Delay Equalizer blocks.

IV. Simulation Results

To analyze the performance of the smart temperature sensor, a linear regression was applied to the results obtained over the proposed temperature range. Hence, it is possible to evaluate how linear the output of the sensor is when submitted to a linear variation in temperature.

![Figure 14 - Full sensor output (blue) vs. Relative error (red)](image)

The error relative to the linear regression applied is calculated through Equation 1.

\[
\text{error} \% = \frac{\text{Linear Regression}}{\text{Regression}} \times 100
\]
As can be observed, there is a non-linearity of the overall sensor throughout the temperature range. To analyze the source of the sensor non-linearity, the ΣΔ-Analog-to-Digital converter is characterized separately from the analog BJT frontend. Therefore, for the following simulation, the frontend was replaced by an ideal voltage source, which simulates $AV_{BE}$ at the input of the ADC. The results are presented in Figure 15.

![Figure 15 - ΣΔ ADC response to linear input (blue) vs. Relative error (red)](image)

The relative error of the ADC is below ±0.06%, showing that the non-linearity of the converter is smaller than the one verified in Figure 14. This means that the source of the complete temperature sensor non-linearity comes mostly from the bipolar frontend and not from the ΣΔ ADC itself. The abrupt current switching at the converter input affects directly the precision of the sensor, as it increases the noise at the input of the modulator.

A resolution of 0.23°C was obtained throughout the temperature range. Temperature variations below this value are, thus, not reflected at the output of the sensor.

The power consumption achieved for this smart temperature sensor using a 1.2V power supply varies from 112.1μA at -55°C to 135.7μA at the maximum operating temperature of 150°C.

The layout of the implemented sensor is shown in Figure 16 and occupies a die area of 55μm x 55μm = 0.009mm².
V. CONCLUSIONS

This paper describes the design and implementation of a low-power smart temperature sensor using a comparator-based ΣΔ modulator, in 130nm CMOS technology.

An operation range from -55 to 150°C was achieved, which is wider than the military range. Below and above these limits, a strong non-linearity is noticed.

The obtained resolution for this sensor is 0.23°C. A non-linearity of +2% to -1.5% is noticed throughout the temperature range. This non-linearity is originated due to the current switching at the sensor frontend, which causes undesired charge injection at the input of the ADC. This affects directly the sensors’ accuracy, hence limiting the variety of applications in which it can be used. For high precision applications, where good performance is mandatory, a sensor with improved accuracy is required.

Although the achieved accuracy of the implemented smart temperature sensor was below expected, nowadays power consumption may have the same importance as accuracy. In some cases, like battery supplied applications or autonomous systems, more importance at all. The implemented sensor consumes typically 114μA in a 4.046ms conversion time. As temperature is considered a very low frequency input, this smart temperature sensor can be integrated on such types of applications as long as it is not constantly operating and elevated accuracy is not required.

The introduced technique of implementing a ΣΔ analog-to-digital converter using a comparator-based circuit presents several advantages when compared to the typical OpAmp-based topology. The typical offset error present in circuits using operational amplifiers usually requires offset compensation techniques. Avoiding the implementation of an OpAmp the design of the modulator is simplified and no offset compensation circuit is required. The low operating frequency of the modulator, 1 MHz, guarantees that the error introduced by the comparator delay is minimal. Also, the latch controlled dynamic comparator is only switched on during the necessary period of time, presenting no static power consumption. These advantages contribute to a low power ΣΔ ADC with high linearity and resolution.

REFERENCES