All-Digital Phase Locked Loop for Bluetooth Low Energy Transmitters

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Abstract— **This paper presents a low power ADPLL architecture in CMOS 130nm for the Bluetooth LE standard. It uses direct modulation of the Digitally Controlled Oscillator (DCO), taking advantage of its very low frequency drift. The ADPLL is opened during the transmission of BLE packets while the tank capacitance is directly modulated. An algorithm controlling the loop convergence reduces the locking time. Due to relaxed BLE requirements the traditional Time-to-Digital Converter in ADPLL is avoided.**

Keywords— All-Digital Phase-Locked Loop (ADPLL), Frequency Synthesizer, Bluetooth Low Energy, Gaussian Frequency Shift Keying (GFSK), Digitally Controller Oscillator (DCO).

I. INTRODUCTION

Wireless communications have grown at an astonishing way due to its reliability and ease of use. This fact has led to growth in research related to communication circuits and architectures. Particularly in wireless sensors applications issues like low-cost, low-voltage, low-power and high level of integration have received a great deal of attention.

Bluetooth Low Energy was recently introduced for low-power systems taking advantage of relaxed specifications comparatively to other communication protocols. Deep-submicron CMOS processes use low supply voltage (at and below 1.2 V) but still relatively high threshold voltages (about 0.5 V). Thus, the available voltage headroom is insufficient for high performance analog functions. On the other hand, the timing accuracy is excellent due to the very high speed of the devices, leading to a new paradigm: *In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals* [1].

II. ALL-DIGITAL PHASED-LOCKED LOOP

The operation is split into two stages. Firstly, in the acquisition stage, the ADPLL is set to the desired channel frequency. Secondly, during the transmission of BLE packets, the loop is opened and the tank capacitance of the oscillator is digitally modulated by the transmit data. The operation in open loop brings two main advantages. Firstly, the baseband blocks are turned off during the transmision of BLE packets allowing to save power, secondly there are no reference clock induced spurs. The major drawback, comparatively to closed loop ADPLL, is the higher low frequency phase noise because the oscillator noise is not filtered, but it still meets Bluetooth LE specifications.

Figure 1 shows the block diagram of the ADPLL. The *Digitally Controlled Oscillator* (DCO) frequency is digitized in a counter (phase accumulator). It is then retimed to the reference clock and compared to the desired frequency, FCW.
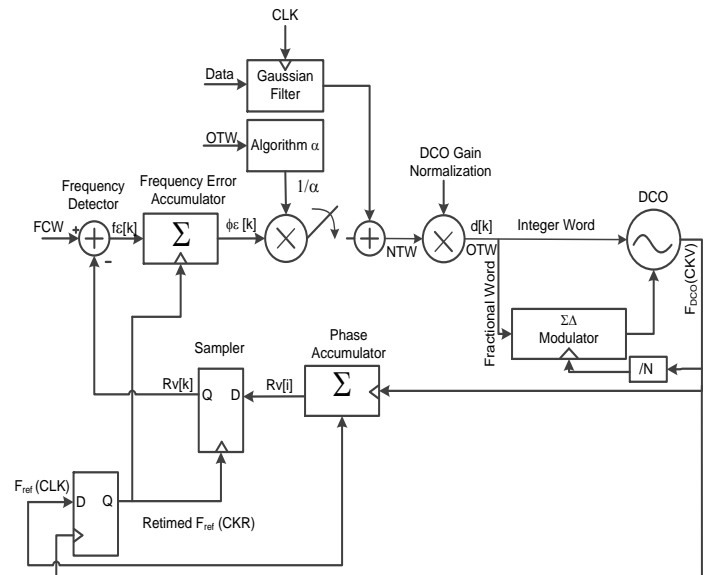

Figure 1 - ADPLL Architecture.

FCW is defined as fractional frequency division ratio $FCW = CKV / F_{ref}$, where *CKV* is the desired output frequency and F_{ref} is the frequency of the reference clock. The frequency resolution can be set by changing the word-length of the *FCW* fractional part.

The frequency error, $f_\varepsilon[k]$, is multiplied by the loop gain, alpha. The variable $\phi_\varepsilon[k]$ is determined by the accumulation of $\alpha * f_\varepsilon[k]$ every cycle of F_{ref} and then normalized by the DCO gain (K_{DCO}), which is obtained by calibration.

The ADPLL architecture is a first-order loop rather than a more typical second-order. In fact, the 1st order ADPLL has a faster start-up time. A second-order PLL allows to better filter-out the DCO noise and to better remove spurs, but during data transmission the loop is open anyway and those

advantages are immaterial. Besides, a first-order loop leads to lower consumption due to the reduced number of blocks.

III. DIGITALLY CONTROLLED OSCILLATOR

The DCO uses an LC tank with resonance controlled digitally by switched-capacitors. Figure 2 shows the basic DCO schematic.
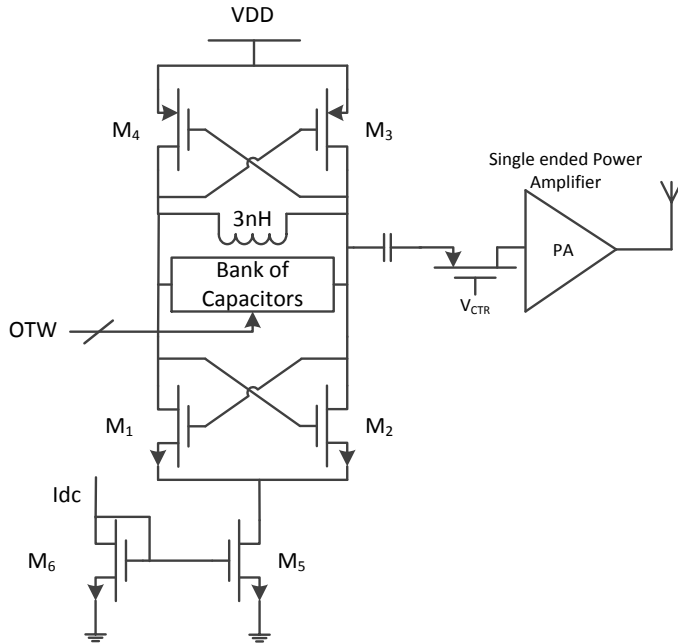
Figure 2 - DCO schematic with Power Amplifier.

Due to its switched nature, its frequency drift is very low compared with VCOs that have an analog control voltage. That property together with the short length of Bluetooth LE packets (below 350us) allows for its operation in open-loop during transmission [3]. Furthermore, a DCO has potentially less phase noise than a comparable VCO, since the control is not susceptible to amplitude noise and analog disturbances [4].
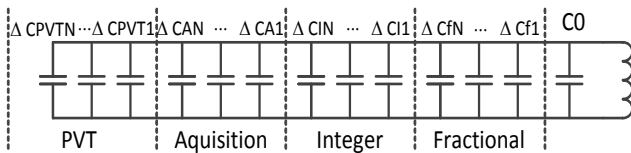
Figure 3 - Bank of Capacitors.

Figure 3 presents the bank of capacitors and it is split into three tanks that are sequentially activated. The first bank has coarse steps and is used during the process-voltage-temperature (PVT) calibration. The second bank has smaller steps and is used during the lock acquisition. The third bank (integer plus fractional) has the finest steps and it is used for fine tuning and for data modulation.

The smaller capacitance available in the technology (17 fF) is not enough for the BLE resolution requirements. Therefore, a digital sigma-delta modulator is used to dither the fractional part over a F_{ref} cycle on the tracking bank of capacitors. The clock for the digital sigma-delta is obtained directly from the DCO through a divider by 8.

During the transmission the loop is opened and the phase noise is not filtered-out. The required phase noise can be calculated from the interferer profile of receiver specifications [5],

$$\text{Phase Noise (dBc/Hz)} = \text{Psig-Pint-SNRmin-10 log(BW)} \quad (1)$$

where Psig is the signal power, Pint is the interferer signal power and the BW is the bandwidth of the signal. For the most strict case of BLE ($\geq$ 3MHz) the specification is -105dBc/Hz.

Figure 4 shows the simulated phase noise and BLE mask. With about-120 dBc/Hz at 3Mhz it achieves a margin of 15dB to the spec. The DCO consumption is 440 μW with 1.2V supply.
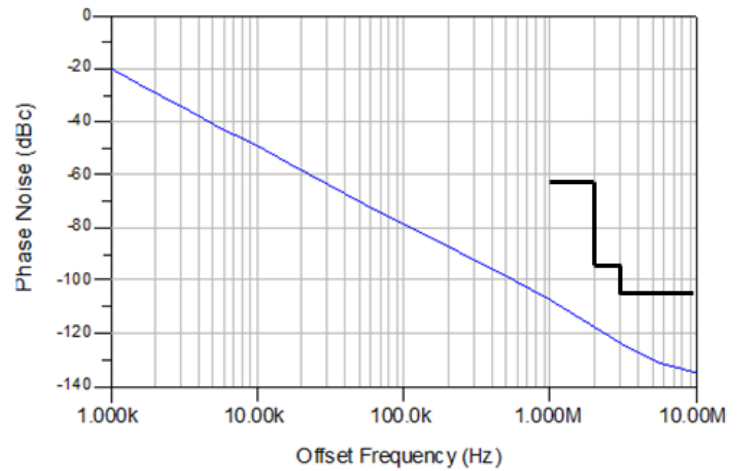
Figure 4 – Simulated phase noise of DCO with BLE mask.

IV. LOCKING ALGORITHM

Since no time-to-digital converter is used in the loop feedback, the digitization of the oscillating frequency is truncated to integer multiples of $Fref$. Special care is therefore required for achieving fine frequency resolution and a fast lock acquisition.

The loop gain, alpha, controls the loop convergence. Higher values lead to a faster convergence to lock, lower values lead to finer resolution. Therefore, by progressively reducing alpha along the frequency acquisition process it is possible to minimize the setup time and achieve the required resolution. The multiplication by alpha is placed before the accumulator to allow its value to be changed without causing any disturbances in the DCO control signal.

The locking algorithm controls alpha and is based on monitoring the oscillator tuning word (OTW) which, during acquisition shows successively lower ripples. The control

machine uses a peak/valley detector and a gradient polarity indicator to identify the ripples. $\overline{OTW}$ is expressed as the average of successive peak and valley values,

$$\overline{OTW} = \frac{OTW_p + OTW_v}{2} \qquad (2)$$

Consecutive $\overline{OTW}$ values are compared and used to estimate the residual error. The value of alpha is recurrently divided by two as the residual error is reduced until the value corresponding to the required resolution is achieved. The update intervals are also progressively lengthened as alfa reduces to keep accuracy and avoid loop divergence.

Figure 5 depicts the ADPLL lock acquisition behavior with the DCO quiescent frequency of 2.4 GHz and the desired frequency of 2.418 GHz. In worst case, lock is achieved in less than 50 μs with a resolution of 32 kHz using a reference clock of 16 MHz.
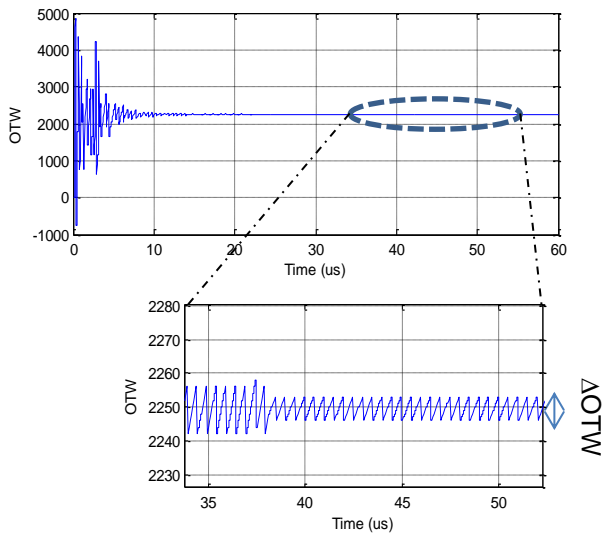

Figure 5 – Settling time of ADPLL.

The OTW LSB has to be 8 kHz to achieve the desired resolution. Thus, the ideal DCO gain is,

$$K_{DCO} = \frac{8000}{LSB} \qquad (3)$$

When the OTW word is saved, it can be any word between ΔOTW, as the Figure 5 depicts. However, taking into account the DCO gain and the DCO quiescent frequency,

$$F_{DCO\max} = 2.4e9 + 2254 * 8000 = 2.418032 \, GHz$$

$$F_{DCO\min} = 2.4e9 + 2246 * 8000 = 2.417968 \, GHz$$

Which gives an frequency error of ±32 kHz.

Table 1 presents the baseband blocks ADPLL results after layout (*.gds). The RF blocks (DCO, Retimer and DCO) performance are not present in this table.

Table 1 - Specifications Summary by simulation - ADPLL Base-band blocks

Item	Simulation after *.gds
Gate Area [μm²]	3.84
Gate Number	1973
Cells	538
Total Area [μm²]	7577.6
Total Internal Power [μW]	48.95
Total Switching Power [μW]	27.73
Total Leakage Power [nW]	2.585
Total Power [μW]	79.27

V. GAUSSIAN FILTER

To limit the bandwidth occupied by the modulated RF spectrum according to the standard, the symbols are pulse-shaped before transmission. BLE requires a Gaussian filter with parameters $BT_s = 0.5$ and $T_s = 1\mu s$, corresponding to the impulse response h[k] expressed as

$$h[k] = \frac{\sqrt{2\pi}}{\sqrt{\ln(2)}} \frac{BT_s}{T_s} exp\left[-\left(\frac{\sqrt{2\pi}}{\sqrt{\ln(2)}} BT_s \frac{k}{OSR}\right)^2\right] \qquad (4)$$

where T_s is the symbol period, B is the 3-dB bandwidth, and $OSR = f_R / (1/T_S) = 16$ is the symbol oversampling ratio by the sampling clock [5].

Since the input data is one-bit signal at the non-oversampling rate, it is possible to greatly simplify the implementation. The allowable transmit spectrum mask is shown in Table 2 and it determines the amount of simplification of the filter coefficients. The coefficients were truncated to canonical form with typically 3 non-zero bits. Figure 6 depicts the filter response for a sequence 001011 and 110100.

Table 2 - Transmit Spectrum mask.

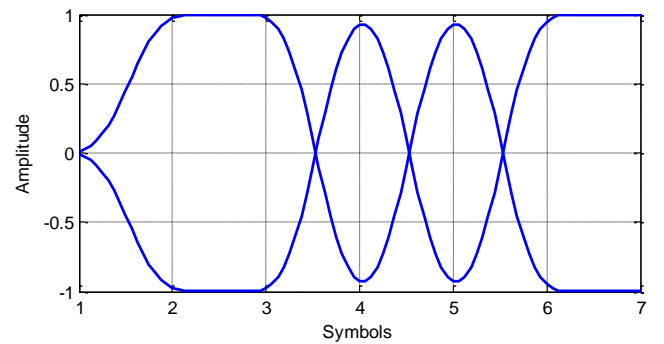| Specifications		Results
Frequency offset	Spurious Power	Spurious Power
2 MHz	- 20 dBm	- 23.61 dBm
3 MHz or greater	- 30 dBm	- 30.90 dBm

Figure 6 - Output of the GFSK transmitter filter for a sequence 00101011

The figure shows that the frequency deviation is always greater than 80%, satisfying the BLE specification.

Figure 7 depicts the filter response. The BLE standard specifies the adjacent channel power at 2 MHz and 3 MHz from the carrier, measured in 1 MHz bandwidth. The results are shown in Table 2.
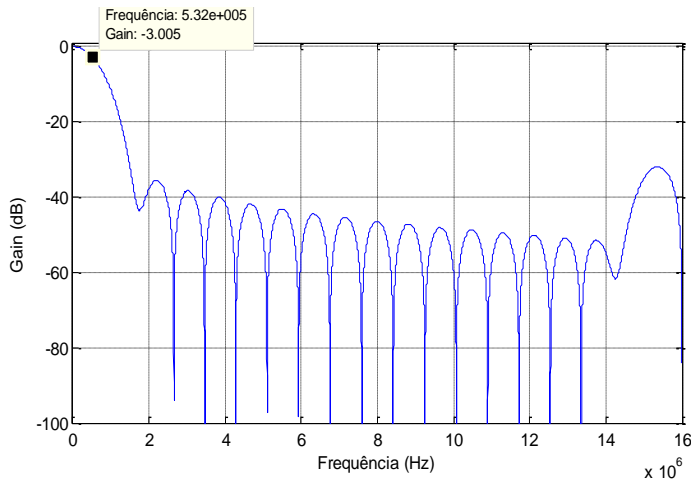

Figure 7 - Filter Response

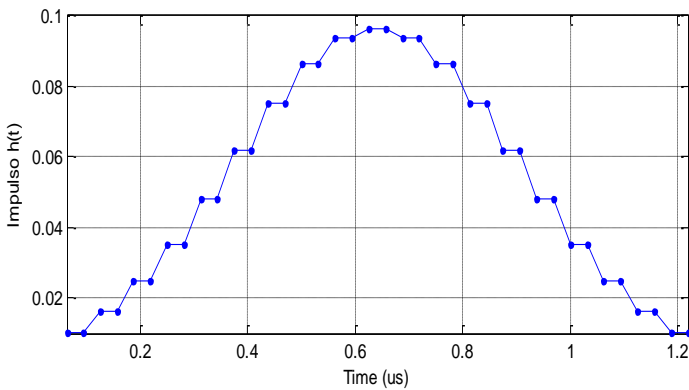Figure 8 presents the Gaussian filter impulse response.

Figure 8 - Impulse Response

Table 3 presents the Gaussian filter results.

Table 3 - Specifications Summary by simulation - Filter

Item	Simulation after *.gds
Gate Area [μm^2]	3.84
Gate Count	1313
Cells	396
Total Area [μm^2]	5044.5
Total Internal Power [μW]	46.85
Total Switching Power [μW]	39.44
Total Leakage Power [nW]	30.61
Total Power [μW]	86.29

VI. CONCLUSIONS

We presented a frequency synthesizer for Bluetooth LE transmitters. It uses a 1st order ADPLL for lock acquisition and during the transmission the loop is opened and the data modulates directly the DCO through a pulse-shaping filter. This allows to reduce the current consumption by having most blocks shut-off during transmission. This implementation is only possible due to the low frequency deviation of the DCO, because its control is digital.

Due to removal of TDC block this systems presents a settling time 10X bigger than [3], however it uses only a third of the time windows provided by the standard.

The system power consumption is about 605 μW. Both counter and retimer were not implemented in CMOS and, since they operate at RF frequency, the power consumption is significant. According to [3], the counter has power consumption about 1 mW.

REFERENCES

[1] Robert Bogdan Staszewski et al., "All-Digital TX Frequency Synthesizer and Discrete-Time REceiver for Bluetooth Radio in 130 nm CMOS," *IEEE Journal Solid-State Circuits,* vol. 39, pp. 2278-2291, Dec. 2004.

[2] Nam-Jin Oh et al., "Building a 2.4-GHZ radio transceiver using IEEE 802.15.4," *Circuits and Devices Magazine, IEEE,* vol. 21, pp. 43 - 51 , Jan. 2006.

[3] Jens Masuch et al., "A sub-10 nJ/b +1.9-dBm output Power FSK Transmitter for Body Area Network Applications," *IEEE Transactions on Microwave Theory and Techniques,* vol. 60, pp. 1413-1423, May 2012.

[4] Robert B. Staszewski et al, "Digitally controlled Oscillator (DCO)-Based Architecture for Frequency Synthesis in a Deep-Submicrometer CMOS Process," *IEEE Transactions on Circuits and Systems - II: Analog and Digital signal Processing,* vol. 50, pp. 815-828, Nov. 2003.

[5] Robert B. Staszewski et al., "ALL-Digital Frequency Synthesizer in deep-submicron CMOS, " 2º ed., A John Wiley & Sons, Inc., 2006.