Ultra Low Power Capless Low-Dropout Voltage Regulator

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Thesis to obtain the Master of Science degree in Electrical and Computer Engineering

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June 2013
In memory of my Grandfathers who were, and still are today, my biggest sources of inspiration and admiration. To their rich and fulfilled lives and above all, to the lessons they shared with their family on the way.

João Aníbal Pereira

Martiniano Santos
First of all, I would like to express my deepest gratitude to my advisors Professor Marcelino Santos and Professor Júlio Paisana, for all the guidance given, for all the patience shown throughout my Master Thesis and above all, for the time they spent investing in me as a Person and as an Electrical and Computer Engineer. I would also like to add that, for me, it was an honor to work with such a team, in such a professional environment and with such a challenging low power, low quiescent current subject. Thank you for this opportunity.

I would also like to thank to Jorge Esteves for accepting me in his high-tech power management team, for the colossal patience he had with me while sharing important intelligence/inputs/skills and for being an extraordinary colleague and friend.

I would like to extend my thanks to the colleagues I worked with, in INESC-ID, Carlos Moreira, Pedro Braga, Pedro Neves, Maria Barradas, Mário Ribeiro and Miguel Neto for their inputs, lively conversations and friendship. I can not fail to thank to Eng. Floriberto Lima, José Proença, Bruno Jacinto, Tiago Moita and the rest of Silicon Gate team for the support and for powering my successes.

In a more personal note, I would like to express a special thanks to Pedro Lamy, Jorge Marcelo and Tiago Moura for being the awesome guys they always were and for igniting my life with interesting challenges and projects.

I would also like to express my deepest gratitude to families Cunha e Sá, Teixeira, Arraiano and Freire for always being there for me, for their inputs and support.

To my Family, to whom I owe the most, I would like to thank them for all their unconditional love, support and encouragement given to me throughout my course and Master Thesis. To my Family, for the values and insights they shared with me, I also owe this dissertation.

Finally, I would like to thank to Margarida Sepúlveda for always being there for me, and above all, with me. Her comprehension and help throughout my course, Master Thesis and personal projects, meant (and still mean) the world to me. Thank you for sharing the wonderful person you are with me.

Thank you.

João Justo Pereira
Monday 1st April, 2013
Abstract

Modern power management System-on-a-Chip (SoC) design demands for fully integrated solutions in order to decrease certain costly features such as the total chip area and the power consumption while maintaining or increasing the fast transient response to signal variations. Low-Dropout (LDO) voltage regulators, as power management devices, must comply with these recent technological and industrial trends.

An ultra low power capless low-dropout voltage regulator with resistive feedback network and a new dynamic biased, multi-loop compensation strategy is proposed. The dynamic close-loop bandwidth gain and dynamic damping enhance the fast load and line LDO transient responses. These are assured by the output class-AB stage of the error amplifier and the feedback loop of the non-linear derivative current amplifier of the LDO. Using the proposed strategy of the dynamic biasing in the derivative loop, the LDO transient response performance is highly improved when the output voltage sensed, in the derivative current amplifier, varies rapidly.

The proposed LDO, designed for a maximum output current of 50 mA in TSMC 65 nm, requires a quiescent current of 3.7 μA and presents excellent line and load transients (<10%) and fast transient response.

Keywords - Low drop-out, LDO, Low Power, Capless, Dynamic Biased, Multiloop Feedback
Resumo

Atualmente, em power management, projectos System-on-a-Chip (SoC) exigem soluções totalmente integradas de forma a reduzir características de custo, como a área total e a potência consumida, enquanto se mantêm, ou aumentam, as suas respostas transientes a variações nos sinais. Reguladores de tensão lineares Low-Dropout (LDO), como dispositivos de power management, têm de obedecer a estas últimas tendências tecnológicas e industriais.

Propõe-se neste trabalho um LDO de muito baixo consumo, sem condensador externo, com realimentação resistiva, polarizado dinamicamente e uma nova estratégia de múltipla realimentação e compensação. O ganho de largura de banda dinâmico, em malha fechada, e o amortecimento dinâmico são responsáveis pela melhoria das respostas transientes de regulação de carga e linha do regulador. Estes são assegurados pelo andar de saída classe-AB do amplificador de erro e pela realimentação do amplificador de corrente derivativo não linear. Pelo uso da estratégia proposta e da polarização dinâmica no amplificador de corrente derivativo, o desempenho do regulador na sua resposta transiente é muito melhorado se a tensão de saída monitorizada no amplificador de corrente derivativo variar rapidamente.

O regulador de tensão proposto, projectado para uma corrente de saída máxima de 50 mA na tecnologia TSMC de 65 nm, requer uma corrente quiescente de 3.7 µA e apresenta uma excelente e rápida resposta transiente de carga e linha (<10%).

PALAVRAS-CHAVE - Regulador de tensão, LDO, baixo consumo, sem condensador, polarização dinâmica, múltipla realimentação
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List of Symbols and Acronyms

AC  Alternating Current
BOM  Bill of Materials
CMOS  Complementary Metal–Oxide–Semiconductor
CPU  Central Processing Unit
DC  Direct Current
DRC  Design Rule Checking
DSP  Digital Signal Processing
ESD  Electrostatic discharge
ESR  Equivalent Series Resistance
FOM  Figure of Merit
GBW  Gain–Bandwidth product
GPS  Global Positioning System
IC  Integrated Circuits
KCL  Kirchhoff’s Current Law
LDO  Low-Dropout
LHP  Left Half-Plane
MOS  Metal-Oxide-Semiconductor
NMOS  N-type Metal-Oxide-Semiconductor
OTA  Operational Transconductance Amplifier
P-M  Process and Mismatch
PMOS  P-type Metal-Oxide-Semiconductor
PMU  Power Management Unit
PSR  Power-Supply Rejection
PSRR  Power-Supply Rejection Ratio
P-V-T Process-Voltage-Temperature

RC Resistor–Capacitor

RF Radio Frequency

SoC System-on-a-Chip

SR Slew-Rate

TSMC Taiwan Semiconductor Manufacturing Company

UGF Unit Gain Frequency

Latin Acronyms

*apud* indirect quotation, to quote someone who quoted someone else

*i.e.* *id est*, that is to say

*ibid.* *ibidem*, citing something that has been cited previously

*e.g.* *exempli gratia*, for example

*et. al.* *et alii*, and other people
1.1 Overview

The consumer electronic industry has been undergoing severe pressures to adapt and to respond to new social and market demands. Nowadays, the demand of mobile and battery-powered consumer electronics is growing exponentially. The demand for gadgets with improved battery life is also growing at a very fast pace. The users requirements and expectations are significantly higher towards the consumer electronic industry and their range of different devices. Finally, the rapid development of semiconductor manufacturing process and its respective miniaturization, in addition to the aforementioned causes, continues to exert severe pressures to the industry.

According to Apple 2012 Annual Report Results [1], the total number of iPhones sold worldwide, in 2012, exceeded the 119 million units. This fact can be seen in Figure 1.1 and illustrates the pressures imposed to the consumer electronic industry by this device alone.

Power Management, as an essential research area and as part of the solution, is rapidly changing in order to meet these rigorous demands [2]. Modern designs imply accuracy, power efficiency, improved response times, less silicon area and less off-chip components for portable and embedded systems, which means, fully integrated solutions known as System-on-a-Chip (SoC) solutions. Low overall energy consumption, including standby mode, will prolong the battery life improving power efficiency. Reducing the number of off-chip components will result in a decrease of the Bill of Materials (BOM) required and, as a direct consequence, contact pads and connections will be reduced and therefore less
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silicon area will be required.

(a) Worldwide demand normalized to 100 which represents the peak of on-line searches for iPhones achieved in this year [3]

(b) Worldwide sales of the iPhone until the end of the same period

Figure 1.1: Worldwide impact of the iPhone until 2013

Until very recently, a complete system was composed by multiple Integrated Circuits (IC). SoC solutions bring the possibility to the electronic industry to integrate the same complete system onto a single IC. It aims mainly to achieve a more compact and robust system while speeding up the manufacturing process with even lower costs of production for the same technology [4].

Sophisticated devices such as laptops, smart phones, video cameras, tablets, Global Positioning System (GPS) devices, among many others, require a clean regulated low-noise and precise voltage supply [5] apud [6]. A voltage supply free of noise contributions is required to power up the internal blocks of each device, many of them noise-sensitive, and to provide increased processing power and functionality for a longer period of time [7]. Furthermore as can be observed in Figure 1.2, the voltage supplied by a single cell is variable by nature. Thus, any battery, as a composition of cells, also inherit this characteristic which makes this an important issue in power management design.

Figure 1.2: Typical cell (i.e. Nickel-Metal Hydride) voltage discharge curve over load, considering the temperature and discharge rate to be constant
Each internal block, for one single device, have different voltage and current requirements so different regulators are required in order to supply these different requirements into one single SoC. The SoC core unit responsible for managing these different requirements and for enabling the batteries to charge is the Power Management Unit (PMU). A typical PMU block diagram is shown in Figure 1.3.

Figure 1.3: Typical power management unit for battery powered devices

Other SoC core units such as the Central Processing Unit (CPU) and the Digital Signal Processing (DSP), whose importance in SoC is indisputable, are units where high power switching occurs and therefore a noisy contribution is generated and added to the expected clean voltage supply. This non-ideal addition degrades the supply decreasing its precision and accuracy.

The real voltage supply, ideally a Direct Current (DC) supply, presents variations over charge cycles, oscillations, frequency spikes and voltage drops [8] and it is not suitable for noise-sensitive applications like Radio Frequency (RF) and audio applications.

The most common way to isolate the switching effects and to remove other non-ideal variations in the voltage supply is by the use of several independent voltage regulators. Voltage regulators are electronic circuits capable of maintaining a steady voltage at their terminals despite battery, ambient and load conditions. Although there are several voltage regulators available in the industry, the focus of this work will be in active DC voltage stabilizers. DC voltage stabilizers can be as simple as a shunt regulator like a Zener diode and as complex as switched regulators.

Linear regulators however, as active DC voltage stabilizers, perform better in a low power environment. Linear regulators benefit from the fact that are able to supply clean and precise output voltages with low levels of noise added to it and are able to respond very quickly to input signal variations when compared to other types of voltage regulators. One drawback of this type of regulation is that it cannot step-up the output voltage, meaning the input voltage has to be always greater than the output voltage [9]. This fact doesn’t pose a problem for most internal blocks or applications but
for those few where a higher voltage is required, several solutions exist. As an example, switching regulators can be used to step-up the supply voltage and afterwards a linear regulator, in series with the switched regulator, can be used to seek even further stabilization.

Low-Dropout (LDO) voltage regulators are linear regulators that can operate with a very small input-output differential voltage [10, 11]. This advantage makes them the optimal solution for voltage regulation in SoC applications where noise-sensitive circuitry exist.

1.2 Motivation

Knowing that the market demand for consumer electronics is growing exponentially, take as an example the demand for iPhones shown earlier in Figure 1.1, the electronic components used in the fabrication of these electronic devices will also grow exponentially so ultimately this demand will also fall over the basic electronic components such as the LDOs.

High-performance ultra low power LDOs are part of the response to this emerging need of efficient and robust electronic components. Concerning LDOs, many researchers are proposing different topologies with different compensation techniques. However, these techniques and analyses assume the small signal analyses and framework when, in fact, most of the transient voltage signals in the non-linear pass device of the LDOs are not small [12].

The small signal analyses is important as a starting point to address issues like accuracy and stability in LDOs but neglects other important contributes that averaged out should not be neglected during large and fast signal transients. The motivation of this dissertation is to better understand the non-linear feedback topologies where small and large signal analyses are both important and to propose an LDO compensation technique based on a new multi-loop feedback strategy with dynamic biasing.

1.3 Objectives

The objective of this thesis is to develop an ultra low power capacitorless LDO voltage regulator capable of maintaining a steady operation under rigorous and uncertain loading conditions. In order to attain these objectives the LDO Complementary Metal–Oxide–Semiconductor (CMOS) transistors are designed to operate in the sub-threshold region except for the pass device due to its size and current range drive capability. Finally, the quiescent current and bias current are kept low in order to improve power efficiency while supplying enough current for correct operation. The project specifications are shown in Table 1.1.

The LDO design is implemented in Taiwan Semiconductor Manufacturing Company (TSMC)®
65 nm CMOS technology. The software used to implement and design the proposed LDO was Cadence® Virtuoso Custom IC Design, Hspice® simulator, WaveView® and CosmoScope® waveform viewers. Matlab and Mathematica were also used to obtain the theoretical results presented in this work.

Table 1.1: Capless LDO voltage regulator design specifications

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<th>PARAMETER</th>
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<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
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<tr>
<td>Technology</td>
<td></td>
<td>TSMC® 65 nm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>( T_j )</td>
<td></td>
<td>-25</td>
<td>25</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>( V_{in} )</td>
<td></td>
<td>1.4</td>
<td>-</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>Digital Low</td>
<td>( V_L )</td>
<td>for PD pin</td>
<td>0 %</td>
<td>-</td>
<td>20 %</td>
<td>( V_{in} )</td>
</tr>
<tr>
<td>Digital High</td>
<td>( V_H )</td>
<td>for PD pin</td>
<td>80 %</td>
<td>-</td>
<td>100 %</td>
<td>( V_{in} )</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>( V_{out} )</td>
<td></td>
<td>0.96</td>
<td>1.2</td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td>Bias Current</td>
<td>( I_{bias} )</td>
<td></td>
<td>80</td>
<td>100</td>
<td>200</td>
<td>nA</td>
</tr>
<tr>
<td>Load Current</td>
<td>( I_{load} )</td>
<td></td>
<td>0</td>
<td>-</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>External Capacitor</td>
<td>( C_{out} )</td>
<td>to filter ( V_{out} )</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>F</td>
</tr>
<tr>
<td>Startup Time</td>
<td>( T_s )</td>
<td>to 90 % of ( V_{out} )</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>µs</td>
</tr>
</tbody>
</table>

**CURRENT CONSUMPTION**

<table>
<thead>
<tr>
<th></th>
<th>( I_{QON} )</th>
<th>( I_{QOFF} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>All blocks ON</td>
<td>-</td>
<td>25 µA</td>
</tr>
<tr>
<td>All blocks in Power Down</td>
<td>-</td>
<td>100 nA</td>
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1.4 Outline

The present dissertation is organized as follows:

- **Chapter 1: Introduction**
  The intent of this chapter is to give some overview and background to better follow and understand the work proposed.

- **Chapter 2: LDO Voltage Regulator**
  This chapter presents the conventional LDO regulator characterization, presents the capacitorless LDO regulators as an improvement of the former and finally the leading edge of LDO design concerning SoC applications. The existing compensation techniques and strategies are also presented as well as their validity and limitations.

- **Chapter 3: Capacitorless LDO Regulator Design**
  In this chapter the theoretical macro-model of the design is presented as a starting point. A basic characterization of the proposed LDO is also provided as well as the compensation and strategy used with all the considerations and limitations taken into account.

- **Chapter 4: Results**
  This chapter presents the simulation analysis, explaining the results achieved, the impact of the
1. INTRODUCTION

considerations made and the measures obtained. It also provides the methodology of this work. A detailed comparison between this dissertation design and state of the art is also given.

- Chapter 5: Layout
  The layout of the proposed topology is given in this chapter complying with the respective Design Rule Checking (DRC).

- Chapter 6: Conclusion
  This chapter summarizes all the work done, all the options taken into account and their result. The main features of the design are also presented. Finally, for future works, a brief reference to relevant research is presented.

1.5 Synopsis

This chapter started by pointing out the worldwide desire for battery-powered consumer electronics (market demand) and pressures felt over the electronic industry. It also pointed out the importance of modern power management SoC design. Showed various applications for modern power management SoC designs. It also indicated the most common problems associated with voltage regulation. Several regulators were briefly discussed and their validities shown and compared. This chapter also introduced LDO voltage regulators as the optimal solution for regulation in integrated systems like SoC, where several noise-sensitive applications exist. Finally, the overall motivation, objectives and structure of this work were presented.
2.1 LDO Characterization

2.1.1 Conventional LDO Topology

LDO voltage regulators fall into the class of linear voltage regulators. The operation and objectives of this class remain the same, so LDOs, like any other voltage regulator, must provide a steady and
2. LDO VOLTAGE REGULATOR

The main blocks of the conventional LDO topology are the error amplifier, the pass device and the linear feedback network ($R_1$ and $R_2$). To operate, the LDO also needs a voltage reference. This reference is established by an electric circuit known as Band Gap. The difference between LDOs and Band Gaps, since both provide a steady voltage, is that an LDO must be able to provide current and voltage to any indefinite number of load blocks. Band Gaps, on the other hand, must provide a steady voltage to a single block with constant input capacitance, which is usually a voltage regulator like an LDO. In short, Band Gaps don’t suffer from fan-out problems like LDOs.

The error amplifier is responsible for the voltage comparison between the reference and the scaled down output voltage obtained by the resistive feedback network. It is also responsible for driving the pass device in function of the comparison result just stated. Due to the advantages of the negative feedback (i.e., regulation and system control) and the signal inversion on the pass device, the scaled down version of the output voltage needs to be fed to the positive terminal of the amplifier and, by exclusion, the Band Gap has to be fed to the negative terminal of the amplifier. As the positive and negative terminals assume roughly the same value, then the output voltage is defined by the Band Gap through the negative terminal and resistive divider. If the output voltage suffers from an undershoot, the positive terminal will drop, forcing the error amplifier output voltage to drop as well thus increasing the pass device’s driving force. To finalize the cycle, the capacitor at the output node will be charged more rapidly, raising the output voltage to the nominal value. The opposite process occurs when the LDO output voltage suffers from an overshoot. As it will be shown later, the error amplifier’s ability to drive the pass device is asymmetrical [8] and depends greatly on the type of oscillation felt at the LDO’s output. Class-A operation, as core circuitry in conventional error amplifiers, can be designed to push or pull a pass device’s gate, charging or discharging it more quickly, but never both [8]. Class-AB operation allows the symmetrical output oscillation, and time response, with a small cost of complexity and silicon area.

The pass device is a power device whose only function is to control the amount of current flow.
to the load. This device is extremely large, it can easily surpass 50% of the total LDO design area in SoC context, as it needs to drive the total current the load. Typically, while driving, a pass device supplies currents from 100 μA to 100 mA, in low power context, as shown in Tsz Yin Man study [13].

Finally, a large capacitor exists at the LDO output in parallel to the load. This large capacitor, in conventional LDO topologies, acts like a charge source during fast load transients improving the response time of the regulator and its stability [14, 15, 16]. However, as referred earlier, this capacitor poses a problem due to the fact that it is too large to be an on-chip capacitor and therefore goes against the modern design trends.

To better understand LDO regulators and follow the work proposed in this and the next chapters a few parameters are introduced in Table 2.1.

Table 2.1: LDO basic parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dropout Voltage $V_{DO}$</td>
<td>Difference between the minimum input voltage, necessary for the regulator to operate, and the regulated output voltage.</td>
</tr>
<tr>
<td>Quiescent Current $I_Q$</td>
<td>Current drawn by the regulator when no load is applied.</td>
</tr>
<tr>
<td>Overshoot</td>
<td>Output voltage peak that occurs in load and line transients when the signal exceeds its target value.</td>
</tr>
<tr>
<td>Undershoot</td>
<td>Output voltage negative peak that occurs in load and line transients when the signal exceeds negatively its target value.</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>Measure of the circuit’s ability to maintain a constant output voltage despite output current variations.</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>Measure of the circuit’s ability to maintain a constant output voltage despite input voltage variations.</td>
</tr>
<tr>
<td>Load Transient</td>
<td>Measurement of the system’s speed response to an overshoot/undershoot in the system’s output current.</td>
</tr>
<tr>
<td>Line Transient</td>
<td>Measurement of the system’s speed response to an overshoot/undershoot in the system’s input voltage.</td>
</tr>
<tr>
<td>Power Supply Rejection</td>
<td>Measure of the circuit’s ability to regulate its output voltage against low to high frequency variations in the input supply.</td>
</tr>
</tbody>
</table>

2.1.2 Pass Device

G. Rincón-Mora and P. Allen published a comparative study between LDO voltage regulators with different pass devices [17] where the advantages and disadvantages of each pass device were identified and its study deepened. This study results, summarized in Table 2.2, together with contributions of other researchers [18], identified what is known and accepted today as the most suitable pass device...
for LDO application, the P-type Metal-Oxide-Semiconductor (PMOS) device.

Table 2.2: Comparison of pass element structures

<table>
<thead>
<tr>
<th></th>
<th>NPN Darlington</th>
<th>NPN</th>
<th>PNP</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{\text{load},\text{max}} )</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
</tr>
<tr>
<td>( I_Q )</td>
<td>Medium</td>
<td>Medium</td>
<td>Large</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>( V_{\text{DO}} )</td>
<td>( V_{\text{sat}} + 2V_{\text{be}} )</td>
<td>( V_{\text{sat}} + V_{\text{be}} )</td>
<td>( V_{\text{ec sat}} )</td>
<td>( V_{\text{sat}} + V_{\text{gs}} )</td>
<td>( V_{\text{sd sat}} )</td>
</tr>
<tr>
<td>Speed</td>
<td>Fast</td>
<td>Fast</td>
<td>Slow</td>
<td>Medium</td>
<td>Medium</td>
</tr>
</tbody>
</table>

The most important criterion for the pass device selection was the dropout voltage, \( V_{\text{DO}} \), where the lower dropout voltages the better.

The NPN Darlington structure is not suited for low power LDOs for two main reasons. The lowest dropout voltage it can stand is given by \( V_{\text{sat}} + 2V_{\text{be}} \) which is superior than 1 V [19]. The other reason is that, since it is composed by bipolar transistors, the quiescent current increases greatly. Single NPN bipolar transistors are not the best option to LDO pass devices because its lowest dropout voltage is given by \( V_{\text{sat}} + V_{\text{be}} \), superior than 1 V [19], when the base of the transistor is fully pulled up to the supply voltage. Once more, quiescent current also increases due to the large base current required. Single PNP bipolar transistors are preferred to NPN bipolar transistors because the base of the PNP transistor can be pulled down to ground, fully saturating the transistor where the dropout voltage is given by \( V_{\text{ec sat}} \). In PNP transistors quiescent current is also increased due to the large base current required. On the other hand, N-type Metal-Oxide-Semiconductor (NMOS) and PMOS transistors can operate as pass devices without increasing the quiescent current and with dropout voltages beneath 1 V. The NMOS transistor can provide a minimal dropout voltage of \( V_{\text{sat}} + V_{\text{gs}} \) while the PMOS transistor can be fully saturated providing a smaller dropout voltage of \( V_{\text{sd sat}} \), being this last candidate the optimal solution for the pass device of low-power LDOs.

### 2.1.3 Efficiency

As explained earlier, efficiency is one major concern in modern power management design. Conventional LDOs, in terms of power efficiency, perform reasonably well. Usually are preferred to other types of voltage regulation because, among others, their applied voltages are low, which translates to low dissipated power.

The input and output power supplied to and by the regulator are given by equations 2.1 and 2.2 respectively.

\[
\text{Input power} = V_{\text{in}} \times I_{\text{in}} \quad (2.1)
\]

\[
\text{Output power} = V_{\text{out}} \times I_{\text{load}} \quad (2.2)
\]
2.1. LDO Characterization

where $V_{in}$ is the input voltage applied to the regulator, $I_{in}$ is the input current supplied to the regulator, $V_{out}$ is the voltage seen at the regulator’s output and finally $I_{load}$ is the current supplied by the regulator to its pending blocks.

The current drawn by the regulator when no load is applied, defined as quiescent current, is an important factor that must also be taken into account and minimized when designing LDOs. The quiescent power is given by:

$$Quiescent\ power = V_{in} \times I_{quiescent}$$ (2.3)

Knowing that the dissipated power of a conventional LDO is given by the difference between the input power, equation 2.1, and the output power, equation 2.2, and that the input current is the sum of the load and quiescent currents ($I_{in} = I_{load} + I_{quiescent}$) then equation 2.4 is obtained.

$$Dissipated\ power = (V_{in} - V_{out}) \times I_{load} + Quiescent\ power$$ (2.4)

From the equations 2.1, 2.2, 2.4 and knowing that the principle of conservation of energy holds true for this topology, then the LDO power efficiency can be obtained, equation 2.5.

$$\eta = \frac{P_O}{P_I} \times 100\% = \frac{V_{out}}{V_{in}} \times \frac{I_{load}}{I_{load} + I_{quiescent}} \times 100\%$$ (2.5)

Since $V_{out}$ and $I_{load}$ are well defined for each application, the only parameters left that can improve the LDO efficiency are $V_{in}$ and $I_{quiescent}$. The efficiency is greatly improved when the quiescent power is reduced, meaning $I_{quiescent}$ decreases. Moreover, as introduced earlier, lower input voltages, $V_{in}$, will allow lower dropout voltages, which, by examination of equation 2.5, will further improve the overall LDO efficiency. This improvement is even bigger for applications where the LDO is directly connected to the battery and as the battery discharges (See Figure 1.2) $V_{in}$ gets closer to $V_{out}$ and therefore the efficiency will get closer to 100%.

2.1.4 Stability

Stability is one key aspect concerning LDO differentiation. All the elements present in Figure 2.1 and their intrinsic characteristics are crucial for defining the LDO stability. As a result, stability is therefore, one of the most important trade-offs of LDOs.
To understand the stability of the system, one needs to obtain the transfer function of the system. This function is obtained from the abstraction model shown in Figure 2.2 where the feedback loop was broken for the purpose of the stability analysis.

Equation 2.6 is the mathematical representation of the conventional LDO model shown. It is a system of two equations with two unknown variables, the output voltage, \( V_{out} \), and the overdrive voltage across the pass device, \( V_{od} \).

\[
\begin{align*}
-g_m V_{ref} &= \frac{V_{od}}{r_o} + s C_{gs} V_{od} + s C_{gd} (V_{od} - V_{out}) \\
-g_{mp} V_{od} &= \frac{V_{out}}{r_{op}} + s C_{o} V_{out} + s C_{gd} (V_{out} - V_{od})
\end{align*}
\]  

(2.6)

where \( V_{ref} \) is the voltage reference of the LDO, considered constant, \( g_m \) and \( g_{mp} \) are the error amplifier and pass device transconductances, \( r_o \) and \( r_{op} \) are the output resistance of the error amplifier and pass device and finally \( C_{gd}, C_{gs} \) and \( C_{o} \) are the capacitances associated with each node of the circuit, being \( C_{o} \) the output capacitance. The \( R_{esr} \) present in Figure 2.1 is briefly neglected due to its low Equivalent Series Resistance (ESR) value [20].

Solving this system to the unknown variables the open-loop gain can be obtained, equation 2.7.

\[
\frac{V_{out}}{V_{ref}} = \frac{g_{mp} g_m r_o r_{op}}{s^2 \left(C_{gd} C_{gs} + (C_{gd} + C_{gs}) C_{o}\right) r_o r_{op} + s \left(r_o (C_{gd} + C_{gs}) + r_{op} (C_{gd} + C_{o}) + C_{gd} g_{mp} r_o r_{op}\right) + 1}
\]  

(2.7)

Being equation 2.7 the conventional LDO mathematical representation, one can observe that, \textit{a priori}, conventional LDOs have two poles and one zero, which is a potentially unstable condition [21].

The minimal requirements that need to be true for the LDO to be stable are: the zero must be located below the unity gain frequency and all high-frequency poles must be located at least three times higher than the unity gain frequency [22, 23].
2.1. LDO Characterization

From equation 2.7 the zero of the system is obtained by equaling the numerator to zero. The poles of the system are equally obtained by equaling the denominator of the equation 2.7 to zero. Considering that the two poles are far apart in the frequency domain, the quadratic term of the low frequency pole and the unitary term of the high frequency pole are neglected. With this approximation the poles location are easily obtained. It is considered that the two poles are far apart in the frequency domain if the frequency of the high frequency pole is at least three times higher than the frequency of the low frequency pole. If this rule doesn’t apply then this approximation is no longer valid and in that case the real poles location is given by the detailed mathematical analysis presented in Appendix A.1.

The zero and poles are given by equations 2.8 and 2.9 respectively.

\[
Z = \frac{g_{mp}}{C_{gd}}
\]

\[
P_1 \simeq -\frac{1}{(C_0 + C_{gd}) r_{op} + (C_{gs} + C_{gd}) r_{o} r_{op} g_{mp}}
\]

\[
P_2 \simeq -\frac{(C_0 + C_{gd}) r_{op} + (C_{gs} + C_{gd}) r_{o} r_{op} g_{mp}}{C_0 (C_{gs} + C_{gd}) + C_{gs} C_{gd}} r_{o} r_{op} \simeq -\frac{g_{mp}}{C_0 (C_{gs} + C_{gd})}
\]

Figure 2.3 represents the frequency response of the conventional LDO in accordance with the mathematical model shown.

The dominant pole, the lower frequency pole, in conventional LDOs is set at the output of the LDO by the large capacitor. This capacitor exists in order to compensate the high output impedance of the LDO, providing a stronger and a more reliable instantaneous source of current improving the LDO transient response. The non-dominant pole is defined by the pass device characteristics, namely at its gate terminal, and finally the zero is defined by the pass device’s transconductance and gate drain capacitance. Furthermore, if a buffer is used between the error amplifier and the pass device a third high frequency pole will appear increasing the negative slope by a 20 dB per decade from its position forward, as shown in Rincón-Mora stability analysis [20].
For the LDO to be stable a 30°, or higher, phase margin need to be achieved for the bandwidth of the LDO, considering the open feedback loop analysis [23]. This phase margin will prevent the LDO to oscillate and become unstable under various loads.

2.1.5 Sub-threshold operation

In the low voltage electronics industry, the sub-threshold operation (weak inversion) is well known and renowned trend. It enables the desired operation of transistors with very high gains and improved responses. For a transistor to be in the sub-threshold region its $V_{gs}$ needs to be below but close to $V_T$. It needs to be operating near the cutoff region. Figure 2.4 shows the $I_{ds}$ vs $V_{gs}$ relationship and the respective regions of operation where any Metal-Oxide-Semiconductor (MOS) transistor could be in. The velocity saturation region is also known as high-current region due to the fact that the current drive capability is large but limited by the velocity of each electron and/or hole.

![Figure 2.4: Regions of operation for MOS transistors ($I_{ds}$ vs $V_{gs}$)](image)

The mathematical formula that models the transistor in the sub-threshold region is given by equation 2.10 [24].

$$I_{d\text{weak\,inversion}} = I_{d0} \frac{W}{L} e^{\frac{V_{gs}}{kT/q}}$$

(2.10)

where $k$ is the Boltzmann constant, $T$ is the temperature, $q$ is the charge of an electron, $W$ is the width of the transistor, $L$ its length and $I_{d0}$ the leakage current. $\frac{kT}{q}$ is about 26 mV at room temperature (27°C).

This region of operation is also called the exponential region due to the above equation where $I_d$ is no longer in the squared law region ($\propto (V_{gs} - V_T)^2$, strong inversion). One can note that in this particular region of operation a CMOS transistor can emulate a bipolar transistor in gain without gate current and therefore achieve its benefits without its disadvantages [24].

The transconductance of the transistors are now given by:
2.2 Capacitorless LDO Voltage Regulators

\[ g_{m\text{weak inversion}} = \frac{I_{d\text{weak inversion}}}{nkT/q} \]  

(2.11)

where \( g_m \) and \( I_d \) relation still holds true being given by the derivative of the current with respect to \( V_{gs} \), also an exponential relationship.

However this region of operation presents its drawbacks. As the voltages, currents and transconductances become significantly smaller, while the noise holds constant, worse signal-to-noise ratio are achieved. Moreover, only low speeds can be obtained. Biomedical applications don’t usually require fast responses and high signal-to-noise ratios so sub-threshold operation is suitable for that particular industry. For most other applications however, better noise performance and higher speeds are required. Therefore, forcing the transistors to operate close to weak inversion, but not in it, better results are achieved.

Overall, low-dropout voltage regulators justify their presence in SoC due to their chip size, fast transient responses, low-noise advantages, power efficiency and adjustable parameters through their different trade-offs. In the next section an improved trend of these types of voltage regulators will be introduced, the capacitorless LDOs.

2.2 Capacitorless LDO Voltage Regulators

Capacitorless LDOs, are an alternative to the conventional LDO voltage regulator that aim to circumvent some of the non-desirable characteristics of the latter voltage regulator. Reviewing what was described before, the conventional voltage regulation has the advantage of lower voltage operation and higher power efficiency. However, its high output impedance raises instability issues. To assure a satisfactory transient response it requires an output capacitor in the microfarad range, large in SoC context. This large capacitor creates a low frequency pole which becomes dominant and severely slows down the LDO dynamic behavior [25, 26]. As told before, this poses a problem and contradicts the modern design trends.

Removing the large capacitor from the conventional LDO and replacing it by a smaller one in the range of ten to hundreds of picofarad [27] apud [13], easily implemented on-chip, a more suitable LDO is achieved according to modern design trends. Furthermore, if the pole created by this smaller capacitor is far higher, frequency wise, than the open loop Unit Gain Frequency (UGF), a higher close loop bandwidth is achieved which is very advantageous [28]. On the other hand, removing the large capacitor leads to other constraints of the LDO responses and performance. With the aforementioned replacement, some output filtering properties are lost, by comparison to the circuit response with the larger output capacitor. The small capacitor acts as a charge source during fast transients as well but in a much smaller scale, therefore the transient responses of the LDO degrade. The lower oscillations on the conventional LDO output voltage are now higher oscillations in the capless LDO output voltage,
considering the same input signals for both the conventional and capless LDO.

The pole set by the smaller capacitor is no longer the dominant one. As this pole is now located in higher frequencies, the LDO, seen from its output, is no longer a stable system. The dominant pole now depends on each topology, being set usually by the error amplifier or buffer connected to the pass device gate. The system stability will be regained as soon as the dominant pole and zero are shifted back to locations well below the UGF and the non-dominant poles are shifted forth to locations well beyond the UGF. To adapt this capless topology and improve it dynamically, when possible, a frequency compensation technique is required to shift the poles and zero back and forth.

2.3 State of the Art

Since high-performance low power LDOs are growing in demand and popularity among mixed-signal system designers, many researchers have been studying different compensation topologies and techniques for LDO stabilization without the large external capacitor, a more attractive implementation of LDOs for SoC applications.

Capacitorless LDOs, also known as capless LDOs, are a step forward in the LDO evolution in a way that less materials are used, a fewer number of input/output pads are required and thus the total silicon area of the LDO can be minimized while maintaining the desired LDO responses.

The most recent compensations techniques and strategies to stabilize and improve the capacitorless LDO responses, in other words, the response of LDOs without the large external capacitor, are presented in this section. A brief analysis is also presented for each technique and their vantages and disadvantages are also pointed out. All of the presented strategies rely on at least one sensing loop of the ratio of output current, or voltage. The sensed parameter is then fed-back to the error amplifier.

2.3.1 Slew-Rate Enhancement Compensation

For LDO designers, it is a well known fact that the slew-rate at the gate of the pass device limits the load transient response of the regulator [5, 29]. The slew-rate enhancement compensation circuit, used to overcome this issue, implements a technique that provides the necessary dynamic current to quickly charge and discharge the gate capacitance of the pass device, improving its transient response.

The dynamic current, supplied by the enhancement circuit, boosts the response of the pass device to signal variation but also incurs in an temporary increase of quiescent current. In order to maintain the low overall consumption and high efficiency of the LDO, this transient should be as narrower as possible and the slew-rate enhancement circuitry should be completely turned off in steady state.

Slew-Rate (SR) enhancement compensation involves two types of electronic circuits: the sens-
2.3. State of the Art

In Figure 2.5 the sensing circuitry adopts a voltage detection method based on capacitive coupling and is responsible for tapping the output node voltage and detect undershoot and overshoot signal variations. If any, then the driving circuitry is enabled acting on the pass device accordingly to the output node voltage detection.

![Slew-Rate Enhancement Topology](image)

Figure 2.5: Slew-Rate Enhancement Topology [29]

Note that $V_G$ is the pass device’s gate voltage (not the regulator’s output) as introduced in Figure 2.1.

The core of this technique is the sensing circuit which must be able to detect and act on signal variations. $C_1$ and $R_1$ implement a high-pass circuit responsible for the output signal variation detection. A more detailed analysis of this type of circuitry will be provided on the next chapter.

Push-Pull Techniques, like the ones reported by Ming [30] and Lee [29], are also commonly applied to enhance the slew-rate issue, as well as Voltage Spike Detection Techniques reported by Or [27] and Guo [31].

### 2.3.2 Buffered Flipped Voltage Follower Compensation

Hua Chen and Ka Nang Leung proposed a buffered flipped voltage follower study based on a single-transistor-control LDO. This technique was built and supported by other previous published studies on flipped voltage followers such as the cascaded and level shifted flipped voltage follower.

The topology in Figure 2.6 combines the best merits of the two referred compensations. It alleviates the minimum loading requirements of the basic flipped voltage follower LDO, provides a large driving force at the gate of the pass device and boosts the loop gain in order to improve load regulation [32]. Moreover, Man et. al. introduced the dynamic biasing technique to the topology present in the Figure 2.6 achieving improved load regulation results. The SR issue was also improved by the push pull output stage [26].
2. LDO VOLTAGE REGULATOR

![Buffered Flipped Voltage Follower Topology](image)

Figure 2.6: Buffered Flipped Voltage Follower Topology [32, 13]

$M_s$ has a key role in the aforementioned vantages. $M_s$ is responsible for reducing the impedance seen at the pass device’s gate and for boosting the loop gain of the LDO. Sufficient conditions to stabilize the LDO. The drain voltage of $M_c$ is determined by the voltage biasing at the gate of transistor, $M_B$, and by $V_{gs}(M_B)$ which are independent of the uncertain loading conditions. The minimum loading constraint is therefore inexistent. $V_{CTRL}$ holds relatively constant over time as it follows the Band Gap output voltage, $V_{ref}$, through a voltage follower buffer, not present in Figure 2.6. As to the $V_B$ constraints, the biasing voltage cannot be set to low or the $I_N$ transistor will enter the linear region and cannot be set to high or $M_B$ transistor will enter the linear region. With this topology and the restricted setting of parameters, a 20 to 40 $\mu$A quiescent current is easily achieved, which for ultra low-power applications is not ideal.

2.3.3 Reversed Nested Miller Compensation

Nested Miller compensation topologies are usually a three stage amplifier topologies that exploits feedback loops and Miller effects through capacitor compensation use. Figure 2.7 represents a Reversed Nested Miller Compensation.

The stability is achieved by splitting the low frequency poles in the frequency domain by using compensation capacitors $C_{C1}$ and $C_{C2}$ in the feedback loop. This technique achieves the desired phase margin and required transient response. On the other hand, bandwidth and slew-rate trade-offs take place [33].
2.3. State of the Art

Reversed active feedback frequency compensation and reversed nested Miller compensation with nulling resistor are two evolutions of the topology shown in Figure 2.7 and operate with the same principles already introduced. The major differences between these two topologies and the one presented in Figure 2.7 are the feedback paths which include transconductance blocks along with passive components, the second stage Operational Transconductance Amplifier (OTA), which is the only inverting one, and finally the inherent bandwidth improvement due to the fact that the inner compensation capacitor, \( C_{C2} \), does not load from the output node.

All these techniques require a 500 pF capacitor at the output node for stability purposes which for low power environment is not ideal.

2.3.4 Q-Reduction Compensation

With the removal of the large external capacitor and with the low power requirements, both set by the latest SoC trends, the non-dominant poles start to suffer some changes such as, higher Q values and locations closer the UGF [28, 34]. A new compensation is shown in Figure 2.8 that aims to reduce the high Q values of the poles and shift the poles locations to higher frequencies moving them away from the UGF.

This topology consists in a three stage circuit. The first stage is the differential amplifier, as input stage, the second stage is a non-inverting gain stage and finally the pass device as the third stage. The first stage also has a current buffer to supply the required current to the second stage.

This topology uses a Miller compensation capacitor, \( C_{m1} \), a feed-forward capacitor to introduce a left-half-plane zero [34], \( C_{cf} \), and gate-drain capacitor, \( C_{gd} \), to stabilize the LDO regulator. With this technique higher values of phase margin are achieved for a given bandwidth.

The current buffer in the first stage together with the feed-forward capacitor have a crucial role reducing the Q value of the non-dominant poles. The \( M_3 \) transistor is a low transconductance transistor that is necessary to reduce the Q values of the poles. The second stage is a rail-to-rail
2. LDO VOLTAGE REGULATOR

push-pull stage that forces the pass device to respond more quickly to signal variations. As shown before the gate capacitance will be charged/discharged more quickly further improving the transient response of the LDO.

Q-Reduction technique usually achieves higher bandwidths than the other techniques presented for a given low quiescent current.

2.3.5 Pole-Zero Cancellation Compensation

The multi-stage amplifier topology represented in Figure 2.9 seen on Surkanti’s and Kwok’s studies [35, 21] improves the capless LDO frequency response by canceling the effect of the existing output pole by determining its location and dynamically adding a zero over it, or near it. The addition of the zero
will be achieved by the Resistor–Capacitor (RC) series connected to the gate of the pass device.

With this technique a greater bandwidth can be achieved for a suitable phase margin. This topology also permits a power device slew rate improvement. On the other hand, the complexity, quiescent current and silicon area are significantly higher.

### 2.3.6 Damping-Factor-Control Compensation

This technique, reported by Leung [7, 36], relies on a pole-splitting compensation to assure that the zero of the system is well below the UGF and that the high-frequency poles are at least three times higher than the UGF. The non-dominant poles location will be set by the power device transconductance and output node capacitance. High values of pass device transconductance and lower values of output node capacitance will result in the improvement of the LDO stability as the non-dominant poles achieve higher frequency locations.

![Figure 2.10: Damping-Factor-Control Topology [7]](image)

Furthermore, small passive components can be used to create high frequency zeros in order to cancel the high non-dominant poles more effectively.

With this technique further improvement is possible regarding fast and load transient response and high Power-Supply Rejection Ratio (PSRR).

Since the pass device cannot function as a high-gain stage in dropout condition [7], the complexity of the system will increase. The classical two-stage amplifier topology will require an extra stage to operate as seen in Figure 2.10.

Damping-Factor-Control Compensation, as the Q-Reduction technique, achieves higher bandwidths than the other techniques presented for a given low quiescent current.
2.3.7 Adaptive Biasing Compensation

The topology in Figure 2.11 represents a 2012 Ming research work [37] and implements an adaptively biasing compensation by injecting more transient current in the biasing circuitry that feeds the regulator. Other researchers also proposed different topologies based on this technique [38, 39]. The regulator is composed by a reference voltage, a voltage follower, a high bandwidth, a SR error amplifier and finally a PMOS pass device. The error amplifier has a push-pull output stage capable of decreasing the SR problems and improving the pass device transient response. The biasing current is controlled by the capacitive coupling path present in the topology and it requires a precise adjustment to operate correctly. The pass device can be designed to work in the linear region for heavy loads.

![Adaptively Biased Compensation with Dynamic Charging Control](image)

The stabilization of the LDO is assured mainly by the adaptive biasing and dynamic charging techniques present in Figure 2.11. The adaptive biasing will provide higher bandwidth and a larger SR for regulation with the pass device in the linear region at heavy loads [40]. The dynamic technique is responsible by the introduction of a pole-zero pair in the frequency response of the amplifier shifting the non-dominant poles to higher frequencies.

The fast transient current injected in the bias circuitry will increase the quiescent current of the LDO in the steady state. The aforementioned trade-off is a common compromise between bandwidth and precision. Furthermore, the adaptive biasing technique is only activated when the gate voltage of the pass device suffers from an undershoot [37]. This drawback demands extra compensation and added complexity for overshoots in the pass device gate node. This regulator relies on the dynamic charge to respond to overshoots and compensate the overshoot problem.

2.3.8 Dynamic Biasing Compensation

Marco Ho and Ka Nang Leung proposed a dynamic bias-current boosting technique for ultra low power LDOs based on rail to rail amplification and on a slewing detection circuit to enable fast large-
2.3. State of the Art

This study was built over other published works such as the ones published by H. Lee [29], T.Y. Man [26], P.Y. Or [27] and finally, E.N.Y. Ho [5].

The great contribution of this study is that it presents a slewing technique that monitors an internal node voltage value, instead of the usual output node monitoring. Since the signal path is smaller, from the node to the control circuitry, it allows a much faster response from the LDO [41]. Furthermore, the overall response is highly increased due to the dynamic boost-current imposed only in the slewing periods, hence the topology name.

Figure 2.12 shows the configuration proposed by M. Ho in his research [41].

The regulator is composed by an error amplifier, a bias-boosting circuitry, a slewing detection and amplification stage and finally by a pass device.

By Figure 2.12, one can observe that when a large oscillation occurs in the LDO output node, the $V_{IN+}$ and $V_{IN-}$ terminals will be highly unbalanced. If the oscillation is positive (overshoot), the internal node $V_P$ will be abruptly pushed down, in order to generate a large source-gate voltage across the pass device, enabling it to drive a larger amount of current to the output node much faster. $V_{HI}$ and $V_{LO}$ are then pulled up, converting the low-to-high $V_{LO}$ signal to supply-to-ground swings at $V_{DOWN}$. On the other hand, if the oscillation is negative (undershoot), the internal node $V_N$ will be abruptly pushed up, both $V_{HI}$ and $V_{LO}$ are pulled down, converting the high-to-low $V_{HI}$ signal to ground-to-supply swings at $V_{UP}$. Signals $V_{UP}$ and $V_{DOWN}$ are the output of the CMOS inverter structures and are also said to be full-swing triggering signals, enabling faster responses from the error amplifier and pass device.

The topology presents some constraints concerning the LDO poles and zeros locations. The stability issue is solved by using a large 10 nF output capacitor (but still small enough to fit a SoC solution, with a cost of core area). Two RC high-pass networks are employed and are responsible for the shut off of the bias-boosting circuit when the steady state is regained. Moreover, with the dynamic boost of current, the error amplifier will extend the overall bandwidth of the capless LDO by pushing its dominant pole to higher frequencies. This extension reveals to be crucial mainly in rapid
output voltage/current changes [41]. If careful attention is given to the dynamic compensation design, a compensation can be achieved with negligible effect on the stability [41].

2.4 Synopsis

In this chapter, the conventional LDO topology was presented. The basic building blocks of a low dropout regulator were pointed out as well as their function and characterization in the system. The reason why the PMOS transistor is more commonly used in LDO regulation was also pointed out along with its advantages. An efficiency and stability theoretical studies were also given. The new generation of LDOs was also presented, the capless LDOs. Their common trade-offs were explained. Finally, the State-of-the-Art was given and the different compensation techniques applicable to capless LDOs briefly explained.
3.1 Design Considerations and Principles

Recent studies regarding compensated capacitorless LDOs have achieved incredible and promising experimental results. It is now possible to use low power capless LDO voltage regulation in a SoC having the expected results to fast transient signal variations without instability issues. Different compensation strategies still resort to different compromises and trade-offs of their own characteristics and specifications, being the low quiescent current restriction and stability the main ones.

The state of the art compensation topologies presented in the previous chapter typically follow one of two strategies: (1) Active feedback compensation strategy [40, 38, 39, 26, 29] and (2) adaptive and dynamic adaptive biasing [41, 27, 31]. The first strategy aims to achieve higher loop responses by increasing the damping characteristics of the system. Miller pole-splitting compensation is also used in this strategy to provide the required stabilization. The second strategy aims to overcome the slew-rate limitations imposed by the error amplifier by embedding a class-AB amplifier inside the error amplifier.
amplifier or by embedding a buffer connected to the gate of the pass device as a push-pull stage [34, 7]. Both strategies also aim to improve the capless LDO transient response by sensing the output voltage through the derivative loop. The non-linear derivative loop will speed up the current amplification and therefore the transient response of the LDO.

Aiming to boost dynamically the bias current of the circuit and the slew-rate of the error amplifier, researchers have recently proposed a hybrid strategy. The core technique behind the hybrid strategy is achieved by sensing and mirroring a current from the fast output voltage dependent derivative loop [13, 16].

The compensation of the ultra low power capacitorless low-dropout voltage regulator in this thesis proposed consists on a new multi-loop feedback strategy and is also based on both the above mentioned strategies. The divergence of this work, to the others based on hybrid strategies for capless LDO compensation, relies on the fact that this one has the damping loop dynamically biased by the error amplifier. This characteristic allows a faster sense of the LDO output voltage thus enabling significant enhancements in the overall performance of the LDO.

This work aims therefore to contribute and add some insight to the recent hybrid strategy used to compensate capless LDOs.

As for the design issues and limitations, the proposed capless LDO was designed to meet the strict requisites demanded by modern power management designs. These requisites constitute the project specifications and are summarized in Table 1.1 showed earlier in Chapter 1.3 Objectives.

The design specifications define the scope of the compromises and trade-offs that can be explored. The error amplifier used in the proposed topology is composed by two gain loops with a folded cascode amplifier [42] and a symmetrical OTA with PMOS common-gate differential inputs instead of the usual common-source differential inputs. This choice will enable a quicker and improved response, for a low quiescent current, as the error amplifier input PMOS transistors show different characteristics like impedance and capacitance at their terminals. Furthermore, common-gate configuration enables a much higher current driving force that is not possible when the error amplifier inputs are made through the gate terminals. This choice, however, comes with a price which is to add two current buffers before the error amplifier inputs, adding complexity to the system. The current amplification buffers serve mainly to supply higher values of current to the error amplifier, when needed, without overcharging the precedent blocks such as the Band Gap, whose current driving force isn’t high and whose design was made to a known and constant value of output capacitance. The buffers are independent from each other and have the same topology thus saving design time. The silicon area required for both buffers is not significant. On the other hand, quiescent current will increase (two more buffers to feed), but it is considered an acceptable compromise as long as it falls within the quiescent specification.

As to the pass device, whose design will be explained in a later section, it presents one only limitation which is its size and consequently its region of operation. Its size is defined by the maximum value of current it will be able to drive and so, as Table 1.1 states that $I_{load}$ can be as low as zero ($\mu$A
range considered zero) and as high as 50 mA it needs to be designed accordingly.

The design of the Band Gap block falls out of the scope of this thesis. However, the error amplifier negative side input buffer is designed to assure that any type of Band Gap topology can be embedded without overcharge issues or change in the designed performance, meaning the current buffer will accept any Band Gap without changing its load regulation and load transient responses.

3.2 Macro-model of the Capacitorless LDO Regulator

3.2.1 Basic Characterization

The study of the present work began based on the macro-model shown in Figure 3.1 from J. Esteves et al. [12]. It represents the integral parts of the capless LDO as well as the pass device parasitic capacitors, gate-source and gate-drain capacitors, $C_{gs}$ and $C_{gd}$ respectively.

![Figure 3.1: Basic components of the proposed capacitorless LDO](image)

The error amplifier output current, $i_G$, is shown in equation 3.1 in accordance to the model presented and neglecting the channel modulation effects. In 3.1, $\tilde{g}_m$ represents the dynamic transconductance of the model while $\tilde{C}_f$ represents the dynamic active Miller capacitance.

$$i_G = \tilde{g}_m \cdot v_{od} + \tilde{C}_f \cdot \frac{dv_{out}}{dt}$$

$$= \left( \sum_{i=0}^{\infty} a_{ij} \cdot |v_{od}| \cdot \left| \frac{dv_{out}}{dt} \right|^j \right) \cdot v_{od} + \left( \sum_{i=0}^{\infty} b_{ij} \cdot |v_{od}| \cdot \left| \frac{dv_{out}}{dt} \right|^j \right) \cdot \frac{dv_{out}}{dt} \quad (3.1)$$

To consider a wider and more generalist analysis where the operating point of the circuit is
3. CAPACITORLESS LDO DESIGN

changed and the non-linear effects of the elements are taken into account, this model admits these last parameters to be non-negative coefficient polynomial functions of $|v_{od}|$ and $|\frac{dv_{out}}{dt}|$ and where their first order coefficients, $a_{00}$ and $b_{00}$ are the conventional transconductance $g_m$ and active Miller capacitance $C_f$ [16]. To perform a more simple and linear analysis to the model, small signal analysis, one should consider all coefficients to be zero apart from the first order ones, thus not taking into account the non-linearities of each component. The aforementioned consideration is easily achieved by one unity gain NMOS current buffer that mirrors the current that passes through the $C_f$ capacitor loop. As $v_{out}$ changes, the current driving through $C_f$ will also change accordingly and consequently the unitary gain mirrored current felt over the gate of $M_P$ will also change.

As this model uses one class-AB amplifier with quadratic transfer function, the coefficients $a_{10}$ and $b_{01}$ in 3.1 also must be non-null. This will enable a much more precise approximated model to understand the second order non-linear effects over $i_G$.

3.2.2 AC Analysis

To obtain the Alternating Current (AC) response of the model, a small signal analysis is required. From Figure 3.1 and knowing that the continuity current condition at the pass device’s terminals needs to be respected, $i_g$ and $i_d$ can be extracted and their values given by:

$$
\begin{align*}
\left\{ \begin{array}{l}
i_d &= (C_{out} + C_{gd}) \frac{dv_{out}}{dt} + I_{out} \\
i_g &= g_m (v_{out} - v_{ref}) = C_{gs} \frac{[v_g - v_{in}]}{dt} + C_{gd} \frac{[v_g - v_{out}]}{dt} 
\end{array} \right.
\tag{3.2}
\end{align*}
$$

Considering that the pass device is operating deep in the saturation region and $V_{in}$ and $I_{out}$ are constant, 3.2 can be rewritten as:

$$
\begin{align*}
\left\{ \begin{array}{l}
C'_{out} \frac{dv_{out}}{dt} = -g_{mp} v_g \\
C_g \frac{dv_g}{dt} = g_m (v_{out} - v_{ref}) + C'_{gd} \frac{dv_{out}}{dt}
\end{array} \right.
\tag{3.3}
\end{align*}
$$

where $C'_{gd}$ is the the effective Miller capacitance, $C_g$ is the error amplifier capacitance and $C'_{out}$ is the pass device output capacitance, given respectively by $C'_{gd} = C_f + C_{gd}$, $C_g = C_{gs} + C_{gd}$ and finally $C'_{out} = C_{out} + C_{gd}$.

By transcribing the system 3.3 to the complex domain, normalizing it and solving it to $v_{out}$, the close loop gain of the model can thus be achieved, 3.4.
3.2. Macro-model of the Capacitorless LDO Regulator

\[
A_{vc} = \frac{v_{out}}{v_{ref}} = \frac{\omega_n^2}{s^2 + \frac{\omega_n^2}{Q} s + \omega_n^2}
\]

\[
= \frac{g_{mp} g_m}{C'_{out} C_g} s^2 + \left( \frac{g_{mp}}{g_m C'_{out} C_g} C'_{out} C_g \right) s + \frac{g_{mp} g_m}{C'_{out} C_g}
\]

(3.4)

where \( \omega_n \) and \( \zeta \) are the undamped natural frequency and the damping ratio respectively given by equations 3.5 and 3.6 respectively.

\[
\omega_n = \sqrt{\frac{g_{mp}}{C'_{out} C_g} g_m}
\]

(3.5)

\[
\zeta = \frac{1}{2 Q} = \frac{1}{2} \sqrt{\frac{g_{mp}}{g_m} \frac{C'_{out} C_g}{C'_{gd}}}
\]

(3.6)

Matching 3.4, 3.7 and 3.8 with \( K = 1 \), one can observe that equation 3.4 is in fact the normalized transfer function of a bi-quadratic low-pass filter. \( D(s) \) is the filter characteristic polynomial and is ultimately responsible for defining the order of the filter. On the other hand, \( N(s) \) defines the type of filter, resulting in a low-pass in this particular case.

\[
T(s) = \frac{N(s)}{D(s)} = \frac{v_{out}}{v_{ref}}
\]

(3.7)

\[
N(s) = K \omega_n^2
\]

(3.8)

Being \( D(s) \) a second order characteristic polynomial, the transfer function will assume two poles. These two poles will be located at \( s_{p1} = -\omega_{p1} = -\frac{\omega_n}{\zeta} \) and \( s_{p2} = -\omega_{p2} = -\zeta \omega_n \) as long as \( \zeta = \frac{1}{2Q} \gg 1 \) holds true, being \( Q \) the quality factor of the model.

Applying the previous analysis to the Figure 3.1, where \( g_m \) emulates a two-stage Miller OTA, the Bode magnitude response of the model is obtained.

The dashed line present in Figure 3.2 represents the open loop gain Bode response while the full dash represents the closed loop gain. To obtain the open loop gain the feedback loop was broken at \( X \) in Figure 3.1 thus cutting the \( V_{out} \) dependency. In the open loop gain Bode response, the \( \omega_{p1} \) assumes the value of the dominant pole, \( \omega_d \), while \( \omega_{p2} \) assumes the value of the high frequency pole, \( \omega_{nd} \). On the other hand, in the closed loop gain Bode response, \( \omega_{p1} \) assumes the value of gain bandwidth frequency, \( \omega_{GBW} \), while \( \omega_{p2} \) maintains the previous value of \( \omega_{nd} \). The undamped natural frequency, \( \omega_n \), can also be given by the geometric mean \( \left( \omega_n = \sqrt{\omega_{GBW} \omega_{nd}} \right) \) of \( \omega_{GBW} \) and \( \omega_{nd} \). Similarly, the quality factor of the system, \( Q \), can also be given by the square root of those frequencies \( \left( Q = \sqrt{\frac{\omega_{GBW}}{\omega_{nd}}} \right) \).
3. CAPACITORLESS LDO DESIGN

Figure 3.2: Capacitorless LDO closed loop gain Bode magnitude response

Note that the result that lead to the conclusion that 3.4 implemented a low-pass filter is confirmed by the low-pass frequency response present in Figure 3.2. Equation 3.9 shows how the gain bandwidth frequency and non-dominant pole frequency relate to the model parameters.

\[
\begin{align*}
\omega_{GBW} &= \frac{g_m}{C_{gd}} \\
\omega_{nd} &= \frac{g_{mp} C_{gd}'}{C_{out} C_g} 
\end{align*}
\]

The proposed topology uses a Miller pole-splitting compensation technique to stabilize itself. The stabilization is achieved by spreading the gain bandwidth pole and the non-dominant pole apart, skewing the gain bandwidth pole to lower frequencies and the non-dominant pole to higher frequencies. The damping ratio, \( \varsigma \), is ultimately responsible for the poles location \( s_{p1} = -\varsigma \omega_n, s_{p2} = -\varsigma \omega_n \) and for that reason has a key role in the pole-splitting compensation due to its linear dependence of \( C_f \). From the equation 3.6, if \( C_f \) increases, then \( C_{gd}' \) increases and the damping ratio will also increase, thus decreasing the gain bandwidth pole frequency and increasing the non-dominant pole frequency. The loop gain and system bandwidth can thus be adjusted by the \( C_f \) Miller capacitor size trade-off, as seen in equation 3.4.

3.2.3 PSR Analysis

Employing the same small signal analysis to the capless LDO, model shown in Figure 3.3, the Power-Supply Rejection (PSR) response of the system is achieved, that is to say, the response of the system is given for all frequencies up to 1 GHz where the system is stressed with fluctuations (emulating noise) at its supply terminal.
As done before, in order to obtain the response of the system in the frequency domain one first needs to find its transfer function. Respecting the Kirchhoff’s Current Law (KCL) at the pass device terminals, namely at the $O$ node, the linear small signal analysis imposes that:

\[
\begin{align*}
    g_m v_{out} &= C_{gd} \frac{d (v - v_{out})}{dt} + C_{gs} \frac{d (v - v_{in})}{dt} \\
    g_{mp} (v - v_{in}) &= C_{out} \frac{dv_{out}}{dt} + C_{gd} \frac{d (v - v_{out})}{dt}
\end{align*}
\]  

(3.10)

where the pass device is assumed to be operating deep in the saturation region.

The transfer function of the system given by 3.11, where $C_g = C_{gs} + C_{gd}$, is then extracted from 3.10 by solving the system to $v_{out}$.

\[
\begin{align*}
    \frac{v_{out}}{v_{in}} &= \frac{\omega_n s}{Q s^2 + \omega_n^2} = \frac{g_{mp} C_{gd}}{C_g C_{out}} \frac{s}{s^2 + s \frac{g_{mp} C_{gd}}{C_g C_{out}} + \frac{g_m g_{mp}}{C_g C_{out}}}
\end{align*}
\]  

(3.11)

As done before, matching 3.11, 3.12 and 3.13 with $K = 1$, one can observe that the equation 3.11 is now the normalized transfer function of a bi-quadratic band-pass filter.

\[
T(s) = \frac{N(s)}{D(s)} = \frac{v_{out}}{v_{in}}
\]  

(3.12)

\[
N(s) = K \frac{\omega_n}{Q} s
\]  

(3.13)

The above transfer function presents one zero and two poles. The undamped natural frequency, $\omega_n$, and damping factor, now $\xi$, maintain their previous values (equations 3.5 and 3.6 respectively) and...
therefore the two existing poles obtained from the denominator of the transfer function \( s_{p1} = -\omega_p = -\frac{\omega_n}{\xi} \) and \( s_{p2} = -\omega_p = -\xi \omega_n \) are still located approximately at \( \omega_{GBW} \) and \( \omega_{nd} \), for the overdamped case, if \( \xi \gg 1 \) holds true. The zero is located at 0 Hz (\( s = 0 \) condition).

Figure 3.4 represents the response of the PSR analysis. The bandwidth of the filter, represented by \( b \) in the PSR response, is defined as the frequencies between \( \omega_L \) and \( \omega_U \) that are the lower and upper passband cutoff edges respectively. Furthermore, by the shape of the gain throughout all frequencies, the band-pass transfer function conclusion is also confirmed.

To preserve or even increase the bandwidth of the error amplifier, as stated earlier, is crucial to have a pole-splitting technique to split apart the lower and upper passband cutoff edges. From 3.9, being \( \omega_L = \omega_{GBW} \) and \( \omega_U = \omega_{nd} \) one can observe that if \( C_{gd} \) increases then \( \xi \) will also increase spreading the poles apart and increasing \( b \) (bandwidth) at the cost of some gain reduction.

As it will be shown later the lower frequency spectrum achieves better attenuation results comparing to the mid and high frequency spectrum. The attenuation before the dominant pole (not shown in Figure 3.4) are better due to the gain of the amplifier. Beyond the dominant pole, the output resistance increases [4] and therefore the ability to regulate decreases. This behavior ends when the error amplifier no longer regulates the loop, at the \( \omega_L \). In \( \omega_U \), the response is slightly improved due to the output capacitor.

The conclusions drawn from the above analysis are positive in a way that are coherent with a more generalized results presented by other researchers on their publications [43] and are therefore suitable for this particular case.

### 3.2.4 Linear Transient Analysis

Transient analysis have an extreme importance in electronic design simulation and testing. Given a model or a chip, it can predict or read the progress and variations of a specific signal to changes in its inputs and/or outputs.
3.2. Macro-model of the Capacitorless LDO Regulator

To obtain the transient response of the capless LDO it is necessary, like in the previous analysis, to obtain the transfer function of the model. Figure 3.1 is the basic topology used to obtain it considering that the feedback loop is closed.

Being \( v_{\text{ref}} \) constant and taking into account the previous analysis, then the \( v_{\text{out}} \) behavior will be given by:

\[
\frac{d^2 v_{\text{OD}}}{dt^2} + 2 \zeta \omega_n \frac{d v_{\text{OD}}}{dt} + \omega_n^2 v_{\text{OD}} = 0
\]

(3.14)

In order to observe how \( v_{\text{out}} \) changes to variations in \( i_{\text{load}} \), simulating the turn-on/turn-off of LDO supply dependent blocks, the analysis imposes a step in the load current with well defined amplitude of \( I_{\text{out}} = -C_{\text{out}} \frac{dv_{\text{out}}}{dt} \). Moreover, knowing that the overdrive voltage is related to the output voltage through \( v_{\text{OD}} = v_{\text{out}} - v_{\text{ref}} \) and that the system is well balanced before the current step, meaning \( v_{\text{OD}} = 0 \iff v_{\text{out}} = v_{\text{ref}} \) resulting in an equilibrium condition in the error amplifier and therefore in the LDO, the response to the step can be safely achieved. The progress of \( v_{\text{OD}} \) is then provided by:

\[
v_{\text{OD}} = -\frac{I_{\text{load}}}{\omega_d C_{\text{out}}} e^{-\zeta \omega_n t} \sin \omega_d t
\]

(3.15)

where \( \omega_d \) is the damped frequency given by \( \omega_d = \omega_n \sqrt{1 - \zeta^2} \).

As, in the real world, the output current will be drawn and divided through the LDO proceeding blocks when they are switched on, its output voltage will tend to suffer from a quick transient undershoot. The opposite behavior, overshoot in the output voltage, takes place for the opposite reaction that is when a large flowing supply current is, all of a sudden, not required by any LDO proceeding block, meaning that they where switched off. Figure 3.5 exemplifies an undershoot and an overshoot behavior over the LDO output voltage.

![Figure 3.5: Typical LDO transient response to a step in the load current](image)

This non-ideal behavior results from the fact that the pass device is large, in order to supply both small and large currents to the load, and therefore has large parasitic capacitances that need
to be charged and discharged fully before responding accordingly, adding an extra delay in the LDO transient response. To prevent this type of non-ideal occurrences, slew-rate techniques are used, slightly improving the LDO transient response. In the next section of this work a more deepened explanation will be given on this subject.

Due to this non-ideal and undesired oscillations, particular care must be paid to the output voltage range to ensure it stays within the specified objectives referred in Chapter 1. The minimum undershoot output voltage extracted from equation 3.15, for the under-damped and over-damped limit cases, assume the value of \((v_{out})_{min} \simeq -\frac{I_{out}}{\omega_n C_{out}}\) and \((v_{out})_{min} \simeq -\frac{I_{out}}{2 \zeta \omega_n C_{out}}\) respectively. Remembering the formulas of \(\zeta\) (equation 3.6) and \(\omega_n\) (equation 3.5) previously presented, one can rewrite equation 3.15 to the minimum undershoot in function of the circuit parameters:

\[
v_{OD_{min}} \simeq \frac{C_g I_{out}}{C'_gd g_{mp}} \tag{3.16}
\]
which reveals the real effect of the active Miller capacitance, \(C_f\), on the reduction of the output voltage undershoot.

### 3.2.5 Global Transient Analysis

As shown in a recent study [12], starting with the linear transient response of the model, in this case equation 3.14, applying a second order approximation of the gate current to the system 3.3, as shown in equation 3.1, and normalizing it both in voltage and in time, a more generalized equation is achieved:

\[
\frac{d^2 v_{ON}}{dt^2} + \left(2 \zeta + k_1 \left| \frac{d v_{ON}}{dt} \right| + k_2 |v_{ON}| \right) \frac{d v_{ON}}{dt} + \left(1 + k_3 |v_{ON}| + k_4 \left| \frac{d v_{ON}}{dt} \right| \right) v_{ON} = 0
\]

\[
\iff \frac{\tilde{d}^2 v_{ON}}{d\tilde{\tau}^2} + 2 \tilde{\zeta} \frac{d v_{ON}}{d\tilde{\tau}} + \tilde{\omega}_N v_{ON} = 0 \tag{3.17}
\]

where the output voltage and time normalization were applied through the following change of variables \(v_{ON} = \frac{v_{OD}}{V_{Ov}}\) and \(\tau = \omega_n t\), being \(v_{ON}\) the normalized output voltage and \(V_{Ov}\) the pass device’s overdrive gate-source voltage. In 3.17, \(\tilde{\omega}_N\) and \(\tilde{\zeta}\) are the normalized undamped natural frequency and dynamic damping ratio respectively. \(K_1\) relates to the non-linear damping force, \(b_{01}\) of 3.1, \(K_2\) to the non-linear effects of the dynamic biasing over the damping feedback loop, \(b_{10}\) of 3.1, \(K_3\) to the restoring force, \(a_{10}\) of 3.1, and finally \(K_4\) to the dynamic biasing of the error amplifier by the derivative loop, \(a_{01}\) of 3.1.

This study [12] also illustrates the numerical solutions of 3.17, where the Krylov-Bogolyubov averaging method was applied to the equation at cause to obtain its asymptotic solutions. Figure 3.6 shows its solutions for the same initial conditions, corresponding to the equilibrium value \(v_{ON} = 0\), and to the same load current step perturbation with amplitude \(I_{out}\). The study pinpointed that the
above averaging method also shows that the average dynamical damping and the average undamping natural frequency increase linearly with the signal oscillation amplitudes, observed in Figure 3.6.

In short, adding all the non-linear contributions and terms resulting of the second order approximation of the gate current as well as the linear damping ratio, \( \varsigma \), the final result is achieved, given by curve (d) in Figure 3.6. The amplitude of this curve is lower than that of the curve (e) foreseen by the linear analytical result given by 3.15 also from the same study.

### 3.3 Derivative Amplifier

The error amplifier present in the proposed topology has a key role in the fast voltage regulation and compensation of the capless LDO. The error amplifier response is greatly increased by its feeding damping loop and its derivative output voltage sensing block, hence its name, derivative amplifier.

The new multi-loop strategy is used to enhance the derivative voltage feedback performance by applying dynamic biasing to it. Furthermore, due to this enhancement of performance, the sensing of the fast output voltage variations will also be improved as well as the quality of the load and line transient responses of the capless LDO. Finally, the enhancement of the damping loop will contribute to, in addition with the aforementioned enhancements, further improve the overall capless LDO response.

Inside the derivative amplifier a small circuit like the one shown in Figure 3.7 exists. It enables the capless LDO active compensation.
3. CAPACITORLESS LDO DESIGN

![Diagram of the current derivative amplifier topology and small signal model](image)

Figure 3.7: Basic topology and small signal model of the current derivative amplifier

The idea behind the topology present in Figure 3.7a is to provide a certain amount of current to its pending blocks when, and only when, it is needed, not supplying current otherwise. In other words, the output sensing block requires a current amplifier that supplies large bursts of current to the derivative amplifier. The supplied current is proportional to the sensed output voltage variations thus enabling a faster derivative amplifier stabilization and therefore a faster LDO regulation. This current amplifier is expected to work and increase the driving force of the PMOS pass device when the capless LDO goes out of its steady state operation thus achieving the output voltage regulation sooner and saving the limited battery charge.

The current amplifier is implemented by a simple NMOS current mirror where the slave transistor (M2) is \( k \) times greater in size than the master transistor (M1) thus amplifying the current through the master transistor by a factor \( k \). The capacitor \( C_f \) connected between the output node of the capless LDO \( (v_X = V_{out}) \) and the \( M_1 \) drain and gate is used as the component responsible for sensing the output voltage variations. The current that flows through \( C_f \) will add with the biasing current \( I_B \) and then be mirrored, with a factor of \( k \), to \( M_2 \) by the imposing \( v_{gs} \) of \( M_1 \).

The incremental model of the topology is shown in Figure 3.7b. It is assumed that \( i_C \ll I_B \) and therefore \( i_f \) becomes proportional to the derivative capacitance voltage \( v_C \) as shown in the system of equations 3.18.

\[
\begin{align*}
  v_X &= v_C + v_{GS} = v_C + \frac{C_f}{g_{m1}} \frac{d v_C}{dt} \\
  i_f &= k C_f \frac{d v_C}{dt}
\end{align*}
\]  

(3.18)

Both \( M_1 \) and \( M_2 \) NMOS transistors should operate in the saturation region in order to act like controlled current sources to obtain the expected result of \( g_{m2} = k g_{m1} \) and therefore \( i_f = k (I_B + i_C) \). In order to save the battery that supplies the LDO, these two transistors will operate in fact in the sub-threshold region (weak inversion) while maintaining the desired behavior. In this region of operation one can drive the desired transistors with lower voltages but with very high gains.
3.3. Derivative Amplifier

From the above system of equations, the transfer function of the topology is achieved:

\[ G(s) = \frac{i_f(s)}{v_X(s)} = \frac{k C_f s}{1 + s/\left(\frac{g_m}{C_f}\right)} \]  

(3.19)

where \(\frac{g_m}{C_f}\) is the pole, \(\omega_p\), of the transfer function. Being the frequency pole location inversely dependent of the \(C_f\) value, then for achieving a wider band in the derivative output voltage sensing block, one must decrease the \(C_f\) value. However, since \(C_f\) has a crucial role in \(i_G\), being \(i_G\) the current that charges the parasitic capacitors of the pass device, and as it depends linearly on \(C_f\), then decreasing \(C_f\) is out of question. As \(C_f\) cannot be changed, the only free parameter left to control the pole location is \(g_m\). \(g_m\) is proportional to \(I_B\) and to increase its value, the biasing current must also increase thus consuming more power in a fast transient until regulation. In practical terms, the equation 3.19 implements a first order high pass filter. This pole limits the derivative contribution and degrades the \(C_f\) Miller capacitance value for higher frequencies [16].

The integration of the high pass derivative output sensing block in the topology of the capless LDO, therefore merging equations 3.4 and 3.19, will result in the increase of order of the characteristic polynomial in the overall transfer function of the capless LDO and in the creation of a Left Half-Plane (LHP) zero. This zero, as briefly explain previously, may conceal and cancel the effects of a pole in the gain and phase margin responses if careful consideration is given to its placement [14].

To illustrate how sensitive the derivative output sensing block is to swings in the output of the capless LDO, a large signal analysis is given, providing that \(\Delta i_C \gg \Delta I_B\) except in the initial condition, \(t_0\), where \(i_D = i_B\):

\[
\begin{cases}
\Delta v_X = \Delta v_C + \Delta \left(\frac{i_D}{\beta}\right) \\
i_f = k (i_B + i_C) = k (i_B + C_f \frac{dv_C}{dt})
\end{cases}
\]

(3.20)

The transistors are operating in the saturation region hence \(i_D = \beta (v_{GS} - V_{Th})^2\) where \(\beta\) is the transconductance and \(V_{Th}\) is the threshold voltage of \(M_1\).

The system of equations 3.20 shows that by dynamically increasing the biasing current and assuming that the variations on the capacitor are much wider than the ones felt over the biasing current, \(i_B\), the derivative amplification range proves to be true even for large signal variations where the high pass pole is dynamically shifted to higher frequencies. However, large negatives swings in \(v_C\) will pull current from the drain of \(M_1\) therefore degrading the quality of the derivative sensing block.

Figure 3.8 shows the basic topology of the non-linear current amplification used in the feedback damping loop. It presents two inputs, currents \(i_1\) and \(i_2\), and one output, \(V_{gate}\), the gate of the pass device that ultimately will drive the pass device under all types of conditions. \(i_1\) and \(i_2\) are obtained directly from the error amplifier inputs and from the derivative sensing block outputs.
To understand the topology presented one must first consider the possible cases of operation that can occur concerning the overdrive voltage at the input of the error amplifier $v_{OD}$. Being the error amplifier a dual input port block, then voltage wise, the positive terminal can be either greater, equal or lower than the negative one. Therefore, $v_{OD}$ can be either positive, zero or negative. When the overdrive voltage is positive, the error amplifier will produce the dominant current, $i_1$, greater than $i_2$, thus biasing $M_1$ stronger and limiting $M_2$, being entirely turned off as a limit case. The opposite will occur for negative overdrive voltages. To the case where, the overdrive voltage is zero, or close to zero, the produced currents $i_1$ and $i_2$ will have a small quiescent current contribution thus keeping $M_1$ and $M_2$ limited.

As the transistors $M_1$ and $M_2$ are more or less biased, the current will flow through the resistive path and through one of the transistors to ground. The amount of current that passes through the transistors and resistors is set by the overdrive voltage and is given by $i_D = i_{\text{common mode}}$ and $i_R = \frac{i_{\text{differential mode}}}{2}$ respectively, where $i_{\text{common mode}} = \frac{i_1 + i_2}{2}$ and $i_{\text{differential mode}} = i_1 - i_2$ [44].

From Figure 3.8, through the current mirrors, the output current is obtained $i_{GF} = i_{D3} - i_{D4}$. This current is responsible for charging parasitic capacitors of the pass device and thus responsible for its reaction time to the drive command.

For the case where $i_{\text{differential mode}} > 0$ and if a large negative voltage swing occurs at node $Y$, a current imposition occurs in $M_2$ well below the quiescent value leading to the limitation of $M_4$ and therefore $i_{D4} \approx 0$ resulting in $i_{GF} \approx i_{D3}$. In a similar way, for the case where $i_{\text{differential mode}} < 0$, if a large positive voltage swing occurs at the same node, a current imposition occurs in $M_1$ well below the quiescent value. Being the transistor $M_3$ chocked, $i_{D3} \approx 0$, the current mirrored through the transistors $M_5$ and $M_6$ will be approximately zero (neglected) and as a result the output current will be given by $i_{GF} \approx -i_{D4}$.

However, the system, when put together, rises a particular problem. When the input voltage, $V_{in}$, or the load current, $i_{load}$, suffer from instantaneous large swings and, at the input of the error...
3.4. Architecture with the proposed dynamic biased derivative amplifier

amplifier, the overdrive voltage is still zero, and therefore the system is still well balanced, the sensing block imposes the derivative amplifier to its maximum gain. Its maximum gain is defined through the derivative term present in equation 3.20, however as the biasing current is still very low (Figure 3.7) the derivative sensing block proves to be inefficient. Only moments after, the error amplifier understands that the output voltage suffered from a quick undershoot/overshoot and reacts to it by dynamically boosting the biasing current, not taking full advantage of the contribution of the derivative sensing block. Note that the full contribution of derivative term is only felt in the instant where, after a large swing, the slope of the signal is still large, not happening here due to the \( v_{\text{out}} \) path signal delay. For the case where a signal is approximately constant the derivative term returns approximately zero not contributing at all for the enhancement of the system. Nonetheless, the growth of the current in the error amplifier and its mirroring to the derivative sensor biasing still enables to take advantage of the multi-loop strategy. Moreover, it was shown in the industry that further improvement is still possible to achieve concerning the time response of the error amplifier. This improvement is obtained by using a class-AB amplifier as the error amplifier [44].

3.4 Architecture with the proposed dynamic biased derivative amplifier

The proposed capless LDO voltage regulator is finally presented in Figure 3.9. It is composed by a PMOS pass device, \( M_{PD} \), an error amplifier that integrates two gain loops with a folded cascode amplifier [42], a symmetrical OTA with common-gate differential inputs, two identical voltage buffers (only one represented) and finally a fast dynamic loop.

Figure 3.9: Circuit schematic of the proposed capless LDO voltage regulator

The reason to why a PMOS is employed as a pass device was already given. However, its calibration in terms of size and current drive capability was not. Quickly revising the concept, the PMOS device is the only pass device to whom the dropout voltage is minimum (\( V_{sd \text{sat}} \)) in the strong
3. CAPACITORLESS LDO DESIGN

inversion region without increasing the quiescent current, Table 2.2. As to its calibration, the pass device must comply with the design specifications given and therefore, by the system 3.21 (two equations, four variables, leaving two free variables) one can conveniently choose/fix $I_d$ and $V_{sg} - V_T$ variables to match to the respective specification. With this, one can ensure the maximum load current of 50 mA to a PMOS pass device in the common-source configuration with 200 mV of dropout voltage.

$$I_d = k_p \frac{W}{L} (V_{sg} - V_T)^2$$

$$g_{mp} = 2 \frac{k_p}{L} (V_{sg} - V_T) = \frac{2I_d}{V_{sg} - V_T}$$

(3.21)

The technology process parameters state that, for TSMC® 65 nm, $k_p$ is approximately 70 $\mu$A/V$^2$ for the model of the transistor employed. Its size is then extracted of equation 3.21 as $W = 800 \mu m$ and $L = 400 nm$ with 20 fingers.

Transistors $M_1 - M_6$ implement the two common-gate differential inputs of the symmetrical OTA. $M_8 - M_9$ implement the main current mirror of the amplifier and $M_{10} - M_{11}$ are simple cascode transistors. The $M_7$ transistor assures the biasing current to the differential input transistors ($M_1$, $M_2$, $M_5$ and $M_6$) through $M_3$ and $M_4$ being $i_{D7} = 200 \mu A$. The core of the symmetrical OTA is composed by the transistors $M_{14} - M_{17}$ plus $R_3$ and $R_4$ resistors. These implement the non-linear mirror explained earlier and enables the class-AB operation of the amplifier as the dynamic biasing for the output sensing block.

The current derivative amplifier (fast dynamic loop) is composed by transistors $M_{18} - M_{29}$ and by resistors $R_5 - R_6$. One can observe that in this current derivative amplifier, two high pass filters like the one previously presented exist. As already explained, the output voltage sensing block highly improves the transient response of the system if a positive swing is detected across the sensing capacitor. For negative voltage swings across the sensing capacitor, the performance of the output voltage sensing block ends up being limited. Therefore, two high pass filters are required, being one, like the one showed in Figure 3.7a and the other its complementary, transistor wise. One is acting on $V_{out}$ swing detection for overshoots while the other for $V_{out}$ undershoots. The dynamic biasing of both high pass filters is achieved through transistors $M_{20}$ and $M_{21}$. As to its operation, for an overshoot in $V_{out}$ one can verify that the conductance of $M_{19}$ is increased and the conductance in $M_{28}$ is decreased thus adjusting the response of the LDO. Similarly, for an undershoot in $V_{out}$ one can verify the opposite. According to equation 3.19 the poles location are directly affected by the transconductance of the main transistor and for the capacitance of the sensing capacitor (both 2 $pF$). Through these derivative sensing blocks is possible to obtain a dynamic control for the poles location in function of the variations felt over $V_{out}$. If the conductance in $M_{19}$ increases and the conductance $M_{28}$ decreases then the pole associated with $M_{19}$ will be shifted to higher frequencies while the other to lower frequencies. The opposite reaction is also true. With both high pass filters one can obtained the desired LDO response while keeping the quiescent low for most of the LDO operation. The transistor $M_{cas}$ serves to decouple
the \( V_{\text{out}} \) node from swings in \( V_{\text{in}} \) typical in line transient analysis. \( M_{28}, M_{29} \) and the resistors \( R_5 \) and \( R_6 \) compose one other non-linear mirror in the output derivative sensing block to enhance its current amplification. Finally \( M_{23} \) and \( M_{25} \) are the output stage of the current derivative amplifier.

The represented voltage buffer implemented by transistors \( M_{30} - M_{38} \) serves mainly to isolate the input from the output and to supply enough current to its pending block, note that the input is done by the gate of the transistor \( M_{36} \). As already stated, the inputs of the error amplifier are in the common-gate configuration, meaning that the actual input is done by the PMOS transistor source terminal. In other words, a great amount of current is required by contrast to regular configurations where the input is done by the transistor gate terminal and no current at all is required. With this voltage buffer any type of Band Gap can be coupled to the proposed capless LDO without overloading or over-draining itself, current wise. The Band Gap will command the voltage buffer and this will respond by injecting the required amount of current to the error amplifier negative input, note that the buffer output is done by a current push-pull configuration of \( M_{30} \) and \( M_{34} \) transistors. In a very similar way, a scaled down version of \( V_{\text{out}} \) is feedback to the error amplifier positive input without draining the capless output node.

Regarding \( R_1 \) and \( R_2 \), responsible for scaling down the output voltage, along with the output voltage buffer and its proper adjustment, different LDO output voltages can be achieved. This enables a comfortable degree of design customization serving a wider range of capless LDO applications.

The proposed capless LDO is redefined to operate in the sub-threshold region, in order to attain the low quiescent specification, by setting all the dropout voltages in all transistors, except the pass device, to be close to 200 mV for NMOS transistors and −200 mV for PMOS transistors. The drain currents and transconductances of each transistor in the proposed circuit were adjusted according to equations 2.10 and 2.11 respectively.

Finally, Table 3.1 summarizes the design parameters values for the sub-threshold operation.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{T_N} )</td>
<td>( \sim 0.41 \text{ V} )</td>
</tr>
<tr>
<td>( V_{T_P} )</td>
<td>( \sim 0.61 \text{ V} )</td>
</tr>
<tr>
<td>( R_3, R_4 : R_5, R_6 )</td>
<td>( 500 \Omega : 1 \text{ M}\Omega )</td>
</tr>
<tr>
<td>( C_1, C_2 )</td>
<td>( 2 \text{ pF} )</td>
</tr>
<tr>
<td>( M_1 - M_6 : M_7 : M_8, M_{10}, M_{12}, M_{13} : M_9, M_{11} : M_{14-17} )</td>
<td>( 1 : 2 : 1 : 10 : 1 (\frac{W}{L})_B )</td>
</tr>
<tr>
<td>( M_{20}, M_{21} : M_{18}, M_{19}, M_{22-24}, M_{26-29} : M_{23}, M_{25} : M_{\text{aux}} )</td>
<td>( 1 : 5 : 10 : 16 (\frac{W}{L})_B )</td>
</tr>
<tr>
<td>( M_{30} : M_{31}, M_{32}, M_{34-38} : M_{33} )</td>
<td>( 6 : 1 : 2 (\frac{W}{L})_B )</td>
</tr>
</tbody>
</table>

The design transistor sizes are defined having the size of the biasing transistors as reference. The biasing transistors size is given by \( (\frac{W}{L})_B \) where their drain current, \( i_{DB} \), is set to 100 nA.

The full design schematics can be consulted in the Appendices chapter. The top level schematic of the proposed capless LDO is given in Appendix B.1. The schematic of the error amplifier is given in
Appendix B.2. The schematic of the input current buffers (Band Gap buffer and LDO output voltage buffer) are given in Appendix B.3 and B.4 respectively, and finally, the schematic of the fast dynamic loop (derivative loop) is given in Appendix B.5.

The power down circuitry can be found in Appendixes B.6a, B.6b, B.6c, B.6d and B.6e.

3.5 Synopsis

In this chapter, the design considerations and principles were given. Particular focus was given to the multi-loop strategy as a compensation to the capless LDO. The theoretical macro-model of the proposed topology was presented, its basic characterization given along with its main analysis. Special focus was also given to the error amplifier main topology and its internal sub-blocks. Enhancements to the derivative output voltage sensing block and damping loop were exploit and its resulting actions on the output voltage response of the capless LDO explained. Finally, a section was dedicated to the integration of the proposed capless LDO where the final schematic was introduced and final considerations like sub-threshold operation were considered.
CHAPTER 4

Results

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4.1 Simulation Results

In order to fully characterize the proposed capless LDO, the results of the performed simulations are presented. The conditions of the simulations and its considerations are also given as well as their validity. All simulations were executed for the minimum dropout voltage across the pass device of 200 mV, \( V_{\text{in}} = 1.4 \) V regulating to \( V_{\text{out}} = 1.2 \) V. It is assumed that the capacitance seen by the output node of the LDO forward is 100 \( pF \), it includes the power line distribution capacitances as well as parasitics capacitances. Nevertheless, the proposed LDO is stable for all output capacitances up to
4. RESULTS

1 nF as it will be shown later.

The design passes all Process-Voltage-Temperature (P-V-T) corners and Process and Mismatch (P-M) Monte Carlo simulations showing a good compromise between its trade-offs.

4.1.1 Open loop GBW Simulations

Figure 4.1 shows the AC response of the design where the open loop gain, bandwidth and phase margin can be drawn to both light and heavy load conditions, $I_{out} = 100 \mu A$ and $I_{out} = 50 mA$ respectively.

Figure 4.1: Open loop frequency response of the proposed capless LDO under light and heavy load conditions (100 $\mu A$ and 50 mA)

One can observe that, for the worst case scenario, the open loop gain, bandwidth and phase margin are always greater than 60 dB, 370 kHz and 66° respectively.

To further characterize the regulator and to prove that it is stable to capacitances up to 1 nF a second simulation was performed where the output capacitor was swept from 0 F to 1 nF with a load current of 100 $\mu A$. Its response is presented in Figure 4.2.

The open loop gain, bandwidth and phase margin for the 1 nF output capacitor case, are 75 dB, 251 kHz and 33° respectively. For capacitances greater than 1 nF and for these set of trade-offs, the phase margin surpasses the 30° threshold and therefore the voltage regulator starts to present oscillations. In other words, the voltage regulator starts to become unstable.

The results achieved are very positive results due to the fact that none of the above results
goes out of the design specifications showed earlier.

Figure 4.2: Open loop frequency response of the proposed capless LDO under different output capacitances (0 F to 1 nF)

The open loop Gain–Bandwidth product (GBW) test bench can be consulted in Appendix C.1.

4.1.2 PSR Simulations

The behavior of the proposed capless LDO to ripples in the power supply node is presented in Figure 4.3.

The PSR values achieved with the proposed capless LDO to the usual values of frequency (1 kHz, 10 kHz and 100 kHz) are −45 dB, −25 dB and −10 dB respectively.

The PSR results achieved are considered positive as they confirm the theoretical behavior of the PSR response for a low power LDO. However, much can still be done to improve the response at issue, namely to improve the attenuation of undesirable ripples at the supply node throughout different segments of the frequency range.

The line regulation value can also be obtained by the system’s PSR response through its mathematical relationship, \( LNR = \frac{1}{PSR_{DC}} \) [8].

The PSR test bench can be consulted in Appendix C.2.
4. RESULTS

Figure 4.3: Power supply rejection of the proposed capless LDO under light and heavy load conditions (100 µA and 50 mA)

4.1.3 Line and Load Regulation Simulations

The input output voltage relationship presented in Figure 4.4 defines the line and load regulation of the presented voltage regulator. In fact, Figure 4.4 only represents the line regulation for both light and heavy load conditions of the capless LDO, 100 µA and 50 mA respectively.

However, more information can be drawn from the line regulation response. Ideally, the line regulation to both light and heavy load conditions should overlap for the whole range of voltages and therefore a zero load regulation response could be achieved. However, in Figure 4.4, one can observe that the line regulation to light and heavy load conditions are not superimposed and therefore load regulation exists.

Applying a linear regression to the signals present in Figure 4.4, two linear slopes are obtained. The slope of the 100 µA load condition reveals a 0.85 mV/V line regulation to the light load condition while the slope of the 50 mA load condition reveals a 0.69 mV/V line regulation to the heavy load condition. The load regulation, on the other hand, is obtained by the difference felt in the output voltage for both light and heavy load conditions, measured as 3.02 mV/mA for the minimum dropout voltage.

The line and load regulation results here presented, show in a very clear way the small impact of the load and its current has over the system and how it affects the behavior of the voltage regulator on its output voltage. Moreover, the obtained results are coherent with the expected ones predicted
by the PSR response.

Figure 4.4: Line and load regulation response of the proposed capless LDO

The line and load regulation test benches can be consulted in Appendix C.5.

4.1.4 Line, Load Transient and Output Voltage Ripple Simulations

Figure 4.5 presents the capless LDO load transient response of the proposed capless LDO. The simulation was performed to the minimum dropout voltage where the output current quickly \((rise/fall_{time} = 500 \text{ ns})\) varied from \(100 \mu A\) to \(50 \text{ mA}\) (at \(5 \mu s\)) and back again to \(100 \mu A\) (at \(15 \mu s\)). Additionally, a simulation was performed to obtain the load transient response of the LDO without the proposed fast dynamic loop (derivative loop).

As expected, the output voltage suffered from an undershoot to the \(100 \mu A - 50 \text{ mA}\) output current transition, and an overshoot to the \(50 \text{ mA} - 100 \mu A\) output current transition.

The settling time is approximately \(625 \text{ ns}\) for the output voltage undershoot case (measured when the output voltage is within \(\pm10\%\) of the regulation value) and approximately \(1.16 \mu s\) for the output voltage overshoot case.

The line transient response of the LDO is presented in Figure 4.6. In this simulation the input voltage was quickly \((rise/fall_{time} = 500 \text{ ns})\) changed from the minimum dropout \((V_{in} = 1.4 \text{ V})\) to \(V_{in} = 1.9 \text{ V}\) and then changed back again to the minimum dropout voltage for a constant output current of \(50 \text{ mA}\). As before, an extra simulation was performed to show the impact of the fast dynamic loop in the proposed LDO.
4. RESULTS

![Load transient response of the proposed capless LDO](image1)

**Figure 4.5:** Load transient response of the proposed capless LDO

![Line transient response of the proposed capless LDO](image2)

**Figure 4.6:** Line transient response of the proposed capless LDO

The output voltage of the LDO recovers to ±10% of its final value within approximately 0.7 μs for both overshoot and undershoot cases when the fast dynamic loop is employed. A 169 mV output voltage overshoot is achieved for the 1.4 V – 1.9 V input transition while a 98 mV output voltage undershoot is achieved for the 1.9 V – 1.4 V input transition.
The line and load transient results achieved are considered good results due to the fact that the regulation is possible even with low quiescent current while the under and overshoot results are kept relatively low.

To complement the already given PSR analysis, the output voltage ripple response is given in Figures 4.7a and 4.7b to an input voltage of 1.4 V and 3.3 V respectively. In the output voltage ripple test bench, and as applied in [16], a 1 kHz sinusoidal input wave with 100 mV of amplitude is added to \( V_{\text{in}} \) to obtain the output ripple for both light and heavy load conditions.

![Graphs showing ripple rejection for both light and heavy load conditions](image)

**Figure 4.7:** Ripple rejection for both light and heavy load conditions (100 \( \mu \)A and 50 mA)

By Figures 4.7a and 4.7b one can observe that for a 100 mV of amplitude in the input voltage, and for the worst case scenario, the proposed LDO can suppress the input ripple to about 3.5 mV.

The line and load transient test benches can be consulted in Appendix C.3 and C.4. The output voltage ripple test bench can be also consulted in Appendix C.7.

### 4.1.5 Start-up Simulations

This simulation aims to show both the start-up response and power-down response of the design since the circuitry only starts up when the power down digital signal is *LOW* (logic level 0). For this simulation the input voltage considered was 3.3 V to both light and heavy load conditions, 100 \( \mu \)A and 50 mA respectively. The design start-up response is shown in Figure 4.8.

This result shows that for the light load condition, smaller current case, the regulator settles to the desired output voltage within 2 \( \mu \)s considering the ±10% settling specification. As to the heavy load condition, higher current case, the regulator settles to the desired output voltage within less than 1 \( \mu \)s revealing a much better start-up performance for high output currents.

In both cases, when the power down signal is *HIGH* (logic level 1), the block is therefore turned off, the quiescent current converges to a steady value of 27.5 \( p \)A (at room temperature). On the other hand, when the power down signal is *LOW*, the block starts-up and its regulation takes place.
4. RESULTS

consuming only 3.7 $\mu$A of quiescent current (at room temperature). In any of the cases, the results are well within the start-up and power down specifications.

The start-up test bench can be consulted in Appendix C.6.

![Figure 4.8: Start-up response of the proposed capless LDO under light a heavy load conditions (100 $\mu$A and 50 mA)](image)

4.2 Monte Carlo Simulations

It is crucial to perform P-M Monte Carlo simulations to any given design mainly because there is a need to understand how it behaves when imposed to uncertainty and variability. Moreover, it is also crucial to understand how the design propagates uncertainty and variability through its outputs before actually printing the design through a lithographic process that is not totally predictable and certain.

P-M Monte Carlo simulations as the name suggests comprise different types of simulations, process simulations, mismatch simulations and/or both of the aforementioned simulations.

Process simulation considers the variations of the parameters of the design while the mismatch simulation shows how adjacent devices, that should be balanced and should behave similarly, are matched depending on their internal parameters such as their width, length, number of fingers, carrier mobility, threshold voltage, layout structure among others.

By applying random variations to both process and mismatch parameters, in Monte Carlo simulations, one can obtain different outcomes (as many as one want) and better forecast the behavior of the design. In other words, one can obtain the overall yield estimation of the design.
4.2. Monte Carlo Simulations

To prove the robustness of the proposed design, a set of 100 runs of Monte Carlo simulations were performed to the open loop frequency response of the design. The open loop frequency response was chosen to be representative of the robustness of the design due to the fact that it represents the main overall compromises of the capless voltage regulator.

4.2.1 Open loop GBW Simulations

![Diagram of open loop GBW simulations](image)

Figure 4.9: P-M Monte Carlo simulations (100 runs) to open loop response in light load condition ($I_{load} = 100 \mu A$)

Figure 4.9 presents the results for the light load condition (lower extreme case) while Figure 4.10 presents the results for the heavy load condition (higher extreme case). For both of the 100 run simulations, for each extreme condition, the frequency response varies around the previously obtained frequency response (Figure 4.1). Although its open loop gain, gain bandwidth and phase margin results present a slight variation it is safe to assert that are safe variations as they do not compromise in any way the systems response.

To further complement the P-M Monte Carlo simulations, the outcome of an extra 100 runs is given, showing the variation range of the capacitors and resistors values obtained, Figure 4.11.
4. RESULTS

Figure 4.10: P-M Monte Carlo simulations (100 runs) to open loop response in heavy load condition ($I_{load} = 50 \, mA$)

Figure 4.11: Capacitor and Resistor Monte Carlo variation to 100 runs
4.3. Corner Simulations

Only the variation of the largest resistor $R_2$ (1 $M\Omega$) is given for simplification purposes. The deviation obtained for the resistors $R_5-6$ (1 $M\Omega$) is roughly the same and equal to the deviation obtained in $R_2$. The deviation obtained for the resistors $R_3-4$ (500 $k\Omega$) presents small variations from each other being always inferior to the variations detected over $R_2$. As to the $R_1$ resistor (265 $k\Omega$), it also presents smaller deviations than the aforementioned resistors.

The matching result seen above, is easily explained by the fact that if both resistors use the same mathematical model, have the same size and are closely located with a suitable configuration, their deviations will be very similar. This effect is observed in the aforementioned resistors and for that reason their deviations are redundant and are not given, presenting only the larger resistive variation detected.

Table 4.1 summarizes the mean, standard deviations and the variation rate for each capacitive and resistive component.

<table>
<thead>
<tr>
<th>Component</th>
<th>$\mu$ (mean)</th>
<th>$\sigma$ (standard deviation)</th>
<th>$\Delta$Sup</th>
<th>$\Delta$Inf</th>
<th>Suprate (2$\sigma$)</th>
<th>Infrate (2$\sigma$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_1$ (2 pF)</td>
<td>2.02 pF</td>
<td>230 fF</td>
<td>200 fF</td>
<td>230 fF</td>
<td>19.8 %</td>
<td>22.7 %</td>
</tr>
<tr>
<td>$C_2$ (2.06 pF)</td>
<td>2.05 pF</td>
<td>53 fF</td>
<td>80 fF</td>
<td>55 fF</td>
<td>7.8 %</td>
<td>5.3 %</td>
</tr>
<tr>
<td>$R_2$ (1.02 $M\Omega$)</td>
<td>997 k$\Omega$</td>
<td>126 k$\Omega$</td>
<td>123 k$\Omega$</td>
<td>127 k$\Omega$</td>
<td>24.6 %</td>
<td>25.5 %</td>
</tr>
</tbody>
</table>

For both capacitor and resistor variation results, one can observe that the mean value is well concentrated around the designed value and the variations obtained (for 2$\sigma$) meet the design specifications. Furthermore, runs where the probability of occurrence is very slim and that are located well beyond the 2$\sigma$ range, can be safely neglected.

4.3 Corner Simulations

P-V-T Corner simulations have also and important role in the design validation as they are responsible for assuring that the final design behavior holds unchanged, with small variations within a certain range to certain conditions, before the actual manufacturing of the device.

The variations implied in this type of analysis are of three types: Process variation (P), Supply voltage variation (V) and finally Operating Temperature variation (T).

The first type of variation refers to variations in the manufacture conditions such as temperature, impurity concentration densities, oxide thicknesses and diffusion depths [45].

The second type of variation refers to the behavior of the design, and therefore the behavior of its transistors, when supplied with different voltages. How does it change the transistor polarizations, currents, delays, among others [45].
4. RESULTS

The last type of variation refers to the robustness of the design to temperature variations. The chip itself, or parts of it, due to switching, short-circuit and leakage power consumption, are actually responsible for the temperature variation throughout the chip in a non uniform way. Furthermore, the threshold voltage of every transistor is temperature dependent. As temperature rises up the threshold voltage decreases, meaning that the transistors will start conducting earlier. The inverse is also true for all transistors [45].

There were performed a total of 16 corner simulations combining slow-slow, fast-fast, slow-fast, fast-slow transistor performances along with variations in supply voltage, from 1.4 V to 3.3 V, and temperature variations, from $-40^\circ$ up to $125^\circ$.

4.3.1 Open loop GBW Simulations

The corner simulations to the open loop frequency response of the proposed capless LDO are depicted in Figure 4.12 and 4.13 respectively for the light load condition and heavy load condition.

![Open loop GBW Simulations](image)

Figure 4.12: Corner simulations to the open loop frequency response, light load condition ($I_{load} = 100 \ \mu A$)

It can be concluded that the open loop results are good presenting only a small and expected variation in the open loop gain and phase margin. As to the bandwidth, it presents an acceptable variation for the corner simulations where, for some corners, it it greatly improved.

Table 4.2 summarizes the obtained results, for the light load condition, showing its variation, maximum and minimum obtained values.
4.3. Corner Simulations

Figure 4.13: Corner simulations to the open loop frequency response, heavy load condition ($I_{\text{load}} = 50 \, mA$)

Table 4.2: Summary of the open loop GBW corner simulation for 100 $\mu A$ load current

<table>
<thead>
<tr>
<th>Maximum Variation</th>
<th>Maximum</th>
<th>Minimum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>8.6 $dB$</td>
<td>81.2 $dB$</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>603 kHz</td>
<td>967 kHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>25.5$^\circ$</td>
<td>68.9$^\circ$</td>
</tr>
</tbody>
</table>

The above results are also congruent with the previously obtained simulations regarding the open loop GBW analysis.

Note also that none of the corner simulations causes the regulator to fail its regulation by becoming unstable.

4.3.2 PSR Simulations

Figures 4.14 and 4.15 present the corner simulations for the PSR design response for light and heavy load conditions respectively.

Analyzing these results, one can see that this topology behaves better in the low frequency spectrum, achieving greater attenuations of perturbations in the input signals. Since the bandwidth of the regulator has a crucial role in its operation, preference was given to the low frequency spectrum in the PSR trade-off. As a direct result, the obtained values of attenuation in the mid and high frequency
4. RESULTS

spectrum were lower where the response is a function of the output node impedance [4]. Moreover, the
divergence between both presented cases, concerning the passband, is due to the fact that when the
load demands high currents (heavy load condition) the ESR zero is shifted to near the upper passband
pole canceling its effect and therefore expanding the passband region [4].

![Graph](image1.png)

Figure 4.14: Corner simulations to the PSR response, light load condition ($I_{load} = 100 \mu A$)

![Graph](image2.png)

Figure 4.15: Corner simulations to the PSR response, heavy load condition ($I_{load} = 50 mA$)

The PSR corner results achieved are congruent with the theoretical result as with the PSR
4.3. Corner Simulations

4.3.3 Line and Load Transient Simulations

The corner simulations applied to the transient response of the proposed voltage regulator is depicted in Figure 4.16.

![Figure 4.16: Corner simulation applied to the design transient response](image)

The transient response of the presented simulation shows the output behavior of the proposed capless LDO. It shows a good compromise between the trade-offs of the design and, as before, none of the corner simulations fails to meet the design specifications. For the worst case scenario, transition from 50 mA to 100 µA, just in 500 ns, the output voltage response is slightly aggravated but as it matches the corner simulations where the voltage supply is 3.3 V, its result is still considered good.

The transient response refers to a small increment and decrement of the output current, a more probabilistic and realistic response. Moreover, with this type of simulation a more robust and rich simulation is obtained, by contrast to the step transition simulation.

4.3.4 Start-Up and Power Down Simulations

Figures 4.17a and 4.17b present the corner simulation for the start-up response of the design.
4. RESULTS

Figure 4.17: Corner simulation for the design start-up response

It presents good start-up results as, for the worst case scenario, it dictates that the system is regulating under less than 6 µs considering the 10% final value rule.

4.4 Comparison with previously reported works

In order to introduce the proposed work in the contextual frame presented earlier in the State of the Art section, a Figure of Merit (FOM) has been adopted [25] (given by equation 4.1) and equally applied to this and other previously reported works.

\[
FOM = \frac{C_{out} \Delta V_{out} I_Q}{I_{loadmax}^2}
\]  

(4.1)

\(C_{out}\) is the estimated on-chip load capacitance, \(\Delta V_{out}\) is the highest voltage spike detected for transient variations, \(I_Q\) is the quiescent current and finally, \(I_{loadmax}\) is the maximum output current that the voltage regulator is able to supply. A lower FOM implies a better overall performance. For this work the FOM obtained was 29 fs.

Table 4.3 summarizes the individual characteristics and trade-offs of each work. It also presents an individual FOM for each reported work thus better enabling a fair comparison between works.

The FOM comparison given above strongly highlights the importance of the proposed improvements and trade-offs. From equation 4.1, one can observe that lower FOMs are achieved when the output capacitance, the maximum output voltage variation and quiescent current are small, the smaller the better, while supplying large output currents. However, as previously showed, these parameters are related to each other in non-linear ways so imposed compromises are always present due to the nature of topology and its internal components.

The proposed topology can also be easily adapted to meet other specifications, concerning the
output voltage, due to its resistive voltage divider. This feature allows this topology to be reused in different SoCs, or several times in the same SoC with different voltage regulations if required, thus saving design time.

The proposed capless LDO is suitable for practical implementation, presents low quiescent current as well as an excellent FOM and excellent line and load transient responses.

### 4.5 Synopsis

This chapter started by presenting the simulations results of the proposed capless LDO (normal operation at room temperature). A brief comparison between the expected theoretical results and the obtained results was given. The design was also subjected to 100 runs of P-M Monte Carlo analysis. The open loop frequency response was preferred to show the robustness of the design as it contains more information about the designs trade-offs. In this chapter, the P-V-T corner simulations applied to the design were also presented. For each set of runs the design behavior was briefly discussed. Finally, a comparison with the previously reported works was provided.
4. RESULTS
5.1 Layout considerations

The proposed design is implemented in TSMC® 65 nm CMOS technology. Its layout is presented in Figure 5.1 and occupies an area of 0.196 $mm^2$ (without pads).

The layout of a design, in this case of an LDO, represents the final product, represents all the simulations, all the efforts made and the real costs of fabrication. Therefore, it has to be robust to all simulations and it should be, ideally, small in area and in layers required. Special care needs to be paid to some issues in order to maintain the design performance.

Good layout techniques imply better protection of transistors against unavoidable mismatching issues during the fabrication process, also imply improved techniques against switching and gradient issues across the design area. Current density over the layout area is also a very important concern. The use of dummy components is also very important to protect the actual components. Metal paths need to be designed accordingly with their maximum tolerable current. By the use of several contact pins between two layers (i.e. Poly and Metal1) the routing resistance can be minimized and so the voltage drop [48]. This technique was extensively used in the pass device terminals. To enable interoperability and to avoid shorts circuits with other nearby blocks, odd metal layers have vertical displacement while even metal layers have horizontal displacement. To save resources this design uses only to the first two layers of metal.
5. LAYOUT

5.2 Ultra low power LDO voltage regulator Layout

The inputs of the error amplifier have crucial importance in the LDO performance and so the offset voltage between each input transistor needs to be reduced. Some techniques exist to minimize the offset voltage between matched components, where the inter-digital and common-centroid techniques [48] are the most employed. In this layout inter-digital techniques were preferred. Furthermore, guard rings were also used around each matched input pair in order to prevent changes from switching and thermal gradient effects.

In fact, large components such as the pass device, the $1 \, M\Omega$ and $500 \, k\Omega$ resistors were also broken several times to improve component yield and allow the use of guard rings to decrease the negative effects of their operation. An extra guard ring was employed around each large component to achieve further protection. Guard rings were also used in every sensitive area, inside the control core.

As the load consumes a maximum of $50 \, mA$ of current then the vdd rail must be designed to deliver such current. The $1 \, \mu m$ (width) of metal path per $1 \, mA$ of current was used as a rule of thumb.

Figure 5.1: Ultra Low Power LDO Voltage Regulator Layout
thus justifying its large width for a metal path. The vdd rail for the control core is fed separately and has much lower length as it needs to supply much smaller currents.

Figure 5.2 presents a close up of the layout where the core circuitry can be found and where each internal component was identified.

![Figure 5.2: Close up of the LDO control circuitry](image)

The capacitors of the derivative amplifier were implemented by MOScap transistors thus saving analog core area.
5. LAYOUT

To further improve the proposed layout, Electrostatic discharge (ESD) circuitry could be applied to each I/O pad in order to save the pass device and the control core from electrostatic discharges. For SoC integration, only the pads that need to be tapped from the outside of the chip need this type of circuitry.

5.3 Synopsis

In this chapter the proposed design layout was presented. The layout considerations taken into account were given as well as the rules imposed by the technology. Special care was provided to current density in the layout process. In the layout, even metal layers were employed to perform horizontal metal paths and odd metal layers to perform vertical metal paths therefore obtaining a more robust layout design. Finally, special attention was also given to the protection and isolation of each component by employing several guard rings and dummy components.
6.1 Summary and Conclusions

The design of an ultra low power capless LDO voltage regulator was the main objective of this work. Its specifications were defined having the State of the Art in consideration. Several topologies were studied and its improvements analyzed in order to add some insight and positive contribution to the present work. The stability without output capacitor and quiescent current issues were the main restraints of the design in its early stages. Several LDO core topologies (error amplifiers) were discarded due to the impossibility of implementation in the technology, or due to its inability of operation at low levels of voltage and quiescent current and finally due to its frequency response to such a small capacitor value. During the research time of this work, three error amplifier topologies seemed suitable and adequate for the job, where the adopted one stood out, performance wise. The following stage of the research was identical to the former relatively to the compensation topology. The multiloop strategy and dynamic biasing of the derivative amplifier proved to be the better choice. Miller compensation was also included as well as the push-pull strategy.

In the end, a new capless LDO topology was successfully implemented based on a new theoretical macromodel. The above compensations and strategies led to significant gains in the overall LDO response. This fact is corroborated by the simulated results showed earlier that, for low quiescent currents, are said to be excellent overall results. The design output voltage undershoots and overshoots, in line and load transients, are great and their settling time minimal.

The performance comparison of the proposed LDO with the other previously reported works, through the adopted FOM, clearly showed the relevance of the proposed solution and the benefits of
6. CONCLUSION

The proposed capless LDO voltage regulator was developed in TSMC® 65 nm CMOS technology at INESC-ID®, Lisbon, Portugal.

6.2 Achievements

The proposed capless LDO, with the fast derivative amplifier, achieved a maximum voltage spike of 198 mV when the load current was changed from light to heavy load conditions (worst case scenario) in only 500 ns. Moreover, when \( V_{in} \) changed from 1.4 V to 1.9 V, and back again to 1.4 V, the obtained output voltage variation was always inferior to 170 mV (worst case scenario). The power efficiency(\( \eta \)) obtained was around 85.7 % while the current efficiency(\( \eta_I \)) obtained was 99.9 %. Finally, while presenting excellent results for a 3.7 \( \mu \)A quiescent current, the proposed topology proved to be stable under all load conditions.

The design specifications introduced in Table 1.1, Chapter 1.3 Objectives, were all met, including for P-V-T Corner and P-M Monte Carlo Simulations. Table 6.1 summarizes the final results obtained with the proposed topology.

Table 6.1: Summary of the capless LDO voltage regulator simulation results

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>COMMENTS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>-</td>
<td>TSMC® 65 nm</td>
<td></td>
<td></td>
<td></td>
<td>mm²</td>
</tr>
<tr>
<td>Analog Core Area</td>
<td>-</td>
<td>0.196</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>( T_j )</td>
<td>-40 - 25 - 125</td>
<td>°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>( V_{in} )</td>
<td>1.35 - 1.4 - 3.3</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage</td>
<td>( V_{out} )</td>
<td>1.07 - 1.2 - 1.4</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load Current</td>
<td>( I_{load} )</td>
<td>0 - 50</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Line Regulation</td>
<td>( \Delta V_{out}/\Delta V_{in} )</td>
<td>1.35V ( \leq V_{in} \leq 3.3V )</td>
<td>0.69 -</td>
<td>0.85</td>
<td>mV/V</td>
<td></td>
</tr>
<tr>
<td>Line Transient</td>
<td>( \Delta V_{out}/V_{in} )</td>
<td>( V_{in} ) from 1.4V to 1.9V</td>
<td>1.102 -</td>
<td>1.198</td>
<td>1.368</td>
<td>V</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>( \Delta V_{out}/I_{load} )</td>
<td>100( \mu )A ( \leq I_{load} \leq 50mA )</td>
<td>3 - 3.02 - 3.5</td>
<td>mV/mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load Transient</td>
<td>( \Delta V_{out}/I_{load} )</td>
<td>( I_{load} ) from 100 ( \mu )A to 50 mA</td>
<td>1.050 -</td>
<td>1.202</td>
<td>1.398</td>
<td>V</td>
</tr>
<tr>
<td>Power Supply Rejection</td>
<td>PSR</td>
<td>1, 10, 100 kHz</td>
<td>-45 -</td>
<td>-25 -</td>
<td>-10</td>
<td>dB</td>
</tr>
<tr>
<td>Gain Bandwidth</td>
<td>( GBW )</td>
<td>165 - 476 - 1080</td>
<td>kHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Phase Margin</td>
<td>( PM )</td>
<td>43 - 66 - 69</td>
<td>°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Startup Time</td>
<td>( T_s )</td>
<td>- to 90% of ( V_{out} )</td>
<td>- - 6</td>
<td>µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resistor Variation</td>
<td>-</td>
<td>24.6 - 25.5</td>
<td>%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor Variation</td>
<td>-</td>
<td>19.8 - 22.7</td>
<td>%</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CURRENT CONSUMPTION**

<table>
<thead>
<tr>
<th>CURRENT CONSUMPTION</th>
<th>( I_{QON} )</th>
<th>( I_{QOFF} )</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>All blocks ON</td>
<td>-</td>
<td>-</td>
<td>3.7</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>All blocks in Power Down</td>
<td>( I_{QOFF} )</td>
<td>-</td>
<td>27</td>
<td>pA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
6.3 Future Work

The initial research for this work made possible to integrate a MATLAB and Mathematica solutions/scripts that can easily be shared and help designers to understand and play with the different LDO trade-offs in a very comfortable way.

In addition, the author of this thesis co-authored a research paper along with M. S. Jorge Esteves, Ph. D. Júlio Paisana and Ph. D. Marcelino Santos. The paper was submitted to Microelectronics Journal with the name of "Ultra Low Power Capless LDO with Dynamic Biasing of Derivative Feedback" [12].

6.3 Future Work

As modern power management trends keep evolving, stronger and stronger forces are felt over the electronic design industry. As a result, improvements to the State of the Art topologies are always a question of time. The proposed concept represents a contribution to the State of the Art for capless LDO voltage regulators. However, concerning the proposed topology, much can still be done to complement this contribution and increase its performance. A few aspects of this work were not fully improved due to the different possible combinations of trade-offs and the limited time available. To mention a few:

- The derivative amplifier current driving capability could be improved allowing a faster source current and current sinking capability from the voltage regulator output node. A different compromise between quiescent current and output voltage might exist and surpass the current one, efficiency wise. Moreover, if the delay felt over the error amplifier is further minimized when a swing in the output voltage is detected, a greater improvement can be achieved.

- In addition to the derivative amplifier, several clipping circuits exit and can be applied to the regulator, ensuring a much thinner output voltage variation range. As before, the compromise of quiescent current, output voltage and analog core area needs to be considered.

- The PSR response of the voltage regulator can be adjusted and further improved by increasing the impedance from $V_{in}$ to $V_{out}$ and decreasing the impedance from $V_{out}$ to ground [8]. Other solution exists such as, attaching an RC low-pass filter in series with the pass device (rises a problem of headroom limit).

- As the lithographic processes are improved, the length of the transistors decrease allowing better results and performances. Porting the current design to better technologies will also lead to better results.
References


APPENDIX A

Theoretical analysis

(*------------------------------------------------------------------*)
(*Two equation system, two free variables (vod, vo).*  *)
(*eq1 = -gm vref == vod/ro + s * cgs + vod + s * cdg * (vod - vo) *)
(*eq2 = -gm vod == vo/rop + s * co + vo + s * cdg * (vo - vod) *)
(*------------------------------------------------------------------*)
ClearAll["Global`*"]
Clear[Vod, Vodsol, Vo, Vosol, Result, vref, co, cgs, cdg, gm, gmp, vod, f, s]

Vodsol = Solve[-gm * vref == vod/ro + s * cgs + vod + s * cdg * (vod - vo), vod]
Vod[s_] = Vodsol[[1, 1, 2]]

((vod → 
  ro (cdg s vo - gm vref) /
  1 + cdg ro s + cgs ro s))

ro (cdg s vo - gm vref)
1 + cdg ro s + cgs ro s

Vosol = Solve[-gmp * Vod[s] == vo/rop + s * co + vo + s * cdg * (vo - Vod[s]), vo]
Vo[s_] = ExpandDenominator[Simplify[Vosol[[1, 1, 2]]]]

((vo → 
  gmp ro vref
  l+cdg ro s+cgs ro s
  +
  cdg gm ro s vref
  l+cdg ro s+cgs ro s
  -
  l rop - cdg s - co s
  l+cdg ro s+cgs ro s
  +
  cdg rop s
  l+cdg ro s+cgs ro s
  +
  cdg' ro s'
  l+cdg ro s+cgs ro s))

(gm ro rop (gmp - cdg s) vref) /
(1 + cdg ro s + cgs ro s + cdg rop s +
  co rop s + cdg gmp ro rop s + cdg cgs ro rop s^2 + cdg co rop s^2 + cgs co rop s^2)

Result[s_] = Vo[s] / vref

(gm ro rop (gmp - cdg s)) /
(1 + cdg ro s + cgs ro s + cdg rop s +
  co rop s + cdg gmp ro rop s + cdg cgs ro rop s^2 + cdg co rop s^2 + cgs co rop s^2)
(*---ZERO---*)
Zero := Solve[Numerator[Result[s]] == 0, s]
Zero[[1, 1, 2]]

gmp

cdg

(*---POLES---(Real poles, without approximation)*)
Polo := Simplify[Solve[Denominator[Result[s]] == 0, s]]
Polo[[1, 1, 2]]
Polo[[2, 1, 2]]

\[-\left(\frac{cdg \text{ ro} + cgs \text{ ro} + cdg \text{ rop} + co \text{ rop} + cdg \text{ gmp} \text{ ro} \text{ rop} +}{(2 (cgs \text{ co} + cdg (cgs + co)) \text{ ro} \text{ rop})}\right)\]
\[-\left(\frac{\sqrt{-4 (cgs \text{ co} + cdg (cgs + co)) \text{ ro} \text{ rop} + (cgs \text{ ro} + co \text{ rop} + cdg \text{ ro} + rop + gmp \text{ ro} \text{ rop})^2}}{(2 (cgs \text{ co} + cdg (cgs + co)) \text{ ro} \text{ rop})}\right)\]

(*---POLES---(poles far apart hypothesis)---*)
(*low frequency pole - the quadratic term can be disregarded*)
(*high frequency pole - the unitary term can be disregarded*)
Poloaltafreq = Solve[cdg \text{ ro} \text{ s} + cgs \text{ ro} \text{ s} + cdg \text{ rop} \text{ s} + co \text{ rop} \text{ s} +
cdg \text{ gmp} \text{ ro} \text{ rop} \text{ s} + cdg \text{ cgs} \text{ ro} \text{ rop} \text{ s}^2 + cdg \text{ co} \text{ rop} \text{ s}^2 + cgs \text{ co} \text{ rop} \text{ s}^2 == 0, s]
Poloaltafreq = Expand[Solve[[1 + cdg \text{ ro} \text{ s} + cgs \text{ ro} \text{ s} + cdg \text{ rop} \text{ s} + co \text{ rop} \text{ s} + cdg \text{ gmp} \text{ ro} \text{ rop} \text{ s} == 0, s]]]

\[
\begin{cases}
\{s \to 0\}, \\
\{s \to \frac{-cdg \text{ ro} - cgs \text{ ro} - cdg \text{ rop} - co \text{ rop} - cdg \text{ gmp} \text{ ro} \text{ rop}}{(cdg \text{ cgs} + cdg \text{ co} + cgs \text{ co}) \text{ ro} \text{ rop}}\}
\end{cases}
\]

\[
\begin{cases}
\{s \to 1\} \\
\{s \to \frac{1}{-cdg \text{ ro} - cgs \text{ ro} - cdg \text{ rop} - co \text{ rop} - cdg \text{ gmp} \text{ ro} \text{ rop}}\}
\end{cases}
\]

(*----------------------------------------------------------*)

(* AC PSR analysis *)
(*eq1 = gmp+v=cdg+d(v-v/o)/dt+cgs+d(v-v/i)/dt *)
(*eq2 = -gmp(v-v/i)-co*d(v/o)/dt+cdg*d(v-v/o)/dt = 0 *)

ClearAll["Global\"""]
Clear[Vosol, vo, vi, v, Vsol, vref, co, cout, cgs, cdg, gm, gmp, f, s]

(*dV/dt := s*sV*)
Vsol = Solve[-gmp (v-v/i) - cout * s*vo + cdg * s * (v-v/o) == 0, v]
V[s_] = Vsol[[1, 1, 2]]

\[
\begin{cases}
\{v \to \frac{\text{gmp} \text{ vi} - \text{cdg} \text{ s} \text{ vo} - \text{cout} \text{ s} \text{ vo}}{\text{gmp} - \text{cdg} \text{ s}}\}
\end{cases}
\]

\[
\text{gmp} \text{ vi} - \text{cdg} \text{ s} \text{ vo} - \text{cout} \text{ s} \text{ vo}
\]

\[
\text{gmp} - \text{cdg} \text{ s}
\]

74
\( \text{Vo}[s_] = \text{ExpandDenominator}[\text{Simplify}[\text{Vosol}[[1,1,2]]]] \)

\[
\begin{align*}
\text{Areal}[s_] &= \frac{\text{Vo}[s]}{\text{vi}} \\
\text{cgd} s (\text{gmp} + \text{cgs} s) v_i \\
\text{gm gmp} - \text{cgd gm} s + \text{cgd gm} s + \text{cgd cgs} s^2 + \text{cgd cout} s^2 + \text{cgs cout} s^2
\end{align*}
\]

(* A real without approximation *)

\[
\begin{align*}
\text{Aapprox}[s_] &= \frac{\text{cgd} s (\text{gmp})}{\text{gm gmp} + \text{cgd gmp} s + (\text{cgd} + \text{cgs}) \text{cout} s^2} \\
\text{gm gmp} + \text{cgd gmp} s + \text{cgd} s^2 + \text{cgd cout} s^2 + \text{cgs cout} s^2
\end{align*}
\]

(*A approx, neglecting the effect of cgs s over the transfer function*)

\[
\begin{align*}
\text{Areal}[s_] &= \frac{\text{cgd} s (\text{gmp})}{\text{gm gmp} + \text{cgd gmp} s + (\text{cgd} + \text{cgs}) \text{cout} s^2} \\
\text{gm gmp} + \text{cgd gmp} s + \text{cgd} s^2 + \text{cgd cout} s^2 + \text{cgs cout} s^2
\end{align*}
\]

\[
\begin{align*}
\text{A} &= \frac{(\text{gm} * \text{cgd} * s)}{(\text{gm} * \text{gmp} + \text{cgd} * \text{gmp} * s + \text{cout} + \text{cg} * s^2)} \\
\text{gm gmp} s
\end{align*}
\]

\[
\begin{align*}
\text{Num} &= \text{cgd} * \text{gm} * s / (\text{cg} * \text{cout}) \\
\text{Den} &= \text{gm} * \text{gmp} / (\text{cg} * \text{cout}) + \text{cgd} * \text{gmp} * s / (\text{cg} * \text{cout}) + s^2
\end{align*}
\]

\[
\begin{align*}
\text{cgd gmp} s \\
\text{cg cout} \\
\text{gm gmp} \text{cgd gmp} s \\
\text{cg cout} + s^2
\end{align*}
\]

(*ZERO in s=0*)

(*POLES*)

\[
\text{poles}[s_] = \text{Solve}\left[\text{gm gmp + cgd gmp s + cg cout s^2 == 0, s}\right]
\]

\[
\text{poles}[s][[1, 1, 2]] \\
\text{poles}[s][[2, 1, 2]]
\]

\[
\begin{align*}
\text{poles}[s] &= \left\{ s \rightarrow \frac{-\text{cgd gmp} - \sqrt{-4 \text{ cg cout} \text{ gm gmp} + \text{cgd}^2 \text{ gmp}^2}}{2 \text{ cg cout}} \right\}, \left\{ s \rightarrow \frac{-\text{cgd gmp} + \sqrt{-4 \text{ cg cout} \text{ gm gmp} + \text{cgd}^2 \text{ gmp}^2}}{2 \text{ cg cout}} \right\}
\end{align*}
\]

\[
\begin{align*}
\text{poles}[s] &= \left\{ s \rightarrow \frac{-\text{cgd gmp} - \sqrt{-4 \text{ cg cout} \text{ gm gmp} + \text{cgd}^2 \text{ gmp}^2}}{2 \text{ cg cout}} \right\}, \left\{ s \rightarrow \frac{-\text{cgd gmp} + \sqrt{-4 \text{ cg cout} \text{ gm gmp} + \text{cgd}^2 \text{ gmp}^2}}{2 \text{ cg cout}} \right\}
\end{align*}
\]
\[ \text{Cg} := \text{cgs} + \text{cgd} \]
\[ \text{Simplify}[\text{Num} / \text{Den}] \]

\[ \frac{\text{cgd gmp s}}{\text{gm gmp} + \text{s} \ (\text{cgd gmp} + \text{cg cout s})} \]
\[ \text{wn} = \text{Sqrt} \left[ \frac{\text{gm gmp}}{\text{cg cout}} \right] \]
\[ \text{Q} = \text{Simplify} \left[ \frac{\text{wn}}{\text{cgd gmp}} \right] \]
\[ \text{xi} = \text{Simplify} \left[ \frac{1}{(2 \ast Q)} \right] \]

\[ \left( \sqrt{\frac{\text{gm gmp}}{\text{cg cout}}} \right) \]
\[ \left( \frac{\text{gm}}{\text{cgd} \sqrt{\frac{\text{gm gmp}}{\text{cg cout}}}} \right) \]
\[ \left( \frac{\text{cgd} \sqrt{\frac{\text{gm gmp}}{\text{cg cout}}}}{2 \ast \text{gm}} \right) \]

(*frequency normalization*)
\[ \frac{(2 \ast \text{xi} \ast \text{S})}{(\text{S}^2 + 2 \ast \text{xi} \ast \text{S} + 1)} \]

\[ \left( \frac{\text{cgd} \sqrt{\frac{\text{gm gmp}}{\text{cg cout}}}}{\text{gm} \left( 1 + \frac{\text{cgd} \sqrt{\frac{\text{gm gmp}}{\text{cg cout}}}}{\text{gm}} + \text{S}^2 \right)} \right) \]

\[ \text{S} := \text{imag} \ast \text{omega} \]
\[ \text{imag} := (-1)^{(1/2)} \]
\[ \frac{(2 \ast \text{xi} \ast \text{S})}{(\text{S}^2 + 2 \ast \text{xi} \ast \text{S} + 1)} \]

\[ \left( \frac{i \text{cgd} \sqrt{\frac{\text{gm gmp}}{\text{cg cout}}}}{\text{gm} \left( 1 + \frac{i \text{cgd} \sqrt{\frac{\text{gm gmp}}{\text{cg cout}}}}{\text{gm}} - \text{omega}^2 \right)} \right) \]

\[ \text{wn} := \text{Sqrt}[\text{gmp} \ast \text{gm} / (\text{cpout} \ast \text{cg})] \]
\[ \text{xi} := 1/2 \ast \text{Sqrt}[\text{gmp} \ast \text{cpgd}^2 / (\text{gm} \ast \text{cpout} \ast \text{cg})] \]
\[ \text{sp1} = \text{Expand}[\text{Simplify}[\text{wn} / \text{xi}]] \]
\[ \text{sp2} = \text{Expand}[\text{Simplify}[\text{wn} \ast \text{xi}]] \]

\[ \frac{2 \ast \text{cg cpout gm}}{\text{cpgd}^2 \ast \text{gmp}} \]
\[ \left( \frac{1}{2} \right) \left( \frac{\text{cpgd}^2 \ast \text{gmp}}{\text{cg cpout gm}} \right) \]
\[ \left( \frac{\text{gm gmp}}{\text{cg cpout}} \right) \]

(* hence sp1 = wn/xi e sp2 = wn*xi*)
(*------------------------------------------------------------------*)
(* Transient analysis *)
(* eq1: cpout+dvout/dt=-gmp*vg *)
(* eq2: cg*dvout/dt = gm *(vout-vref) + cpgd + dvout/dt *)
(*------------------------------------------------------------------*)
ClearAll["Global`*"]
Clear[Vod, wn, varsigma, Vg, vg, Vgt, Vodsol, Vo, Vosol, Result, vref, co, cgs, cdg, gm, gmp, vod, f, s]

Vgt := Solve[{-gmp + vg = cpout + vod[t]'}, vg]
Vg[t_] = Vgt[[1, 1, 2]]

cpout vod[t]'
_______________
gmp

Vodt = Solve[cg*cpout + vod[t]'' - gmp == gm*vod + cpgd*vod[t]'' + vod]  
Vod[t_] = Simplify[Vodt[[1, 1, 2]]]

{(vod -> -cpgd gmp vod[t]'' + cg cpout vod[t]'') 
gm gmp

-gmp - cpgd gmp vod[t]' + cg cpout vod[t]'"

(gm gmp

(*where vod = vout - vref*)
eq[t_] = vod[t]'' - gm + cg*cpout - gmp + cpgd + vod[t]'' - gm*vod[t] == 0

gm vod[t]' + cpgd gmp vod[t]'' + cg cpout vod[t]''
gmp

vod[t]' + cpgd + gm / (cg + cpout) + vod[t]' + gm + gmp / (cg + cpout) + vod[t] == 0

gm gmp vod[t] + cpdg gmp vod[t]' + vod[t]'' == 0

cpout

cpout

gmp

(*and therefore*)
eq := vod[t]'' + 2 wn varsigma + vod[t]' + wn^2 + vod[t] == 0

*****
(assuming a solution in the form \( Ae^{^H(st)} \))

\[ \text{Vod} := Ae^{^H(st)} \]

\[ \text{eq} := A \ast s^2 + e^{^H(st)} + A \ast s \ast e^{^H(st)} \ast 2 \ast \text{wn} \ast \text{varsigma} + A \ast e^{^H(st)} \ast \text{wn}^2 = 0 \]

(*characteristic eq*)

Clear[\( \text{wn}, \text{varsigma} \)]

Simplify[Solve[\( s^2 + s \ast 2 \ast \text{varsigma} \ast \text{wn} + \text{wn}^2 = 0, s \)]

\[ \text{s1} := -\text{varsigma} \ast \text{wn} + \sqrt{-1 + \text{varsigma}^2} \ast \text{wn} \]

\[ \text{wd} := \text{wn} \ast \sqrt{1 + \text{varsigma}^2} \]

\[ \text{Vod} := A_1 \ast e^{^H \text{s1} \ast t} + A_2 \ast e^{^H \text{s2} \ast t} \]

\[ \text{Vodt} := A_1 \ast e^{^H (-\text{varsigma} \ast \text{wn} \ast t) \ast e^{^H (j \ast \text{wd} \ast t)} + A_2 \ast e^{^H (-\text{varsigma} \ast \text{wn} \ast t) \ast e^{^H (j \ast \text{wd} \ast t)} \}} \]

eulereq := e^{^H (j \ast \text{wd} \ast t) = \text{Cos}[\text{wd} \ast t] + j \ast \text{Sin}[\text{wd} \ast t]}

\[ \text{Vod} := K_1 \ast e^{^H (-\text{varsigma} \ast \text{wn} \ast t) \ast \text{Cos}[\text{wd} \ast t] + K_2 \ast e^{^H (-\text{varsigma} \ast \text{wn} \ast t) \ast \text{Sin}[\text{wd} \ast t] \}} \]

(*Vod(0) = 0 \( \Rightarrow \) 0 = K1 + 0 \( \Rightarrow \) K1 = 0*)

\[ \text{Vodfinal} := K_2 \ast e^{^H (-\text{varsigma} \ast \text{wn} \ast t) \ast \text{Sin}[\text{wd} \ast t]} \]

(*Iout = \( -\text{Cout} \ast \text{Dvod}/\text{dt} \))

\[ \text{Ioutf} := -\text{cout} \ast (K_2 \ast \text{wd} \ast \text{Cos}[\text{wd} \ast t] - K_2 \ast \text{varsigma} \ast \text{wn} \ast \text{Sin}[\text{wd} \ast t]) \ast e^{^H (-\text{varsigma} \ast \text{wn} \ast t)} \]

\[ t := 0 \]

Solve[Iout == -\text{cout} \ast (K_2 \ast \text{wd} \ast \text{Cos}[\text{wd} \ast t] - K_2 \ast \text{varsigma} \ast \text{wn} \ast \text{Sin}[\text{wd} \ast t]) \ast e^{^H (-\text{varsigma} \ast \text{wn} \ast t)}, K_2] \]

\[ \{K_2 \rightarrow \frac{\text{Iout}}{\text{cout} \ast \text{wd}}\} \]
Figure B.1: Top level schematic of the proposed capless LDO (with resistive divider embedded inside the error amplifier)
Figure B.2: Schematic of the error amplifier
Figure B.3: Schematic of the input current buffer to tap the Band-Gap output voltage. It also allows the isolation and acceptance of any Band-Gap from this LDO

Figure B.4: Schematic of the input current buffer inside the error amplifier to tap the LDO output voltage (with resistive divider)
Figure B.5: Schematic of the fast dynamic loop (derivative loop)
(a) Power down CMOS inverters

(b) Power down schematic to the error amplifier core

(c) Power down schematic to the derivative loop topology

(d) Power down schematic to the input current buffer (Band-Gap buffer)

(e) Power down schematic to the input current buffer (LDO output voltage buffer)

Figure B.6: Power down schematics
APPENDIX C

Test Benches

Figure C.1: Test Bench used to obtain the open loop frequency response of the proposed capless LDO
Figure C.2: Test Bench used to obtain the PSR response of the proposed capless LDO

Figure C.3: Test Bench used to obtain the load transient response of the proposed capless LDO
Figure C.4: Test Bench used to obtain the line transient response of the proposed capless LDO

Figure C.5: Test Bench used to obtain the line and load regulation responses of the proposed capless LDO
Figure C.6: Test Bench used to obtain the start-up and power down responses of the proposed capless LDO

Figure C.7: Test Bench used to obtain the ripple response of the proposed capless LDO