Ultra Low Power Capless Low-Dropout Voltage Regulator

(Master Thesis Extended Abstract)

João Justo Pereira
Department of Electrical and Computer Engineering
Instituto Superior Técnico - Technical University of Lisbon, Portugal
Email: joao.miguel.pereira@ist.utl.pt

Abstract—Modern power management System-on-a-Chip (SoC) design demands for fully integrated solutions in order to decrease certain costly features such as the total chip area and the power consumption while maintaining or increasing the fast transient response to signal variations. Low-Dropout (LDO) voltage regulators, as power management devices, must comply with these recent technological and industrial trends.

An ultra low power cap-less low-dropout voltage regulator with resistive feedback network and a new dynamic biased, multiloop compensation strategy is proposed. Its dynamic close-loop bandwidth gain and dynamic damping enhance the fast load and line LDO transient responses. These are assured by the output class-AB stage of the error amplifier and the feedback loop of the non-linear derivative current amplifier of the LDO.

The proposed LDO, designed for a maximum output current of 50 mA in TSMC 65 nm, requires a quiescent current of 3.7 μA and presents excellent line and load transients (<10%) and fast transient response.

Index Terms—low drop-out, ldo, low power, capless, dynamic biased, multiloop feedback.

I. INTRODUCTION

The consumer electronic industry has been undergoing severe pressures to adapt and to respond to new social and market demands. In addition, the rapid development of semiconductor manufacturing process and its respective miniaturization continues to exert severe pressures to the industry.

Power Management, as an essential research area and as part of the solution, is rapidly changing in order to meet these rigorous demands [1].

SoC solutions bring the possibility to the electronic industry to integrate the same complete system onto a single IC. It aims mainly to achieve a more compact and robust system while speeding up the manufacturing process with even lower costs of production for the same technology [2]. Each internal block, integrated onto a single IC system, requires a clean regulated low-noise and precise voltage supply [3] in order to provide increased processing power and functionality for a longer period of time [4].

Low-Dropout (LDO) voltage regulators are usually employed in voltage regulation due to their ability to regulate with a very small input-output differential voltage [5]. This advantage makes them the optimal solution for voltage regulation in SoC applications where noise-sensitive circuitry exist and where current efficiency matters.

A. Motivation

High-performance ultra low power LDOs are part of the response to the emerging need of efficient and robust electronic components. Concerning LDOs, many researchers are proposing different topologies with different compensation techniques. However, these techniques and analyses assume the small signal analyses and framework when, in fact, most of the transient voltage signals in the nonlinear pass device of the LDOs are not small [6].

B. Objectives

The objective of this thesis is to develop an ultra low power capacitor-less LDO voltage regulator capable of maintaining a steady operation under rigorous and uncertain loading conditions.

The LDO design is implemented in TSMC 65 nm CMOS technology. The software used to implement and design the proposed LDO was Cadence Virtuoso Custom IC Design, Hspice simulator, WaveView and CosmoScope waveform viewers.

C. Outline

The present paper is organized as follows: Section II: The conventional LDO regulator characterization is presented. The capacitor-less LDO regulators as an improvement of the former is also introduced. Section III: A theoretical macro-model of the design is given as starting point and a basic characterization of the proposed LDO is also provided. Section IV: The design simulation analysis are provided, explaining the results achieved. A comparison between this work and state of the art is also given. Section V: The layout of the proposed topology is given. Section VI: This section summarizes all the work done and all the options taken into account.

II. LDO VOLTAGE REGULATOR

The main blocks of the conventional LDO topology are the error amplifier, the pass device and the linear feedback network. The conventional LDO topology is presented in Figure 1. To operate, the LDO also needs a voltage reference.
The error amplifier is responsible for the voltage comparison between the reference, set by a Band Gap, and the scaled down output voltage obtained by the resistive feedback network. It is also responsible for driving the pass device in function of the comparison result just stated.

The pass device is a power device whose only function is to control the amount of current flow to the load. Typically, while driving, a pass device supplies currents from 100 A to 100 mA as shown in Tsz Yin Man study [7].

Finally, a large capacitor exists at the LDO output in parallel to the load. This large capacitor, in conventional LDO topologies, acts like a charge source during fast load transients improving the response time of the regulator and its stability [8], [9], [10]. However, as referred earlier, this capacitor poses a problem due to the fact that it is too large to be an on-chip capacitor.

A. Pass Device

G. Rincn-Mora and P. Allen published a comparative study between LDO voltage regulators with different pass devices [11] where the advantages and disadvantages of each pass device were identified and its study deepened. This study results, together with contributions of other researchers [12], identified what is known and accepted today as the most suitable pass device for LDO application, the PMOS device.

B. Efficiency

Conventional LDOs perform reasonably well and are usually preferred to other types of voltage regulation because, among others, their applied voltages are low, which translates to low consumed, low dissipated power and therefore higher power efficiency, equation 1.

$$\eta = \frac{P_O}{P_I} \times 100\% = \frac{V_{out}}{V_{in}} \frac{I_{load}}{I_{load} + I_{quiescent}} \times 100\%$$ (1)

Since $V_{out}$ and $I_{load}$ are well defined for each application, the only parameters left that can improve the LDO efficiency are $V_{in}$ and $I_{quiescent}$. The efficiency is greatly improved when the quiescent power is reduced. Moreover, as introduced earlier, lower dropout voltages will permit lower input voltages, $V_{in}$, which, by examination of equation 1, will further improve the overall LDO efficiency.

C. Stability

Stability is one key aspect concerning LDO differentiation. All the elements present in Figure 1 and their intrinsic characteristics are crucial for defining the LDO stability. As a result, stability is therefore, one of the most important trade-offs of LDOs.

The transfer function of the system is obtained from the abstraction model shown in Figure 2 where the feedback loop was broken for the purpose of the stability analysis.

The open-loop gain of the model shown is extracted as shown in equation 2.

The minimal requirements that need to be true for the LDO to be stable are: the zero must be located below the unity gain frequency and all high-frequency poles must be located at least three times higher than the unity gain frequency [13], [14].

The zero and poles are given by equations 3 and 4 respectively.

$$Z = \frac{g_{mp}}{C_{gd}}$$ (3)

$$P_1 \approx -\frac{1}{(C_o + C_{gd}) r_{op} + (C_{gs} + C_{gd}) r_o + C_{gd} g_{mp}}$$ (4)

Figure 3 represents the frequency response of the conventional LDO in accordance with the mathematical model shown. The dominant pole, the lower frequency pole, in conventional LDOs is set at the output of the LDO by the large capacitor. This capacitor exists in order to compensate the high output impedance of the LDO, providing a stronger and
\[
V_{out} = \frac{g_m g_m r_o r_{op} \left[ 1 - s \frac{C_{gd}}{g_m} \right]}{s^2 \left(C_{gd}C_{gs} + (C_{gd} + C_{gs})C_o\right)r_{op} + s \left(r_o(C_{gd} + C_{gs}) + r_{op}(C_{gd} + C_o) + C_{gd} g_{mp}r_{op}\right) + 1}
\] (2)

a more reliable instantaneous source of current improving the LDO transient response. The non-dominant pole is defined by the pass device characteristics, namely at its gate terminal, and finally the zero which is defined by the pass device’s transconductance and gate drain capacitance. Furthermore, if a buffer is used between the error amplifier and the pass device a third high frequency pole will appear increasing the negative slope by a 20 dB per decade from its position forward, as shown in Rincon-Mora stability analysis [15].

Overall, low-dropout voltage regulators justify their presence in SoC due to their chip size, fast transient responses, low-noise advantages, power efficiency and adjustable parameters.

D. Capacitor-less LDO Voltage Regulators

Capacitor-less LDOs, are an alternative to the conventional LDO voltage regulator that aim to circumvent some of the non-desirable characteristics of the latter voltage regulator.

Removing the large capacitor from the conventional LDO and replacing it by a smaller one in the range of ten to hundreds of picofarad [16], easily implemented on-chip, a more suitable LDO is achieved according to modern design trends. On the other hand, removing the large capacitor leads to other constraints of the LDO responses and performance. With the aforementioned replacement, some output filtering properties are lost.

III. CAPACITOR-LESS LDO DESIGN

A. Design Considerations and Principles

Recent studies regarding compensated capacitor-less LDOs have achieved incredible and promising experimental results.

The state of the art compensation topologies typically follow one of two strategies: (1) Active feedback compensation strategy [17], [18], [19], [20], [21] and (2) adaptive and dynamic adaptive biasing [22], [16], [23]. The first strategy aims to achieve higher loop responses by increasing the damping characteristics of the system. Miller pole-splitting compensation is also used in this strategy to provide the required stabilization. The second strategy aims to overcome the slew-rate limitations imposed by the error amplifier by embedding a class-AB amplifier inside the error amplifier or by embedding a buffer connected to the gate of the pass device as a push-pull stage [24], [4]. Both strategies also aim to improve the cap-less LDO transient response by sensing the output voltage through the derivative loop. The non-linear derivative loop will speed up the current amplification and therefore the transient response of the LDO.

Aiming to boost dynamically the bias current of the circuit and the slew-rate of the error amplifier, researchers have recently proposed a hybrid strategy. The core technique behind the hybrid strategy is achieved by sensing and mirroring a current from the fast output voltage dependent derivative loop [7], [10].

The compensation of the ultra low power capacitor-less low-dropout voltage regulator in this work proposed consists on a new multi-loop feedback strategy with internal node sensing also based on both the above mentioned strategies.

The error amplifier used in the proposed topology is composed by two gain loops with a folded cascode amplifier [25] and a symmetrical OTA with PMOS common-gate differential inputs instead of the usual common-source differential inputs.

B. Macro-model of the Capacitor-less LDO Regulator

1) Basic Characterization: The study of the present work began based on the macro-model shown in Figure 4. It represents the integral parts of the cap-less LDO as well as the pass device parasitic capacitors, gate-source and gate-drain capacitors, \(C_{gs}\) and \(C_{gd}\) respectively.

The error amplifier output current, \(i_G\), is shown in equation 5 in accordance to the model presented and neglecting the channel modulation effects. In 5, \(\tilde{g}_m\) represents the dynamic transconductance of the model while \(\tilde{C}_f\) represents the dynamic active Miller capacitance.

\[
i_G = \tilde{g}_m v_{od} + \tilde{C}_f \frac{dv_{out}}{dt} = \left(\sum_{i=0}^{M} \sum_{j=0}^{N} a_{ij} |v_{od}|^i \left|\frac{dv_{out}}{dt}\right|^j\right) v_{od} + \\
+ \left(\sum_{i=0}^{M} \sum_{j=0}^{N} b_{ij} |v_{od}|^i \left|\frac{dv_{out}}{dt}\right|^j\right) \frac{dv_{out}}{dt}
\] (5)

To consider a wider and more generalist analysis where the operating point of the circuit is changed and the non-linear effects of the elements are taken into account, large signal analyses, this model admits these last parameters to be non-negative coefficient polynomial functions of \(|v_{od}|\) and...
\[ \frac{dv_{out}}{dt} \] and where their first order coefficients, \( a_{00} \) and \( b_{00} \) are the conventional transconductance \( g_m \) and active Miller capacitance \( C_f \) [10].

2) AC Analysis: To obtain the AC response of the model, a small signal analysis is required. From Figure 4 and knowing that the continuity current condition at the pass device terminals needs to be respected, \( i_g \) and \( i_d \) can be extracted and considering that the pass device is operating deep in the saturation region and \( V_{in} \) and \( I_{out} \) are constant. By transcribing \( i_g \) and \( i_d \) to the complex domain, normalizing it and solving it to \( v_{out} \), the close loop gain of the model can thus be achieved, 6.

\[
A_{vc} = \frac{v_{out}}{v_{ref}} = \frac{v_{out}}{s^2 + \frac{\omega_n^2}{\overline{Q}} + \omega_n^2} = \left( \frac{g_{mp} g_m}{C_{out} C_g} \right) s^2 + \left( \frac{g_{mp} C_{gd}^2 g_m}{g_m C_{out} C_g} \right) s + \frac{g_{mp} g_m}{C_{out} C_g} \tag{6}
\]

where \( C_{gd} \) is the the effective Miller capacitance, \( C_g \) is the error amplifier capacitance and \( C_{out} \) is the pass device output capacitance, given respectively by \( C_{gd}^* = C_f + C_{gd} \), \( C_g = C_{gs} + C_{gd} \) and finally \( C_{out}^* = C_{out} + C_{gd} \) and \( \omega_n \) and \( \zeta \) are the undamped natural frequency and the damping ratio respectively given by equations 7 and 8 respectively.

\[
\omega_n = \sqrt{\frac{g_{mp} g_m}{C_{out} C_g}} \tag{7}
\]

\[
\zeta = \frac{1}{2} Q = \frac{1}{2} \sqrt{\frac{g_{mp} C_{gd}^2 g_m}{g_m C_{out} C_g}} \tag{8}
\]

One can observe that equation 6 is in fact the normalized transfer function of a bi-quadratic low-pass filter, as its denominator is a second order characteristic polynomial and therefore it will assume two poles. These two poles will be located at \( s_{p1} = -\omega_p \) and \( s_{p2} = -\omega_p \) as long as \( \zeta = \frac{1}{2Q} \gg 1 \) holds true, being Q the quality factor of the model.

Applying the previous analysis to the Figure 4, where \( g_m \) emulates a two-stage Miller OTA, the Bode magnitude response of the model is obtained.

The dashed line represents the open loop gain Bode response while the full dash represents the closed loop gain. To obtain the open loop gain the feedback loop was broken at X in Figure 4 thus cutting the \( V_{out} \) dependency. In the closed loop gain Bode response, \( \omega_1 \) assumes the value of gain bandwidth frequency, \( \omega_{GBW} \), while \( \omega_2 \) assumes the value of the high frequency pole, \( \omega_{nd} \). On the other hand, in the open loop gain Bode response, the \( \omega_1 \) assumes the value of the dominant pole, \( \omega_d \), while \( \omega_2 \) maintains the previous value of \( \omega_{nd} \). The undamped natural frequency, \( \omega_n \), can also be given by the geometric mean \( \left( \omega_n = \sqrt{\omega_{GBW} \omega_{nd}} \right) \) of \( \omega_{GBW} \) and \( \omega_{nd} \).

Similarly, the quality factor of the system, Q, can also be given by the square root of those frequencies \( Q = \sqrt{\frac{\omega_{GBW}}{\omega_n}} \).

The proposed topology uses a Miller pole-splitting compensation technique to stabilize itself. The stabilization is achieved by spreading the gain bandwidth pole and the non-dominant pole apart. The damping ratio, \( \zeta \), is ultimately responsible for the poles location \( s_{p1} = -\frac{\omega_n}{2}, s_{p2} = -\zeta \omega_n \) and for that reason has a key role in the pole-splitting compensation due to its linear dependence of \( C_f \).

3) PSR Analysis: In order to obtain the response of the system in the frequency domain one first needs to find its transfer function. Respecting the KCL at the pass device terminals, now in the model shown in Figure 6, namely at the \( O \) node, the linear small signal analysis imposes that:

\[
\begin{align*}
\frac{g_{mp} v_{out}}{dt} = \frac{C_{gd}}{C_{out}} \frac{dv}{dt} + \frac{C_{gs}}{g_m} \frac{dv}{dt} + \frac{C_{gd}}{g_m} \frac{dv}{dt} \\
\end{align*}
\tag{9}
\]

where the pass device is assumed to be operating deep in the saturation region.

The transfer function of the system given by 10, where \( C_g = \)
$C_{gs} + C_{gd}$, is then extracted from 9 by solving the system to $v_{out}$.

$$\frac{v_{out}}{v_{in}} = \frac{\frac{\omega_n s}{Q}}{s^2 + \frac{\omega_n s + \omega_n^2}{Q}} = \frac{g_{mp} \frac{C_{gd}}{C_g} s}{s^2 + \frac{g_{mp} \frac{C_{gd}}{C_g} + g_m g_{mp}}{C_g C_{out}}}$$  \hspace{1cm} (10)$$

The above transfer function presents one zero and two poles. The undamped natural frequency, $\omega_n$, and damping factor maintain their previous values and therefore the two existing poles obtained from the denominator of the transfer function $s_{p1} = -\omega p_1 = -\frac{\omega_n}{\tau}$ and $s_{p2} = -\omega p_2 = -\zeta \omega_n$ are still located approximately at $\omega_{GBW}$ and $\omega_{nd}$. The zero is located at 0 Hz ($s = 0$ condition).

Figure 7 represents the response of the PSR analysis. The bandwidth of the filter, represented by $b$ in the PSR response, is defined as the frequencies between $\omega_L$ and $\omega_U$ that are the lower and upper passband cutoff edges respectively.

![Graph showing PSR response](image)

**Fig. 7.** Capacitor-less LDO PSR response

4) **Linear Transient Analysis:** Figure 4 is the basic topology used to obtain the transfer function considering that the feedback loop is closed and that $v_{ref}$ is constant, then the $v_{out}$ behavior will be given by:

$$\frac{d^2 v_{OD}}{dt^2} + 2 \zeta \omega_n \frac{dv_{OD}}{dt} + \omega_n^2 v_{OD} = 0$$  \hspace{1cm} (11)$$

In order to observe how $v_{out}$ changes to variations in $i_{load}$, the analysis imposes a step in the load current with well defined amplitude of $I_{out} = -C_{out} \frac{dv_{OD}}{dt}$. The progress of $v_{OD}$ is then provided by:

$$v_{OD} = -\frac{I_{load}}{\omega_d C_{out}} e^{-\zeta \omega_n t} \sin \omega_d t$$  \hspace{1cm} (12)$$

where $\omega_d$ is the damped frequency given by $\omega_d = \omega_n \sqrt{1-\zeta^2}$.

5) **Global Transient Analysis:** Starting with the linear transient response of the proposed model, equation 11, applying a second order approximation of the gate current to the system, as shown in equation 5, and normalizing it both in voltage and in time, a more generalized equation is achieved 13.

In 13, the output voltage and time normalization were applied through the following change of variables $v_{ON} = \frac{v_{OD}}{V_{OD}}$ and $\tau = \omega_n t$, being $v_{ON}$ is the normalized output voltage and $V_{OD}$ is the pass device overdrive gate-source voltage. In 13, $\omega N$ and $\zeta$ are the normalized undamped natural frequency and dynamic damping ratio respectively. $K_1$ relates to the non-linear damping force, $b_{01}$ of 5, $K_2$ to the non-linear effects of the dynamic biasing over the damping feedback loop, $b_{10}$ of 5, $K_3$ to the restoring force, $a_{10}$ of 5, and finally $K_4$ to the dynamic biasing of the error amplifier by the derivative loop, $a_{01}$ of 5.

A study [6] was performed to illustrate the numerical solutions of 13, where the Krylov-Bogolyubov averaging method was applied to the equation at cause to obtain its asymptotic solutions. The study pinpointed that the averaging method employed shows that the average dynamical damping and the average undamping natural frequency increase linearly with the signal oscillation amplitudes.

6) **Derivative Amplifier:** Inside the derivative amplifier a small circuit like the one shown in Figure 8 exists. It enables the cap-less LDO active compensation.

The idea behind the topology present in Figure 8 is to provide a certain amount of current to its pending blocks when, and only when, it is needed, not supplying current otherwise. The supplied current is proportional to the sensed output voltage variations thus enabling a faster derivative amplifier stabilization and therefore a faster LDO regulation.

Both $M_1$ and $M_2$ NMOS transistors should operate in the saturation region in order to act like controlled current sources to obtain the expected result of $g_{m2} = k g_{m1}$ and therefore $i_I = k (i_B + i_C)$.

To illustrate how sensitive the derivative output sensing block is to swings in the output of the cap-less LDO, a large signal analysis is given, providing that $\Delta i_C \gg \Delta i_B$ except
\[
\frac{d^2 v_{ON}}{dt^2} + (2 \zeta + k_1 \left| \frac{d v_{ON}}{dt} \right| + k_2 |v_{ON}|) \frac{d v_{ON}}{dt} + (1 + k_3 |v_{ON}| + k_4 \left| \frac{d v_{ON}}{dt} \right|) v_{ON} = 0
\]

(13)

in the initial condition, \( t_0 \), where \( i_D = i_B \):

\[
\begin{align*}
\Delta v_X &= \Delta v_C + \Delta \left( \sqrt{\frac{1}{\beta} \frac{d v_C}{dt}} \right) \approx \Delta v_C + \frac{C_{\text{f}}} {g_{\text{m}_1}} \left( \frac{d v_C}{dt} \right) \bigg|_{t=t_0} + \Delta t \\
i_f &= k \left( i_B + i_C \right) = k \left( i_B + C_f \frac{d v_C}{dt} \right)
\end{align*}
\]

\[ (14) \]

The system of equations 14 shows that by dynamically increasing the biasing current and assuming that the variations on the capacitor are much wider than the ones felt over the biasing current, \( i_B \), the derivative amplification range proves to be true even for large signal variations where the high pass pole is dynamically shifted to higher frequencies.

Figure 9 shows the basic topology of the non-linear current amplification used in the feedback damping loop.

When the overdrive voltage is positive, the error amplifier will produce the dominant current, \( i_1 \), greater than \( i_2 \), thus biasing \( M_1 \) stronger and limiting \( M_2 \), being entirely turned off as a limit case. The opposite will occur for negative overdrive voltages. To the case where, the overdrive voltage is zero, or close to zero, the produced currents \( i_1 \) and \( i_2 \) will have a small quiescent current contribution thus keeping \( M_1 \) and \( M_2 \) limited.

As the transistors \( M_1 \) and \( M_2 \) are more or less biased, the current will flow through the resistive path and through one of the transistors to ground. The amount of current that passes through the transistors and resistors is set by the overdrive voltage and is given by \( i_D = i_{\text{common mode}} \) and \( i_R = \frac{i_{\text{differential mode}}}{2} \) respectively, where \( i_{\text{common mode}} = \frac{i_1 + i_2}{2} \) and \( i_{\text{differential mode}} = i_1 - i_2 \) [26].

From Figure 9, through the current mirrors the output current is obtained \( i_{GF} = i_{D3} - i_{D4} \). This current is responsible for charging parasitic capacitors of the pass device and thus responsible for its reaction time to the drive command.

7) Architecture with the proposed dynamic biased derivative amplifier: The proposed cap-less LDO voltage regulator is finally presented in Figure 10. It is composed by a PMOS pass device, \( M_{PD} \), an error amplifier that integrates two gain loops with a folded cascode amplifier [25], a symmetrical OTA with common-gate differential inputs, two identical voltage buffers (only one represented) and finally a fast dynamic loop.

Transistors \( M_1 \) – \( M_4 \) implement the two common-gate differential inputs of the symmetrical OTA. \( M_5 \) – \( M_9 \) implement the main current mirror of the amplifier and \( M_{10} \) – \( M_{11} \) are simple cascode transistors. The \( M_7 \) transistor assures the biasing current to the differential input transistors (\( M_1 \), \( M_2 \), \( M_5 \) and \( M_6 \)) through \( M_3 \) and \( M_4 \) being \( i_{DS} = 200 \) nA. The core of the symmetrical OTA is composed by the transistors \( M_{14} \) – \( M_{17} \) plus \( R_3 \) and \( R_4 \) resistors. These implement the non-linear mirror explained earlier and enables the class-AB operation of the amplifier as the dynamic biasing for the output sensing block.

The current derivative amplifier (fast dynamic loop) is composed by transistors \( M_{18} \) – \( M_{29} \) and by resistors \( R_5 \) – \( R_6 \). The dynamic biasing of the high pass filters employed is achieved through transistors \( M_{20} \) and \( M_{21} \). As to its operation, for an overshoot in \( V_{out} \) one can verify that the conductance of \( M_{19} \) is increased and the conductance in \( M_{28} \) is decreased thus adjusting the response of the LDO. Similarly, for an undershoot in \( V_{out} \) one can verify the opposite. The transistor \( M_{Cas} \) serves to decouple the \( V_{out} \) node from swings in \( V_{in} \) typical in line transient analysis. \( M_{28} \), \( M_{29} \) and the resistors \( R_5 \) and \( R_6 \) compose one other non-linear mirror in the output derivative sensing block to enhance its current amplification. Finally \( M_{22} \) and \( M_{25} \) are the output stage of the current derivative amplifier.

The represented voltage buffer implemented by transistors \( M_{30} \) – \( M_{38} \) serves mainly to isolate the input from the output and to supply enough current to its pending block, note that the input is done by the gate of the transistor \( M_{36} \).

Regarding \( R_1 \) and \( R_2 \), responsible for scaling down the output voltage, along with the output voltage buffer and its proper adjustment, different LDO output voltages can be achieved. This enables a comfortable degree of design customization serving a wider range of cap-less LDO applications.

Finally, Table I summarizes the design parameters values for the sub-threshold operation.

The design transistor sizes are defined having the size of the biasing transistors as reference. The biasing transistors size is given by \( \left( \frac{W}{L} \right)_B \) where their drain current, \( i_{DB} \), is set
to 100 nA.

IV. RESULTS

In order to fully characterize the proposed cap-less LDO, the results of the performed simulations are presented. All simulations were executed for the minimum dropout voltage across the pass device of 200 mV, $V_{in} = 1.4$ V regulating to $V_{out} = 1.2$ V. It is assumed that the capacitance seen by the output node of the LDO forward is 100 pF. It includes the power line distribution capacitances as well as parasitics capacitances. Nevertheless, the proposed LDO is stable for all output capacitances up to 1 nF as it will be shown later.

The design passes all P-V-T corners and P-M Monte Carlo simulations showing a good compromise between its trade-offs.

A. Open loop GBW Simulations

Figure 11 shows the AC response of the design where the open loop gain, bandwidth and phase margin can be drawn to both light and heavy load conditions, $I_{out} = 100$ nA and $I_{out} = 50$ mA respectively.

One can observe that, for the worst case scenario, the open loop gain, bandwidth and phase margin are always greater than 60 dB, 370 kHz and 66° respectively.

B. PSR Simulations

The behavior of the proposed capless LDO to ripples in the power supply node is presented in Figure 12.

C. Line and Load Regulation Simulations

The input output voltage relationship presented in Figure 13 defines the line and load regulation of the presented voltage regulator. In fact, Figure 13 only represents the line regulation for both light and heavy load conditions of the capless LDO, 100 µA and 50 mA respectively.

However, in Figure 13, one can observe that the line regulation to light and heavy load conditions are not superimposed and therefore load regulation exists.

Applying a linear regression to the signals present in Figure 13, two linear slopes are obtained. The slope of the 100 µA load condition reveals a 0.85 mV/V line regulation to the light load condition while the slope of the 50 mA load condition reveals a 0.69 mV/V line regulation to the heavy load condition. The load regulation, on the other hand,
D. Line, Load Transient and Output Voltage Ripple Simulations

Figure 14 presents the capless LDO load transient response of the proposed capless LDO. The simulation was performed to the minimum dropout voltage where the output current (rise/fall time = 500 ns) varied from 100 μA to 50 mA and back again to 100 μA. Additionally, a simulation was performed to obtain the load transient response of the LDO without the proposed fast dynamic loop (derivative loop).

As expected, the output voltage suffered from an undershoot to the 100 μA – 50 mA output current transition, and an overshoot to the 50 mA – 100 μA output current transition.

The settling time is approximately 625 ns for the output voltage undershoot case (measured when the output voltage is within ±10% of the regulation value) and approximately 1.16 μs for the output voltage overshoot case.

The line transient response of the LDO is presented in Figure 15. In this simulation the input voltage was quickly changed from the minimum dropout (V_{in} = 1.4 V) to V_{in} = 1.9 V and then changed back again to the minimum dropout voltage for a constant output current of 50 mA. As before, an extra simulation was performed to show the impact of the fast dynamic loop in the proposed LDO.

The output voltage of the LDO recovers to ±10% of its final value within approximately 0.7 μs for both overshoot and undershoot cases when the fast dynamic loop is employed. A 169 mV output voltage overshoot is achieved for the 1.4 V – 1.9 V input transition while a 98 mV output voltage undershoot is achieved for the 1.9 V – 1.4 V input transition.

E. Comparison with previously reported works

In order to introduce the proposed work in the research contextual frame, a FOM has been adopted [27] (given by equation 15) and equally applied to this and other previously reported works.

\[
FOM = \frac{C_{out} \Delta V_{out} I_Q}{I_{load_{\text{max}}}} \tag{15}
\]

\(C_{out}\) is the estimated on-chip load capacitance, \(\Delta V_{out}\) is the highest voltage spike detected for transient variations, \(I_Q\) is the quiescent current and finally, \(I_{load_{\text{max}}}\) is the maximum output...
current that the voltage regulator is able to supply. A lower FOM implies a better overall performance. For this work the FOM obtained was 29 $fs$.

Table II summarizes the individual characteristics and trade-offs of each work. It also presents an individual FOM for each reported work thus enabling better and fair comparison between works.

The FOM comparison given above strongly highlights the importance of the proposed improvements and trade-offs. From equation 15, one can observe that lower FOMs are achieved when the output capacitance, the maximum output voltage variation and quiescent current are small, the smaller the better, while supplying large output currents. However, as previously showed, these parameters are related to each other in non-linear ways so imposed compromises are always present due to the nature of topology and its internal components.

The proposed topology can also be easily adapted to meet other specifications, concerning the output voltage, due to its resistive voltage divider. This feature allows this topology to be reused in different SoCs, or several times in the same SoC with different voltage regulations if required, thus saving design time.

The proposed capless LDO is suitable for practical implementation, presents low quiescent current as well as an excellent FOM and excellent line and load transient responses.

V. LAYOUT

The layout of a design, in this case of an LDO, represents the final product, represents all the simulations, all the efforts made and the real costs of fabrication. Therefore, it has to be robust to all simulations and it should be, ideally, small in area and in layers required. Special care needs to be paid to some issues in order to maintain the design performance.

Good layout techniques imply better protection of transistors against unavoidable mismatching issues during the fabrication process, imply improved techniques against switching and gradient issues across the design area. Current density over the layout area is also a very important concern. The use of dummy components is also very important to protect the actual components. Metal paths need to be designed accordingly with their maximum tolerable current. By the use of several contact pins between two layers (i.e. Poly and Metal1) the routing resistance can be minimized and so the voltage drop [31]. This technique was extensively used in the pass device terminals. To enable interoperability and to avoid shorts circuits with other nearby blocks, odd metal layers have vertical displacement while even metal layers have horizontal displacement. To save resources this design uses only to the first two layers of metal.

A. Ultra low power LDO voltage regulator Layout

The inputs of the error amplifier have crucial importance in the LDO performance and so the offset voltage between each input transistor needs to be reduced. Some techniques exist to minimize the offset voltage between matched components, where the inter-digital and common-centroid techniques [31] are the most employed. In this layout inter-digital techniques were preferred. Furthermore, guard rings were also used around each matched input pair in order to prevent changes from switching and thermal gradient effects.

In fact, large components such as the pass device and the 1 MΩ resistors were also broken several times to improve component yield and allow the use of guard rings to decrease the negative effects of their operation. An extra guard ring was employed around each large component to achieve further protection. Guard rings were also used in every sensitive area, inside the control core.

The capacitors of the derivative amplifier were implemented by MOScap transistors thus saving analog core area.

To further improve the proposed layout, ESD circuitry could be applied to each I/O pad in order to save the pass device and the control core from electrostatic discharges. For SoC integration, only the pads that need to be tapped from the outside of the chip need this type of circuitry.

VI. CONCLUSION

The design of an ultra low power capless LDO voltage regulator was the main objective of this work. Its specifications were defined having the State of the Art in consideration. Several topologies were studied and its improvements analyzed in order to add some insight and positive contribution to the present work. The multiloop strategy and dynamic biasing
of the derivative amplifier proved to be the better choice. Miller compensation was also included as well as the push-pull strategy.

In the end, a new capless LDO topology was successfully implemented based on a new theoretical macromodel. The above compensations and strategies led to significant gains in the overall LDO response. This fact is corroborated by the simulated results showed earlier that, for low quiescent currents, are said to be excellent overall results. The design output voltage undershoots and overshoots, in line and load transients, are excellent and their settling time minimal.

The performance comparison of the proposed LDO with the other previously reported works, through the adopted FOM, clearly showed the relevance of the proposed solution and the benefits of the compromises made. It also showed that the proposed capless LDO voltage regulator is a viable solution for SoC integration.

The proposed capless LDO voltage regulator was developed in TSMC® 65 nm CMOS technology at INESC-ID®, Lisbon, Portugal.

A. Achievements

The proposed capless LDO, with the fast derivative amplifier, achieved a maximum voltage spike of 198 mV when the load current was changed from light to heavy load conditions (worst case scenario) in only 500 ns. Moreover, when $V_{in}$ changed from 1.4 V to 1.9 V, and back again to 1.4 V, the obtained output voltage variation was always inferior to 170 mV (worst case scenario). The power efficiency ($\eta_p$) obtained was around 85.7 % while the current efficiency ($\eta_I$) obtained was 99.9 %. Finally, while presenting excellent results for a 3.7 $\mu$A quiescent current, the proposed topology proved to be stable under all load conditions.

Table III summarizes the final results obtained with the proposed topology.

In addition, the author of this thesis co-authored a research paper along with M. S. Jorge Esteves, Ph. D. Jlio Paisana and Ph. D. Marcelino Santos. The paper was submitted to Microelectronics Journal with the name of "Ultra Low Power Capless LDO with Dynamic Biasing of Derivative Feedback" [6].

B. Future Work

As modern power management trends keep evolving, stronger and stronger forces are felt over the electronic design industry. As a result, improvements to the State of the Art topologies are always a question of time. The proposed concept represents a contribution to the State of the Art for capless LDO voltage regulators. However, concerning the proposed topology, much can still be done to complement this contribution and increase its performance. A few aspects of this work were not fully improved due to the different possible combinations of trade-offs and the limited time available. To mention a few:

- The derivative amplifier current driving capability could be improved allowing a faster source current and current sinking capability from the voltage regulator output node.
- In addition to the derivative amplifier, several clipping circuits exit and can be applied to the regulator, ensuring a much thinner output voltage variation range. As before, the compromise of quiescent current, output voltage and analog core area needs to be considered.
- The PSR response of the voltage regulator can be adjusted and further improved by increasing the impedance from

---

**Figure 16. Layout of the proposed capless LDO**

**Table III**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>-</td>
<td>-</td>
<td>0.19</td>
<td></td>
<td>m$m^2$</td>
</tr>
<tr>
<td>Core Area</td>
<td>$T_j$</td>
<td>-40</td>
<td>25</td>
<td>125</td>
<td>C</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>$V_i$</td>
<td>1.35</td>
<td>1.4</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>$V_o$</td>
<td>1.07</td>
<td>1.2</td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td>Load Current</td>
<td>$I_o$</td>
<td>0</td>
<td>50</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Int. Capacitor</td>
<td>$C_{out}$</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>pF</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>$\Delta V_o/\Delta V_i$</td>
<td>0.69</td>
<td>-</td>
<td>0.85</td>
<td>mV/V</td>
</tr>
<tr>
<td>Line Transient</td>
<td>$\Delta V_o/\Delta I_o$</td>
<td>-</td>
<td>-</td>
<td>169</td>
<td>mV</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$\Delta V_o/\Delta I_o$</td>
<td>-</td>
<td>-</td>
<td>3.02</td>
<td>mV/mA</td>
</tr>
<tr>
<td>Load Transient</td>
<td>$\Delta V_o/\Delta I_o$</td>
<td>-</td>
<td>-</td>
<td>198</td>
<td>mV</td>
</tr>
<tr>
<td>Ripple Rejection</td>
<td>PSR</td>
<td>-45</td>
<td>-25</td>
<td>-10</td>
<td>dB</td>
</tr>
<tr>
<td>Gain Bandwidth</td>
<td>$GBW$</td>
<td>364</td>
<td>370</td>
<td>967</td>
<td>kHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>$PM$</td>
<td>43</td>
<td>66</td>
<td>69</td>
<td></td>
</tr>
<tr>
<td>Startup Time</td>
<td>$T_s$</td>
<td>-</td>
<td>-</td>
<td>6</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Res. Variation</td>
<td>-</td>
<td>24.6</td>
<td>-</td>
<td>25.5</td>
<td>%</td>
</tr>
<tr>
<td>Cap. Variation</td>
<td>-</td>
<td>19.8</td>
<td>-</td>
<td>22.7</td>
<td>%</td>
</tr>
</tbody>
</table>

**CURRENT CONSUMPTION**

<table>
<thead>
<tr>
<th></th>
<th>$I_{QON}$</th>
<th>$I_{QOFF}$</th>
<th>$I_{ON}$</th>
<th>$I_{OFF}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>All blocks ON</td>
<td>-</td>
<td>-</td>
<td>3.7</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>All blocks OFF</td>
<td>-</td>
<td>-</td>
<td>27</td>
<td>pA</td>
</tr>
</tbody>
</table>
$V_{in}$ to $V_{out}$ and decreasing the impedance from $V_{out}$ to ground [32].

- In order to save the battery life, the reference of the capless LDO can be supplied by itself. It can only happen after the start up time and respective transient oscillations. This option will add complexity to the circuit as it will have an extra loop with a control circuit, more analog area, more quiescent current, but will allow the power down of the Band Gap reference circuitry, so careful attention should be paid on this subject.

- As the lithographic processes are improved, the length of the transistors decrease allowing better results and performances. Porting the current design to better technologies will also lead to better results.

REFERENCES


