A 7.875 GHz IR-UWB Receiver Using a Narrowband Approach

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Abstract—This work describes the implementation of an IR-UWB receiver in a standard 0.13 µm CMOS technology, with an operation frequency around 7.875 GHz. The circuit topology presented in the paper does not require any external circuit and has four main blocks: a narrowband low noise amplifier tuned at 7.875 GHz, which is the central frequency of the universal 7.25-8.5 GHz sub-band; a self-mixer working as a squarer circuit; a baseband amplifier; a comparator to produce a digital output signal. The circuit is designed at layout level with pads and ESD protection devices, and simulation results, considering parasitic extraction are presented. The circuit is capable of bearing a 100 Mbps data rate transmission, has a power consumption of 105 mW drained from a 1.2 V voltage source, an active area of 0.4784 mm² and a high robustness against interference.

Keywords—IR-UWB, CMOS Receiver, Narrowband, Low Area, High Data Rate, Robustness Against Interference

I. INTRODUCTION

In the past decade, short-range wireless networks became a major priority, creating a demand for the increase of transmission data rythm. At circuit level, mass market devices require the development of compact circuits with minimum area and cost and low voltage supply, as well as an increase of robustness against interference. Towards short-range applications, Ultra-Wideband (UWB) radio technology can be a solution for many of the identified problems, as UWB is based on the optimally sharing of the existing radio spectrum resources [1].

Modern UWB regulations require signals with a minimum bandwidth of 500 MHz, (for operation frequencies above 3.1 GHz and below 10.6 GHz) [2], by comparison with traditional narrowband communication systems, with bandwidths of a few kHz. The UWB regulations do not specify any type of modulation scheme, so it is possible to use many different techniques to create an UWB signal [2]. Three of the most common implementation techniques are Frequency Modulation UWB (FM-UWB), Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM), and Impulse Radio UWB (IR-UWB).

The IR-UWB technique consists in creating a pulse wave or by generating a baseband envelope impulse to modulate a sinusoidal wave, shifting the signal spectrum to radio frequencies. The short-duration pulses (usually nanoseconds or picoseconds) will lead to wide energy spreading, acting like information carriers.

This paper explores the development of an IR-UWB receiver using a 0.13 µm CMOS technology, based on a narrowband topology, since the only goal is to detect the presence of an IR-UWB pulse.

This paper is organized as follows: in Section II the receiver architecture, with emphasis on the response time of the narrowband low noise amplifier (NBLNA) is presented; in Section III the circuit implementation is described; in Section IV simulation results with parasitic extraction, along with the circuit layout are presented; finally in Section V the conclusions are drawn.

II. RECEIVER ARCHITECTURE

IR-UWB transmissions use a train of short-duration and high-frequency pulses. Therefore, it is necessary to translate the central frequency of the received pulses to baseband, and afterwards it is useful to generate a digital output signal for further data processing. The receiver architecture and its working principle are illustrated in Fig.1.

![Fig. 1 – IR-UWB receiver block diagram, and time-domain view of the input signal x(t) and the respective output signal y(t).](image-url)
A. Transmission Specifications

The clear definition of the transmission specifications is a key aspect in any communications system. Considering a sinusoidal pulse is sent, its duration must be minimized in order to reduce the power consumption of the transmission, therefore its bandwidth must be maximized as shown in (1)

\[ P_D = \frac{2}{p_w} \quad (1) \]

where \( B_w \) is the pulse bandwidth and \( P_D \) is the pulse duration. In order to take advantage of all the available universal subband, the receiver is made to be compatible with 1.25 GHz bandwidth pulses. The transmission specifications are presented in Table I.

<table>
<thead>
<tr>
<th>Technique</th>
<th>IR-UWB</th>
<th>Pulse frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse shape</td>
<td>Sinusoidal</td>
<td>7.875 GHz</td>
</tr>
<tr>
<td>Envelope shape</td>
<td>Rectangular</td>
<td>1.25 GHz</td>
</tr>
</tbody>
</table>

B. Receiver Specifications

The receiver presented in this paper must be able to generate a rectangular output signal with the minimum duration of 1 ns and the minimum amplitude of 600 mV whenever an IR-UWB pulse with the minimum amplitude of 2.4 mV and the characteristics shown in Table 1 is present to the receiver. Otherwise, a 0 V DC voltage must be the output of this circuit. Also, the sum of the rise time, the fall time and the duration of the output rectangular pulse must be less than the duration of the received IR-UWB pulses, in order to respect the established data rate. The circuit is meant to be fully single-ended with the input matched to 50 Ω.

C. Narrowband Low Noise Amplifier

The first thing to be taken in account while designing the NBLNA is its response time, due to the small duration of the received pulses. Considering that the NBLNA can be seen as a linear time-invariant system (SLIT), it is possible to define its transfer function (2)

\[ H(s) = K \frac{\prod_{i=1}^{p} (s-z_i)}{\prod_{i=1}^{p} (s-p_i)} \quad (2) \]

where \( K \) is a gain, \( p_1, p_2, ..., p_p \) are poles and \( z_1, z_2, ..., z_c \) are zeros. The Laplace transform (LT) of the NBLNA response to a continuous sinusoidal signal is given by (3) [3]

\[ Y(s) = X(s)H(s) = \frac{a_0 \prod_{i=1}^{p} (s-z_i)}{(s^2+a_0^2)\prod_{i=1}^{p} (s-p_i)} \quad (3) \]

where \( a_{0} \) is the angular frequency of the sinusoidal signal. The LP of the response can be written as in (4)

\[ Y(s) = \frac{A}{s^2+j a_{0}} + \frac{A*}{s-j a_{0}} + \sum_{i=1}^{p} \frac{C_i}{s-p_i} \quad (4) \]

assuming that all the poles are different from each other and are not equal to \( \pm j a_{0} \), and also assuming that \( P + 2 > Z \), which is guaranteed by the stability of the system. In (4), the constants which are yet to be defined, can be calculated through (5) and (6) assuming that \( H(-j a_{0}) = H'(j a_{0}) \).

\[ C_i = \frac{(s-p_i) a_{0} K \prod_{j=1}^{p} (s-z_j)}{(s^2+a_0^2)\prod_{j=1}^{p} (s-p_j)} \quad (5) \]

\[ A = \frac{(s-j a_{0}) a_{0} K \prod_{j=1}^{p} (s-z_j)}{(s^2+a_0^2)\prod_{j=1}^{p} (s-p_j)} \quad (6) \]

The NBLNA time-domain response to a continuous sinusoidal can be defined now as in (7).

\[ y(t) = Ae^{-j a_{0} t}u(t) + A*e^{j a_{0} t}u(t) + \sum_{i=1}^{p} C_i e^{p_i t}u(t) \quad (7) \]

Replacing \( A \) and \( A^* \) for its values, the time-domain response can be written as in (8).

\[ y(t) = [H(j a_{0})] \sin(a_{0} t + arg(H(j a_{0}))) + \sum_{i=1}^{p} C_i e^{p_i t}u(t) \quad (8) \]

Considering the stability of the system, (9) and (10) are to be considered.

\[ \text{Re}(p_i) < 0 \quad (9) \]

\[ \lim_{t \to +\infty} e^{p_i t} = 0 \quad (10) \]

Thus, for \( t>0 \), the NBLNA time-domain steady-state response to a continuous sinusoidal can be defined as in (11).

\[ y(t) \equiv |H(j a_{0})| \sin(a_{0} t + arg(H(j a_{0}))) \quad (11) \]

The instant where (11) becomes a good approximation of the NBLNA response to the considered signal is determined by the slowest pole. Defining the slowest pole as \( \lambda = \max \{\text{Re}(p_i), 1 \leq i \leq P\} \), the time constant associated to \( \lambda \) is \( T_s = 1/\lambda \). For \( t > 5T_s \), it is obtained for any \( i, |e^{p_i t}| < e^{t \lambda} < e^{-5} < 0.007 \). Thus, the settling time of the NBLNA response to a sinusoidal pulse can be written as in (12).

\[ S_T = \frac{5}{\lambda} \quad (12) \]

Through (1) and (12), a relationship between the slowest pole of the NBLNA and the received pulse duration can be obtained, in order to define the maximum pulse bandwidth to which the NBLNA guarantees a well-defined response. This relationship is shown in (13).

\[ B_w \leq 0.4 \times L \quad (13) \]

Considering \( L \) to be approximately equal to 7.875 GHz, by (12) the NBLNA has a settling time of 0.6 ns, which is considerably less than the duration of a 1.25 GHz bandwidth pulse, which by (1) is equal to 1.6 ns.
In order to provide a differential output, the NBLNA is composed by two common-source stages in cascade. The first stage inverts the phase of the input signal and the second stage restores it, thereby creating a differential output. The block diagram of the NBLNA is presented in Fig. 2.

![NBLNA block diagram](image)

**D. Self-Mixer**

The mixer topology chosen in this work is a typical Gilbert Cell. Its conversion gain, when working as a squarer circuit, is given by (14) [4].

\[
G_C = \frac{V_{out}}{V_{in}} \quad (14)
\]

The main purpose of this stage is to translate the power in the higher frequencies to baseband, through the multiplication of the amplified input signal by itself. Thus, the expected output signal of this stage is a 15.75 GHz pulse with a DC offset. This way, no synchronism circuit, such as a local oscillator or a phase-locked loop, is needed.

**E. Baseband Amplifier**

The proposed baseband amplifier (BBA) topology is composed by six differential pairs in cascade, keeping in mind that each differential pair has a low-pass characteristic with the same pole location. The differential-mode gain expression of the BBA is presented in (15) and its block diagram is shown in Fig. 3.

\[
G_{BBA}(f) = \prod_{i=1}^{6} G_i(f) \quad (15)
\]

![BBA block diagram](image)

**F. Comparator**

In order to generate a rectangular-shaped output signal, the comparator is composed by two stages. The first stage works as a switch and the second stage is a CMOS inverter.

**III. RECEIVER IMPLEMENTATION**

Due to the high operation frequency, the inductive effect of bonding wires and the capacitive effect of the pads are considered in the implementation process. All the elements used to implement the receiver are RF elements from the UMC 0.13 μm.

**A. NBLNA Implementation**

The NBLNA is implemented with two NMOS stages, both in common-source configuration, with inductive degeneration of the first one, to avoid instability due to negative input resistance. The NBLNA core schematic is presented in Fig. 4.

![NBLNA core circuit schematic](image)

The inductor \(L_1\) and the parasitic capacitance between \(V_{out}^-\) and \(GND\) tune the first NMOS stage through the resonance effect of a small-signal LC-parallel equivalent circuit, as well as the inductor \(L_2\) and the capacitor \(C_2\) tune the second NMOS stage the same way. The inductor \(L_0\) is set to compensate the capacitive effect of the input pad.

**B. BBA Implementation**

The main concern while sizing the BBA is to guarantee that the common-mode output voltage of each differential pair is approximately equal to its common-mode input voltage, thus keeping the BBA stable instead of saturated. For the same reason, each differential pair must be matched and working in the linear region. The BBA core schematic is shown in Fig. 5.

![BBA core circuit schematic](image)

All PMOS loads are designed to be operating in the triode region. Thus, the overall gain of the BBA is adequate and the receiver gains robustness against interferences.

**C. Comparator Implementation**

The transistor M41 and the resistors \(R1\) and \(R2\) generate a digital signal in the output of this stage. Thus, a second stage is necessary to generate a digital “1” when a pulse is detected and a digital “0” otherwise. The second stage is composed by the transistors M42 and M43. The comparator circuit schematic is presented in Fig. 6.

![Comparator circuit schematic](image)
IV. SIMULATION AND RESULTS

The receiver core schematic is presented in Fig. 7.

![Comparator circuit schematic](image1)

**Fig. 6** – Comparator circuit schematic.

![Receiver core circuit schematic](image2)

**Fig. 7** – Receiver core circuit schematic.

In Table II the final elements parameters used in the receiver are shown. The transistor models used to implement the NMOS and the PMOS type are the N_12_RF and P_12_RF. The models used to implement the inductors, the capacitors and the resistors are the L_CR20K_RFVIL, the MIMCAPS_RF and the RNNPO_RF respectively.

<table>
<thead>
<tr>
<th>Gate Finger Width [m]</th>
<th>Length[m]</th>
<th>Number of Gate Fingers</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M8, M11-M20</td>
<td>7.2µ</td>
<td>120n</td>
</tr>
<tr>
<td>M5-M10</td>
<td>4µ</td>
<td>120n</td>
</tr>
<tr>
<td>M27</td>
<td>7.2µ</td>
<td>120n</td>
</tr>
<tr>
<td>M28</td>
<td>7.2µ</td>
<td>120n</td>
</tr>
<tr>
<td>M41</td>
<td>7.2µ</td>
<td>120n</td>
</tr>
<tr>
<td>M42</td>
<td>9.6µ</td>
<td>120n</td>
</tr>
<tr>
<td>M43</td>
<td>6µ</td>
<td>120n</td>
</tr>
</tbody>
</table>

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In Fig. 8 it is possible to observe that the receiver is capable of bearing a 100 Mbps data rate. The output signal V_out has amplitude above 600 mV during approximately 1 ns if the input signal V_in is a sinusoidal impulse with a frequency of 7.875 GHz and amplitude of 2.4 mV. The presented simulation results include biasing circuits, models for pads, bonding wires, ESD and 50 Ω loads both in the input and output of the circuit.

![Post-layout simulation results considering parasitic extraction](image3)

**Fig. 8** – Post-layout simulation results considering parasitic extraction.

The layout presented in Fig. 9 is the complete IR-UWB receiver having an area with pads of 910 µm × 520 µm.

![IR-UWB receiver layout with pads and ESD protection devices](image4)

**Fig. 9** – IR-UWB receiver layout with pads and ESD protection devices.

V. CONCLUSIONS

This paper describes the implementation of an IR-UWB receiver operating in 7.875 GHz, in 0.13 µm CMOS technology. The circuit topology was selected to target high data rate, high robustness against interference and low area through the exemption of the need for a local oscillator, a phase locked-loop or any other synchronism circuit.

To implement the receiver a narrowband low noise amplifier, a self-mixer, a baseband amplifier and a comparator are used; therefore a narrowband concept is applied in an UWB communications system element.

REFERENCES


