SPACE-DC/DC II

DC-DC Converter for Aerospace Industry

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Abstract—This document addresses the design of a low power (3 to 10 W) DC/DC converter to be employed in the aerospace industry.

The work developed in this dissertation is a follow up of previous dissertations (1) [1] [2] [3] that designed radiation hardened DC/DC converters controlled with PWM current mode control or PFM methods. Some stability issues and the galvanic isolation feature were left as suggestions for future improvements, being a requirement imposed by ESA.

Firstly, the behavior of electronics in space is analyzed and the constraints that this environment poses to microelectronics are described. Knowing this, the appropriate architecture for the DC/DC converter that suits the application is chosen between many benchmark topologies. Subsequently various solutions to implement the galvanic insulation are studied, giving special emphasis to high performance and efficiency, as well as low feedback signal distortion.

In order to solve the stability issues of previous works, the PWM switch model will be applied to a multi-output forward converter. The PWM and PFM control schemes will be simulated in LTSpice environment in order to observe their response to transient loads and validate their stability and determine efficiency. Finally the controller circuit scheme will be implemented in an integrated circuit using CADENCE software.

I. INTRODUCTION

A. Overview

DC/DC converters are high efficiency power supplies that convert a continuous voltage level into a different level, using semiconductor devices switching at high frequency and passive filtering. Their usage in the Aerospace Industry is crucial since the power generators, mainly photovoltaic cells and radioisotope thermoelectric generators, produce high voltages levels which electronics cannot operate with. The design of any electronic circuit to operate in space is a remarkable engineering challenge, due to the harsh environment conditions. Radiation, vacuum and high temperature gradients are just some of the main design constrains imposed by space in electronics.

Due to the supply of DC/DC converter controllers in the European territory being low or non-existent, the European Space Agency (ESA) has been compelled to resort to the North American market. However, this grade of electronic circuits has military applications, making them difficult to be purchased, since the importation of this material must pass a long chain of bureaucracy imposed by the U.S. Ministry of Defense. This causes the costs to increase, and also the European space programs dependent on those materials to be delayed. In order to solve this problem, ESA is now looking for a “made in Europe” fully integrated DC/DC converter controller circuit, tolerant to radiation, with complete galvanic insulation between the input and outputs and more cost-effective than the former imported ones.

B. Objectives

The main objectives of this work are:

- Study and implement a DC/DC converter control circuit that ensures the input to output galvanic insulation;
- Re-study the DC/DC converter closed loop stability, as to ensure the proper dynamic behavior during load steps;
- Study the need and feasibility of the PFM control mode and improve the transient response when toggling from PWM to PFM mode, and vice-versa;
- Design the integrated circuit implementing the studied features;
- Simulate the circuit, presenting the results and validating its functionality.

C. Electronics in space environment

In order to design an integrated circuit that can operate in space, it is first important to comprehend what are the design constrains that this harsh environment imposes. The following presented issues were chosen to be the most important ones in the framework of this paper, since their mitigation is a direct responsibility of an electronic circuit designer.

1) Temperature and vacuum

Abrupt temperature variations and the high operating temperature ranges (between approximately -170 and 900°C at low-earth orbit [4]) are the main design constrains related to temperature. These two phenomena can cause a variation of the semiconductor parameters, such as the response time, threshold voltages and conductance, as well as mechanical stress due to contraction and expansion of the materials. To mitigate these effects, the circuit designer can only ensure that the circuit will operate for a certain range of temperatures (-50 to 125°C), by simulating the circuit and afterwards...
testing the actual chip, under these conditions. The electronic circuitry must be placed inside the spacecraft in order to guarantee this temperature range.

The absence of atmosphere and no capability to sink heat through convection, also poses design predicaments to engineers. Because of this electrolytic capacitors are prohibited in space environment, since vacuum conditions cause them to explode. Ceramic or tantalum capacitors have to be used instead.

2) Radiation

Radiation is the most important design constrain because it will determine how the electronic design will proceed. The main sources of radiation in space are characterized as trapped radiation and transiting radiation. Trapped radiation is composed by regions in space where the planetary magnetic fields trap charged particles; these regions are denominated radiation belts. Transiting radiation is associated with subatomic particles originated form the sun and from outside of the solar system (cosmic rays). The sun emits occasionally high-energy plasma bursts, from both solar flares and coronal mass ejections, and continually emits low energy plasma, known as the solar wind. [5] [6]

Outer space radiation can cause two different types of effects in electronics, cumulative effects and single event effects. Cumulative effects persist even when the spacecraft is not exposed to radiation, and they become more noticeable the more radiation doses are absorbed by the circuit. Single event effects occur when a single charged particle collides with the circuit and transfers its energy into the electronic device, creating unintended waveforms and electrical perturbations.

a) Cumulative effects

Cumulative effects are tied to the Total Ionizing Dose (TID) that the circuit has withstood since its fabrication. This measure tells how much energy in the form of ionizing radiation was absorbed by the circuit. Electronic circuits design from space must comply with a minimum TID value before failing.

Charged particles gradually absorbed by an integrated circuit can get trapped in the gate oxide of a MOS device (Figure 1), creating drifts in their threshold voltage values and gate capacitances (Figure 2), depending on how big the dose is. In addition, the field oxide also can trap charged particles, giving birth to Radiation Induced Leakage Currents [7], that circulate in between two adjacent transistor devices. Leakage source to drain currents in a single transistor (Edge Currents, Figure 3) may also appear in the edge of the source and drain regions with the field oxide, since the imperfections of the fabrication process are worsened by the trapped charges due to radiation. Bipolar technologies are also highly affected by cumulative radiation effects, such as Displacement Damage. This effect is caused by trapped charges in the bipolar doped regions and causes the transistor gain to decrease dramatically. Optocouplers that are used conventionally to create the galvanic insulation between the power stage and the low power controller integrated circuit are one of the main affected components by this displacement damage. [8]

Figure 1. Trapped positive charges in the gate oxide.

Figure 2. Effects of the trapped charges in the C(V) curve [8]

Figure 3. Edge current between the source and drain [9]

Figure 4. Comparison between layouts of conventional integrated MOS device (a) and the Enclosed Layout Transistor (b)

The solution to the cumulative effects is mainly secured by designing the fundamental electronic devices to mitigate the leakage currents and to establish design rules to minimize the impact of threshold voltages shifts. Enclosed-layout
transistors (Figure 4) have to be used in analog circuits, in order to reduce the leakage currents [10]. These types of transistors eliminated the edge leakage currents because their architecture does not allow edges. Placing guard rings and extending the space in between adjacent transistors greatly reduces leakage currents. In digital circuits, no more than three transistors in series must be placed to design a digital gate, since the threshold voltage shifts can degrade the circuit expected behavior.

b) Single event effects

Single event effects can be divided in three types, depending on the energy levels of the causing particle and its effects. Single Event Transients (SET) occur when a low energy particle collides with a circuit node and creates an abnormal temporary perturbation that can propagates throughout the circuit. Static effects, such as Single Event Upsets (SEU), occur when a particle collides with memory circuit and causes the stored value to be altered. Single Event Functional Interrupts (SEFI) are worst case scenario of a SEU and only happens when the memory affected causes the circuit to interrupt its operation. Permanent effects occur when the circuit is permanently compromised or destroyed by a colliding massive high energy particle. These effects can either be Single Event Burnout (SEBO), if a power transistor is unintentionally put in conduction by a particle while in cutoff state; Single Event Gate Rupture (SEGR), when the particle causes the disruption of gate capacitance of a MOSFET; and a Single Event Latchup (SEL), when two adjacent complementary MOS transistors form a parasitic thyristor that is put in ON state by the particle.  

There cannot be a permanent solution to single event effects, but their effects can be mitigated if several design rules are considered. To mitigate the SET in analog circuits, it is advisable that at least 5 µA circulate in all circuit branches. While this may augment the power required, it decreases greatly the likely that a radiation induced current by a transiting particle will produce a transient signal large enough to affect the overall circuit. Static effects can be mitigated ensuring redundancy in memory circuits, such as the Triple Modular Redundancy method [11]. With this digital design method each individual memory block is triplicated and then a voter circuit decides the output from the majority. If a particle only affects one flip-flop, the output is unchanged because it selects the signal in majority. [12]

Permanent effects are mitigated by ensuring that complementary devices are spread out from each other and have guard rings. The converter power stage topology must also ensure that there is no way to short-circuit the input source by having two or more power semiconductors conducting at the same time caused by a particle collision. This implies that there can only be one power transistor between the input source and the return path. [13]

II. STATE-OF-THE-ART

This state-of-the-art will contemplate three different sections. First the power stage must be selected to comply with the previously stated design requirements; second a set of control methods will be analyzed and the most appropriate will be chosen; and finally several galvanic insulation techniques will be analyzed and compared in order to select the one that offers more advantages for this particular design.

A. Power stage circuit

It was previously mentioned that a DC/DC converter for aerospace cannot have more than one power transistor, due to single event effects that can short the input source. It also has to ensure galvanic insulation between input and output and multiple output capability. From all the different benchmark topologies, only a few comply with these restrictions; they are: flyback, forward, isolated SEPIC and the isolated Ćuk converters.

From the mentioned topologies, the forward converter presents more advantages than the others for this particular application. It has the lowest output ripples; the most simple and straightforward control, since the power transistor current waveform is identical to the output inductor waveform, which is a good particularity when using current-mode control regulation; the transformer is small comparing to the flyback converter, however it needs an extra winding to reset the iron core each switching period; and the nonexistence of capacitors like in the isolated SEPIC and Ćuk converters, removes some resonance issues that can arise. The multiple output feature is implemented by connecting several secondary windings to the transformer and the forward converter allows the cross-regulation capability by making the output inductors of each secondary circuit all share the same iron core.

B. Control circuit

In the last decade the integration of power supply controllers led to the emergence of new control methods. Subsequently several of these control methods will be presented and the most suitable for this application will be chosen.

1) Pulse Width Modulation control

PWM control techniques include a wide range of control schemes that generate the duty cycle at a constant frequency. The diverse architectures differ on how the duty cycle is elaborated and what state variables are used. The voltage-
mode control (VM) only uses the output voltage to generate the duty cycle. The output voltage is subtracted by a reference, and the resulting error voltage is compensated with the error amplifier and afterwards compared with a sawtooth signal that generates the exact duty cycle in order to minimize the error.

2) Pulse frequency modulation control

PFM control is a direct hysteretic output voltage control method. It compares the output voltage directly with a reference and determines whether or not the power transistor must be ON, according to the error between the output voltage and the reference. If the output voltage is greater than a tolerable level, the power transistor is put in OFF state; if the output voltage is lower than the tolerable level, the power transistor is put in ON state. This, however, generates very high voltage ripples when the output load is high and without the compensation that PWM methods have, the transient response to step loads is not as smooth. The main advantage over the PWM methods is that the switching frequency depends on the output load demand, therefore the switching losses become much less for lower output power levels.

C. Feedback insulation

The feedback insulation block is very important because it will feed the controller circuit with the output voltage that is on the secondary side of the power stage. Since the controller circuit is placed in the primary side, in order to retain the galvanic insulation, the output voltage information must be transferred from the secondary to the primary side without galvanic connections.

Due to radiation being present in space environment is not advisable to use optocouplers to isolate the power stage because of displacement damage, therefore other types of state-of-the-art galvanic isolation techniques must be researched instead. The following galvanic isolation schemes must ensure low power consumption, low signal distortion and immunity to radiation, as their main characteristics to comply with the current project. There were three different kind of galvanic isolation schemes that were researched: magnetic, acoustic and capacitive isolations.

The magnetic isolation, as the name suggests, uses the magnetic field to transfer information. In a forward converter the voltage across the output inductor can be written as a function of the output voltage:

$$v_{D2} + v_L + v_o = 0 \Rightarrow v_L = -v_o - v_{D2}$$  \hspace{1cm} (1)

This voltage only develops when the power transistor is in cutoff state, and not in DCM, consequently in order to use this voltage to sample the output voltage signal, a sample and hold circuit must be added and the sample clock must be synchronized with the power transistor conducting state (Figure 9) [14]. Since only transformers and integrated electronics are used in this technique, magnetic isolation is resilient against radiation effects.
The capacitive and acoustic isolation techniques are very similar in the way the data is transferred, with the only difference in the medium used. In the capacitive isolation the output voltage is modulated in PWM and then passed throw a pair of capacitors that detect the PWM signal transitions. In the receiver side, the signal is reconstructed using comparators and other electronics, as explained in [15] and [16]. In acoustic isolation the output voltage signal is modulated too and it is used to drive a piezoelectric material. These materials have the capability of producing voltages when subjected to mechanical stresses. This stress propagates to the receiver side and the signal can be reconstructed as it was in capacitive isolation. Whether or not this technique is immune to radiation is not yet known, but piezoelectric materials have been used in spacecraft before in other applications and have shown radiation immunity. [17] [18]

D. DC/DC converters available in aerospace industry

Now that the main different architectures and control techniques were presented, it is pertinent to elaborate a list of solutions offered by the aerospace industry market. A research of both American and European enterprises that sell the type of power supplies under study was made, in order to determine at what state of the art they are working. This market investigation was done to analyze the products specifications and functionalities, with special consideration to the control method used, how the feedback insulation is implemented and how efficient these power supplies are. In addition to the aerospace industry, solutions provided by conventional international electronic retailers were also investigated. Although not radiation hardened, some interesting feedback isolation and control techniques were found.

Among the investigated market solutions, PWM current-mode control was found to be the most used control technique in aerospace converters, yet some retailers offered also voltage-mode with current limitation [19], and also V^2 control [20]. Outside of the aerospace industry two PFM [21] [20] and one hybrid PFM/PWM [22] products were found presenting very high efficiency, but only for very low output power levels and with relatively high output voltage ripples (+2.5%).

Reported efficiencies can be as low as 60% to 93% with an average efficiency in the 80’s % level. Some converters or regulators report a power down current consumption of less than 100 µA, but without radiation hardening.

TID tolerance was measured between the 25 krad and 1 Mrad. Most of the radiation hardened solutions found respect the ESA specifications.

The isolated topologies analyzed were mostly forward converters, but also an appreciable number of flyback converters. Curiously a Half-bridge converter was found to operate in space [23], which goes against some design rules that were established before in this dissertation. Most of the multiple output converters found work in parallel topologies or in dual voltage mode. No converter was found that can individually generate the output voltage levels imposed by ESA specifications.

In regards to the feedback isolation, only two different types of architectures were found. Some solutions still use optocouplers, one of which using a temperature compensation circuit, but not a TID compensation [19] [24]. The other feedback isolation architecture found was magnetic feedback with an amplitude modulation scheme. [25] [23]

III. CONTROL AND STABILITY

This section will focus on the control and stability of the DC/DC converter under design. The chosen control method was PWM current-mode control, because it offers advantages over other methods, say better line regulation and audio susceptibility, and intrinsic current regulation. The use of PFM mode will also be studied, in order to determine whether is worth using it in conjunction with PWM mode to improve efficiency at low output power levels.

A. PWM-switch model

Obtaining the DC/DC converter model is crucial to size the correct compensation in order to achieve the proper dynamic behavior. The task of modeling a DC/DC converter is not trivial, because this electronic circuit is highly non-linear, since the power transistors and power diodes create non-linearities in the voltage and current waveforms. In the late 80’s Dr. Vatché Vorpérian developed the concept of the PWM-switch model as an attempt to create a linearized universal small signal model, that can be used in any DC/DC converter topology by replacing the non-linear transistor and diode, with the linear PWM Switch. This method is the same used with bipolar transistor circuits in small signal analysis.

![Figure 10. PWM Switch model concept and state variables. 'a' stands for the active port, 'p' the passive and 'c' the common.](image-url)
In reference [26], Prof. Basso derived both the large and small signal PWM Switch CM models. The large signal model is obtained by taking the important state variables and averaging them over a switching cycle (’d’ stands for the duty cycle value, as function of time d(t); \( R_{\text{sense}} \) is the current sensing resistance; \( T_{\text{sw}} \) the switching period; \( S_c \) the compensation slope and \( v_c \) the control voltage):

\[
\begin{align*}
    i_s &= d_i, \quad v_c = dv_{ap} \\
    i_c &= \frac{v_c}{R_{\text{sense}}} - \frac{S_c}{R_{\text{sense}}} dT_{\text{sw}} - v_{cp}(1 - d) \frac{T_{\text{sw}}}{2L}
\end{align*}
\]  

(2) 

(3)

The small signal model is obtained by perturbing the above equations and neglecting the cross alternating products. Prof. Basso described this derivation in his book [26], and the result obtained is:

\[
\begin{align*}
    i_s &= g_i\tilde{v}_{ap} + g_0\tilde{v}_{cp} + k_1\tilde{v}_c \\
    i_c &= g_i\tilde{v}_{ap} + g_o\tilde{v}_{cp} + k_0\tilde{v}_c
\end{align*}
\]  

(4) 

(5)

\[
\begin{align*}
    g_i &= \frac{d}{R_{\text{sense}}} \\
    g_o &= \frac{T_{\text{sw}}}{L} \left( 1 - d \right) \frac{S_c}{S_{\text{on}}} + \frac{1}{2} - d \\
    k_i &= \frac{d}{R_{\text{sense}}} \\
    k_o &= \frac{1}{R_{\text{sense}}}
\end{align*}
\]  

(6) 

(7)

This model can be denoted by the circuit presented in Figure 12, being the \( C \) capacitor responsible of modeling the subharmonic oscillations. These oscillations are a stability issue that arises in current-mode control and that is normally mitigated by summing a ramp to the sensed current signal. These oscillations only occur when the duty cycle is greater than 50% and require a slope equal to 50% of the current falling slope to be completely eliminated for all the range of duty cycles.

Now that the small signal model has been derived, it can now produce the s-domain Laplace transfer function, simply by placing it in the circuit schematic of Figure 11. The resulting transfer function is given by the following equation:

\[
P(s) = \frac{V_o(s)}{V_c(s)} \approx \frac{R_o}{n_1 R_{\text{sense}}} \times \frac{1}{1 + \frac{R_o K_{sh}}{P_{swL}}} \times \frac{1 + s r_c C}{s + \frac{1}{R_o C} + \frac{K_{sh}}{P_{swL}}} \times \frac{\omega_{sh}^2}{s^2 + s \pi \omega_{sh} + \omega_{sh}^2}
\]

\[
K_{sh} = \frac{S_c}{S_{\text{on}}} \frac{1}{(1 - D) - \frac{1}{2}}
\]

(8) 

(9)

1) Multiple output forward converter power stage transfer function

In a multiple output forward converter using cross-regulation, the derived transfer function still holds however the power stage parameters are not directly values of the main output, such has the capacitance, the capacitor ESR and output resistance. These parameters are obtained by impedance reflection taking into account the transformer ratios of Figure 6, that is, the cross-regulated passive components are reflected to the primary output. The capacitors are multiplied by the square of the transformer winding ratio, while the resistors (the output resistance and the capacitor ESR) are divided by the same factor.

Prof. Basso’s in his book calculates that the output inductors would appear all in series in the single output equivalent mode, and the equivalent inductance would be \( N \) (number of outputs) times the main output inductance. However Basso did his calculation without considering the output inductors all sharing the same iron core, which is fundamental for the cross-regulation scheme. With cross-regulation, only the main output inductor appears on the secondary side of the power transformer in the single output equivalent, because all the output inductors are treated as transformer where the magnetizing coil is the main output inductor.

2) Compensation of a multiple output forward converter

Now with the multiple output transfer function, compensating the converter is just a matter of applying control theory. The objective is to achieve an open loop transfer function with the highest possible low frequency gain, crossover frequency at 0 dB equal to 10% of the switching frequency and a phase margin at the crossover frequency approximately equal to 80°. [26]

The error amplifier capable of achieving the above specifications is a type-2 amplifier, with an integrator, and a pole zero pair. (Figure 13)
3) Averaged model (PWM Switch) vs. Switched model

Now that the multiple output forward converter is fully compensated, it is important to test the model credibility by comparing its dynamic behavior with two different models: a linear small signal model using the PWM-switch and a non-linear model using the transistors and diodes switching at high frequency. Both models will be put in the same conditions and a load step will be applied to the main output, in order to observe the output voltage response. The results are presented in Figure 14.

![Figure 14. Output voltage during a step load transient using the PWM-switch average model (blue) and the switched model (superimposed in green).](image)

It is clearly visible that both models have similar responses, however with the linear model the output voltage ripple cannot be observed because the waveforms are averaged over a switching cycle (1 µs). This confirms the validity of the derived model.

B. Pulse frequency modulation

PFM control was stated to be advantageous comparing to PWM for low output power conditions. The combined low voltage ripple with less number of power transistor switching, reducing the switching losses, may be advantageous to exploit. The efficiency of the PFM and PWM modes were measured in LTSpice, and in fact it is observed that for low loads the PFM can be up to 9% more efficient than PWM mode.

![Figure 15. Output inductor voltage waveform in a forward converter.](image)

IV. Feedback insulation

The selected feedback insulation technique was the magnetic insulation, because it fits the power stage converter topology. Connecting an extra winding around the output inductor will generate a voltage that depends on the output voltage, when the power MOSFET is in cutoff state, and the converter is not in DCM. A sample & hold circuit will track this voltage and sample the value when it is available; this is, shortly after the power switch was turned off. The sampled output voltage is then fed to the compensator (Figure 13), as if it were the actual output voltage. The main drawback of this method is that only one sample can be taken for each switching period. This can cause a delay in the response, but since the compensator crossover frequency is at 100 kHz (10% of Fsw) this delay is almost negligible.

![Figure 16. Output voltage during step load transients, with magnetic insulation (green) and without magnetic insulation (red).](image)

Now that the magnetic insulation scheme is presented, system simulations were carried out in LTSpice environment in order to validate the proper operation and behavior during transient step loads. The simulation results are presented in
Figure 16. They suggest that introducing the magnetic insulation causes the output voltage to deviate from its nominal value, depending on the output current level. This phenomenon is due to the sample and hold circuit sampling a voltage not exactly equal to the output voltage. The voltage drops across the diode and the inductor depend on the current value, therefore for different currents, the sensed voltage differs and this is translated into a static error.

The proposed controller block diagram is presented in Figure 12. It contemplates all the proposed pins: reference circuits, such as the band gap voltage reference and the reference current generators; the oscillator; undervoltage lockout block (UVLO); short-circuit protection and the PWM control circuit blocks.

The oscillator was chosen to have a frequency of 16 MHz, because the compensation ramp signal is implemented with a counter and a digital to analog converter. In order to have the highest precision in its slope, the counter would need also high bit value.

The soft-start block guarantees that the reference voltage that feeds the error amplifier ramps up slowly, preventing an output voltage overshoot in the startup.

The four input AND gate ensures that the power transistor is only driven when supposed to, that is, when the circuit is not in power down, when the input voltage is over the lockout value, while the PWM controller commands it and when the clock signal has logic value ‘high’. This last condition is a restriction imposed by the forward converter topology, since this converter was sized to work for duty cycles less than 50%, in order to prevent the transformer saturation.

The sensing winding responsible for the magnetic insulation is connected via the circuitry presented before (Figure 18) to the $V_{\text{osense}}$ pin. The S&H output is connected to the $V_{\text{osample}}$ pin, which connects to the compensation network of the error amplifier by the $v_f$ (feedback voltage) and $v_c$ (control voltage) pins. The compensation network was chosen to be implemented with discrete external components because the capacitance value is too large to be implemented in integrated technology. This capacitor could have been implemented with ELT transistors, but since it was previously mentioned that radiation causes large shifts in the $C(V)$ curve of MOSFET gate capacitances, this would arise stability issues. With discrete compensation components the controller becomes usable for more than one single application. In order to preserve this flexibility, the compensation ramp slope also depends on an external resistor ($R_{\text{ramp}}$).

Figure 17. PFM control with magnetic insulation. Green is the output voltage, red is the S&H voltage, blue is the power transistor drive voltage.

V. IMPLEMENTED CIRCUIT

The final implemented controller circuit incorporates the magnetic insulation feature but only with PWM control, since it was concluded in the previous section that PFM mode cannot be implemented with this feedback insulation scheme.

B. PFM control with magnetic insulation

Unfortunately PFM control cannot be used with magnetic insulation, because the output voltage is only sensed after the power transistor is put in cutoff mode. Unlike PWM mode, that the power transistor is always put in cutoff at least once in each switching period, in PFM mode there is nothing that can obligate the transistor to turn ON, and subsequently OFF, besides the hysteric comparator and possibly forced switching, which would put in jeopardy the advantage of less switching losses. What is expected to observe is the output voltage rising at first until it reaches the maximum level tolerable by the hysteric comparator. From this point on, the S&H output would remain constant, apart from parasitic charge losses, but the real output voltage would start to fall as there would be no additional samples taken (Figure 17).

Figure 18. Magnetic feedback insulation in a forward converter, using a sample & hold circuit feeding the error amplifier.
Now that the top circuit schematic was presented and explained, the final task is to put the implemented integrated circuit to test and validate the circuit functionality. The results are presented in Figure 20.

The top simulation results show that the implemented circuit complies with its expected functionality. The steady state operation is working as intended since the three tested outputs (5, 4.5 and 3.5 V) are all within the error margin of their nominal values. The output voltage and current ripples are also under the expected specified values. However, during step load transients the output voltage exhibits an oscillatory behavior. Two possible explanations were found to characterize this oscillatory behavior: the first is associated with the intrinsic duty cycle limitation to 50%; the second explanation rests with the slight delay between the sampling and the instant of time where the power transistor is turned on.

VII. CONCLUSION

A DC/DC converter with magnetic insulation designed for space environment was studied in this paper. Most of the objectives of this work were achieved since the galvanic insulation was successfully implemented, the PWM current-mode control model was put to test and its theory validated, the practicality of the PFM mode was carefully analyzed, and the integrated circuit was design...
and simulated, however no layout was produced due to time constrains.

It is important now to point out many of the critical design decisions that were taken. Firstly the feedback insulation was chosen to be implemented with magnetic insulation, because theoretically it would be the cheapest and less power demanding of the three studied techniques. However, it turned out that magnetic insulation, as it was implemented for this dissertation, may not be reliable enough due to parasitic second order effects, for example, the bonding wire parasitic inductances. The critical circuit block for this magnetic insulation is the sample and hold circuit, because if the output voltage is not sensed correctly, the whole control scheme is put in jeopardy. For future developments it is recommended that the feedback insulation scheme has to ensure more reliability. Capacitive insulation technique might be the solution for a reliable feedback insulation scheme, however the cost of the overall project would most likely increase, along with power consumption. The second choice that completely overhauled this project is associated with the exclusion of PFM control mode. The main objective of this dissertation was to design a DC/DC converter with feedback insulation, being the efficiency second priority when comparing to this specification. It was realized that with the way feedback insulation was implemented, PFM control is virtually worthless, since it would offer no additional benefit over PWM, while still giving arise to several stability issues.

There are still several issues that need to be addressed for future developments, in order for the converter to pass the ESA specifications. For example, the duty cycle limitation to 50% caused some transient stability issues. This can be mitigated by sizing the transformer winding relation in order to guarantee that the maximum steady state duty cycle is much lower than 50%.

The proposed implemented integrated circuit offers a new high efficiency solution for a fully galvanic isolated multiple output DC/DC converter for aerospace industry. The used technology (AMS 0.35) led to small power dissipation in the controller circuits when comparing to other radiation hardened solutions available in the market. In addition, this controller circuit is flexible regarding the configuration of the power stage. It can accommodate any number of outputs, with diverse voltage levels, where the only alteration that needs to be done is to recalculate the compensation component values, and size the transformer winding ratios for a proper cross-regulation feature. This multiple application flexibility can lead to the reduce cost since scaling economics can be applied when the chip is mass produced for multiple different applications.

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