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Universidade Técnica de Lisboa

Integrated Overcurrent Detection System for Bridge-tied Load Class-D Audio Amplifiers

Frederico Bernardes da Silva Tavares Cadete

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Júri

Presidente: Prof. Marcelino Bicho Santos
Orientador: Prof. Nuno Horta
Co-orientador: Prof. Jorge Guilherme
Vogal: Prof. Jorge Fernandes

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Resumo

Ao longo das duas últimas décadas as vendas de dispositivos electrónicos portáteis, como telemóveis ou leitores multimédia, tiveram um crescimento sem precedentes. Nestas aplicações, os amplificadores áudio Classe-D têm sido adoptados em detrimento de arquitecturas lineares, e dentro desta classe as topologias de carga diferenciais ou em “ponte-H“ oferecem vantagens notáveis sobre as de saída única ou “meia-ponte”.

Um dos componentes necessários para o amplificador classe-D é um sistema que detecte correntes excessivas no andar de saída, e que actue para prevenir danos permanentes no amplificador. Sistemas deste tipo estão bem descritos para topologias de meia-ponte. No entanto, as implementações conhecidas para ponte-H limitam-se a duplicar o sistema para meia-ponte. Nesta tese, é proposto um sistema de detecção de sobrecorrente para amplificadores em ponte-H que usa metade dos comparadores do que trabalhos prévios.

Para validar o sistema proposto, foi desenhada uma implementação em tecnologia CMOS 0,18 µm a 3.3 V, no contexto de um andar de saída ponte-H com potência de saída máxima de 1 W. Comparando com uma configuração convencional usando sub-blocos similares, este sistema consome até 38% menos corrente, comprometendo apenas algum tempo de detecção na modulação BD.

Abstract

The last two decades have seen an unprecedented rise in the sales of mobile devices, such as cell phones or media players. For these applications, Class-D audio amplifiers have been widely adopted over linear architectures, and within this class differential or bridge-tied load (BTL) topologies offer key advantages over single-ended (SE) topologies.

One necessary component of the Class-D amplifier is a system to detect excessive current through the output stage, and act to prevent damage to the amplifier. Such systems have been well described for SE topologies. However, known implementations for BTL only duplicate that approach. In this thesis, a new overcurrent detection system for BTL amplifiers is presented which uses half the comparators than previous works. This translates into chip area and current savings.

A proof-of-concept implementation of the proposed system was designed on a 3 V, 0.18 µm CMOS technology, within a BTL output stage rated for maximum output power of 1 W. Compared with using the same components in a conventional configuration, this system provides current savings of up to 38%, with a small increase in the detection time for BD-modulation.

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Abbreviations

AD-modulation – Binary modulation

BD-modulation – Ternary modulation

BTL – Bridge-tied load

CMOS – Complementary MOS

DMOS – Double-diffused MOS

DRC – Design Rules Check

GND – Ground reference

HI – high logical value; near-supply voltage

LO – low logical value; near-ground voltage

LVS – Layout Versus Schematic

MOS – Metal-oxide-silicon

MOSFET – MOS field-effect transistor

MUX - multiplexer

NMOS – N-type MOS transistor

PDM – Pulse-density modulation

PMOS – P-type MOS transistor

PMU - power-management units

PTAT – proportional to absolute temperature

PWM – Pulse-width modulation

SE – Single-ended

SoC – system-on-chip

VDD – positive power supply

1 Introduction

1.1 Motivation

Portable consumer electronic devices have become very popular in the last few decades. In the last year alone, more than 1 billion cell phones were sold worldwide. A device designer for the mobile context must reach strict requirements regarding battery life, heat dissipation and device size. This leads to demand for power efficient electronic building blocks requiring fewer external passive components.

In the area of speaker drivers, these demands are met with wide adoption of switched or class-D amplifiers, instead of linear architectures such as class-AB. Class-D amplifiers have unrivalled efficiency and reduced heat production, which allows for longer battery life and increased integration with other cell phone subsystems. There has been relevant academic and industrial interest in fully integrated class-D amplifiers this past decade. Within this class, differential output or bridge-tied load (BTL) topologies offer key advantages over single-ended (SE) topologies, such as increased output power (from the same voltage supply) and the possibility of ternary modulation.

As any other integrated power system, class-D amplifiers must withstand robustness tests where extreme external conditions are applied to the operating circuit. It must withstand accidental shorts between the outputs, for example. These conditions can lead to excessive current through the power devices, and cause permanent damage to the amplifier if there is not a proper protection system in place.

Such systems have been well described for SE topologies. However, known implementations for BTL only duplicate that approach, leading to redundancy in some components. An overcurrent detection system truly designed for BTL output stages can eliminate redundancies and lead to current and chip area savings. One such system is the main contribution of this thesis.

1.2 Research Goals

This work proposes a new configuration for overcurrent detection systems for BTL class-D output stages, and demonstrates its feasibility on a CMOS technology. Its main goals are to:

- Analyse overcurrent detection systems for class-D single-ended output stages, previously described in bibliography, with an emphasis on threshold current precision;
- Establish the redundancy of certain sub-blocks when such systems are directly applied to BTL output stages, and propose a configuration that avoids it;
- Demonstrate the feasibility of the proposed configuration by implementing it on a 0.18 µm, 3.3 V CMOS technology, for a target powerstage rated for 1W of output power;
- Evaluate the sources of imprecision in the implemented system, and compare its performance with a hypothetical conventional configuration using identical components.

1.3 Outline

Following this introductory chapter, the thesis is organized as follows:

- Chapter 2 provides an overview of class-D amplifiers and the different load configurations and modulations; establishes the need for a system that protects the amplifier from permanent damage when under extreme conditions; and evaluates possible solutions described in bibliography;
- Chapter 3 describes the principles of operation of the most promising solution; obtains equations for threshold current; establishes the compromises involved in choosing key design parameters; and presents a configuration suitable to BTL amplifiers;
- Chapter 4 presents a proof-of-concept implementation of the proposed configuration on a 0.18 µm, 3.3 V CMOS technology, describing the design of its sub-blocks and characterizing them;
- Chapter 5 analyses the results of the simulation of the implemented system, regarding precision, functioning, detection delay and power consumption; and evaluates the advantages of the proposed configuration;
- Chapter 6 draws conclusion from the performed work, and proposes future developments.

2 Protection Systems for Class-D Power Stages

This chapter details the context and key concepts of protection systems for class-D power stages. A small introduction to class-D stages' load topologies and possible modulations is provided. The need for protection of the switch transistors is established, and a few solutions are explored and compared.

2.1 Class-D Power Stage

Switching amplifier architectures such as Class-D are, today, the standard for high-power consumer audio applications. Their efficiency cannot in practice be rivalled by linear architectures. Although this advantage is not as pronounced in low-power areas such as mobile devices, it is still dominant and is driving the emergence of these architectures in speaker and even headphone drivers for portable devices.

The underlying basic principle of operation is driving the output(s) to either V_{DD} or GND, at any given instant. This way the output stage transistors either have very small voltage to their terminals or very small current through them, and thus dissipate little power. To achieve, at the load, a recognizable amplification of the original audio signal, the input signal should be modulated through pulse-width modulation (PWM) or pulse-density modulation (PDM). Finally, the signal must be "demodulated" to analog; the modulated signal has energy in high frequencies, due to both the modulation itself and the switching of the devices. This demodulation is achieved by a low-pass filter which is implemented with bulk components or, as in the case of many speaker drivers, is inherent to the load.

2.1.1 Load Topologies and Modulation Types

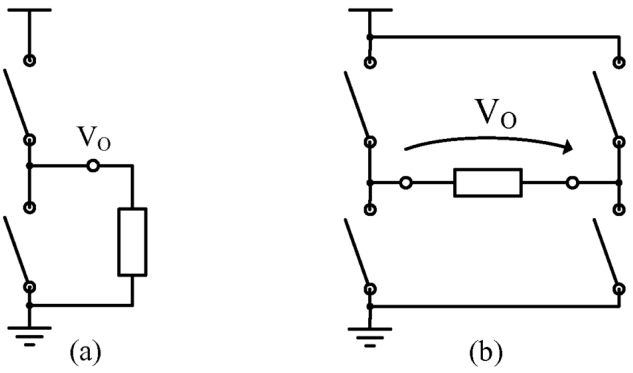


Figure 2-1: Class-D output stages (a) Single-ended and (b) Bridge-Tied Load. The load may include a low-pass filter with bulk components or be simply composed of a speaker with low-pass characteristics ("filter-less").

Class-D output stages can be classified between single-ended (SE) and differential (or bridge-tied load, BTL), based on their load topologies (see [1]). Although the latter have the disadvantage of doubling the number of power devices in the system and through the current path, they effectively quadruple the maximum output power (for the same supply voltage). Another important advantage is the possibility of using either binary (AD-) or ternary (BD-) modulation, whereas SE stages only allow binary.

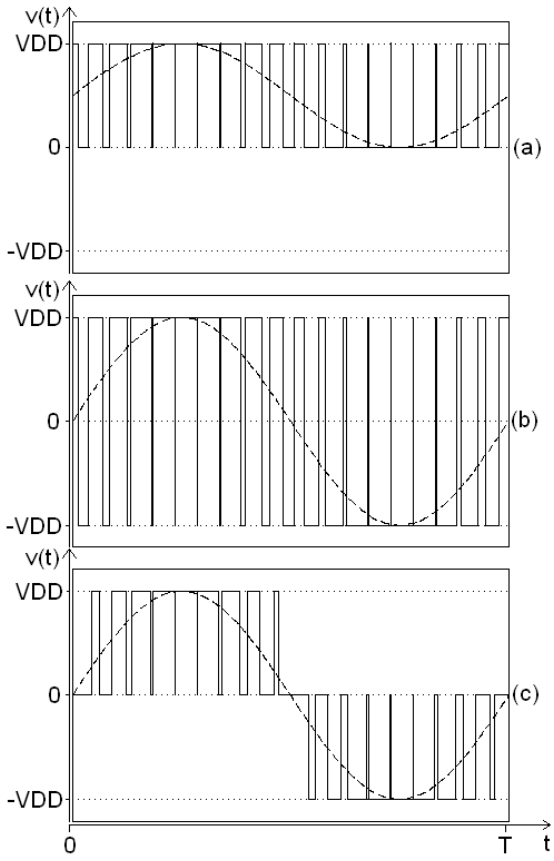


Figure 2-2: Modulation of a full-scale sine-wave in Class-D output stages: (a) SE, AD-modulation; (b), BTL, AD-modulation; (c), BTL, BD-modulation

BD-modulation, by having less power in high frequencies, is more suitable to applications without a discrete filter. The fact that during this modulation there are moments when both power PMOS or both power NMOS are conducting current will have to be taken into account when designing the overcurrent detection system.

Table 2:- Comparison of class-D load topologies

Single-ended	Bridge-tied Load
• Cheaper • Simple design • Can drive common-ground multiple channels	• Quadrupled output power • Ground-centered output (AD-modulation) • “Filterless” applications (BD-modulation)

2.1.2 Switch Safe Operating Area

The switches in Figure 2-1 can be implemented in a variety of technologies, from discrete IBGTs' to integrated MOSFET's. Recent integrated amplifiers overwhelmingly use either standard MOSFET's or double-diffused MOSFET's (DMOS). The latter are more appropriate to this application, because of their smaller drain-to-source resistance; yet most general-purpose processes, such as the one used in this work, don't include DMOS devices. In mobile applications, there is a trend to integrate audio drivers in DMOS system-on-chips (SoC's) along with power-management units (PMU's), or in CMOS with other analog interfaces [1].

For both technologies, the transistors must remain in a "safe operating area" (SOA). This "area" is limited by three main factors [2,3]:

- **Maximum drain current, I_{MAX}**; is usually determined by the electromigration limits of the metallization leading to the transistor itself;
- **Drain breakdown** voltage, BV_{DS}: the maximum drain-to-source voltage before breakdown of the drain-to-body junction occurs. For standard processes, this voltage is safely above the supply voltage[4] (although that is not always the case [5]);
- **Maximum power dissipation, $P_{max}(\tau)$**: the maximum junction temperature; this parameter's limiting action on I-V SOA will depend on the whole setup's (i.e. package, application) thermal dissipation characteristics and on the duration of the dissipation τ.

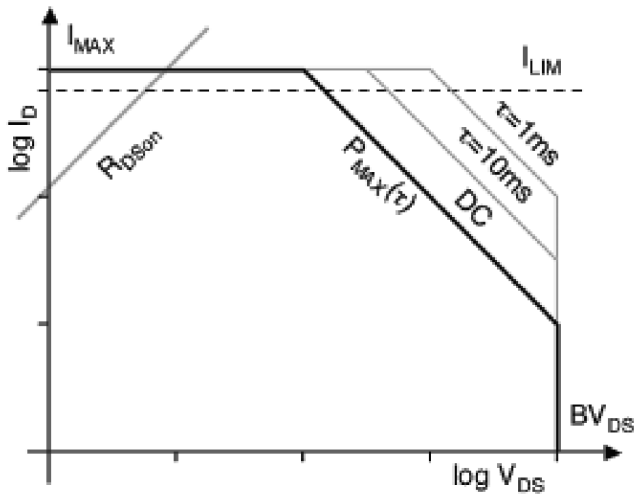


Figure 2-3: Safe Operating Area of MOSFET. From [3]

In a properly designed power stage, the load curve when the transistor is on (determined by its output resistance, R_{DSon}) crosses the upper limit of the SOA. The SOA itself can vary greatly with temperature and process corners but a conservative sizing of the power transistors can ensure that, for normal conditions, the operating point is inside the SOA. Unfortunately, those conditions cannot always be met. As stated by Krabbenborg:

> "Audio power ICs are usually equipped with a protection circuit to prevent damage caused by the following six fault conditions:
>
> short circuit from output to supply voltage,
> short circuit from output to ground,
> short circuit across the load (BTL or SE),
> wrong speaker impedance,
> wrong heat sink or
> high ambient temperature."

Benno Krabbenborg, [6]

To protect against such damage, it is sometimes necessary to implement subsystems to detect unsafe operation.

2.2 Detection Methods in Bibliography

A variety of methods to detect unsafe operation of switches have been proposed in literature. These can be mainly divided between protection against over-temperature and protection against overcurrent. In this section we will evaluate a few solutions, focusing on how they translate operating point limitations into a concrete measurable condition. The protection strategy itself, what to do once unsafe operation is detected, is outside the scope of this project.

A simplified schematic of each method applied to an NMOS transistor is included. The same principles apply to protecting PMOS.

2.2.1 Requirements

The solutions here presented will be evaluated based on two main criteria:

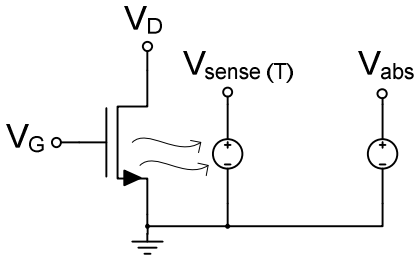
- **Detection delay**. This specification determines how much time a transistor remains in unsafe operation before that situation is detected. This criterion is important not because the devices can suffer damage in so short a period of time, but because it limits the modulation indexes at which the device is protected. For example, in a single-ended stage, a slow protection system will not detect a shortcut from output to ground if the pull-up switch is only open during very short periods at a time. Delay can limit the (protected) modulation index and switching frequency.

- **Protection precision.** A protection system that varies too much with process corners or operating conditions can end up not protecting the system effectively, on one hand, or limiting its operation, on the other. The power transistors should be sized for the least protective case, but the finished product's performance will be limited by the most protective. Precise protection allows efficient sizing.

Besides these two specifications, and as with any other circuit, more general specs such as power consumption, occupied IC area and design complexity will be taken into account.

2.2.2 Temperature detection

Krabbenborg [6] uses temperature sensing for detecting fault conditions. This solution involves embedding a temperature sensing device in a bipolar junction power device, and so is not applicable to the CMOS power stage. Detection time is limited by the time it takes to heat up the sensor in the case of short-circuit; that paper reports that it takes 100µs to reach 50% temperature error after a short-circuit is applied. Iwamuro *et al.* [7], using a similar technique on a IGBT device, reports "a time lag of a few µsec".



Over-temperature condition:

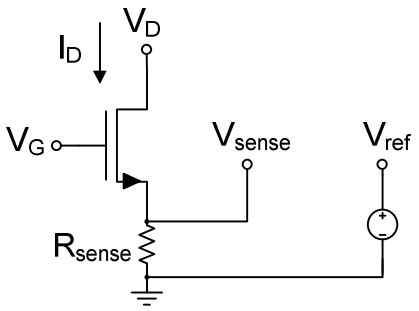
$$V_{sense(T)} > V_{abs}$$

Figure 2-4: Over-temperature detection for CMOS.

Over-temperature protection systems for standard MOS power stages, such as [8,9], use proportional-to-absolute-temperature (PTAT) voltages, and compare them with a temperature-independent reference voltage. Again, imperfect thermal coupling from the power device to the PTAT voltage source will delay the detection time.

2.2.3 Passive current sensing

Many switched amplifiers and DC-DC converters use a measure of the output current to control their operation. Sometimes this is done with a resistor placed in the path of the current to be sensed [10,11].



Overcurrent condition:

$$V_{sense(T)} > V_{\text{ref}}$$

$$I_D > V_{ref}/R_{sense}$$

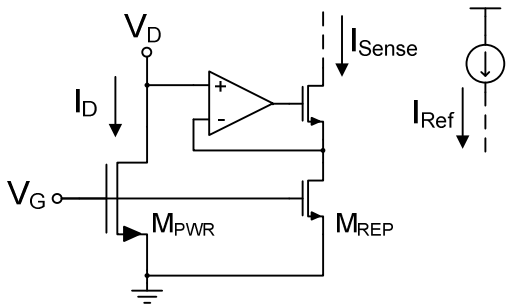
Figure 2-5: Overcurrent detection by series resistance

Berkhout [3] and C. Lee *et al.* [12] point out the disadvantages of this solution. For one, inserting a resistance in the current path can lead to considerable power dissipation (according to $P=I^2.R$). Even if a resistance intrinsic to the system is used, like that of the metallization of the transistor, the sensing would be very inaccurate because process spread and temperature variations would likely affect the resistor and the reference voltage in different ways.

The delay in overcurrent detection is dominated by the comparison delay of the circuit that would compare the two voltages.

2.2.4 Active current sensing

MOSFET transistors can take advantage of their matching properties to solve the current sensing problem. Many applications, including class-D amplifiers, use “active current sensing” for control [13-16]. A scaled replica of the power MOS (sometimes called “sense transistor”) is forced by active feedback to have the same node voltages. Its drain current will then be proportional to the power MOS’s current, and can be compared with a reference current to detect over-current.



Overcurrent condition:

$$I_{sense} > I_{Ref}$$

$$I_D > I_{ref}\frac{(W/L)_{PWR}}{(W/L)_{REP}}$$

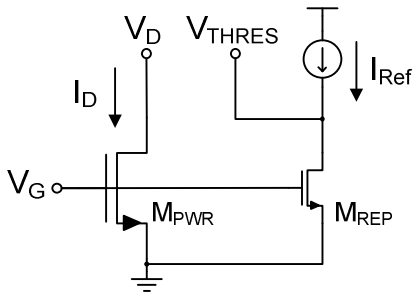
Figure 2-6: Overcurrent detection by active current sensing

The core of this setup, the replica transistor, is immune to process and temperature variations, since they have the same effects on the two matched transistors. Process mismatch, on the other hand, can considerably affect overcurrent precision, especially if the replica transistor is very small. Offset in the loop amplifier can add to the overall imprecision.

The delay of this configuration has two main contributions factors: first, the delay of the feedback loop that biases M_{REP}'s drain; second, the delay of the circuit that would compare the two currents.

2.2.5 Threshold-state replica

Solutions of this kind [3,13-18] employ a scaled replica, just like active current sensing. However, it is not forced to the same operating point as the power MOS. Instead, a current source places it in a constant state that mimics that of the power MOS *if it were at the current limit*. The replica's drain voltage is used as a threshold voltage; if the power MOS's drain is at a higher potential, overcurrent is occurring.



Over-current condition:

$$V_D > V_{THRES}$$

$$I_D > I_{ref} \frac{(W/L)_{PWR}}{(W/L)_{REP}}$$

Figure 2-7: Overcurrent detection by way of a replica in "threshold" state

As in the previous solution, good matching between M_{PWR} and its replica is necessary for precise current limiting. Delay in detection is dominated by the comparison delay.

2.2.6 Method comparison

Having explored several possibilities, the most promising one must be chosen. Table 1 contains a summarized comparison.

Table 1: Comparison of protection methods

Method	Precision	Delay	Notes
Temperature detection	Poor	Thermal coupling (~100µs)	Can be necessary anyway, e.g. in case of high ambient temperature.
Passive current sensing	Poor	Comparison delay	Sensing in metallization is simplest and could have the lowest system overhead.
Active current sensing	Good	Comparison and active loop delay	May be already implemented in current-controlled systems.
Threshold-state replica	Better	Comparison delay	Second simplest implementation.

Temperature detection can't compete in terms of precision or detection speed, but robust systems often include it anyway because it may be the only way of detecting a fault like high ambient temperature. In the case of a mobile device, for example, if it is operating in an environment that allows very few heat dissipation then the power dissipation limit in Figure 2-3 can decrease significantly. The device could risk junction damage without any of the other systems detecting the situation.

Passive current sensing seems to be only desirable in the case where minimum overhead is needed. Measuring the voltage drop across the transistor's metallization could be a crude but simple way of protecting it from electromigration damage.

The last two solutions are the most directly comparable. Both use the same principle of operation, and share its inherent imprecision. Active current sensing, however, is hampered by the delay in the feedback loop and by the imprecision introduced by an eventual input offset in the amplifier. Plus, the current-mode comparison seems, to the author, more complex than the more documented voltage comparison. The threshold-state replica is definitely the favoured solution**.** In the case where active current-sensing is already implemented for control purposes, however, that will likely be enough to adequately protect the transistors.

2.3 Synopsis

Class-D amplifiers are a good fit for mobile applications due to high efficiency and low heat dissipation. For operation from low battery voltages and without discrete filters, BTL topologies are preferable. Whatever the topology, robust Class-D audio amplifiers must include systems that detect extreme operating conditions; preferably over-temperature and overcurrent. The most promising overcurrent detection solution is that with threshold-state replicas of the power transistors.

It should be noted that no overcurrent detection system specifically for BTL topologies has been described; references such as [18] simply duplicate a system intended for SE. The redundancies in that "conventional solution" are an opportunity to be explored.

3 System analysis and design

In this chapter an analysis of the most referenced overcurrent detection solution is performed. A DC large-signal analysis is made on the basic overcurrent detection cell. The conventional configuration of four of these cells for BTL stages is described and some redundancies are observed. A new configuration that avoids these redundancies is proposed.

3.1 Overcurrent detection cell

This section describes and analyzes circuits that detect overcurrent in a single transistor. For convenience, this is done for a power NMOS transistor, but the analysis applies equally to the complementary circuit for PMOS.

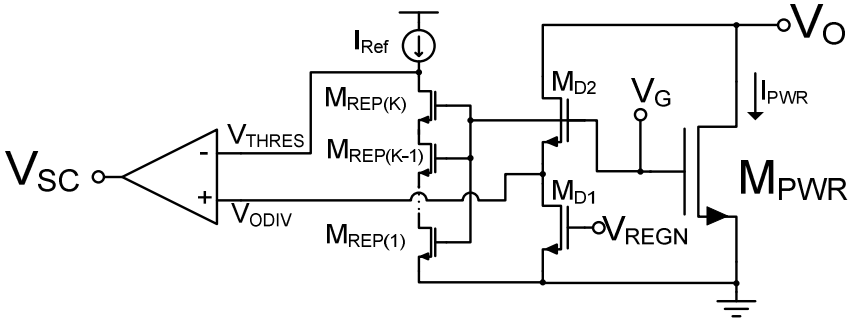


Figure 3-1: Overcurrent detection system as in [3]

This analysis will focus on the equations for the limiting current, I_{LIM}. This current is defined as the current through the power transistors that triggers detection, visible at the digital output that flags the short-circuit, V_{SC}. That is:

$$I_{LIM} \stackrel{\text{def}}{=} I_{PWR}|_{V_{SC}=V_{DD}/2} \qquad \text{Eq. 3-1}$$

$$I_{LIM} = I_{PWR}|_{V_{THRES}=V_{ODIV}} \qquad \text{Eq. 3-2}$$

(for comparator with no input offset)

Berkhout [3] proposes an overcurrent detection system as reproduced in Figure 3-1. Two changes are made from the basic “threshold-state replica” from Figure 2-7:

- The replica is now composed of various stacked transistors;
- The replica voltage V_{THRES} is compared with V_{ODIV}, a division of the output voltage performed by M_{D1} and M_{D2}.

The stacked replicas are a way of increasing the I_{LIM}/I_{Ref} factor without forcing a too small value to the replica’s width. For simplicity they all have the same channel width and length. $(W/L)_{REP(1)} = (W/L)_{REP(2)} = \cdots = (W/L)_{REP}$

The divider composed by M_{D1} and M_{D2} serves two purposes. One is pulling V_{ODIV} down to ground when M_{PWR} is turned off (V_G=LO), by way of M_{D1}. The other is increasing the I_{LIM}/I_{Ref} factor, again without incurring mismatch problems. For simplicity, let's define D as its divisive factor:

$$D \stackrel{\text{def}}{=} \frac{(W/L)_{D1} + (W/L)_{D2}}{(W/L)_{D2}} \quad \text{Eq. 3-3}$$

When M_{PWR} is conducting, V_G=V_{DD} and V_{DS} is very low for all transistors. A preliminary first analysis of the system can be made if we take the linear approximation for the triode equation. That is:

$$I_D = KP_n\left(\frac{W}{L}\right)V_{DS}(V_{GS} - V_{th} - \frac{V_{DS}}{2}) \quad \text{Eq. 3-4}$$

$$V_{GS} - V_{th} \gg \frac{V_D}{2} \Rightarrow I_D \approx KP_n\left(\frac{W}{L}\right)V_{DS}(V_{GS} - V_{th}) \quad \text{Eq. 3-5}$$

If we further consider that all source voltages are much smaller than the gate voltages, any transistor M_X can be treated as a resistor R_{MX} scaled by its (W/L) ratio. Putting in equation form:

$$V_G = V_{DD} \gg V_S \Rightarrow$$
$$V_{GS} \approx V_{DD} \quad \text{Eq. 3-6}$$

$$R_{M_X} = \frac{V_{DS}}{I_D} \approx \frac{1}{KP_n(V_{DD} - Vth)\left(\frac{W}{L}\right)_X} \quad \text{Eq. 3-7}$$

A quick analysis for the threshold situation (V_{THRES}=V_{ODIV},I_{LIM}=I_{PWR}) goes as:

$$V_O = I_{LIM}.R_{M_{PWR}} \quad \text{Eq. 3-8}$$

$$V_{ODIV} = V_O.\frac{R_{M_{D1}}}{R_{M_{D1}} + R_{M_{D2}}} \approx I_{LIM}.R_{M_{PWR}}/D \quad \text{Eq. 3-9}$$

$$V_{THRES} = I_{Ref}.K.R_{M_{REP}} \quad \text{Eq. 3-10}$$

$$V_{ODIV} = V_{THRES} \Rightarrow I_{LIM}.R_{M_{PWR}}/D = I_{Ref}.K.R_{M_{REP}} \Rightarrow$$
$$I_{LIM} = I_{Ref}.K.D.\frac{R_{M_{REP}}}{R_{M_{PWR}}} \quad \text{Eq. 3-11}$$

$$I_{LIM} = I_{Ref}.K.D.\frac{\left(\frac{W}{L}\right)_{PWR}}{\left(\frac{W}{L}\right)_{REP}} \quad \text{Eq. 3-12}$$

It can be seen that this system is equivalent to that of Figure 2-7 if K=1 (single replica instead of stack) and D=1 (no divider).

This formula is very useful for a first approach to designing an overcurrent system. But it is dependent on the linear approximation of Eq. 3-5. A more thorough analysis is made in the next few sub-sections.

3.1.1 Stacked replica

A. First-order analysis

The stacked replica transistors from Figure 3-1 are in the triode region and have the same drain current. A quick analysis is performed here to ascertain its equivalent I-V characteristic.

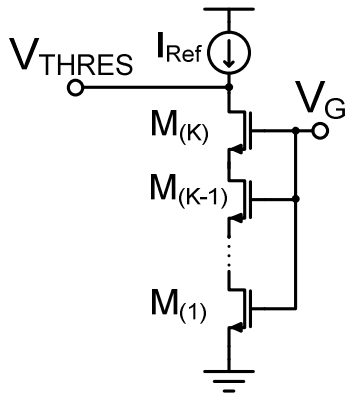


Figure 3-2: NMOS stacked replica

A generic equation can be written for every transistor $M_{(k)}$.

$$I_{Ref} = KP_{n(k)} \left(\frac{W}{L}\right) V_{DS(k)} \left(V_{GS(k)} - V_{th(k)} - \frac{V_{DS(k)}}{2}\right) \quad \text{Eq. 3-13}$$

$V_{th(k)}$ is specific to each transistor because of body effect. Solving the quadratic equation for $V_{DS(k)}$ results in:

$$V_{DS(k)} = V_{GS(k)} - V_{th(k)} \pm \sqrt{(V_{GS(k)} - V_{th(k)})^2 - \frac{2I_{Ref}}{KP_{n(k)}(W/L)}} \quad \text{Eq. 3-14}$$

from which we will take the lowest solution. Noting that one transistor's drain is the next transistor's source, an iterative expression to $V_{D(k)}$ with boundary conditions is:

$$\begin{cases} V_{D(k)} = V_G - V_{th(k)} - \sqrt{(V_G - V_{D(k-1)} - V_{th(k)})^2 - \frac{2I_{Ref}}{KP_{n(k)}(W/L)}} \\ V_{D(0)} = 0 \\ V_{D(K)} = V_{THRES} \end{cases} \quad \text{Eq. 3-15}$$

In the $V_{D(k)}$ expression, recursively substituting $V_{D(k-1)}$ by its expansion until hitting $V_{D(0)}$ results in an analytic expression, but only if we disregard second-order effects like body effect and mobility reduction due to transversal electrical field. That means considering $V_{th(k)} = V_{th}$ and $KP_{n(k)} = KP_n$. With that simplification,

$$\begin{cases} V_{D(k)} = V_G - V_{th} - \sqrt{(V_G - V_{th})^2 - k.\frac{2I_{Ref}}{KP_n(W/L)}} \\ V_{D(K)} = V_{THRES} \end{cases} \quad \text{Eq. 3-16}$$

Finally, an expression for I_{Ref} as a function of V_{THRES} is obtained by manipulation of Eq. 3-16:

$$I_{Ref} \cong KP_n \left(\frac{W}{L}\right) \frac{1}{K} V_{THRES} \left(V_G - V_{th} - \frac{V_{THRES}}{2}\right) \quad \text{Eq. 3-17}$$

From Eq. 3-17 we confirm that when not considering second-order effects, the K stacked transistors correspond to one single transistor with one K'th aspect ratio, and with an area K times larger.

A widely used model [19,20] for the mismatch between transistor states that the error is inversely proportional to the square root of the gate area. The greater gate area obtained with higher values for K is then expected to diminish error due to process mismatch. The second-order effects not considered will be visible as systematic error relative to Eq. 3-17, and as mismatch to M_{PWR} between different corners. Simulations were performed to ascertain these effects.

B. Mismatch Simulation

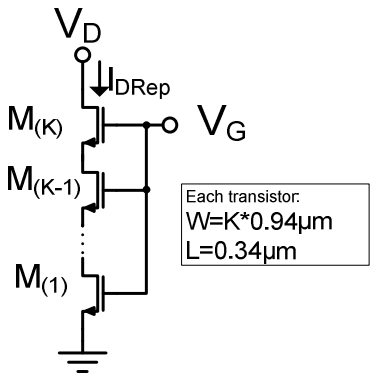


Figure 3-3: Testbench for Monte Carlo simulation for stack mismatch.
V_G=3.3V, V_D=0.1V

A Monte Carlo simulation was performed to evaluate the effect of K on the mismatch of the replica. Stacks of K transistors were simulated, where each transistor has W proportional to K. Thus, according to Eq. 3-16, they all have approximately the same I-V characteristic. 10000

cases were evaluated for each K value, from 1 to 8. The relative variance of I_D was taken as a measure of mismatch.

$$c_v(I_{DRep}) \stackrel{\text{def}}{=} \frac{\sigma(I_D)}{\mu(I_D)} \times 100 \ \ (\%) \qquad \text{Eq. 3-18}$$

Figure 3-4 presents the simulation results, along with a trend line calculated according to a power rule. It is clear that increasing K decreases mismatch. The calculated trend is in accordance with the model for mismatch being considered ($c_v(I_D) \propto \text{Area}^{-0.5}$), noting that total area is proportional to K squared ($\text{Area} \propto K^2$). Then:

$$c_v(I_{DRep}) \propto \frac{1}{K} \qquad \text{Eq. 3-19}$$

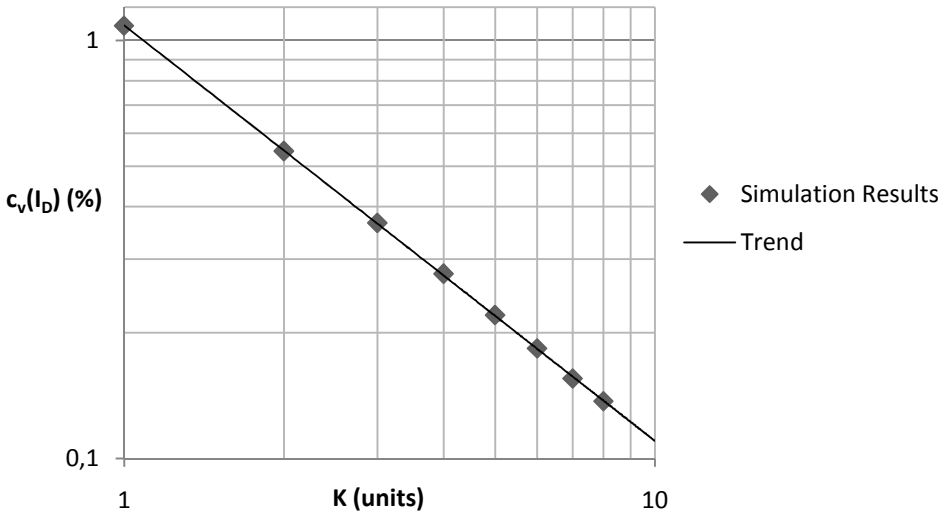


Figure 3-4: Monte Carlo simulation results for stack mismatch.
Number of samples: 10000 per K value. Trend: $c_v(I_D) \approx 1.0865.K^{-0.994}$ (%)

C. Alters simulation

Besides having to match the power MOS independently of small process mismatches, there is the need for robustness against larger variations of process parameters, temperature and supply voltage. This robustness is evaluated in “corners” or “alters” simulation.

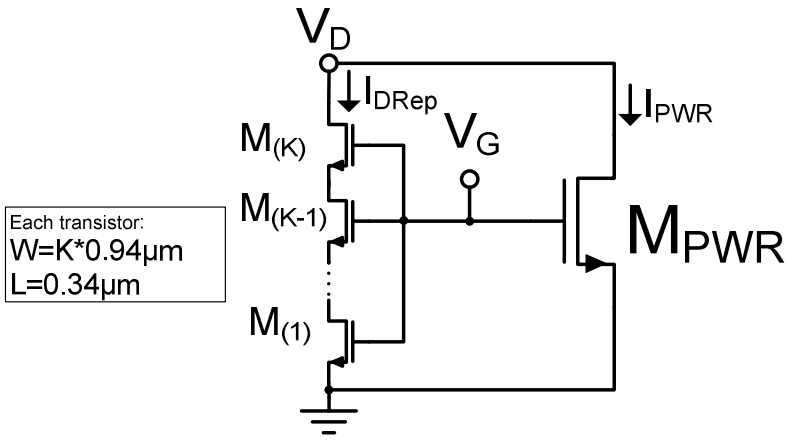


Figure 3-5: Testbench for corners simulation for stack error.

As a measure of mismatch, we measured the ratio I_{PWR}/I_{DRep}. For each corner, results are presented as the relative error (in percentage) against the value in typical conditions. The sixteen corners evaluated were the combinations of minimum and maximum values for temperature, supply voltage, and MOS speed.

$$\varepsilon_{corner}(x) \stackrel{\text{def}}{=} \left(1 - \frac{x_{corner}}{x_{typ}}\right) \times 100 \ (\%) \qquad \text{Eq. 3-20}$$

$$\varepsilon_{corner}\left(I_{DRep}/I_{PWR}\right) = \left(1 - \frac{\left(I_{DRep}/I_{PWR}\right)_{corner}}{\left(I_{DRep}/I_{PWR}\right)_{typ}}\right) \times 100 \ (\%) \qquad \text{Eq. 3-21}$$

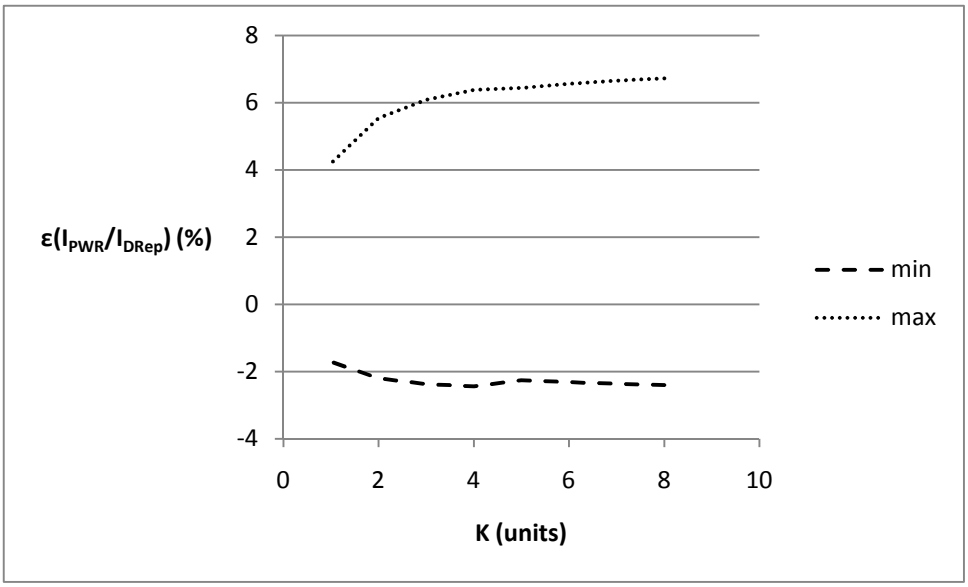


Figure 3-6: Corners simulation results for stack error.

It can be seen that the maximum error between different corners generally increases with K. This effect is more pronounced from K=1 to K=4, after which it seems to taper off.

3.1.2 Sensed Output Voltage

A direct comparison of the output voltage V_O with V_{THRES} allows overcurrent detection, but only when the output is set to low and M_N is conducting current. Whenever the output is set to high and M_N is at cut-off, a false overcurrent alert would be likely to result.

One solution to this problem is comparing V_{THRES} with a "sensed" output voltage V_{ODIV}, that is set to low when the corresponding power device is at cut-off. When the device is conducting, the sensed output voltage is set to a division of the output voltage.

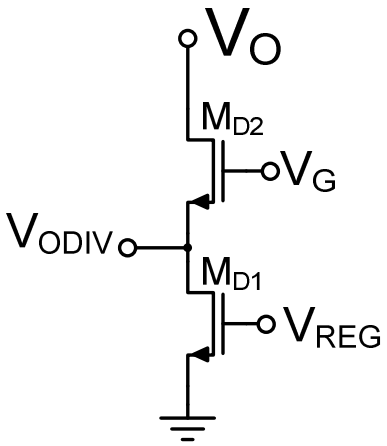


Figure 3-7: Voltage divider

M_{D1}'s gate voltage, V_{REG}, is constantly set to V_G's "HI" value. So when the power transistor M_{PWR} is conducting, M_{D1}'s and M_{D2}'s gate voltages are equal:

$$V_{REG} = V_G \leftarrow \mathrm{M_{PWR}\,is\ conducting} \qquad \text{Eq. 3-22}$$

As seen in Figure 3-1, V_{ODIV} connects to a comparator's input, which will not draw DC current. We can then equal the drain currents of M_{D1} and M_{D2}.

$$I_{M_{D1}} = I_{M_{D2}} \qquad \text{Eq. 3-23}$$

Substituting each current term according to the equation for triode operation, and disregarding body effect, we have:

$$KP_n\left(\frac{W}{L}\right)_{D1} V_{ODIV}\left(V_G - V_{th} - \frac{V_{ODIV}}{2}\right) = KP_n\left(\frac{W}{L}\right)_{D2} (V_O - V_{ODIV})\left(V_G - V_{ODIV} - V_{th} - \frac{V_O - V_{ODIV}}{2}\right) \qquad \text{Eq. 3-24}$$

from which we'll take an expression that will be useful later on:

$$V_{ODIV}\left(V_G - V_{th} - \frac{V_{ODIV}}{2}\right) = \left(\frac{(W/L)_{D2}}{(W/L)_{D1} + (W/L)_{D2}}\right) V_O\left(V_G - V_{th} - \frac{V_O}{2}\right) \qquad \text{Eq. 3-25}$$

We can write this expression in terms of the divisive factor D, as defined previously.

$$D \stackrel{\text{def}}{=} \frac{(W/L)_{D1} + (W/L)_{D2}}{(W/L)_{D2}} \quad \text{Eq. 3-26}$$

$$V_{ODIV}\left(V_G - V_{th} - \frac{V_{ODIV}}{2}\right) = \frac{1}{D}\, V_O \left(V_G - V_{th} - \frac{V_O}{2}\right) \quad \text{Eq. 3-27}$$

It is important to note that the above equations depend on matching only between M_{D1} and M_{D2}. Unlike the transistors in the replica, M_{D1} and M_{D2} don't have their gate area constrained by system specifications, so eventual matching problems can be easily solved.

3.1.3 Large-signal analysis

Having determined useful expressions for the two added elements, we can perform a large-signal analysis on the system in Figure 3-1 to obtain a more exact formula for I_{LIM}. It is defined as the current I_{PWR} for which the short-circuit flag V_{SC} is activated. If the comparator has no input offset:

$$I_{LIM} = I_{PWR}|_{V_{ODIV}=V_{THRES}} \quad \text{Eq. 3-28}$$

We start by writing the current equations for the power transistor and the replica stack (using Eq. 3-17 as an approximation).

$$\begin{cases} I_{Ref} = KP_n \left(\frac{W}{L}\right)_{REP} \left(\frac{1}{K}\right) V_{THRES} \left(V_G - V_{th} - \frac{V_{THRES}}{2}\right) \\ I_{PWR} = KP_n \left(\frac{W}{L}\right)_{PWR} V_O \left(V_G - V_{th} - \frac{V_O}{2}\right) \end{cases} \quad \text{Eq. 3-29}$$

Applying Eq. 3-28 results in:

$$\begin{cases} I_{Ref} = KP_n \left(\frac{W}{L}\right)_{REP} \left(\frac{1}{\mathrm{K}}\right) V_{ODIV} \left(V_G - V_{th} - \frac{V_{ODIV}}{2}\right) \\ I_{LIM} = KP_n \left(\frac{W}{L}\right)_{PWR} V_O \left(V_G - V_{th} - \frac{V_O}{2}\right) \end{cases} \quad \text{Eq. 3-30}$$

$$I_{LIM} = I_{Ref} \frac{(W/L)_{PWR}}{(W/L)_{REP}}\, K \frac{V_O \left(V_G - V_{th} - \frac{V_O}{2}\right)}{V_{ODIV}\left(V_G - V_{th} - \frac{V_{ODIV}}{2}\right)} \quad \text{Eq. 3-31}$$

where the last term can be simplified through Eq. 3-27.

$$I_{LIM} = I_{Ref} \frac{(W/L)_{PWR}}{(W/L)_{REP}}\, KD \quad \text{Eq. 3-32}$$

Eq. 3-32 confirms the previous formula for I_{LIM} *without using the linear triode approximation* of Eq. 3-5. It still disregards second-order effects, which will be more visible in simulations later on.

3.1.4 Comparator-induced error

The comparator is the block that ultimately generates the short-circuit signal V_{SC}. If it is unbalanced, that is, if it does not trip exactly when its inputs are equal, that will be visible in the threshold current I_{LIM}. We will evaluate the effect of the comparator's *input offset*, V_{OS}, on the system's precision. The threshold condition is now written as:

$$I_{LIM} = I_{PWR}|_{V_{THRES}=V_{ODIV}+V_{OS}} \quad \text{Eq. 3-33}$$

For simplicity, we will use the linear triode approximation. The analysis closely follows that at the start of this chapter.

$$V_{THRES} = V_{ODIV} - V_{OS} \Rightarrow I_{LIM}.R_{M_{PWR}}/D = I_{Ref}.K.R_{M_{REP}} + V_{OS} \Rightarrow$$

$$I_{LIM} = I_{Ref}.K.D.\frac{R_{M_{REP}}}{R_{M_{PWR}}} + V_{OS}.\frac{D}{R_{M_{PWR}}} \quad \text{Eq. 3-34}$$

$$I_{LIM} = I_{Ref}.K.D.\frac{\left(\frac{W}{L}\right)_{PWR}}{\left(\frac{W}{L}\right)_{REP}} + V_{OS}\frac{D}{R_{M_{PWR}}} \quad \text{Eq. 3-35}$$

We can conclude that if the comparator is affected by a fixed input offset V_{OS}, it will translate as an error of $V_{OS}\frac{D}{R_{M_{PWR}}}$ in the threshold current. Here is one drawback of increasing D: it exacerbates the effect of the comparator's offset.

3.1.5 Summary

The analysis of the system, disregarding second-order effects, yielded the following equation for the threshold current I_{LIM}:

$$I_{LIM} = I_{Ref}\frac{(W/L)_{PWR}}{(W/L)_{REP}}\,KD \quad \text{Eq. 3-36}$$

In this equation, $(W/L)_{PWR}$ and I_{LIM} are constrained during the design of the powerstage. When designing the overcurrent detection system, a compromise must be reached between the remaining parameters. Table 2 summarizes the main factors limiting for each parameter, according to the results of this chapter's analysis.

Table 2: Main design parameters and their limits

Design parameter	Lower limit	Upper limit
I_{Ref}	Remaining parameters	Excessive current consumption
$(W/L)_{REP}$	Error due to process mismatch	Remaining parameters
K	Remaining parameters	Variations in corners
D	Remaining parameters	Multiplies comparator error

3.2 Overcurrent Detection for BTL

The system described in the previous pages has been reported in detail when applied to SE class-D output power stages. Mentions of overcurrent detection systems for BTL output stages are somewhat vague and, in the author's opinion, show room for improvement.

Y. Feng et. al. [9] mention in passing a class-D BTL power stage with overcurrent detection based on [3] without detailing specifics for BTL systems. Guilherme and Duarte [18] uses a simple parallel current sensing system, duplicated for each arm. We refer to this kind of solution as "conventional configuration".

3.2.1 Conventional Configuration

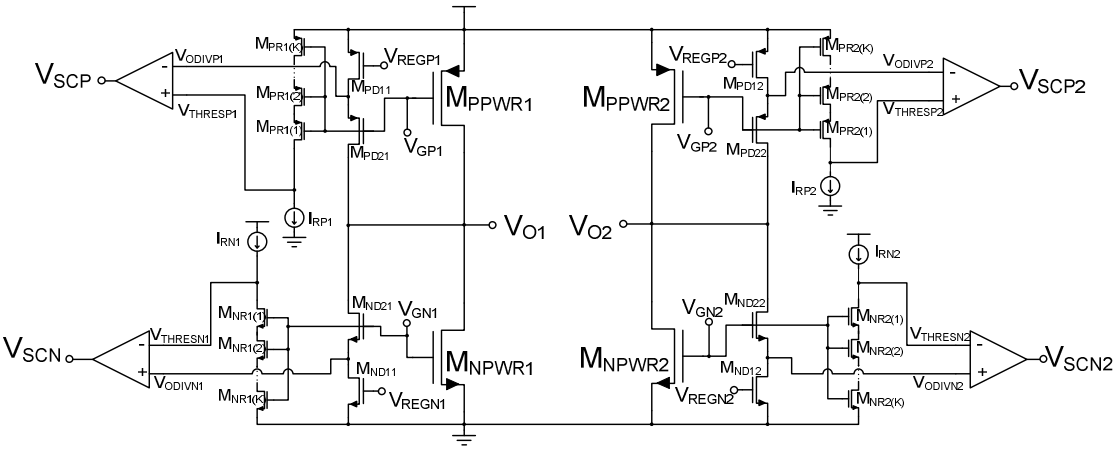


Figure 3-8: Conventional configuration for overcurrent detection system for BTL power stages

Figure 3-8 represents a possible overcurrent detection system for Class-D BTL output stages using CMOS power transistors. It is a simple duplication of the system in [17], and uses 4 detection cells (as described in section 3.1) to detect overcurrent in all 4 power devices, at any given time. This configuration will certainly work, but let's evaluate its operation for all the possible states of the class-D power stage (except blanking time).

Table 3: Overcurrent detection per power stage state

$V_O=V_{O1}-V_{O2}$	Power transistor state				Overcurrent flag relevant?			
	M_{NPWR1}	M_{NPWR2}	M_{PPWR1}	M_{PPWR2}	SCLow1	SCLow2	SCHigh1	SCHigh2
V_{DD}	OFF	ON	ON	OFF	N	Y	Y	N
$-V_{DD}$	ON	OFF	OFF	ON	Y	N	N	Y
0	ON	ON	OFF	ON	Y	Y	N	N
0	OFF	OFF	ON	ON	N	N	Y	Y

If a power device is in the OFF state, there is no need to sense if it is on overcurrent. It can be seen that for every state, two of the four overcurrent detection sections are not evaluating useful information. These unused sections needlessly occupy IC area and consume current.

We propose that a configuration using only part of the redundant sections could provide the needed functionality while saving current and IC area.

3.2.2 Proposed Configuration

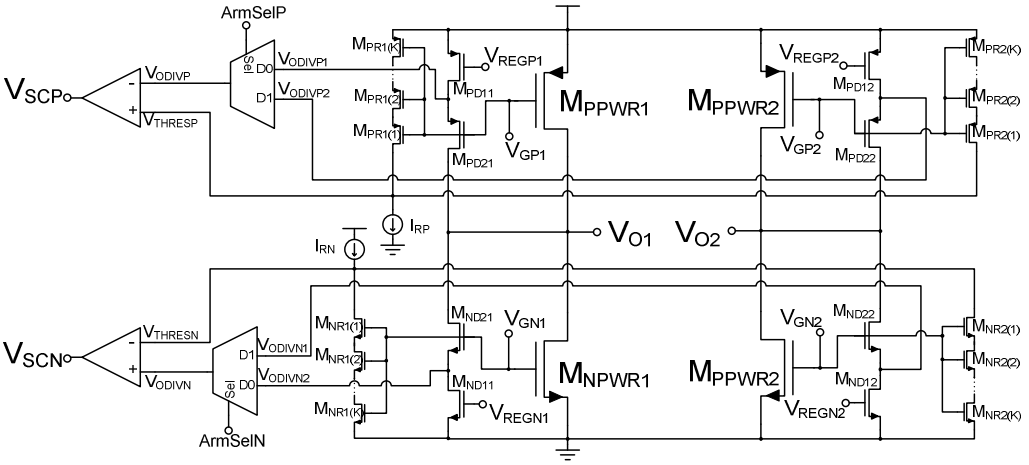


Figure 3-9: Proposed configuration for overcurrent detection system for BTL power stages

Figure 3-9 represents the proposed configuration for an overcurrent detection system for BTL class-D output stages. Main differences from the conventional configuration are the **multiplexed sensed voltages** and the **shared replica drains**. Their purpose is explained in the following subsections.

A. Multiplexed sensed voltage

The sensed voltages from the two arms go through analog multiplexers. These two independent switches, one for lowside and another for highside, select which sensed voltage is to be compared with the threshold voltage. They effectively select which arm is being checked for overcurrent.

In AD-modulation, only one highside and one lowside power devices are active at any time. The selection is simple: select the active device.

During BD-modulation, however, there is the possibility that both lowside or both highside devices are conducting current. In this case, the single comparator cannot, at the same time,

evaluate for overcurrent in the two active power transistors. A compromise solution, adopted here, is alternating between observing one arm and the other, according to a supplied clock signal. This has the disadvantage that detection time is increased, when comparing to the conventional solution. The actual delay due to this selection can go from 0 (if the overcurrent event coincides with the selection of that device) to one clock period.

B. Shared replica drains

In the proposed configuration, the replicas from the same side (high or low) have their drains connected. There is only one overcurrent threshold voltage to be compared with the selected sensed voltage for that side.

During AD-modulation, the system naturally drives the current I_{REF} to the replica corresponding to the active device. Since the replicas share the same gate voltage as the corresponding active devices, the replica corresponding to the inactive device will be at cutoff, while the other will draw I_{REF}, and the threshold voltage is correctly defined as in the conventional configuration.

In BD-modulation, on the other hand, there are times when both replicas are in saturation and both draw current from their current source. To maintain the same current to each replica, the current source doubles its output in these moments.

Table 4: Operation of replica current sources. "X" denotes "N" for lowside, "P" for highside.

Power transistor's state		Current injected into replicas
M_{XPWR1}	M_{XPWR2}	I_{RX}
OFF	OFF	0
OFF	ON	I_{Ref}
ON	OFF	I_{Ref}
ON	ON	2 I_{Ref}

3.2.3 Summary

The proposed configuration saves two comparators relatively to the conventional solution. This is done with no significant drawback when using AD-modulation. For BD-modulation, there will be increased detection delay and a slightly more complex reference source scheme will be needed.

3.3 Synopsis

The overcurrent detection cell for a generic large MOS transistor was analyzed. Design equations and guidelines for the compromises involved were set. A new configuration of an overcurrent protection system for BTL class-D amplifiers was proposed. This configuration avoids the use of two out of four comparators, resulting in current and area savings while only compromising detection time in BD-modulation.

4 Proof-of-concept implementation

This chapter describes the target power stage and the implementation of all the blocks of the proposed architecture.

4.1 Target Power Stage and specifications

The power stage to be targeted by the overcurrent detection system is part of a test-chip designed in the context of the HEAD Project. It will be built on a 0.18 µm, 3.3 V CMOS technology.

The topology chosen for the power stage is that of a typical P/N CMOS inverter. Each power transistor is split in 4 parallel "slices". The number of active slices can be scaled to adapt to different load resistances and output power; the desired threshold current changes accordingly. Hence, the power transistors behave as if they have variable width.

Table 5: Variability of Power Stage Width and desired I_{LIM}

Active Slices	Active power NMOS width	Active power PMOS width	R_L (minimum)	P_O (maximum)	I_{LIM}
4	7.560 mm	18.900 mm	4 Ω	1 W	960 mA
3	5.670 mm	14.175 mm	5.33 Ω	0.75 W	720 mA
2	3.780 mm	9.450 mm	8 Ω	0.5 W	480 mA
1	1.890 mm	4.725 mm	16 Ω	0.25W	240 mA

Besides this variability according to the desired output power, the threshold current must also be configurable by way of a 2-bit input iscadj<1:0>.

Table 6: Adjustment of I_{LIM}

iscadj<1:0>	Limiting current adjustment	α_{adj}
00	-16.6%	0.833
01	+0%	1.000
10	+16.6%	1.166
11	+33.3%	1.333

The specification for the current I_{LIM} can be expressed as depending on the number of active slices, N_{SLICES}, and the adjusting factor α_{adj}.

$$I_{LIM} = 240mA \times (N_{SLICES}\alpha_{adj}) \quad \text{Eq. 4-1}$$

Furthermore, the target system includes two different supply domains: the regular domain, modelled with an ideal 3.3V voltage source, and the power domain which is modelled with a 3.3V supply with 100 mΩ leads. The power stage and other power-heavy components are on the power domain, but all the sensitive blocks should be on the quieter regular supply if possible.

4.2 System topology and main parameters

The overcurrent detection system configuration from section 3.2.2 must be implemented in a way that adapts to the power transistor's variable width while providing the desired threshold current.

To provide accurate matching from replica to power transistor at the layout level, it is useful that each slice has its own replicas. That means that the active replica widths will scale with the active power transistor's width. This maintains the width ratio in Eq. 3-32. Parameters K and D are hardly configurable and will remain fixed. To achieve the scalability of I_{LIM} defined in Table 5 and Table 6, the reference current itself will be adaptable.

Main parameters W_{NPWR}/W_{NREP} and W_{PPWR}/W_{PREP} (the ratio between a power MOS and each one of its replica transistors), D (divisive factor), and K (number of replica transistors in the stacks), as well as specification for the limiting current I_{LIM} will define the reference currents I_{RN} and I_{RP}. Choosing these parameters in order to optimize I_{LIM} precision, for example, would have to take into account process mismatch parameters and second-order effects and as such is very difficult to perform analytically or through simulation of a simplified model.

The best design method would involve exploring various compromises between these parameters, and fine-tuning the most promising one. Unfortunately, other tasks in the HEAD project had greater priority. Hence, the iterative design process had to be hastened and the key parameters were fixed to values consistent with bibliography and the system's current constraints. A later analysis will allow insight into the suitability of the chosen values.

Table 7: Key parameters

Parameter	Abbreviation	Chosen value
Power MOS to replica transistor ratio	W_{NPWR}/W_{NREP}, W_{PPWR}/W_{PREP}	2000
Stacked transistors in replica	K	4
Dividers' divisive factor	D	2

The reference current that goes through each active replica will have to be programmable according to the following equation:

$$I_{Ref} = \frac{I_{LIM}}{16000} \qquad \text{Eq. 4-2}$$

which along with Eq. 4-1 yields:

$$I_{Ref} = 15\mu A \times (N_{SLICES}\alpha_{adj}) \qquad \text{Eq. 4-3}$$

Figure 4-1 shows the final topology chosen. Notice how the dividers are in the power domain but not split in four.

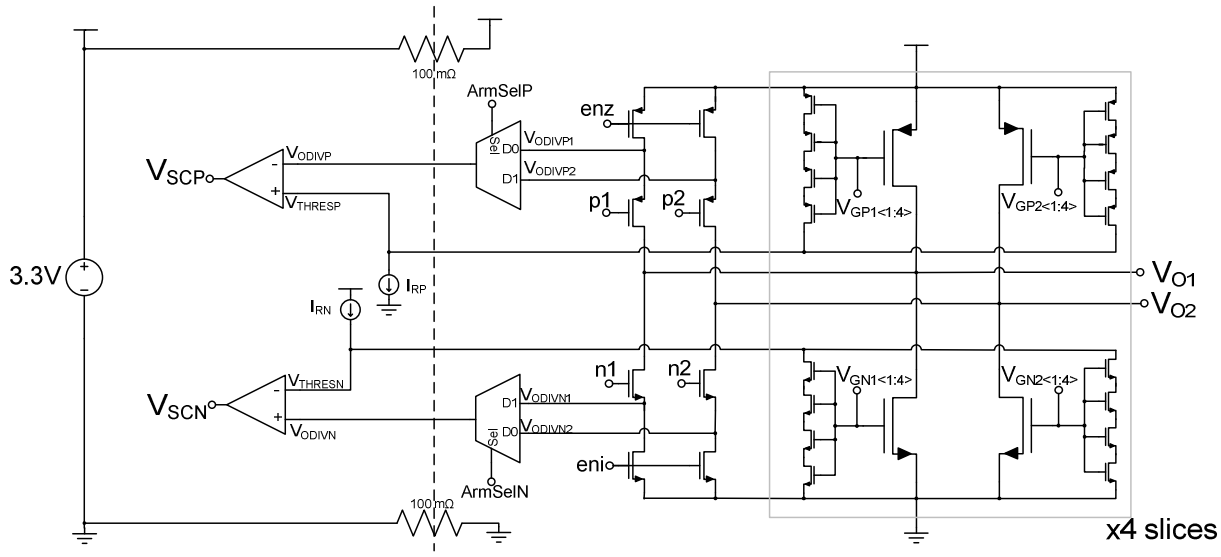


Figure 4-1: Implementation for selectable-width class-D output stage

4.3 Replica transistors

One replica of K=4 stacked transistors is positioned parallel to each power MOS slice. Power PMOS slices have W=4.725 mm, and NMOS slices have W=1.89 mm. Having chosen a power MOS to replica ratio of 2000 (section 4.2), it can be determined that P replicas should have a width of W_{PREP}=2.36 µm and N replicas have W_{NREP}=945 nm. Both replica and power transistors have minimum channel length L=0.34 µm.

4.4 Programmable current sources

This block provides the current for both highside and lowside replicas. This current must be programmable according to Eq. 4-3, and it must also quickly double when both highside or both lowside replicas are turned on (see Table 4). Other requisites are low variation within the intended simulation corners, and small adjustment time following abrupt variations in the load (i.e. switching events in the power stage).

The target system includes a precision current source which provides reference currents of 2.5 µA. The programmable current source will use this external bias current, $I_{biasext}$, as a reference to the output currents. This block's current multiplicative factors can be defined as the ratio between its output currents and the initial reference current:

$$C_N = \frac{I_{RN}}{I_{biasext}}, \qquad C_P = \frac{I_{RP}}{I_{biasext}} \qquad \text{Eq. 4-4}$$

By applying Eq. 4-3, those parameters can be expressed as a function of the system's configuration:

$$C_N = C_P = 6 \times (N_{SLICES}\alpha_{adj})$$ Eq. 4-5

Figure 4-2 shows this block's schematic, not including the logic that controls programmability.Figure 4-2:

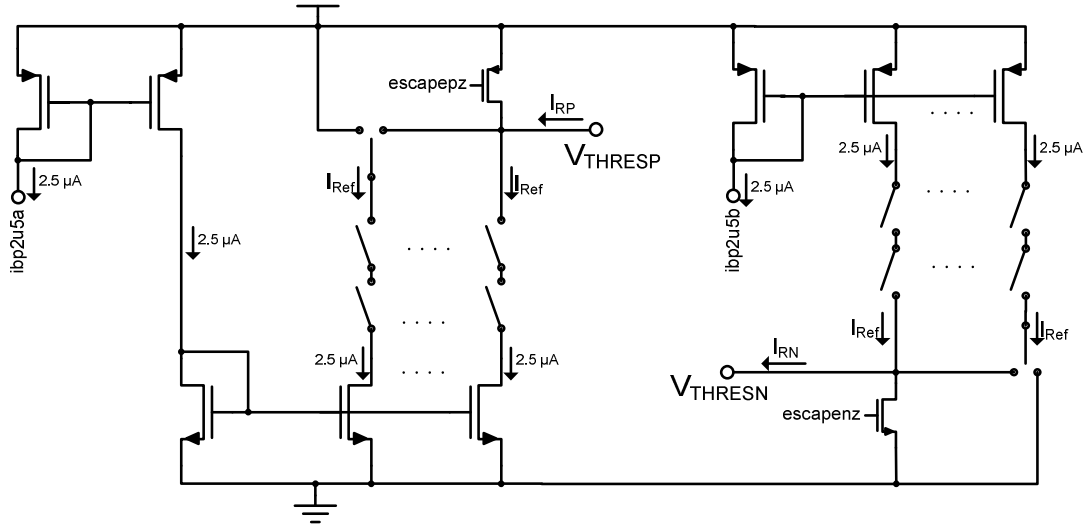


Figure 4-2: Schematic of programmable current source

Arrays of simple current mirrors, produce current increments of 2.5 µA each from $I_{biasext}$. For the programmability, simple MOS switches (controlled by digital logic) then allow this current to pass through to the output or block its path. When blocked, the base transistor for that current increment will be in triode; when it is unblocked, the current will take some time to recover to the intended value (programmability is not fast, but that was not a requisite). The increments of 2.5 µA add up to two lines each carrying I_{Ref}, in accordance with Figure 4-2.

Those lines are added or blocked by simple current steering to yield the desired I_{RN} or I_{RP} (see Table 4). One transistor provides an escape path for when the replicas being fed by that current are both at cut-off.

One major disadvantage of adopting current-steering for the doubling of the current is that the system's total current consumption is considerably increased. In BD-modulation mode, this block consumes $4.I_{REF}$ (disregarding branches carrying the original 2.5 µA reference); of that current, $2.I_{REF}$ goes to the load but the rest is dumped. For AD-modulation mode, the current-doubling is not needed and the system appropriately consumes $2.I_{REF}$. If the base current mirrors had better settling time, current steering could possibly be avoided without significantly affecting overcurrent detection delay.

4.5 Voltage dividers

There are 4 voltage dividers in the system, one for each power MOS. They provide a "sensed voltage" based on one output voltage: if the corresponding power MOS is active, sensed voltage is proportional to the output voltage; else, the sensed voltage is shunted to ground or V_{DD}, avoiding false positives in the overcurrent detection flag.

To deal with the 4 different slices, digital signals p1, p2, n1 and n2 (which control the dividers, as seen in Figure 4-1) are constructed from the 16 gate signals of the power transistors. These are in the same voltage domain as the enable signal eni and its complement enz, so as to satisfy Eq. 3-22.

$$\begin{aligned} \mathrm{p1} &= \mathrm{NOR}(\mathrm{V_{GP1<1:4>}}) \\ \mathrm{p2} &= \mathrm{NOR}(\mathrm{V_{GP2<1:4>}}) \\ \mathrm{n1} &= \mathrm{AND}(\mathrm{V_{GN1<1:4>}}) \\ \mathrm{n2} &= \mathrm{AND}(\mathrm{V_{GN2<1:4>}}) \end{aligned} \qquad \text{Eq. 4-6}$$

Since one transistor in each divider connects to an output pin, the ESD guidelines for this technology advise that a series resistance of at least 200Ω be placed in series with its drain. To keep the divisive factor, an equal resistance is placed in series with the other transistor's drain. The voltage drop in these resistors will be verified to be negligible.

Finally, the highside divider's transistors had a direct body-source connection, eliminating body effect. This was not done for the lowside divider since the technology does not allow separated p-wells.

4.6 Analog multiplexer and arm selection logic

The analog multiplexer consists of simply of two CMOS switches controlled by opposite signals. Figure 2-1 shows this block's schematic. The CMOS switch cell, as well as all the basic logic cells used in this work, was kindly designed by António Rodrigues. It has a maximum impedance of 6 kΩ. Considering that its load capacity (the comparator's input capacity) is circa 0,15pF, the resulting ~1ns time constant is negligible when compared to the total detection time of the system.

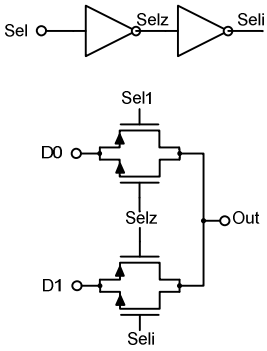


Figure 4-3: Schematic of analog multiplexer

The 2 multiplexers in the system are controlled by a logic block. This block receives the PWM signals from **Eq. 4-6**; a bit determining if BD-modulation is on; and a clock signal to alternate between one arm and the other when applicable.

The desired state of the MUX for each state of the output stage can be inferred from Table 3. If one side's both power MOS's are inactive, the desired arm is irrelevant. If both are active, the watched arm should be the one that was not watched during the last clock cycle. Table 8 includes the truth tables for the highside and lowside arm selection logic.

Table 8: Arm selection logic

p1	p2	Watched arm	$\mathrm{ArmSelP_i}$
0	0	Alternate between arms	$\overline{\mathrm{ArmSelP_{i-1}}}$
0	1	Arm 1	0
1	0	Arm 2	1
1	1	Arm 1 (irrelevant)	0

n1	n2	Watched arm	$\mathrm{ArmSelN_i}$
0	0	Arm 1 (irrelevant)	0
0	1	Arm 2	1
1	0	Arm 1	0
1	1	Alternate between arms	$\overline{\mathrm{ArmSelN_{i-1}}}$

4.7 Comparators

The two comparators perform the comparison between the voltages from the replica drains and the voltages sensed from the outputs. Key specifications are:

- Near-rail input common-mode
- Low comparison delay
- Small input offset
- Small current footprint

The first specification can be met by choosing a folded cascade amplifier as an input stage. For the lowside comparator, a PMOS input differential pair is used; conversely, the highside comparator uses a NMOS differential pair. The schematics are in Figure 4-4.

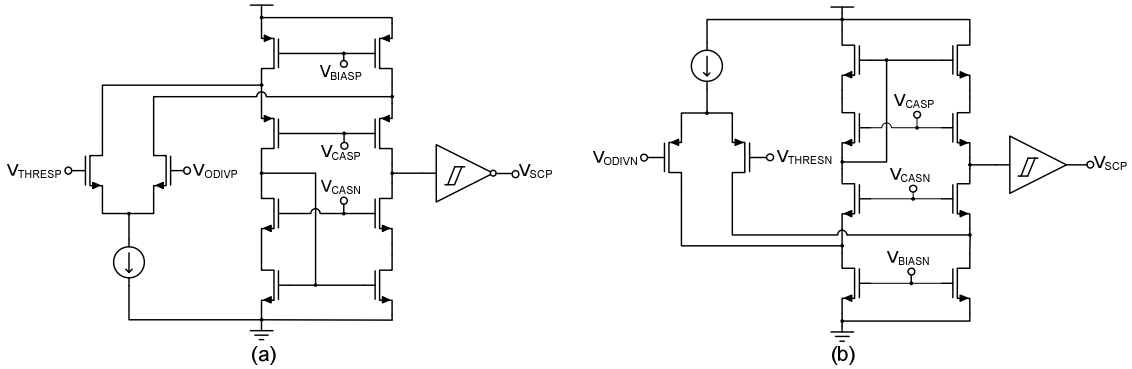


Figure 4-4: Schematic of the comparators. (a) Highside comparator; (b) Lowside comparator.

The folded cascode stage is simply followed by a general-purpose Schmitt trigger, which was designed by António Rodrigues. More complex topologies with more than one analog stages could possibly have helped to reach a better compromise between speed, offset and current consumption, but the design time parameter was deemed of greater importance.

Some revelant specs of the comparators are 30 ns comparison time and current consumption of 40 μA.

4.8 Support Blocks

A pair of other blocks were included that, although not intrinsic to the overcurrent detection system, can be critical to its precision.

An integrated reference current source and an accompanying current mirror, were kindly designed by António Rodrigues for providing a stable 2.5 μA to the overcurrent detection system and the other chip's components. It can be self-biased, as tested in this work, or ultimately adjusted using external resistors.

One of the 2.5 μA reference currents provided by that cell is further mirrored, in the overcurrent detection system block, by a self-biased cascode current mirror of the author's design.

4.9 Layout

The layout of the powerstage, its drivers and support logic, and the overcurrent detection system is reproduced in Figure 4-5.

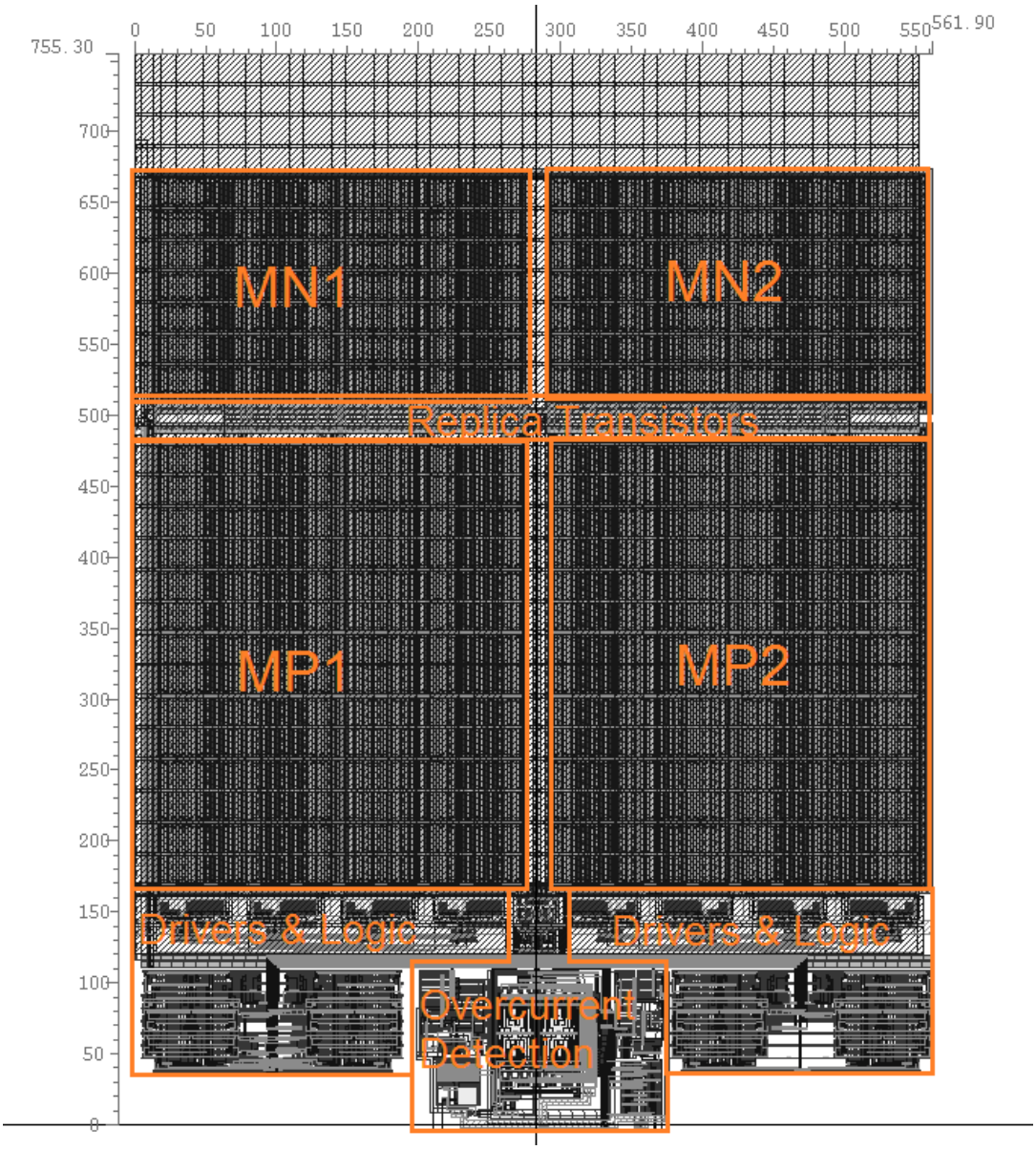


Figure 4-5: System layout

The layout implementation of the replicas is relevant in assessing the process and thermal matching between replica and power MOS. Ideally, the replica transistors and power MOS are part of the same finger matrix and share a common centroid. However, the design steps taken for this chip impeded this approach. Instead, the replica transistors are in the center of the powerstage, in the space between the power devices, as reproduced in Figure 4-6.

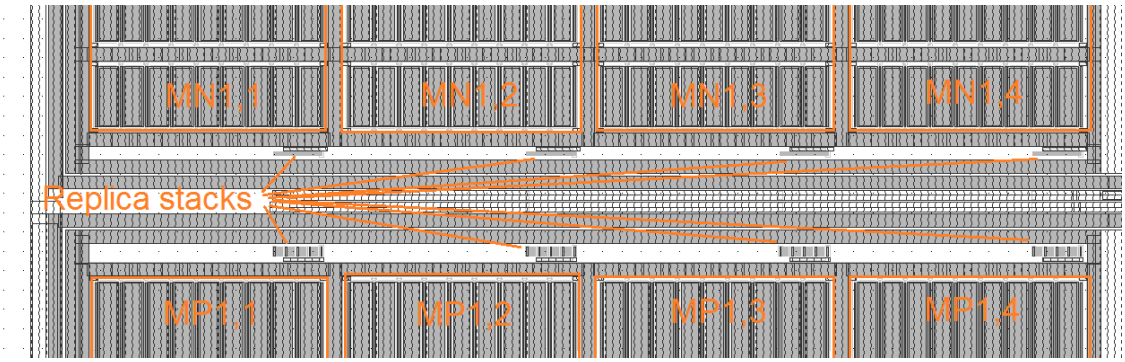


Figure 4-6: Placement of replica stacks, relative to power transistor slices.

Apart from the replica transistors, the overcurrent detection system is separated from the powerstage, to the south.

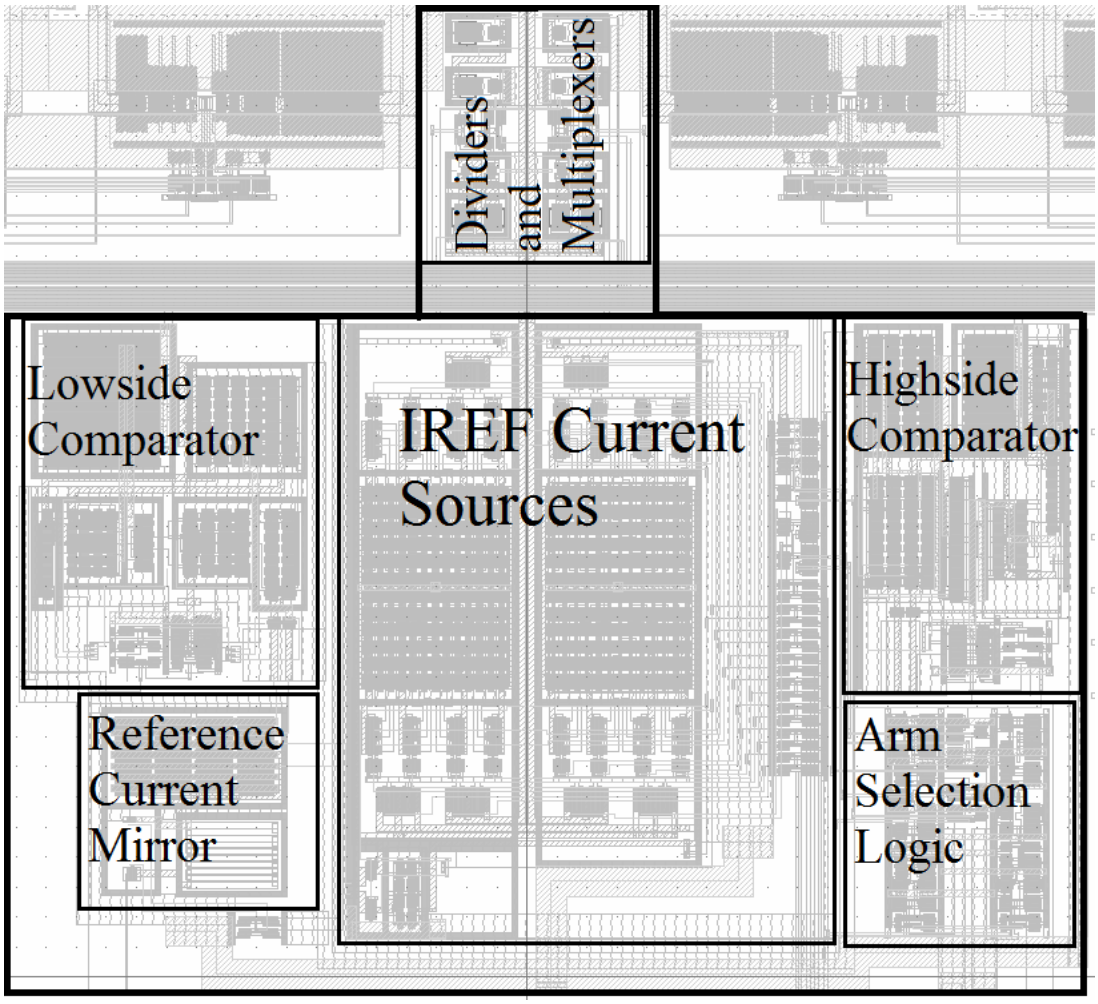


Figure 4-7: Layout of the overcurrent detection systems. Replicas are located within the powerstage.

The layout was verified to be in accordance with the technology design rules (DRC), and to correspond with the designed schematic (LVS). Both verification steps were made using the Calibre tools from Mentor Graphics.

4.10 Synopsis

The target powerstage and its requirements were set. The key design parameters were chosen, with optimization limited by the project's time constraints. The various sub-blocks and their working were described. Views of the layout implementation were reproduced.

5 Simulation Results

The design of this system and of its sub-blocks relied extensively on simulations using the HSPICE tool. While describing all these simulations and including their results would fall out of the scope of this document, the top-level results are key to validating the work here presented. In this chapter, the relevant testbenches are described and the extracted measures are registered.

5.1 Ramp Simulation - for precision

This simulation is performed with the aim of measuring the limiting currents for lowside and highside, I_{LIMN} and I_{LIMP}, and their variation with corners and process mismatch. Furthermore, a few other figures are extracted to evaluate the sources of error in the system.

5.1.1 Simulation Description

A transient simulation is performed on the system from Figure 4-1. The powerstage's input signals are set so that M_{N1} and M_{P2} are conducting and M_{N2} and M_{P1} are at cut-off. Its load is a variable resistance, whose value is slowly ramped down to zero. This results in a slow increase of the current through the active transistors, which will eventually trigger the detection system's outputs.

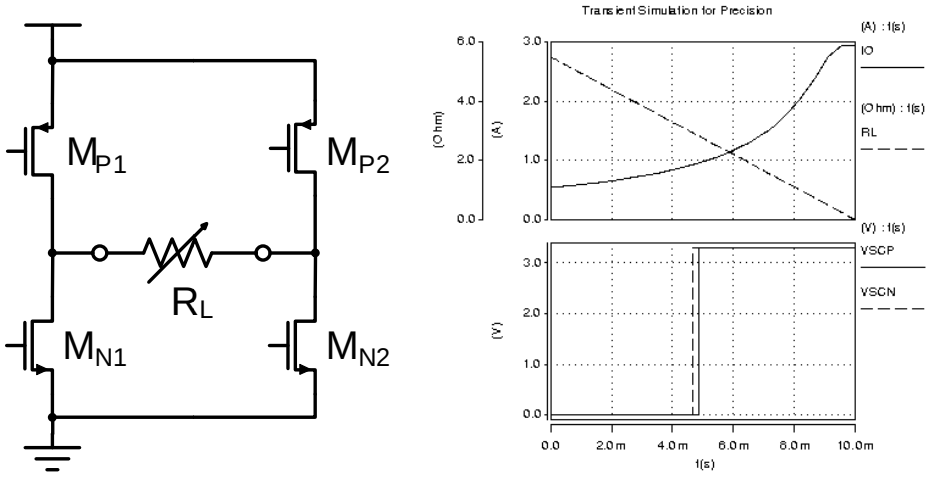


Figure 5-1: Transient simulation for precision.

5.1.2 Evaluated Benchmarks

A few relevant measures are extracted from the simulation for precision. The aim is to separate the system's imprecision sources from one another. The delimited sources of imprecision are the input 2.5 µA current, the programmable current source, the replica and divider (as a whole), and the comparators' input offset.

Table 9: Evaluated benchmarks for simulation for precision.

Benchmark	Symbol	Expression	Notes	Nominal Value
NMOS limiting current	I_{LIMN}	$I_O\|_{V_{SCN}=V_{DD}/2}$	Is the final desired parameter	Depends on setting. See Eq. 4-1.
PMOS limiting current	I_{LIMP}	$I_O\|_{V_{SCP}=V_{DD}/2}$		
Input reference current	$I_{biasext}$	-	The original bias current.	2.5 µA
NMOS reference current multiplicative factor	C_N	$\frac{I_{RefN}}{I_{biasext}}$	Defined by the programmable current source.	Depends on setting. See Eq. 4-3
PMOS reference current multiplicative factor	C_P	$\frac{I_{RefP}}{I_{biasext}}$		
NMOS N factor	N_N	$\frac{I_O\|_{V_{THRESN}=V_{ODIVN}}}{I_{RefN}}$	Limiting current to replica current ratio, excluding error from comparator offset. Defined by replica and divider.	16000
PMOS N factor	N_P	$\frac{I_O\|_{V_{THRESP}=V_{ODIVP}}}{I_{RefP}}$		
Lowside comparator induced error	ε_{CmpLow}	$\frac{I_O\|_{V_{SCN}=V_{DD}/2}}{I_O\|_{V_{THRESN}=V_{ODIVN}}}$	Measure of the error introduced by the comparator's input offset.	1
Highside comparator induced error	$\varepsilon_{CmpHigh}$	$\frac{I_O\|_{V_{SCP}=V_{DD}/2}}{I_O\|_{V_{THRESP}=V_{ODIVP}}}$		

The many figures obtained only allow us to separate the sources of imprecision if we know their relevance in the system. For that, note that the threshold currents can be written as the product of the other figures:

$$I_{LIMN} = I_{biasext}.C_N.N_N.\varepsilon_{CmpLow} \quad \text{Eq. 5-1}$$

$$I_{LIMP} = I_{biasext}.C_P.N_P.\varepsilon_{CmpHigh} \quad \text{Eq. 5-2}$$

5.1.3 Corners results

The figures above were extracted for all possible configurations, and for typical conditions plus 32 alters. A more thorough analysis could have looked into the values for each corner, but for clarity we focus on the maximum, typical and minimal values obtained for each measured parameter.

Figure 5-2 shows the results for the most important parameter: the threshold current. Extracted values for I_{LIMN} and I_{LIMP} are shown, both as absolute values and as a percentage of its nominal value. It can be seen that, for typical condition, the extracted threshold currents closely follow the desired nominal value. This is especially true of the threshold current for the highside.

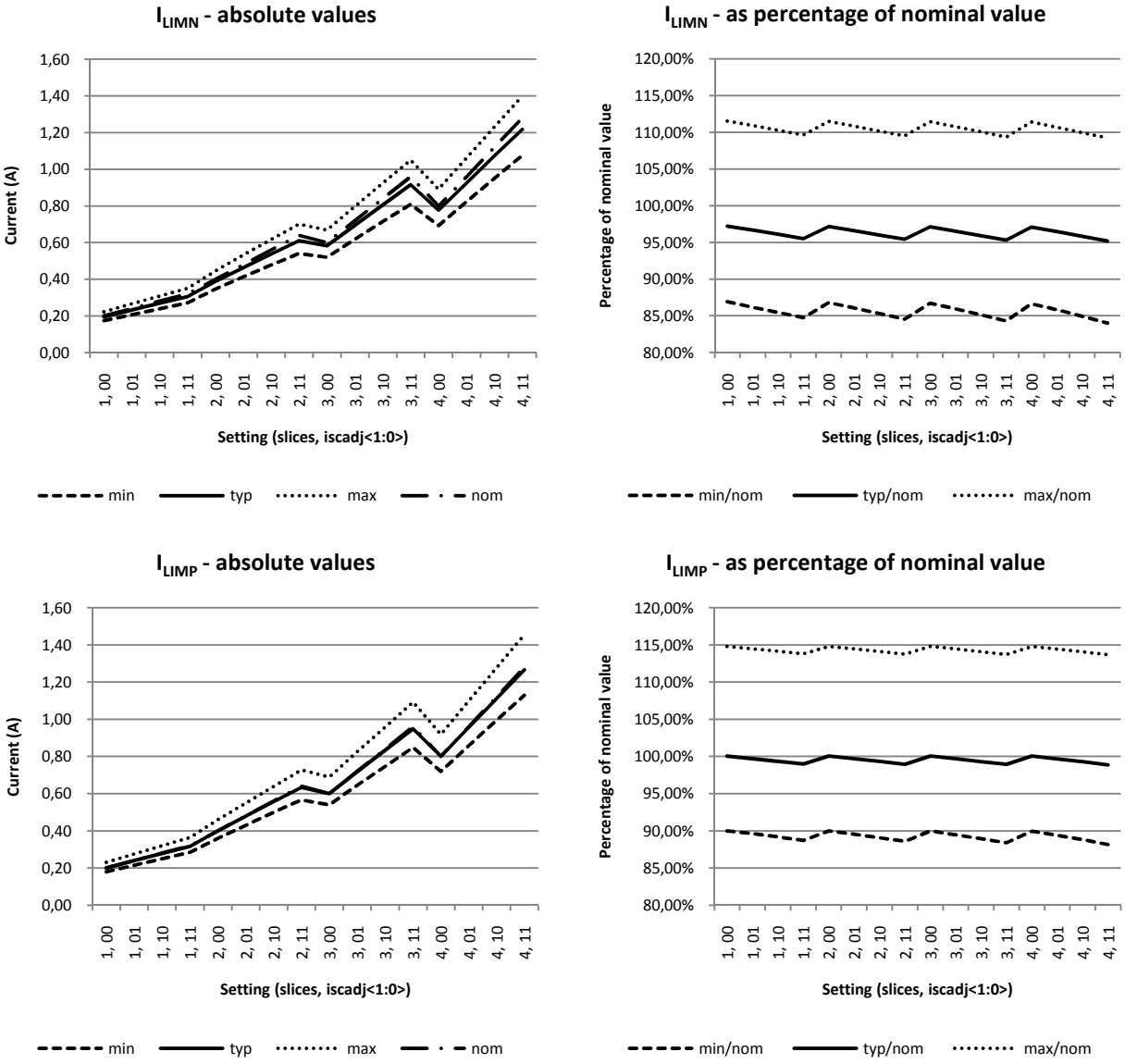


Figure 5-2: I_{LIMN} and I_{LIMP} results for corners simulation.

A more precise analysis of the results is made for the typical settings: 4 active slices, and iscadj<1:0>=01. These figures are presented in Table 10, as a percentage of their nominal value. The spread, that is, the difference between maximum and minimum results, can be useful to determine which component produces the most variation against corners.

Table 10: Precision analysis on corners simulation. For 4 active slices, iscadj<1:0>=01

Measure	Min	Typ	Max	**Spread**
I_{LIMN}	85,82%	96,47%	110,71%	**24,89%**
$I_{biasext}$	93,08%	98,56%	113,28%	**20,20%**
C_N	94,41%	100,41%	100,70%	**6,29%**
N_N	95,38%	97,38%	98,94%	**3,56%**
ε_{CmpLow}	100,07%	100,10%	100,11%	**0,04%**

Measure	Min	Typ	Max	**Spread**
I_{LIMP}	89,40%	99,68%	114,44%	**25,04%**
$I_{biasext}$	93,08%	98,56%	113,28%	**20,20%**
C_P	95,12%	101,77%	102,33%	**7,21%**
N_P	98,19%	99,31%	101,00%	**2,81%**
$\varepsilon_{CmpHigh}$	100,04%	100,09%	100,09%	**0,05%**

From Table 10, it is clear that the external reference current generates the most variation with corners, followed by the internal programmable current source and then by the replica and divider. The comparators' contribution to this imprecision seems to be negligible. It should also

be noted that the external current source and the replicas and dividers (especially on the lowside) show a somewhat significant error for typical conditions.

Finally, the error from the various components has been verified to be independent of the setting (number of active slices and adjustment bits), except for the limiting current to replica current ratio. In this case, a correlation with the adjustment bits was observed. The higher the adjustment bits, the smaller the N factor. The author speculates that this increase is caused by the larger current through the replicas, which exacerbates the second-order effects not taken into account in the calculations of Chapter 3.

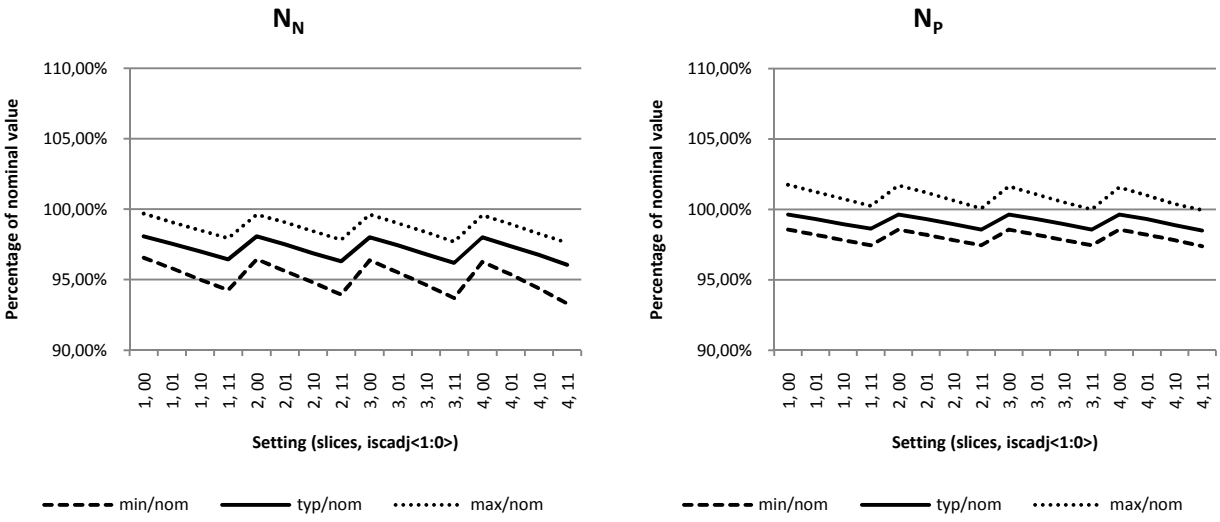


Figure 5-3: N_N and N_P results for corners simulation.

It can be concluded that improvements to the external reference current source with the aim of reducing corners variation (such as using an externally calibrated reference, as will be possible after chip fabrication) could greatly improve the system's precision. Also, the deviations of typical results from nominal value are a failure on the designer's part; it could have very easily been fixed by adjusting the replica's width or the divider's divisive factor.

5.1.4 Monte Carlo results

The same figures were extracted for a Monte Carlo simulation over typical conditions. 1000 Monte Carlo cases were performed for each configuration, with mismatches introduced in the system's MOSFET's and resistances. The relative variance (defined in Eq. 3-8) was taken as a measure of each figure's sensitivity to process variations.

It is important to understand how the threshold current's relative variance is affected by each source of imprecision. If we consider that the measured parameters are statistically independent, and since the threshold current is the multiplication of these parameters, it is true that:

$$c_v(I_{LIMN}) = \sqrt{c_v(I_{biasext})^2 + c_v(C_N)^2 + c_v(N_N)^2 + c_v\left(\varepsilon_{CmpLow}\right)^2} \quad \text{Eq. 5-3}$$

$$c_v(I_{LIMP}) = \sqrt{c_v(I_{biasext})^2 + c_v(C_P)^2 + c_v(N_P)^2 + c_v\left(\varepsilon_{CmpHigh}\right)^2} \quad \text{Eq. 5-4}$$

That is: the threshold current's relative variance is the root mean square of the various blocks' relative variances. It is then possible to talk of a dominant error. If one block's relative variance is much larger than the others', the total variance will be approximately equal to that value and it is that block that should be the target of optimizations.

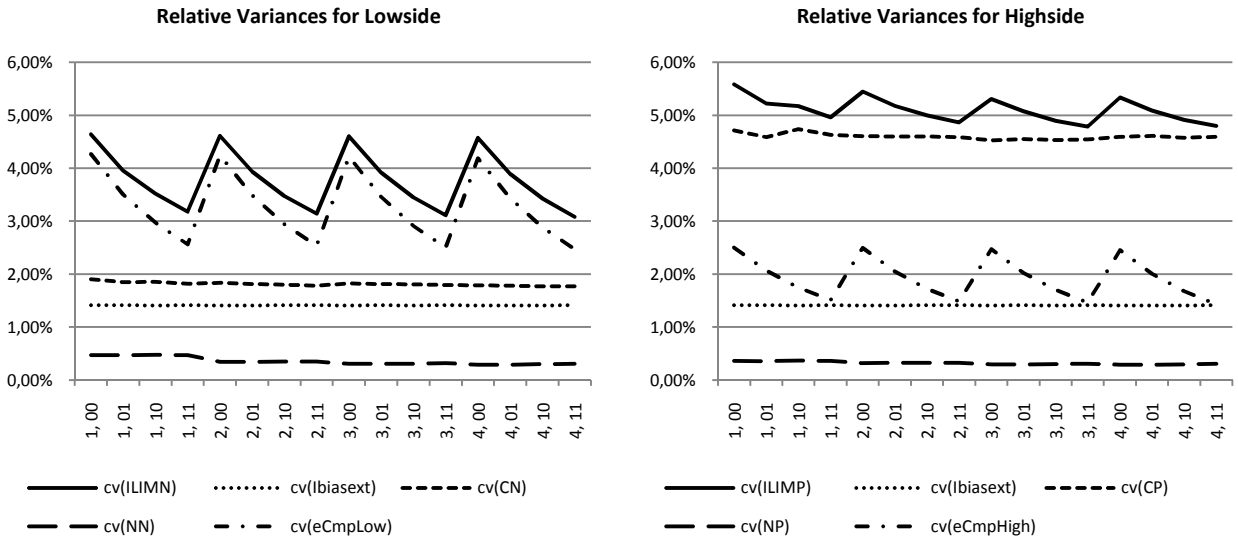


Figure 5-4: Monte Carlo simulation results. Relative variance for the extracted measures.

Figure 5-4 shows the results for the relative variance. It can be seen that for the lowside, the error induced by the comparator is dominant. This figure also shows a strong correlation with the iscadj<1:0> setting; higher iscadj<1:0> lead to lower comparator-induced error. This is because higher iscadj<1:0> leads to higher V_{THRESN}, and the comparator's input offset is diluted in this higher value.

For the highside, the error in the current source is now dominant. This difference from the lowside case can be explained by the fact that the current signal (from the external reference current generator to the replica) suffers an extra mirroring in the highside case (see Figure 4-2). This current mirror's error becomes dominant over the error in the rest of the system.

Keeping in mind that adjusting design parameter D allowed a trade-off between error due to replica mismatch and error due to comparator offset, we can conclude that the compromise achieved was not the most desirable. For the lowside, based on Eq. 3-33, we can speculate that changing D from 2 to 1 (and reducing the replica's width, to maintain I_{LIM}) could have reduced the dominant error. Error due to mismatch ($c_v(N_N)$) would have increased by a factor of $\sqrt{2}$, but it would still be far from dominant. Summing up: the trade-off reached was not the best and the resolution would have benefitted from a more thorough design.

5.2 Functional simulation – for delay and power consumption

Another simulation was performed with three goals: determining proper function of the system when the power stage is switching; measuring the delay in detecting overcurrent; and measuring the power consumption of the overcurrent detection system.

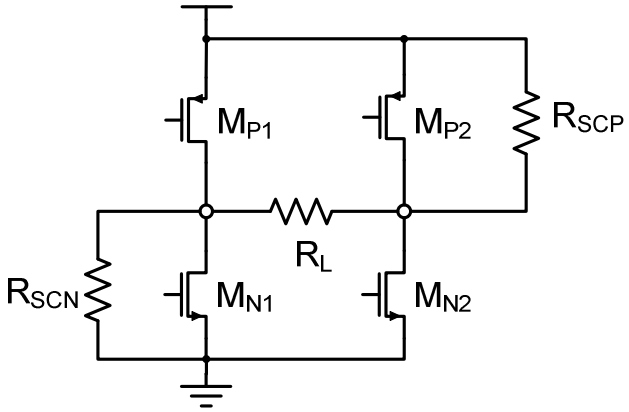


Figure 5-5: Testbench for functional simulation.

The testbench's simplified schematic, from the perspective of the load, is shown in Figure 5-5. The load R_L is set to the minimum for the number of active slices, according to Table 5. To emulate short-circuits, two branches are added from one output to ground and to the supply, with R_{SCN}=R_{SCP}=R_L. The power stage is fed a zero-average, 384kHz PWM signal; as the power stage switches, it enters and exits overcurrent, and the needed measures can be taken. The clock signal used by the arm selection logic is set to a frequency of 6.144MHz.

5.2.1 Evaluated Benchmarks

The measures extracted from this simulation are described in Table 11. Apart from detection times, the power consumptions of the two comparators and of the overcurrent detection system are measured.

Table 11: Extracted benchmarks for functional simulation.

Benchmark	Symbol	Formula	Description
Lowside detection delay	T_{SCLO}	$t\left(V_{SCN} = \frac{V_{DD}}{2}\right) - t(I_{MN1} = I_{LIMN})$	Delay between current crossing the nominal threshold current and activation of the corresponding short-circuit flag.
Highside detection delay	T_{SCHI}	$t\left(V_{SCP} = \frac{V_{DD}}{2}\right) - t(I_{MP2} = I_{LIMP})$	
Current consumption	I_{VDD}	-	Current consumption of overcurrent detection system. Averaged over one clock cycle.
Current consumed by comparators	I_{Comps}	-	Current consumption of the two comparators. Averaged over one clock cycle.

5.2.2 Functional Verification

A very straightforward check of the resulting waveforms allows us to verify if the system is functioning as intended. Figure 5-6 shows the output voltages and the short-circuit signals.

For AD-modulation, there are periods of normal operation, when M_{N1} and M_{P2} are conducting and so are shunting the added short-circuit paths; no overcurrent occurs. On the other hand, when M_{P1} and M_{N2} are the ones conducting, current flows through the normal current path plus the short-circuit paths formed by R_{SCN} and R_{SCP}. Overcurrent occurs and the V_{SCLO} and V_{SCHI} signals are activated.

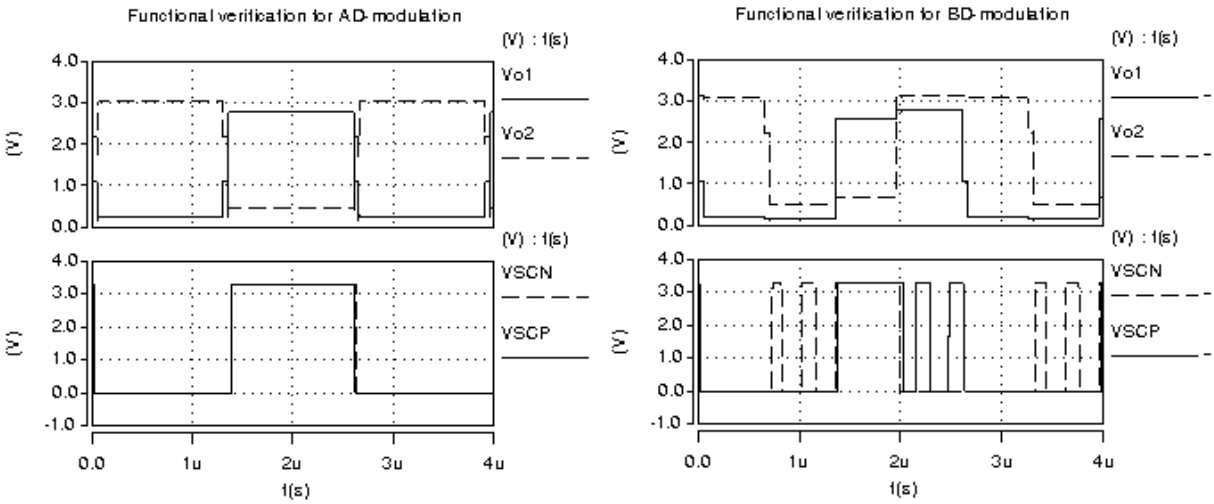


Figure 5-6: Functional verification on transient operation of power stage.

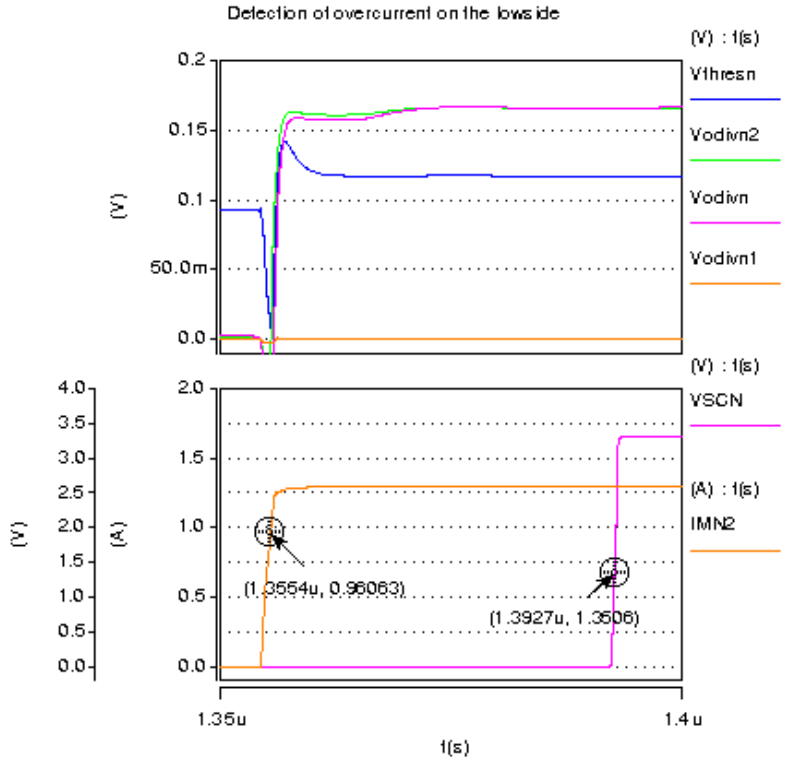


Figure 5-7: Detailed waveforms for lowside overcurrent detection.

For BD-modulation, the power stage also goes through moments of no overcurrent (when V_{O1} is low and V_{O2} is high) and overcurrent on both transistors (for the opposite output

voltages). On top of that, there are overcurrent situations in the moments specific to BD-modulation: when V_{O1} and V_{O2} are both high or both low. Around t=1µs, for example, both M_{N1} and M_{N2} are conducting; M_{N2} is on overcurrent due to R_{SCP}. The overcurrent detection system is watching one arm on each clock period, and so V_{SCN} is toggling with the clock. The analogous situation happens on the highside, starting at t=2µs.

Figure 5-7 shows the transition into overcurrent on the lowside in more detail. The points marked on I_{O1} and V_{SCN} are the ones used for measuring the detection delay. It can be seen that the arm selection logic has V_{ODIVN} following V_{ODIVN2}. The delay caused by the multiplexer's resistance, and the settling time of V_{THRESN} are seen to be negligible relatively to the comparison time of the comparator.

5.2.3 Benchmark Results

The functional simulation was performed on typical conditions, with iscadj<1:0>=01, for all possibilities for active slices and modulation types (AD or BD). The detection delay for BD-modulation is very hard to measure, as it can depend on the phase the clock is when there is an overcurrent event. For that reason, a worst-case value was taken by adding one clock period (162.7 ns, in this case) to the value measured for AD-modulation.

To ascertain the advantage of the proposed configuration over one with 4 comparators, we derive the current savings as a percentage of the classic configuration's consumption.

$$savings = \frac{I_{Comps}}{I_{VDD} + I_{COmps}} \times 100 \quad (\%) \qquad \text{Eq. 5-5}$$

The measured values and the calculated current savings are included in Table 12.

The current consumed by the comparators is observed to fairly constant; the small variations likely have the same cause as the variations in the detection time. The current consumed by the overcurrent system, I_{VDD}, varies much more due to the programmable replica currents I_{RefN} and I_{RefP} (recall Eq. 4-3 and Table 4). The proposed configuration saves up to 38% current when compared to the conventional one.

Table 12: Benchmark results for functional simulation

Modulation type	Active slices	T_{SCLO} (ns)	T_{SCHI} (ns)	I_{VDD} (µA)	I_{Comps} (µA)	Current Savings
AD	1	24.1	29.4	110	68.4	38%
	2	26.5	34.2	140	68.0	33%
	3	30.5	36.4	169	67.6	29%
	4	37.4	38.4	199	67.2	25%
BD	1	179	185	139	68.4	33%
	2	182	189	198	68.0	26%
	3	186	192	257	67.6	21%
	4	193	194	317	67.2	18%

5.3 Layout Simulation

Besides the DRC and LVS verifications, a simulation step is important to validate the layout. To that end, the parasitic capacitances and resistances were extracted from the system's layout, again using the Calibre tool from Mentor Graphics. The resulting netlist was then simulated with the HSPICE tool.

5.3.1 Simulation Description

The testbench used was very similar to the one described in 5.1.1. Besides the ramping down of R_L, a startup of the circuit was performed during the first milisecond of the simulation. The power supply was ramped up from 0 to 3.3V, and then the same was done with the enable (en) digital signal.

Given that the simulated netlist was automatically extracted, it includes a very high number of small components (when compared to directly designed netlists). Besides, the components representing parasitics are defined as ideal discrete components and not using the technology models for physical components (e.g.: ideal resistances instead of "metal" or "poly"), and so the will not necessarily behave correctly in the corners and Monte Carlo simulations. For these reasons, the simulation was only performed for typical conditions.

Due to computing time constraints, the only setup used was the nominal one: 4 active slices, iscadj<1:0>=01.

5.3.2 Evaluated Benchmarks

Given the nature of the extracted netlist it was not possible to measure parameters internal to the system. For that reason, the only evaluated benchmarks were I_{LIMN} and I_{LIMP}, as defined in Table 9.

5.3.3 Benchmark Results

The measured results for the layout simulation are detailed in Table 13. Besides absolute value, the results are shown as a percentage of the schematic simulation (see section 5.1) and as a percentage of the nominal value.

Table 13: Benchmark results for layout simulation

Measure	I_{LIMN}	I_{LIMP}
Absolute value	975.9 mA	799,0 mA
As % of schematic simulation	105,37%	83,49%
As % of nominal value	101,65%	83,22%

The table shows satisfactory values for I_{LIMN}, especially when comparing to the nominal value. The detection for the highside shows much greater error and would merit further investigation.

5.4 Comparison with bibliography

Comparing the results for this system with the ones available in bibliography has proven to be difficult, for two reasons: the scarcity of documented implementations of other systems, and the differences in the target systems between the cases found and this one. Even within the few cases found [3,9,17], most do not give enough information to compare the whole system. Still, a subjective comparison can be made.

Regarding precision, Berkhout [3] states an accuracy of ±10% of nominal threshold current, including spread of reference current, on an “industrial test” of its system. While it’s hard to compare an undetailed “industrial test” with our corners/Monte Carlo analysis, based on corners analysis alone we can say that the system in this work does not fare as well as Berkhout’s; but given a more precise external reference source, precision should be much better (~±5%).

As to settling time, more information is available, though the measurement conditions (e.g. the current when on short-circuit) are probably not the same. Still; Berkhout [3] reports a detection delay 50ns or 75ns (depending on highside or lowside), Guo et. al. [17] report a delay of the comparator alone of 150ns (to their credit, it’s a micropower system), and Feng et. al. [9] report an “overcurrent response time” (i.e. overcurrent detection and actuation) of 50 ns. Again, a strict comparison is impossible to make; we speculate that detection delay in our work is smaller than documented cases for AD-modulation, but becomes higher than the competition if the worst-case for BD-modulation is considered.

Finally, data regarding consumption of the overcurrent detection system was not available on comparable terms.

5.5 Synopsis

The precision of the system was measured and the different sources of error were separated. Improvements to the system with the aim of better precision were proposed. The proper functioning of the system was verified for the two possible types of modulation. The detection delays were determined and their main source was identified. The current savings of this configuration against the conventional one were calculated. A subjective comparison of this system’s performance with similar systems in bibliography was made.

6 Conclusions

6.1 Summary and Conclusions

This work focuses on an overcurrent detection system for BTL Class-D amplifiers. A brief comparison of the possible approaches to overcurrent detection concluded that the threshold-state replica, as detailed in [3], is the most suitable for class-D amplifiers. The precision of this solution was analyzed in more detail, resulting in guidelines for the compromises between the main system parameters that must be determined when designing a particular implementation. A configuration specifically designed for BTL output stages was proposed which avoids the use of two (out of four) comparators, when compared to conventional configurations such as in [18].

The proposed configuration was implemented on a 3.3 V, 0,18 µm CMOS technology, detecting overcurrent on a Class-D power stage with a maximum output power of 1W. Simulations at the transistor level lead to the conclusion that a more thorough design could have allowed better precision. Nevertheless, the proposed architecture was functionally validated. For this particular implementation, current savings (when compared to using four comparators with the conventional configuration) range from 18% percent to 38%, with the only disadvantage being a 155ns added delay in the detection when using BD-modulation. These savings can be even more pronounced in systems where the comparators' current consumption is greater in relation to the other components, as is the case of ultra-low power switched amplifiers such as in [17].

6.2 Future Work

Given the simulation results, the overcurrent detection system designed seems to be a working solution for the class-D amplifier designed for the HEAD project. Still, the author feels that a future iteration of this chip could include a redesign of the overcurrent detection given the precision analysis of Chapter 5. Specifically, the precision obtained is not optimal and could benefit from a better trade-off between design parameters; and deviations of typical results from the nominal value could be fixed. Furthermore, the programmable current source and the external bias current should be refined for fewer variations with corners. It would also be interesting to evaluate the benefits of the stacked replica versus one replica with larger channel length.

At the configuration level, there is the possibility of refining the arm selection logic such that during BD-modulation the overcurrent detection system keeps watching an arm if it is on overcurrent. This change is very simple and could be made in the relevant logic block without requiring much work in adapting other blocks or on layout

Finally, there is the need to validate all this work on a fabricated chip. That will likely happen in the next year within the HEAD project.

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Appendix – Cadence Schematics

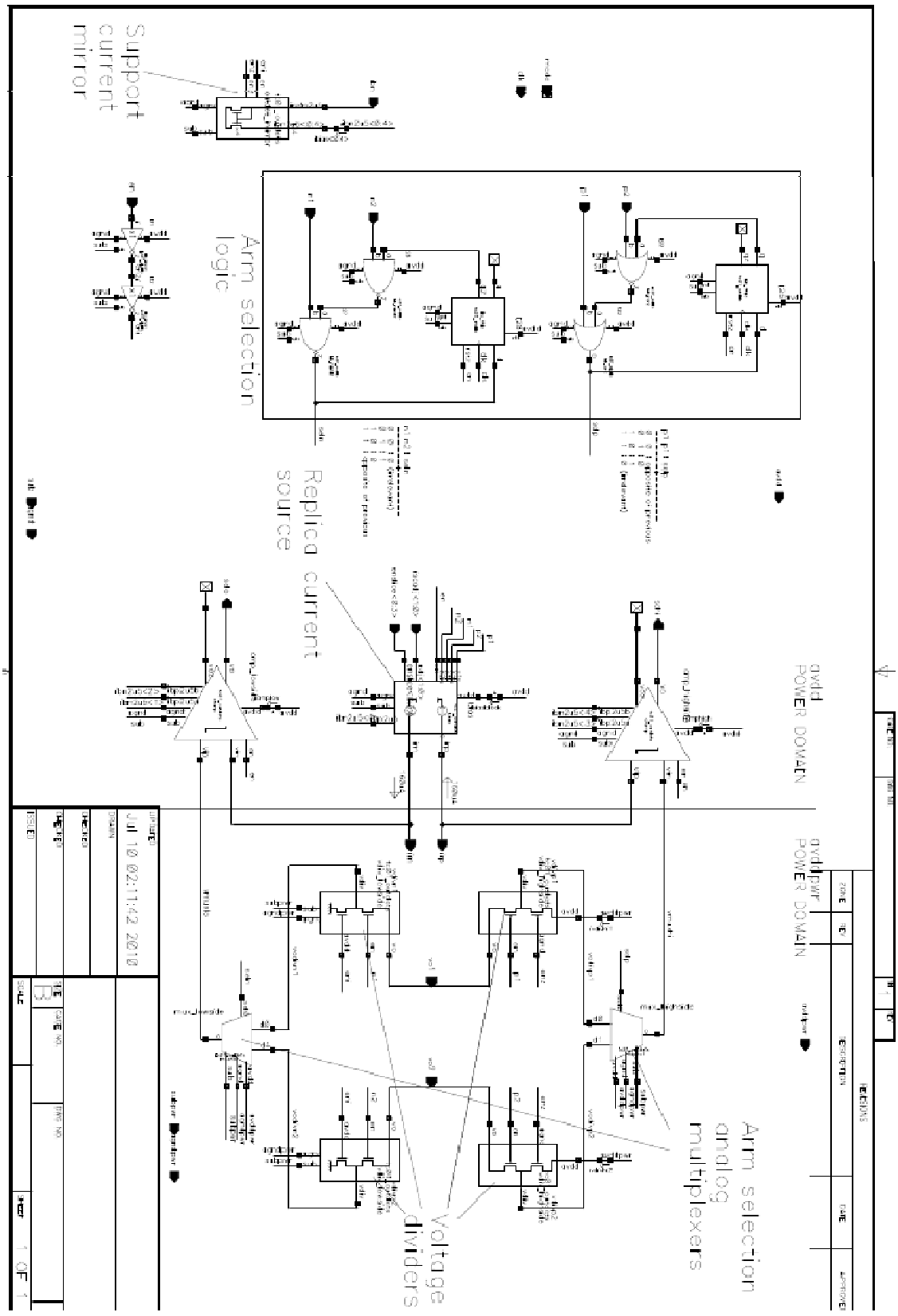

Figure 8: Overcurrent detection system schematic

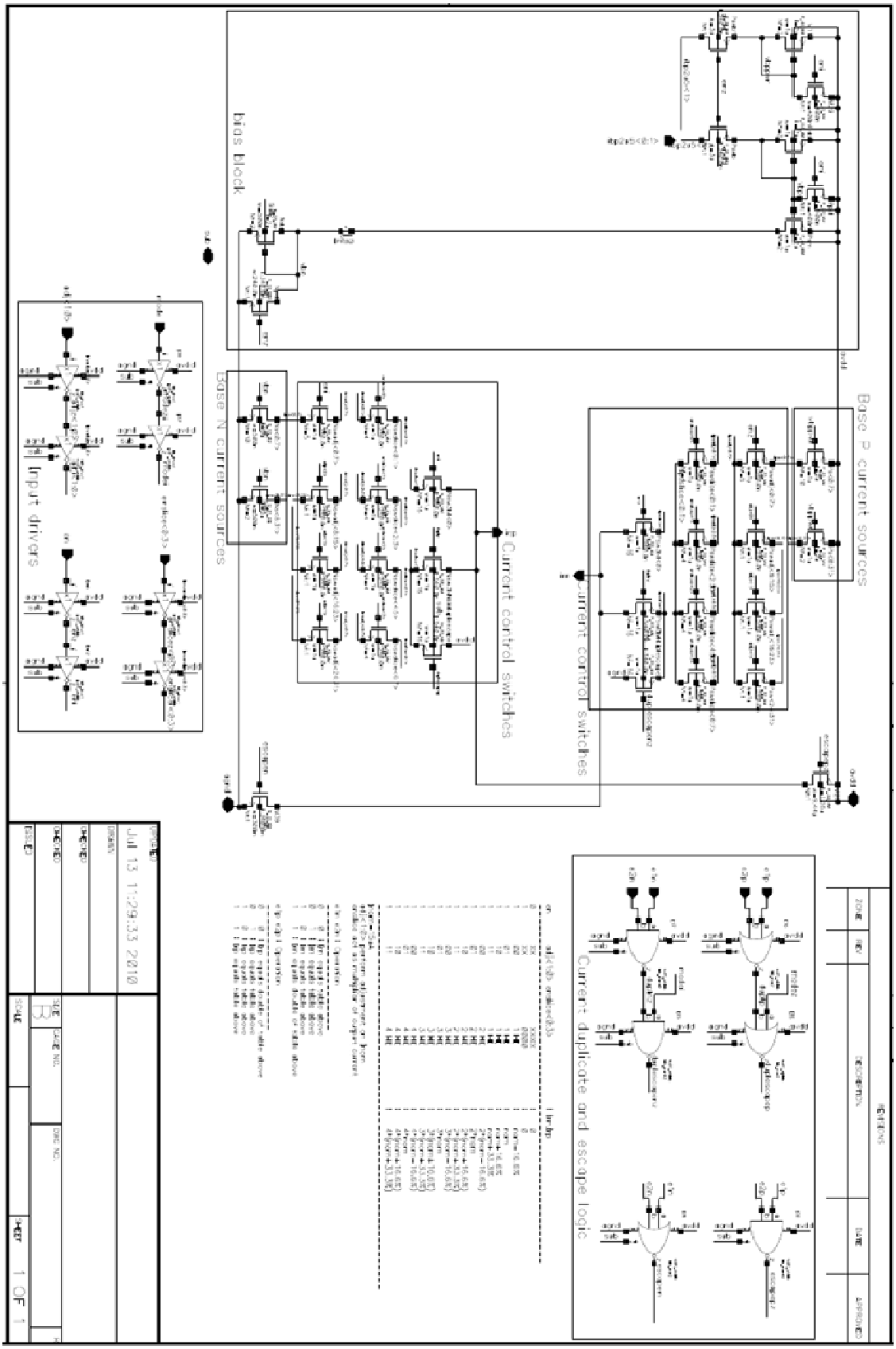

Figure 9: Programmable current sources' schematic

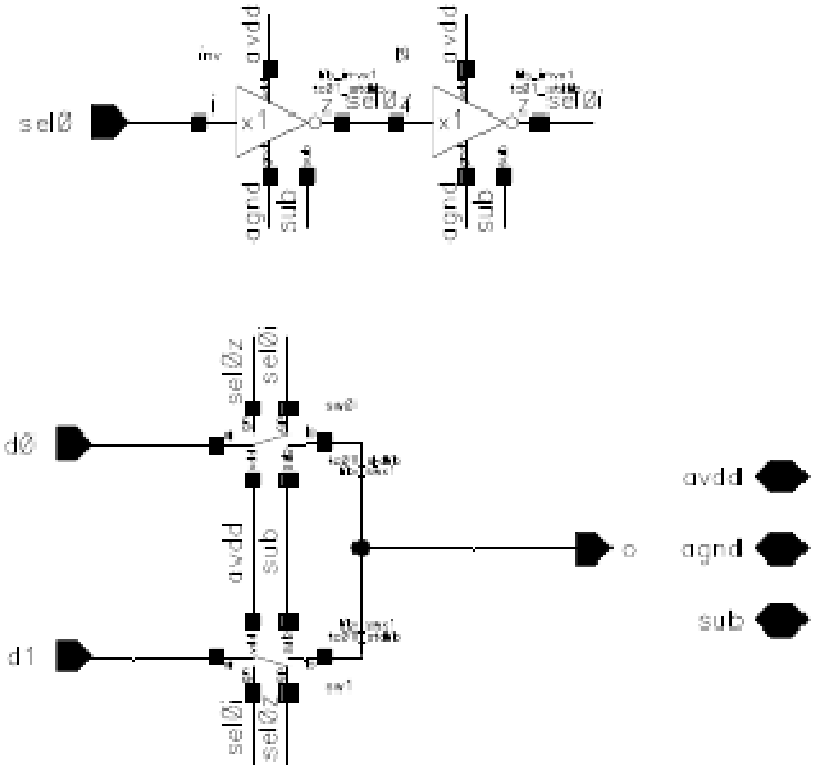

Figure 10: Analog multiplexer's schematic

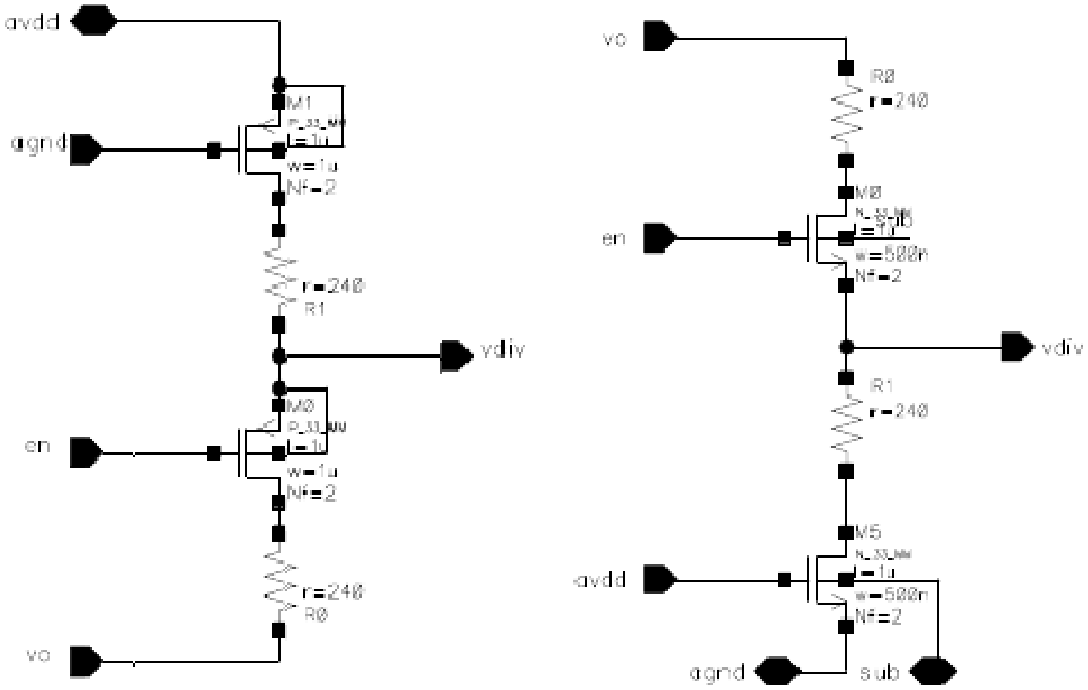

Figure 11: Voltage dividers' schematics

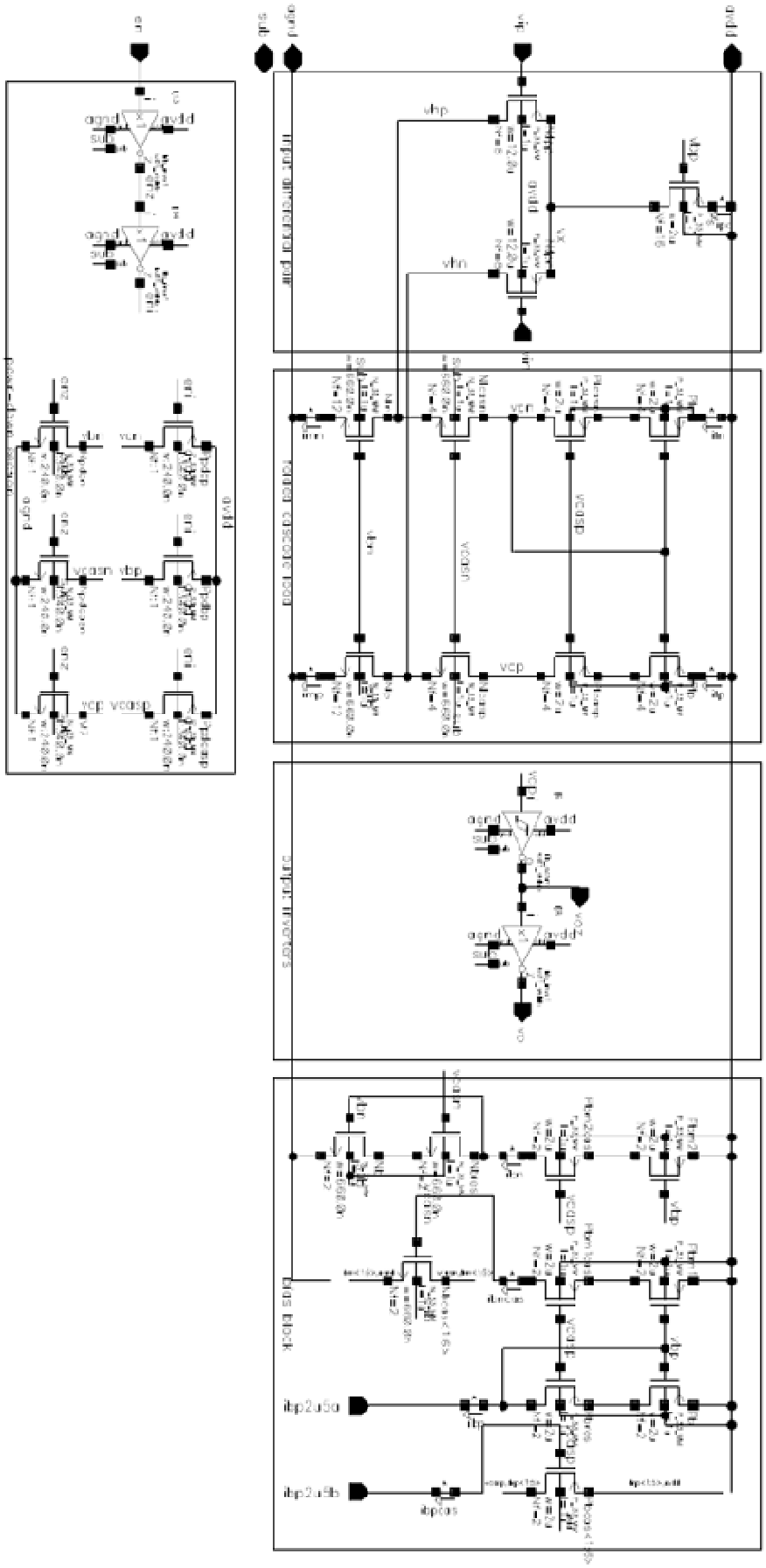

Figure 12: Lowside comparator's schematic

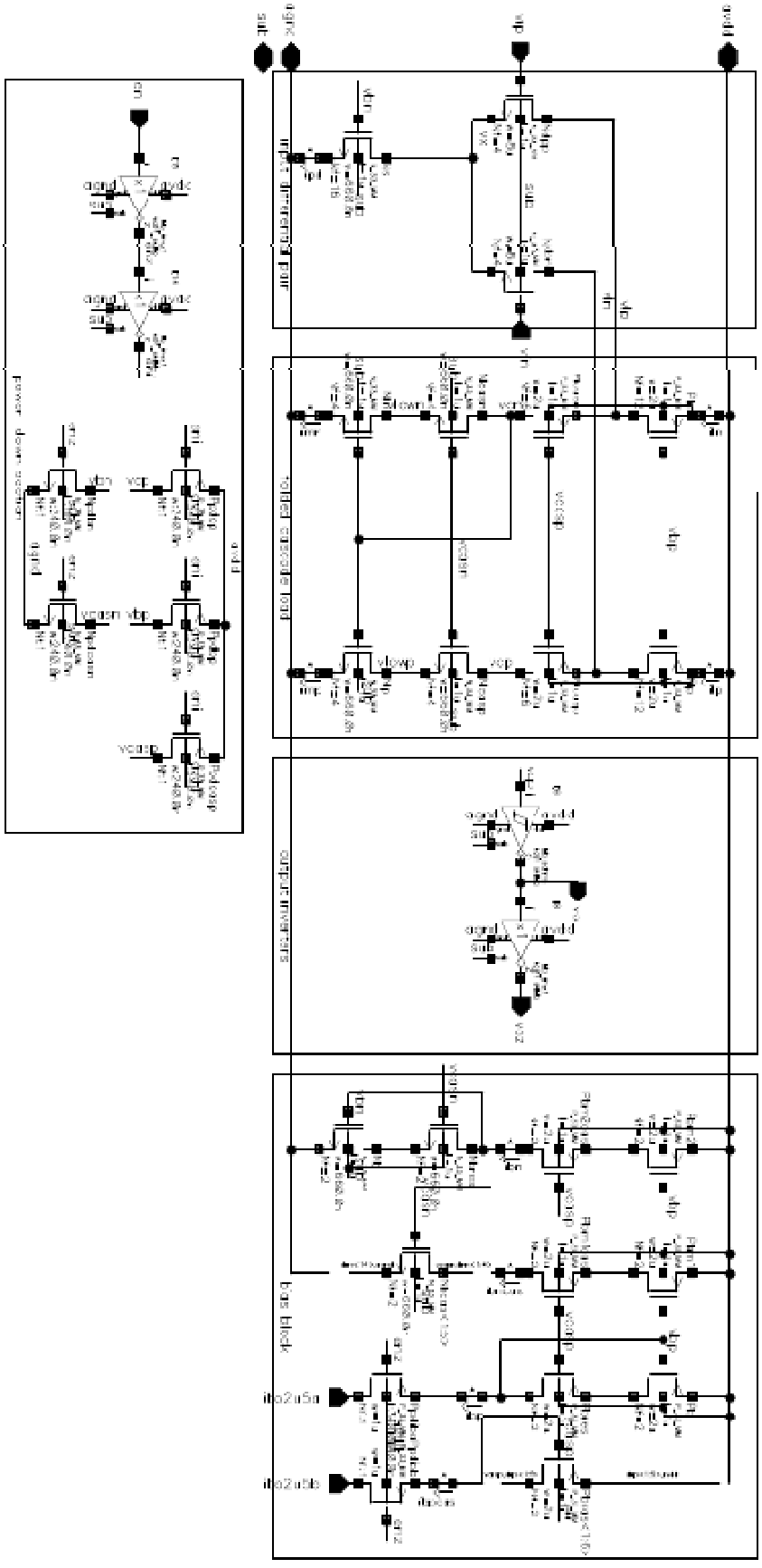

Figure 13: Highside comparator's schematic