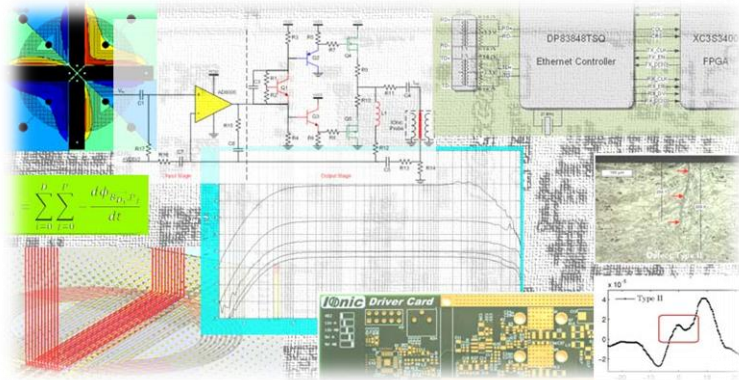




INSTITUTO SUPERIOR TÉCNICO  
Universidade Técnica de Lisboa



## Non-Destructive Testing Based on Eddy Currents

*Detector de Falhas em Soldaduras*

**Luís Filipe Soldado Granadeiro Rosado**

Master's Degree Dissertation in  
Electronics Engineering

President:	Prof. Maria Beatriz Mendes Batalha Vieira Vieira Borges
Supervisor:	Prof. Moisés Simões Piedade
Co-supervisor:	Prof. Pedro Miguel Pinto Ramos
Member:	Prof. Leonel Augusto Pires Seabra de Sousa
Member:	Prof. Mário Ventim Neves

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# Abstract

Non-destructive testing plays a crucial role in quality management and on ensuring safety of use to a broad range of industrial components especially in aerospace, power generation, automotive, railway and petrochemical applications. From the several non-destructive testing methods, eddy currents evaluation is the preferred method to inspect metallic parts and welding joints searching for flaws and other material discontinuities. Eddy currents evaluation is based on the generation and analysis of electrical currents through the test material.

Friction stir welding is a solid-state joining process executed without any material addition and at lower temperatures than the fusion temperature of the involved materials. This process leads to lower joint distortions and residual tensions together with excellent mechanical properties. Friction stir welding is seen as a great potential technology but the actual technological state on non-destructive testing isn't able to ensure the detection of defects with structural influence. This work studies a new concept of eddy currents probe by analytical and finite element models together with their experimental validation. This new IOnic probe and a preliminary version of a non-destructive testing system were used to inspect friction stir welds on industrial conditions detecting superficial defects about 60  $\mu\text{m}$  deep.

To extract the maximum advantage from the new probe concept, a tailor-made non-destructive testing system was developed. This new system has a Field Programmable Gate Array based processing core enabling the digital generation and analysis of the probe signals through multiple digital signal processing algorithms. Communication with personal computers is ensured by Ethernet 10/100 or USB 2.0 High Speed interfaces. The proposed system architecture enables to set several combinations of peripherals cards to generate or acquire probe signals. Two different peripheral cards have been developed to interface the IOnic probes. Signal acquisition is guaranteed by a programmable gain amplifier and an analog to digital converter while the signal generation is made through a digital to analog converter and a high output current transconductance amplifier. Together, the two peripherals cards are able to operate the probe within the frequency range from 10 kHz up to 10 MHz.

## Keywords

Non-Destructive Testing, Eddy Currents, Planar Probe, Field Programmable Gate Array, Digital Signal Processing.

# Resumo

O ensaio não destrutivo tem um papel crucial no processo de gestão da qualidade bem como em garantir segurança de utilização a uma vasta gama de componentes para aplicações aeroespaciais, geração de energia, transportes rodoviário e ferroviário e nas indústrias química e petrolífera. Dos vários métodos de análise não destrutiva, o ensaio por correntes induzidas (*eddy currents*) é o preferido para inspeccionar componentes metálicos e soldaduras, localizando defeitos e outras discontinuidades materiais. O ensaio por correntes induzidas baseia-se na geração e análise de correntes eléctricas no material a testar.

A soldadura por fricção linear é um processo de ligação no estado sólido levado a cabo sem qualquer adição de material e a temperaturas abaixo das temperaturas de fusão dos materiais envolvidos. Por este processo, é possível obter juntas com uma baixa distorção e baixas tensões residuais e ao mesmo tempo com excelentes características mecânicas. Apesar do seu potencial, o estado actual em matérias de controlo não destrutivo não permite a detecção de defeitos com influência estrutural relevante nas juntas obtidas por este método. Este trabalho estuda um novo conceito de sonda de correntes induzidas através da sua modelação analítica e por elementos finitos bem como através de validação experimental. A nova sonda IOnic em conjunto com um sistema preliminar de ensaios não destrutivo, foram utilizados na inspecção de juntas obtidas pelo processo de fricção linear em condições industriais detectando defeitos superficiais com cerca de 60 µm de profundidade.

Para extrair a máxima performance do novo conceito de sonda, um sistema de ensaio não destrutivo foi especialmente projectado. Este novo sistema possui um núcleo de processamento baseado num dispositivo de lógica programável permitindo a geração e análise dos sinais na sonda através de múltiplos algoritmos de processamento digital de sinal. A comunicação com computadores pessoais é assegurada pelas interfaces Ethernet 10/100 e USB 2.0 *High Speed*. A arquitectura do sistema proposto permite a configuração de múltiplas combinações de periféricos para geração e aquisição dos sinais na sonda. A aquisição de sinais é garantida por um amplificador de ganho programável e um conversor analógico-digital enquanto que a geração de sinais é conseguida através de um conversor digital-analógico e um amplificador de transcondutância com elevada corrente de saída. Em conjunto, os dois periféricos mostraram-se adequados para operar a sonda na gama de frequências desde 10 kHz a 10 MHz.

## Palavras-chave

Ensaio não destrutivo, Correntes Induzidas, Sonda planar, Dispositivo de Lógica Programável, Processamento Digital de sinal.

# Acronyms

<b>ADC</b>	Analog to Digital Converter
<b>ALU</b>	Arithmetic Logic Unit
<b>ASIC</b>	Application-Specific Integrated Circuit
<b>ATX</b>	Advanced Technology Extended
<b>CAD</b>	Computer Aided Design
<b>DAC</b>	Digital to Analog Converter
<b>DFT</b>	Discrete Fourier Transform
<b>DIL</b>	Dual In-Line
<b>DSP</b>	Digital Signal Processing
<b>ENOB</b>	Effective Number of Bits
<b>FEM</b>	Finite Element Modeling
<b>FIFO</b>	First In First Out
<b>FPGA</b>	Field Programmable Gate Array
<b>FR4</b>	Flame Retardant 4
<b>FSW</b>	Friction Stir Welding
<b>GBW</b>	Gain-Bandwidth Product
<b>GMI</b>	Giant Magneto Impedance
<b>GMR</b>	Giant Magneto Resistance
<b>I<sup>2</sup>C</b>	Inter-Integrated Circuit
<b>IEEE</b>	Institute of Electrical and Electronics Engineers
<b>IO</b>	Input/Output
<b>IP</b>	Intellectual Property
<b>JTAG</b>	Joint Test Action Group
<b>LAN</b>	Local Area Networks
<b>LED</b>	Light Emitting Diode
<b>LVDS</b>	Low Voltage Differential Signaling
<b>MAC</b>	Media Access Controller
<b>MII</b>	Media Independent Interface
<b>MOSFET</b>	Metal Oxide Semiconductor Field Electric Transistor
<b>MSPS</b>	Mega Samples per Second
<b>MWM</b>	Meandering Winding Magnetometer
<b>NCO</b>	Numerically Controlled Oscillator
<b>NDT</b>	Non-Destructive Testing
<b>OPAMP</b>	Operational Amplifier
<b>PCB</b>	Printed Circuit Board
<b>PDN</b>	Power Distribution Network
<b>PGA</b>	Programmable Gain Amplifier

<b>PLB</b>	Peripheral Local Bus
<b>POR</b>	Power On Reset
<b>RAM</b>	Random-Access Memory
<b>RISC</b>	Reduced Instruction Set Computer
<b>ROM</b>	Read Only Memory
<b>SIMM</b>	Single In-Line Memory Module
<b>SPI</b>	Serial Peripheral Interface
<b>SQUID</b>	Superconducting Quantum Interference Devices
<b>THD</b>	Total Harmonic Distortion
<b>USB</b>	Universal Serial Bus
<b>VBE</b>	Voltage Base to Emitter

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*Luis Barroso*



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# Chapter 1 – Introduction

## 1.1 Purpose and motivation

Non-Destructive Testing (NDT) comprise the techniques that are based on the application of physical principles employed for the purpose of determining the characteristics of materials and for detecting and assessing the flaws and harmful defects without any change on their usefulness or serviceability [1]. These techniques concern all aspects of material characterization, their microstructure, texture, morphology, and physical and chemical properties [2]. NDT has gained in importance as a result of the rapid technological progress made during the past half-century and is considered today one of the fastest growing technologies.

NDT plays a crucial role in ensuring cost effective operation, safety of use and reliability of a wide range of industrial components especially on aerospace, power generation, automotive, railway and petrochemical applications. Although NDT was originally intended to be applied only for human safety reasons, nowadays, it is widely accepted as a cost saving technique in the quality assurance process performed by almost all manufacturing companies.

There is a broad range of NDT methods based on different physical principles but the most commonly used are ultra-sonic, eddy currents evaluation, X-radiography, magnetic particles inspection and dye penetrant application [3]. The choice between these methods should take in account safety, economic and efficiency issues. Eddy currents evaluation is the preferred NDT method for superficial and internal flaws detection on conducting materials especially on metal welding applications. Eddy currents evaluation is based on electromagnetic induction and analysis of electrical currents on conductive materials. This method is used for thickness measurements, corrosion evaluation, electrical conductivity measurements, magnetic permeability measurements and flaw detection. The principal advantages on using this technology are that surface preparation is minimal and it is a quite intuitive method, setting aside the need for highly qualified personnel.

The development of new welding and joining processes leads to a constant demand on improved NDT techniques. In fact, the quality assessment of Friction Stir Welding (FSW) remains an actual paradigm on NDT technology. As an example, the defects created on friction stir welds are characterized by no physical material discontinuities with very low size and low energy reflection effect leading to increased difficulties in their detection [4]. In order to increase the defects detection on such applications, a new type of eddy currents probe was designed and patented [5].

The new IONic probe is based on an entirely new concept and allows enhanced probe lift-off immunity and improved sensitivity for micro size defects. To extract the maximum advantage from this new technology it is essential the study of its operation theory together with the development of a tailor-made electronic system featuring the digital generation and processing of the probe signals.

## 1.2 Goals and challenges

The main goal of this work is to build a NDT system based on the new IOnic probes. To accomplish this task, three key objectives have been established:

- Study the IOnic probe operation theory with Finite Element Modeling (FEM) and experimental validation;
- Build a digital signal processing system to use together with the new probe. This new system features a Field Programmable Gate Array (FPGA) processing core, communication interfaces and conversion devices attached to analog electronics to interface the probe;
- Design an embedded software application to control the signal generation and acquisition of the probe signals. The application should communicate with a personal computer to exchange characterization parameters and data.

The central challenge is to design high speed analog, data conversion and digital processing electronic to handle the IOnic probe. Driving the probe along a wide range of frequencies will permit to extract maximum information about the defects presence, thus the target frequency operation range for probe stimulus was set from 10 kHz to 10 MHz.

## 1.3 Document organization

Chapter 2 includes an overview on eddy currents evaluation covering the associated physical phenomenon, applications and the state-of-the-art on this topic. Some considerations on FSW process are presented. The purpose of this chapter is to transmit to the reader an essential background to understand the next content.

On the third chapter, the innovative concept of IOnic probe and their electromagnetic simulation using a FEM analysis tool is presented. Further content on this chapter describes the design and application of a preliminary version of the NDT system used for the experimental validation of the IOnic design. Results on inspecting FSW specimens are included highlighting the potential of the probe on such application.

Chapter 4 introduces a new approach to handle the probes. This new system addresses the Digital Signal Processing (DSP) of the probe signals, in order to overcome the limitations found in the first approach. Emphasis is given to the analog electronics designed to interface the probe including their dynamic characterization results.

In Chapter 5, an embedded software application designed to the new system is presented. Some considerations about their architecture are discussed and the design of the application cores is described.

Finally, some conclusions about the achieved results and future work suggestions are presented in Chapter 6.

# Chapter 2 – Eddy currents evaluation overview

## 2.1 Introduction

Even though the validation of eddy currents physical principle enunciated by Faraday dates back to 1851 when Jean Bernard Léon Foucault demonstrated that electrical currents are set up in a copper disk moving in a inhomogeneous magnetic field, the first recorded eddy currents test was performed in 1879 by Hughes [6]. At that time, Hughes was able to distinguish the difference between some metals by registering the coil inductance variation when approaching the metals to the coil. On 1926, the first eddy currents based instrument with the ability to measure metal thickness was developed. Through World War II and the early 1940s, further developments resulted in better and more practical eddy currents instruments. The principal discoveries, observations and explanations of eddy currents phenomenon are listed on Table 2.1.

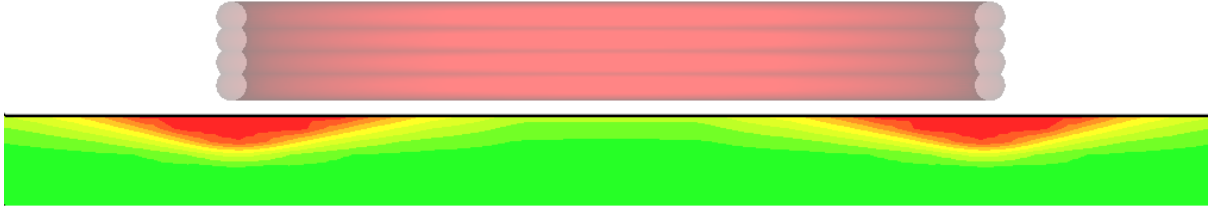
**Table 2.1** - Historical outline of eddy currents evaluation.

Individual	Year	Description
H.C. Oersted	1819	Change of electric current affected a magnet
W. Sturgeon	1823	Copper wire around a horseshoe produced an electromagnet
Gamby	1824	Oscillations of suspended bar magnet damped by presence of metal plate
M. Faraday	1832	Law of electromagnetic induction
J. B.Foucault	1851	Demonstrated existence of eddy currents
D.E. Hughes	1879	Electric pulses from a microphone coil to induce eddy currents in metals
F. Krantz	1920	Eddy currents thickness measurements
C. Farrow	1926	Eddy currents inspection of steel tubes on an industrial scale
Reutlingen Institute, Germany	1948	Development of eddy currents instrumentation
F. Förster	1952	Impedance plane diagrams

Recently, a confluence of developments in the fields of electronics, computer technology, simulation tools and signal processing is contributing to exciting developments and unprecedented performance on eddy currents evaluation [7].

## 2.2 Conventional eddy currents evaluation

An alternating current made to flow in a coil produces an alternating magnetic field around it. This coil, when brought close to the surface of a metallic material, induces an eddy current in the material due to electromagnetic induction generally parallel to the coil winding, Figure 2.1. These eddy currents, in turn, will change the magnetic field disposition. This alteration may be detected either with a magnetic field sensitive sensor or by the change in the original coil impedance.



**Figure 2.1** - Eddy currents density generated by a coil, sectional view.

### 2.2.1 Eddy currents phenomenon

Eddy currents phenomenon can be explained using Maxwell equations. The involved electromagnetic relations are

$$\oint_S \vec{H} d\vec{l} = I_S + \frac{d\phi_{\vec{D},S}}{dt}, \quad \vec{D} = \epsilon \vec{E} \quad (2.1)$$

$$\oint_P \vec{E} d\vec{l} = -\frac{d\phi_{\vec{B},P}}{dt}, \quad \vec{B} = \mu \vec{H}. \quad (2.2)$$

Assuming a one loop coil called  $L$  close to a metallic material, and  $S$  an orthogonal and concentric surface around the coil, and that the frequency is low enough to discard the displacement current term in (2.1), the magnetic field lines around  $L$  are governed by

$$\oint_S \vec{H} d\vec{l} = I_L. \quad (2.3)$$

Now, considering  $P$  as a surface defined on the material and  $dA$  their area element, the magnetic flux through  $P$  is given by

$$\phi_{\vec{B},P} = \int_P B dA, \quad B = \mu H \quad (2.4)$$

and the induced electromotive force

$$\oint_{\partial P} \vec{E} d\vec{l} = -\frac{d\phi_{\vec{B},P}}{dt}. \quad (2.5)$$

By finding a conductive path, this electromotive force creates eddy currents in the test material.

### 2.2.2 Depth of penetration

The importance of the magnetic field frequency is that it determines eddy currents depth of penetration in the material. Electric current density decreases exponentially from the material surface with rate determined by frequency, electrical conductivity and magnetic permeability [8]. For a given frequency  $f$  the eddy currents density at depth  $x$  is

$$J_x = J_0 e^{-x(\pi f \mu_0 \mu_r \sigma)^{1/2}} \quad (2.6)$$

where  $J_0$  is the superficial current density,  $\mu_0$  the free space magnetic permeability expressed in H/m,  $\mu_r$  the material relative magnetic permeability and  $\sigma$  the material electrical conductivity expressed in S/m.

The standard depth of penetration is defined as the point where the electric current density has decreased by the factor of  $1/e \approx 36.8\%$  [9] and can be determined by

$$\delta = \frac{1}{\sqrt{\pi f \mu_0 \mu_r \sigma}}. \quad (2.7)$$

By reducing the test frequency, it is possible to achieve higher penetration depths. However, this will also reduce the superficial current density. The chart on Figure 2.2 shows the different standard penetration depths as a function of frequency for aluminum.

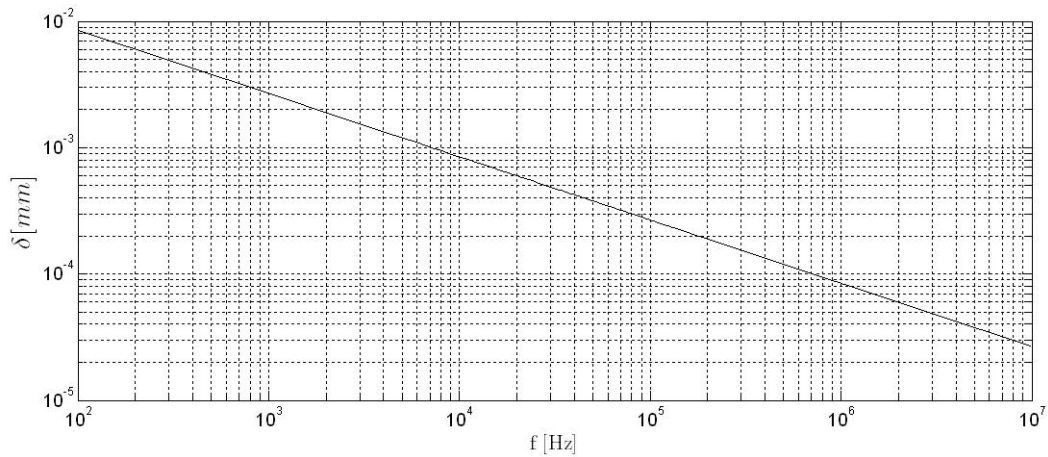


Figure 2.2 - Standard depth of penetration for aluminum ( $\mu_0 = 1.000022$  and  $\sigma = 3.54 \times 10^7$ ).

### 2.2.3 Impedance plane

Eddy currents are mainly affected by electrical conductivity, magnetic permeability, geometry of the material, test frequency and the distance between coil and material (also known as lift-off). Furthermore, flaws and other material discontinuities modify the eddy currents so that the magnetic field disposition is altered.

Measuring the coil impedance provides information about eddy currents disposition and intensity on the material. Impedance planes allow an easy interpretation of inspection results based on comprehensive changes. Figure 2.3 shows an impedance plane and the effect of different sources perturbations.

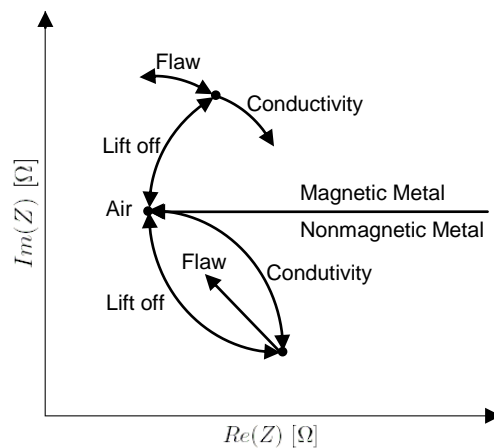


Figure 2.3 - Impedance plane analysis.

When the coil is moved from air to a nonferromagnetic metal, the real component of the impedance will increase as the generation of eddy currents will take energy from the coil. This happens because the material is not a perfect conductor. Furthermore, eddy currents affect the magnetic field through the coil by reducing it and consequently the imaginary part of the impedance. If a flaw is present in the material, fewer eddy currents will be able to form increasing the imaginary part and decreasing the real part.

If the coil is placed on a ferromagnetic metal something different happens. Like with nonferromagnetics, because of the material resistivity, eddy currents will be wasting some energy from the coil, increasing the impedance real component. However the imaginary part increases as the field strength is augmented by the presence of such materials.

#### **2.2.4 Eddy currents probes**

There are several types of eddy currents probes and each one is adjusted to a special evaluation purpose. Although there isn't a rigid probe classification, based on their operating mode is possible to define some usual arrangements:

- Absolute mode probes, devices containing a single coil that is used to generate eddy currents and sense changes in the magnetic field. They can be used for defects detection, and for conductivity and thickness measurements;
- Differential mode probes have two active coils usually wounded in opposition. When the two coils are over a defect-free material area, there is no signal developed between the coils since the common mode contribution is canceled. However, when only one coil is over a defect, the signal developed between the two coils increases. These probes are very sensitive to defects yet insensitive to unwanted variations. There are also disadvantages on using this type of probes, especially the difficult on the output signal interpretation;
- Reflection probes employ one coil for eddy currents dissemination and another to sense the magnetic field among the material. This arrangement is often referred to as driver/pickup and allows to independently optimizing each coil for their intended purpose. The driver coil can be wounded to produce a strong and uniform flux field, while the pickup coil can be made very small in order to increase their sensibility to small defects;
- A hybrid probe makes use of a coil to disseminate eddy currents but uses a different type of magnetic sensitive element to detect changes in the material. Hall Effect and Giant Magneto Resistance (GMR) sensors are the most commonly used.

Eddy currents probes can be made helicoidally or on a planar disposition. Planar probes provide a better contact with the material and can be flexible, allowing the inspection of complex geometry surfaces. Probe shielding can be added to reduce the interaction of the generated magnetic field with non relevant structures near the probe. Also, ferrite cores can be used as magnetic flux concentrators leading to more sensitive probes.

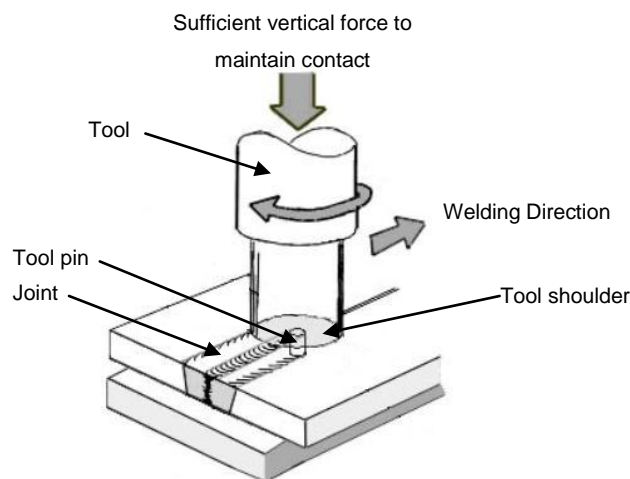
### 2.2.5 Advantages of eddy currents evaluation

There are some advantages on using eddy currents for NDT purposes:

- Quick, simple, and reliable inspection technique to detect surface and near-surface defects;
- It can be used to perform several tasks like thickness measurements, corrosion valuation electrical and magnetic permeability measurements;
- There is no need for consumables and the inspection surface preparation is minimal;
- Results are drawn immediately. Equipment can be made very portable;
- It is well suited for inspecting complex part geometries;
- Personal skills and training are low, it is a very intuitive evaluation method;
- Can be easily automated and included in production lines.

## 2.3 Friction Stir Welding: A challenge on NDT

FSW is a solid-state joining process patented by The Welding Institute UK in 1991 [10]. There is a huge potential on using this technology and it is considered the main advance on joining technology during the last decade [11]. FSW is performed without any filler material or gas protection and at lower temperatures than the fusion temperature of the involved materials, leading to a low level of joint distortion and residual tensions. In FSW, a non-consumable cylindrical tool is rotated at a constant speed through a joint line involving the work pieces to be joined which are overlapped or butted together, Figure 2.4. The pieces to be joined should be rigidly fixed to avoid their separation during the welding process.

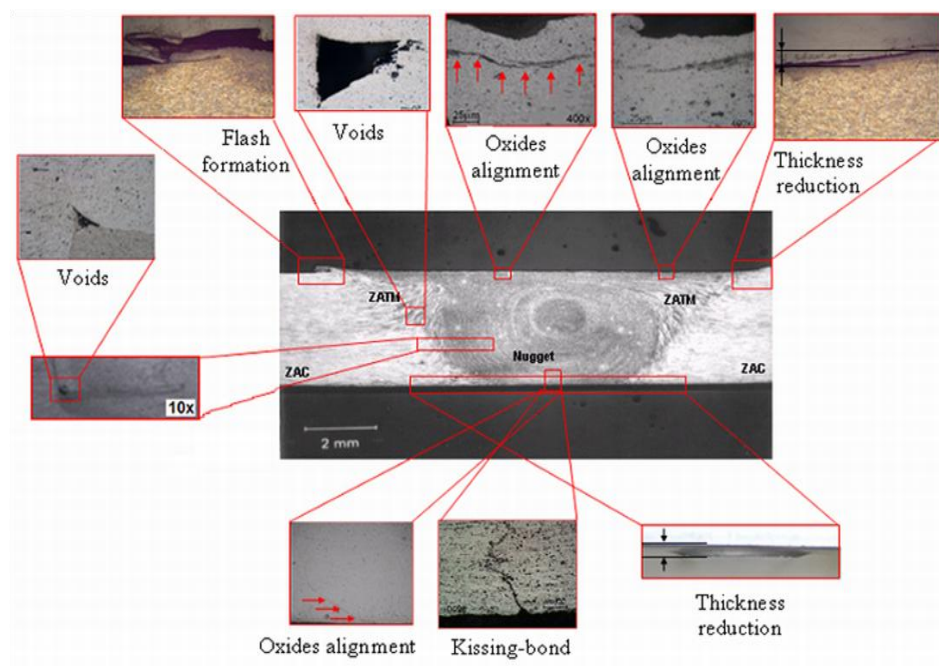


**Figure 2.4** - FSW process [12].

The tool pin length should be slightly less than the weld depth required and the tool shoulder should be in intimate contact with the work surface. Frictional heat is generated both internally by viscous dissipation and at the interfaces between the tool and the material of the work pieces. This heat causes the materials to soften without reaching the melting point, entering the plastic domain. As the tool is moved in the welding direction, its leading face forces plasticized material to flow back,

mainly around the retreating side, while applying a substantial force to consolidate the weld. FSW is based on severe plastic deformation in the solid state, involving the material crystal reconstruction.

There are several welding parameters that influence the final weld quality, namely: vertical force, rotation speed, travel speed, tool geometry and tilt angle between the tool and welding materials. The right choice and application of the welding parameters will result in good welds. Nevertheless, under industrial production some defects may arise. Defects on FSW are very different from fusion weld typical defects and can have different origins, morphologies and sizes. Figure 2.5 shows the variety of defects that can be found on a FSW weld bead. In addition, there are conductivity changes that result from FSW process itself, even in a non-defective weld bead.



**Figure 2.5** - Sectional view of a friction stir weld bead and their possible defects [13].

Friction stir welding can use purpose-designed equipment or modified existing machine tool technology. The process is also suitable for automation and adaptable for robot use. Other advantages are:

- Low mechanical distortion and excellent mechanical properties as proven by fatigue, tensile and bend tests;
- Energy efficient;
- Almost non-consumable tool;
- No grinding, brushing or pickling and excellent reproducibility make FSW suitable for mass production industry.

FSW has been applied in a broad range of applications like shipbuilding, aerospace, railway and others. However, FSW consolidation and application requires NDT procedures which the current development state does not allow to detect defects with influence over the structural performance of the weld beads [14].

## 2.4 State-of-the-art

The main field of investigation on eddy currents evaluation relies on the development of new probes. Nevertheless, there are many works on the study of the electromagnetic phenomenon behind eddy currents and on the optimization of conventional probes.

In [15], the application of a FEM analysis with mesh refinement and error estimation to a conventional eddy currents probe is reported. Different error estimation criteria were defined and used to define the mesh refinement zone. Results include a convergence study for each criteria and the coil impedance calculation. In [16] the use of FEM to study the influence of several probe structural parameters over their linearity and sensibility is reported. An interesting work on the modeling of conventional eddy currents probes is shown in [17] where a genetic algorithm together with FEM are used to optimize the coil shape.

The electromagnetic induction in a coil is caused by changes on the magnetic field, thus, coils have less sensitivity at low frequency. The inspection of deep flaws is improved at low frequencies, creating the need for magnetic field sensors with frequency independent sensitivity. Hybrid probes with different magnetic field sensors are being developed. The use of Superconducting Quantum Interference Devices (SQUID) for analyzing eddy currents induced on the material is reported in [18]. In [19], an Hall Effect sensor together with a flat coil for eddy currents generation were used. In [20], the use of GMR sensors detecting flaws at 1.6 mm deep is reported. The employment of Giant Magneto Impedance (GMI) sensors for eddy currents testing is described in [21].

Due to the advantages on manufacturing and operating, planar probes are seen as promising for NDT. Meandering Winding Magnetometer (MWM) patented technology [22] is based on a driver/pickup arrangement where the driver element generates a magnetic field over a mesh of pickup coils. The entire probe is manufactured on a flexible substrate. Results on using this technology are presented in [23] and [24]. In [25], coils etched on thin Kapton film were used to inspect complex geometry surfaces. A comparison study between planar probes and the presentation of the first IOnic probe version are available in [26].

Pulsed eddy currents analysis is based on a different mode for stimulus generation. With this technique, a broadband pulse is applied as excitation and the transient response is analyzed. There is a big effort on this theme and new probes are been designed to improve this concept [27][28][29].

DSP techniques are being applied to extract the magnetic field information from raw voltage data. A good study on this theme is [30] where a DSP algorithm was used to improve the overall NDT system performance.

The use of personal computers in eddy currents evaluation supports complex analysis algorithms and provides powerful visualization modes. In [31] a commercial system based on a laptop computer is described and tested. Other researchers are using neural network analysis and pattern recognition to flaw reconstruction and classification [32][33].

## **2.5 Summary**

In this chapter an overview about eddy currents NDT was discussed. Some basic concepts were introduced and the electromagnetic phenomenon behind eddy currents was described. Different types of probes were analyzed and some considerations on interpreting their behavior were registered. The state-of-the-art of eddy currents evaluation was presented in order to better understand the scope of this work. FSW joining process was described underlining the advantages resulting from its applicability and the increased difficulties regarding NDT techniques applied to FSW.

# Chapter 3 – IOnic Probe

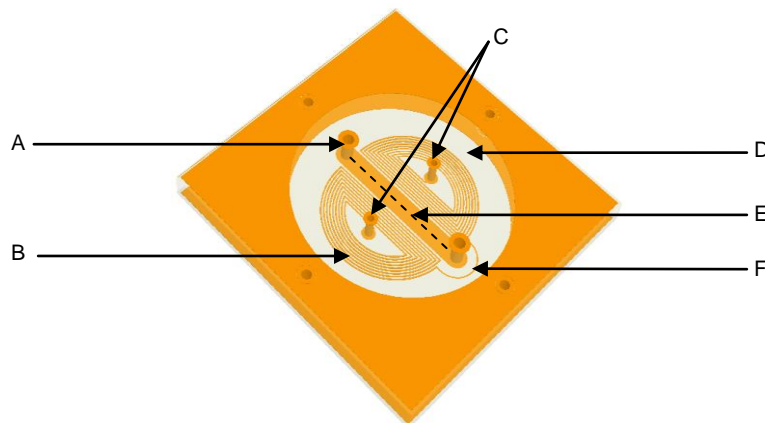
## 3.1 Introduction

IOnic is an emerging concept of eddy currents probe. This technology was patented in 2008 by a researchers group of IST [5] and their name is inspired on the likeness between the probe appearance and a Greek Ionic order column. This concept introduces a new approach to induce and sense the eddy currents in the material.

Along this chapter the morphology and operation theory of the IOnic probe will be discussed. The electromagnetic phenomena related with the probe operation theory will be described and analyzed making use of electromagnetism classic examples and FEM. After this initial content, some advantages of the IOnic concept when compared with conventional eddy currents probes will be presented. The design of a preliminary NDT system used in the probe experimental validation and its appliance to FSW it is reported. Finally, concept variations planned to overcome some of the probe limitations are presented at the end of the chapter.

## 3.2 Probe morphology and operation theory

IOnic probe morphology exhibits a driver/pickup arrangement and at the same time, a differential based operation. The driver element is a copper trace placed in the middle of two pickup planar coils wired on opposite directions as shown in Figure 3.1.

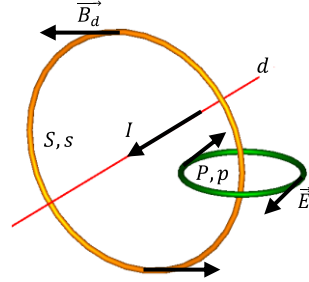


**Figure 3.1** - IOnic probe tri-dimensional view. A) Driver trace, B) Pickup coil  
C) Pickup coils output terminals, D) Substrate, E) Symmetry axis, F) Pickup coils common terminal.

When an alternate current is made to flow in the driver trace, the lines of the generated magnetic field are orthogonal and concentric around it. This magnetic field induces eddy currents on the material and at same time is sensed on the pickup coils as electromotive force. By being symmetrical and sharing a common terminal, the pickup coils form a differential magnetic field sensor. In the presence of any perturbation that could modify the symmetry of the magnetic field among the axis on Figure 3.1, a signal is created between the pickup coils output terminals.

### 3.2.1 Electromagnetic Phenomena

A good approach to understand how the magnetic stimuli are created and their response is sensed is to study an infinite, straight and current carrying wire. Figure 3.2 represent the infinite length wire  $d$  in where an electric current  $I$  is flowing. In a cross section like  $S$ , the magnetic field  $\vec{B}_d$  is tangent and uniform along their boundary circle  $s$ .



**Figure 3.2** - Electromagnetic relations on an infinite, straight and current carrying wire.

Assuming a quasi-stationary condition, the magnetic field intensity for the successive  $s$  radius,  $r$ , is given by

$$B_d = \frac{\mu I}{2\pi r} \quad (3.1)$$

where  $\mu$  is the magnetic permeability of the medium around the wire. Considering the surface  $P$  orthogonal to the circle  $s$  and  $dA$  their area element, the magnetic flux through  $P$  is defined as

$$\phi_{\vec{B}_d, P} = \int_P B_d dA. \quad (3.2)$$

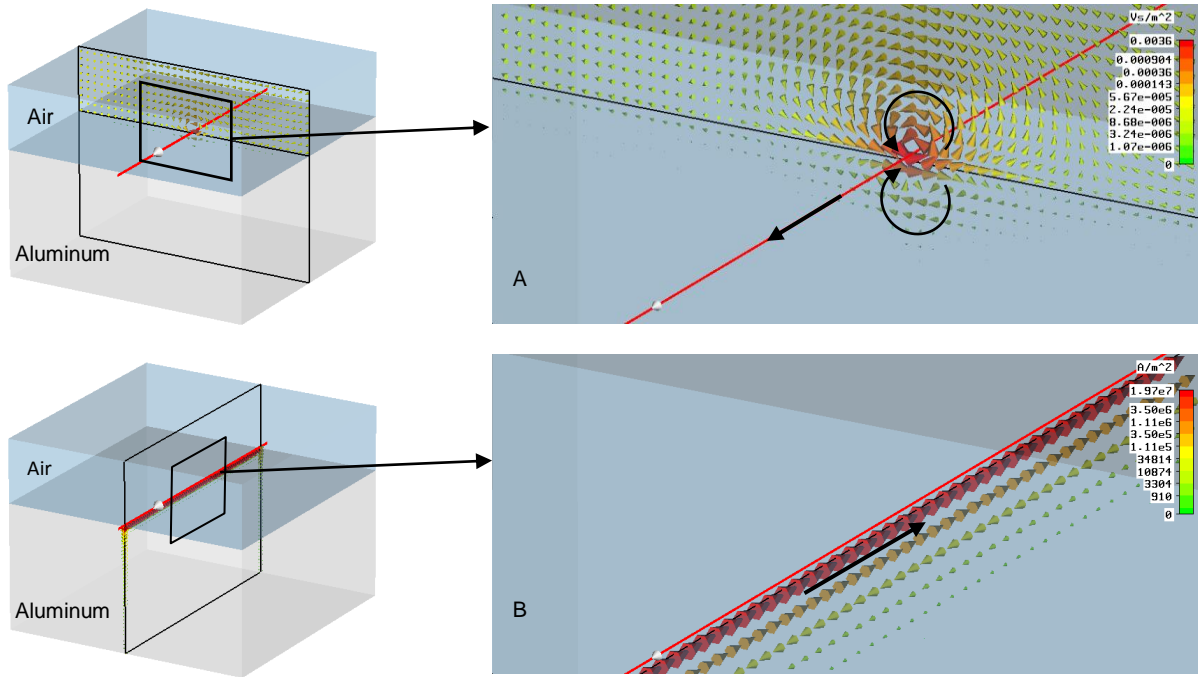
If the boundary circle  $p$  is a one loop coil, the electric field is tangent and has the same magnitude on any point of the coil. Then, the electromotive force sensed by  $p$  is

$$\varepsilon = \oint_p \vec{E} d\vec{l} = -\frac{d\phi_{\vec{B}_d, P}}{dt}. \quad (3.3)$$

If this wire is near to a metallic material, eddy currents appear as a reaction to oppose the magnetic field. Furthermore, these eddy currents modify the magnetic field disposition and intensity from the original  $\vec{B}_d$  to

$$\vec{B} = \vec{B}_d + \vec{B}_e \quad (3.4)$$

where  $B_e$  refers to the magnetic field generated by the eddy currents. The interaction between eddy currents and defects shows up as the magnetic field perturbation  $\vec{B}_e$  and can be sensed by a coil as seen before. Figure 3.3 shows the infinite length wire 100  $\mu\text{m}$  away from a piece of aluminum being driven by a sine wave  $I$  with 1 A amplitude and frequency of 500 kHz. These plots are drawn when the current  $I$  is at its maximum amplitude. As can be seen, the magnetic field around the wire is changed by the presence of the eddy currents which take the inverse direction of the electrical current on the wire.

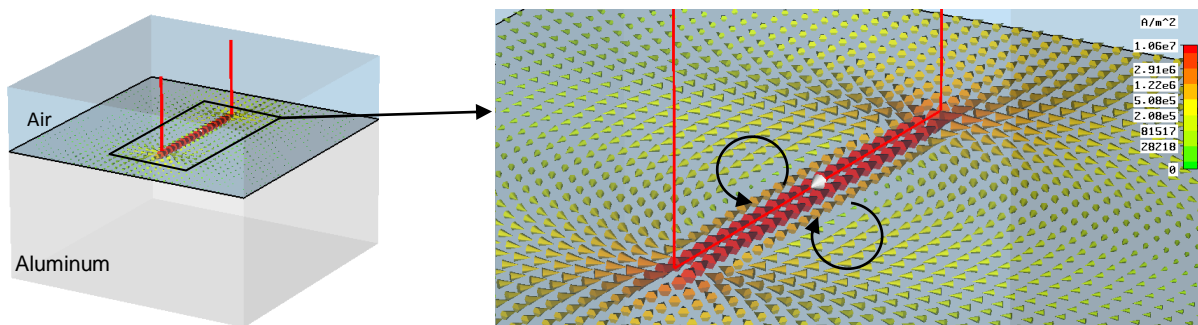


**Figure 3.3** - Current carrying wire over an aluminum piece. A - Magnetic field, B - Eddy currents.

### 3.2.2 Finite Element Modeling

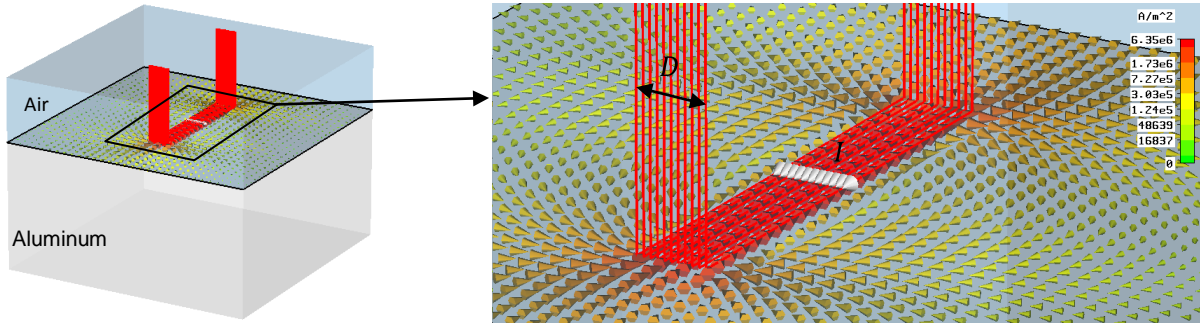
Two models were created using the finite element analysis software CST EM Studio. These models provided baseline information about the magnitude of the generated signals and the expected behavior in the presence of defects. From Figure 3.14 to Figure 3.7, a sine wave with 1 A amplitude and frequency of 500 kHz is flowing in the driver trace. Also, these plots are drawn when the stimulus current is at its maximum amplitude.

Unlike the previous wire, the driver trace has a finite length and is limited by two vertical segments. On those conditions, current flowing on the vertical segments will also generate magnetic field. Although, as the main component of the magnetic field generated by the vertical segments lays on the horizontal plane, few eddy currents will be induced due to this modification. However, limiting the wire length causes quite interesting changes over the induced eddy currents. They will describe loops passing underneath the driver trace and circular paths defined through the material, Figure 3.4.



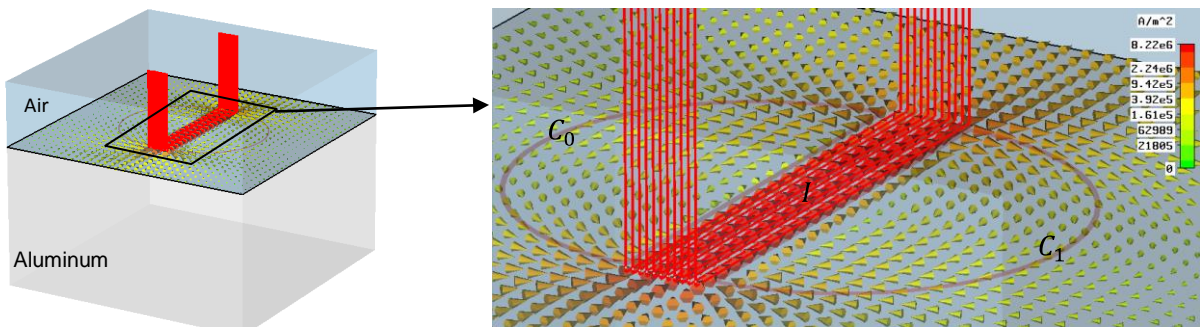
**Figure 3.4** - Eddy currents induced by a limited length current carrying wire.

To model the IOnic probe driver trace, there will be multiple current paths established through a single trace. This is modeled by adding parallel wires carrying together the same current than the initial one. The initial trace can now be considered the array of  $D$  wires represented in Figure 3.5. It is possible to observe how the eddy currents have changed to occupy all the area underneath the wire array.



**Figure 3.5** - Eddy currents induced with the wire array.

The subsequent and final step to complete the first probe model is to define the pickup coils. One of the available elements on the software package is an ideal coil defined by their path and loops number. Two D shaped ideal coils were created over the area where eddy currents flow, Figure 3.6. Both coils are constituted by  $P$  closed loops and were named  $C_0$  and  $C_1$ .



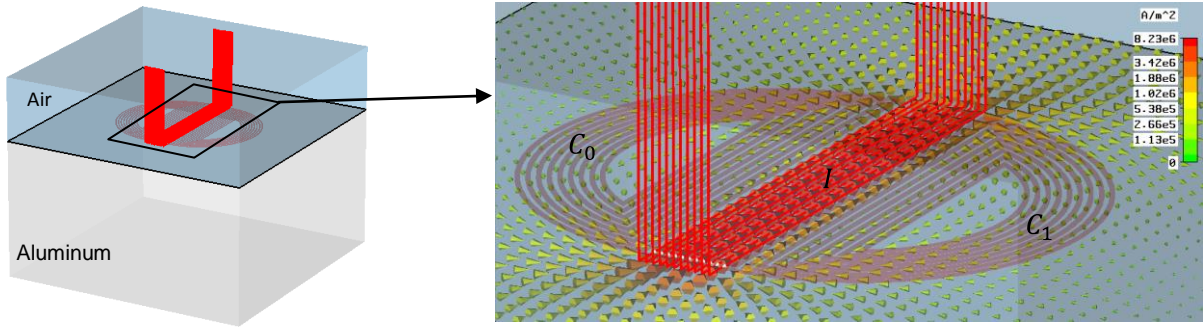
**Figure 3.6** - Basic probe model and superficial eddy currents.

The electromotive force sensed on the coils can be modeled as

$$\varepsilon_{C_n} = P \sum_{i=0}^D - \frac{d\phi_{\vec{B}_{D_i}, P_n}}{dt} \quad (3.5)$$

where  $P_n$  is the transversal area defined by the coil.

The second model was introduced to evaluate how the performance of the probe is changed by using spiral coils. The initial pickup coils were replaced by a more realistic coil model, Figure 3.7.



**Figure 3.7** - Advanced probe model and superficial eddy currents.

By doing this, the area defined by each loop is approximated to that on the real probe. On those circumstances, the electromotive force on each coil is

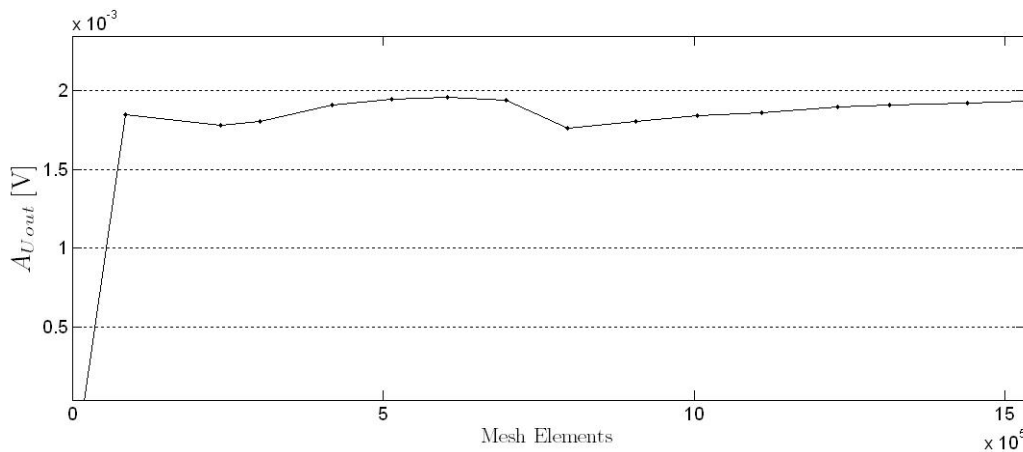
$$\varepsilon_{C_n} = \sum_{i=0}^D \sum_{j=0}^P - \frac{d\phi_{\vec{B}_{D_i}, P_j}}{dt} \quad (3.6)$$

where  $P_j$  is the transversal area defined by each loop.

Because of the common terminal and the fact that they are wired in opposite directions, considering the differential operation, the electromotive force induced between the two output terminals is, for both models,

$$U_{out} = \pm \varepsilon_{C_0} \mp \varepsilon_{C_1}. \quad (3.7)$$

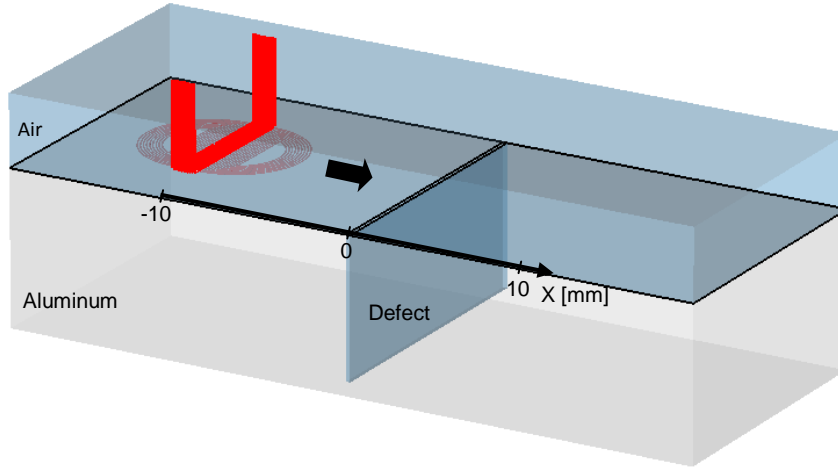
After modeling the probe, the structure was studied and a symmetry axis was defined. This symmetry axis was set perpendicular to the driver trace and equally on both models. In order to evaluate how many mesh elements were needed for a good analysis, a convergence study was then necessary. This convergence study was performed with the advanced model since it has a more complex structure than the basic one. On Figure 3.8 is represented the amplitude of the induced voltage on the coil  $C_0$ , when the driver trace current amplitude is 1 A, for an increasing number of mesh elements.



**Figure 3.8** - FEM Convergence analysis.

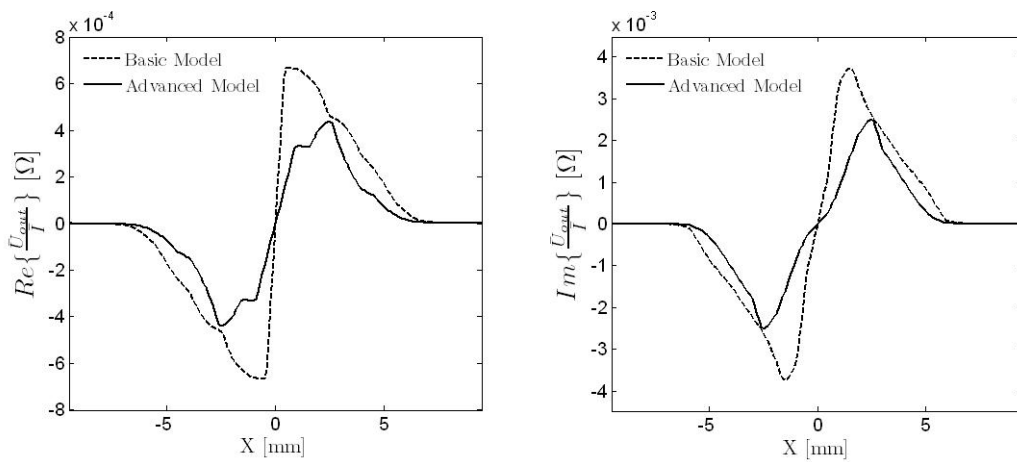
It is observed that for a mesh with more than one million elements, the amplitude on the coil remains almost unchanged. On FEM, the calculation time is highly dependent on the number of mesh

elements. Thus, a mesh with 1.22 millions of elements was chosen as it provides a good approximation and yet a tolerable computation time. At this point, a defect with 10 mm depth and 300  $\mu\text{m}$  width was defined on the aluminum piece. Then, a positional sweep is performed with 500  $\mu\text{m}$  steps in the conditions shown on Figure 3.9.



**Figure 3.9** - Defect characterization sweep.

During the sweep, the successive values for the ratio  $\bar{U}_{out}/\bar{I}$  were registered. The results for both models are presented in Figure 3.10. As expected, when the probe is away from the defect, the induced voltage is roughly zero. Although, since the sensitive coils overlap the defect, the signal output increases returning to zero when the defect is perfectly centered with the probe. This behavior is observed on both real and imaginary part. However, the defect contribution is mainly observed on the imaginary part of  $\bar{U}_{out}/\bar{I}$  as the pickup coils voltage results from the electromagnetic induction. Due to the pickup coils differences, the basic probe model is much more sensitive than the advanced one where the maximum expected output amplitude for defects like this and similar driver trace current is about 2.4 mV. The advanced model will be experimentally validated on the next pages.



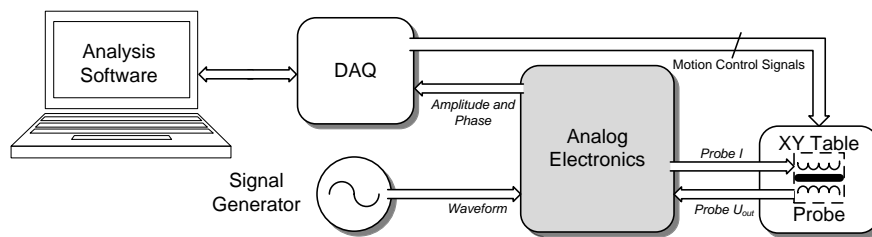
**Figure 3.10** - Real and imaginary part of the ratio  $\bar{U}_{out}/\bar{I}$  along the sweep.

### 3.3 Preliminary NDT system

To perform the experimental validation of the probe concept, a preliminary version of the NDT system was developed in collaboration with the IST Solid-State Welding Group. The system provided a test bench to quickly bring the probe into operation and is composed by the following components:

- XY table to move the probe along the test material;
- Signal generator;
- IOnic eddy currents probe prototype;
- Analog electronics;
- National Instruments USB-6251 DAQ for data acquisition and to control the XY table;
- Analysis software developed on LabVIEW to process, and save the acquired signals.

The system architecture is shown in Figure 3.11. From all the represented components, this dissertation contributes mainly on the analog electronics whose architecture, design and prototyping will be discussed.



**Figure 3.11** - Preliminary NDT system overview.

The analog electronics block is responsible for the generation of the driver trace current, and for recovering the amplitude and phase information of the probe output signal. In this first approach, this is achieved using general purpose analog integrated circuits which generate DC signals proportional to the probe output signal amplitude and the phase difference between this signal and the driver trace current. These DC signals are then acquired by the DAQ and received by a personal computer where the processing is done in a LabVIEW application. This application is also responsible for the probe positioning by controlling the stepper motors on the XY Table.

The functional diagram of the developed analog electronics system can be seen in Figure 3.12. Two driver circuits were included with the possibility to set the relative amplitude and phase difference between them. This feature was implemented to allow the operation of a concept variant based on the IOnic probe which will be described later. Four amplitude and phase detectors were included allowing to simultaneously process the output signal from four pickup coils.

Probe driver circuits are powered by a 10 V AC-DC supply connected to 230 V AC power. The 5 V supply voltage needed for the amplitude and phase detectors is achieved with a Low Drop Out (LDO) linear regulator.



OPA561 dissipates about 3 W, for this reason, some precautions are necessary to avoid the damaging or performance degradation of the integrated circuit. OPA561 has a thermally enhanced package offering a very low thermal resistance path to the Printed Circuit Board (PCB) of 1.4 °C/W. The PCB region where this integrated circuit was soldered has been carefully designed to extract the heat generated directly to the system metallic enclosure box.

The manufactured circuit was able to drive the probes with a sine wave with 1 A amplitude along a frequency range from 10 kHz to 1 MHz.

### 3.3.2 Amplitude and phase difference detector

As seen in the FEM study, even when inspecting an extreme defect, Ionic probe output signal amplitude has no more than 3 mV. Because of that, the very first stage on this circuit is a 40 dB gain voltage amplifier made by a high speed AD8031 OPAMP wired on a non-inverting configuration, Figure 3.14.

Other devices are responsible for generating DC signals proportional to the amplitude of the probe  $\bar{U}_{out}$  signal and the phase difference between this signal and the current  $\bar{I}$ . The amplitude detection is realized using an AD8361 RMS-DC converter and the phase difference is computed with a XOR type phase detector. All the circuits are powered by the 5 V power supply and a voltage divider with appropriate filtering capacitors provide the mid-supply reference.

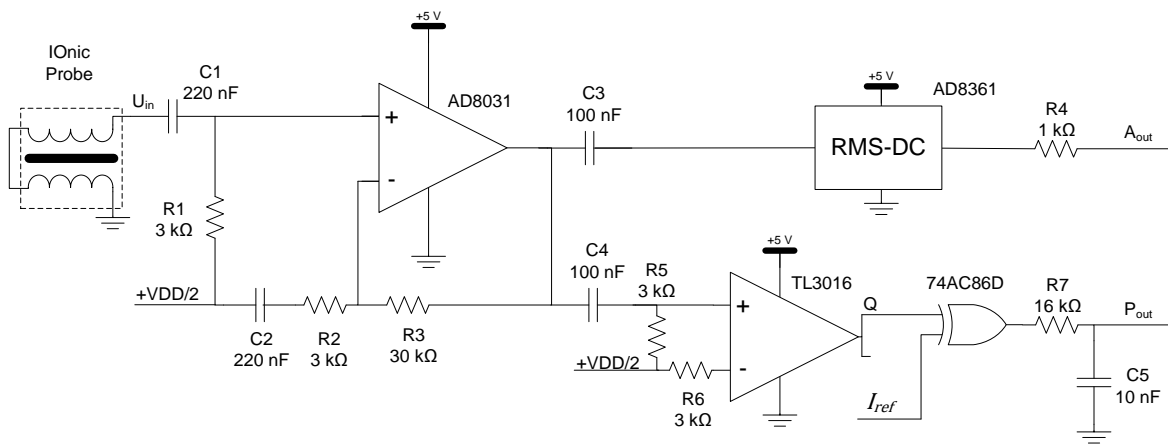


Figure 3.14 - Amplitude and phase difference detectors circuits.

The amplitude output is related with  $\bar{U}_{in}$  amplitude by

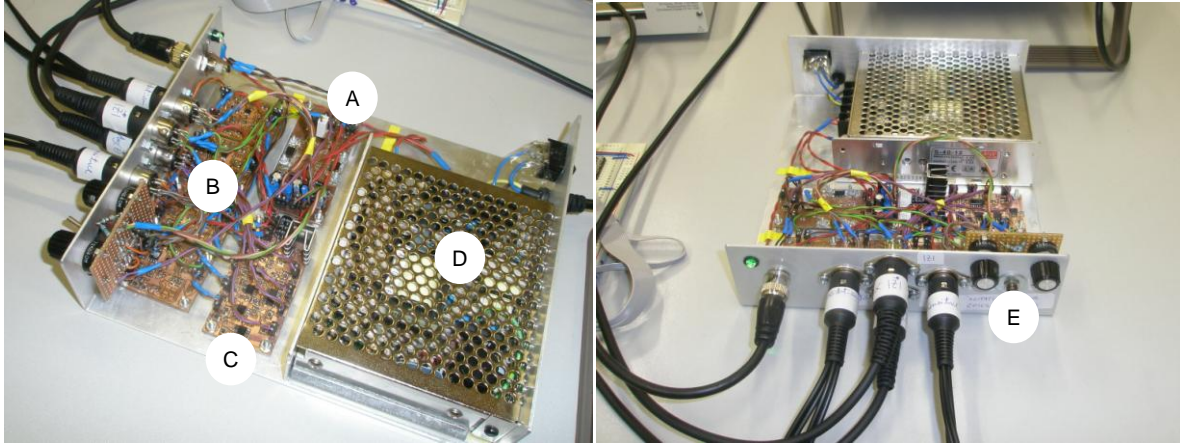
$$A_{out} \approx 7.5 \frac{100 \times A(\bar{U}_{in})}{\sqrt{2}}. \quad (3.10)$$

Phase difference is computed by digitalizing both the signals with a comparator, execute the XOR binary operation and then extract the mean value. A TL3016 fast comparator and a 74AC86D XOR function array ensure digital conversion and processing. The low pass RC filter bandwidth was set to 1 kHz and its output is given by

$$P_{out} \approx \Delta\varphi(\bar{U}_{out}, \bar{I}_{ref}) \times 5. \quad (3.11)$$

### 3.3.3 Analog Electronic System Prototype

The system was manufactured and assembled in the IST Taguspark rapid prototyping facilities. Two layers PCBs were produced making use of a circuit board plotter and an electroplating processing system. After the PCB production stage, a soldering station was used to assembly the circuits which were placed together in the same metallic enclosure box shown in Figure 3.15. The development and prototyping activities needed to achieve a functional prototype took about four weeks.



**Figure 3.15** - Analog electronics system prototype.

A - Probe drivers, B - Amplitude detectors, C - Phase difference detectors, D - Power supply, E -  $\Delta A$  and  $\Delta \phi$  controls.

## 3.4 IOnic probe concept validation

An IOnic probe was manufactured on 1.6 mm dual layer Flame Retardant 2 (FR2) PCB substrate with an external dimension of 12 mm. The two pickup coils are formed by 9 winding tracks of 100  $\mu\text{m}$  width separated by same dimension gaps, Figure 3.16.



**Figure 3.16** - Manufactured IOnic probe.

The defect used on the FEM was reproduced by electro-erosion on a piece of aluminum and an identical sweep was performed. Once again the driver trace current is a sine wave with 500 kHz frequency and 1 A amplitude. The plots for the experimental validation and the FEM are included in

Figure 3.17. Note that there is a very good similarity between the two results mainly on the imaginary part of  $\bar{U}_{out}/\bar{I}$  which is about one order of magnitude greater than the real part.

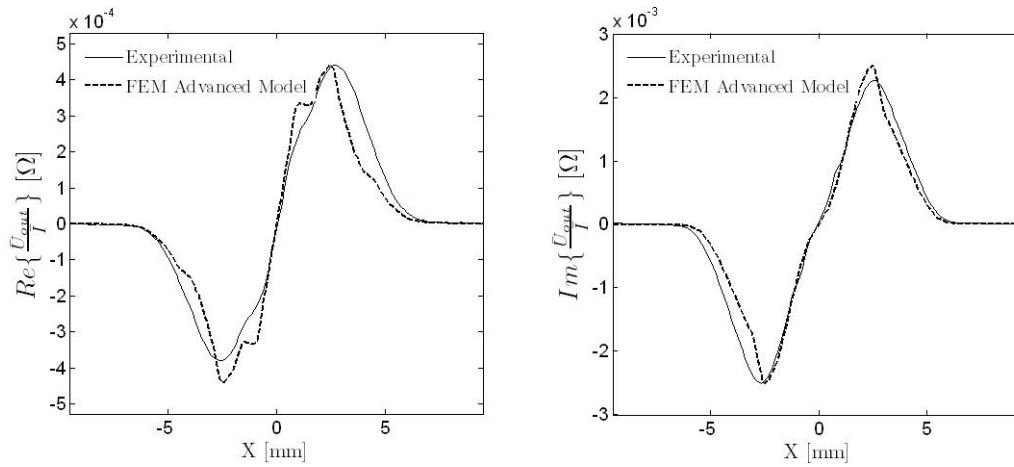


Figure 3.17 - Experimental and FEM results for the standard defect.

After the probe concept validation, a defect free FSW weld bead was inspected. This specimen was obtained by performing a FSW sweep in a plate of aluminum alloy AA2024-T531 of 3.8 mm thickness. By using a single piece of base material and selecting proper welding parameters it is possible to achieve almost perfect weld beads. In fact, bead on plate samples provide an excellent quality standard for FSW process. The bead on plate was inspected along a sweep on the perpendicular direction of the weld, with the driver trace parallel to it. The starting point of the test is set to 25 mm before the weld bead and 50 mm long segments are characterized with 250  $\mu$ m space steps. In all the acquisitions, the real and imaginary part of  $\bar{U}_{out}/\bar{I}$  are measured at 50, 100 and 250 kHz. The imaginary part of  $\bar{U}_{out}/\bar{I}$  for the specified sweep is shown in Figure 3.18. As FSW process causes material conductivity changes, even without a defect, the weld bead is responsible for the large curve on the processed imaginary part.

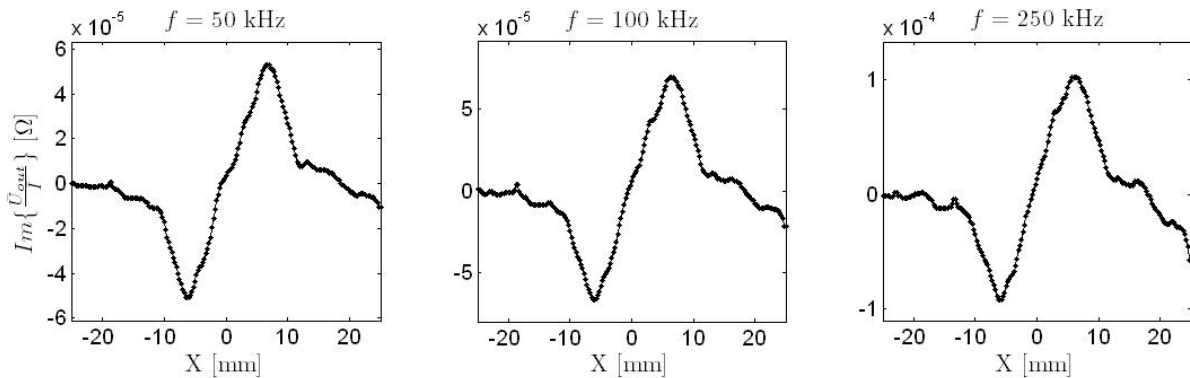
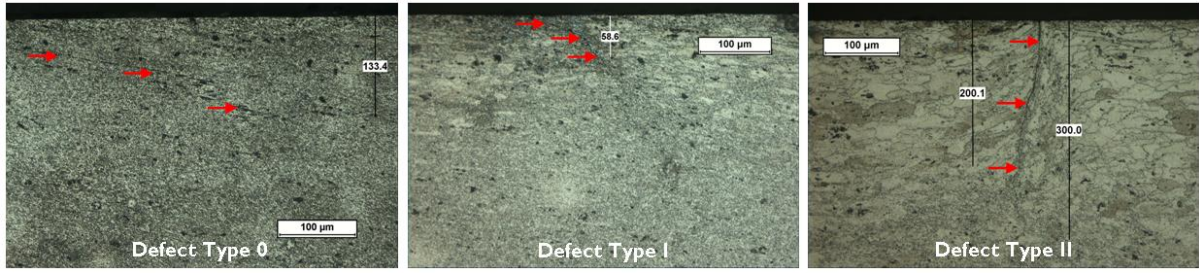


Figure 3.18 - Results for the FSW bead on plate for 50, 100 and 250 kHz.

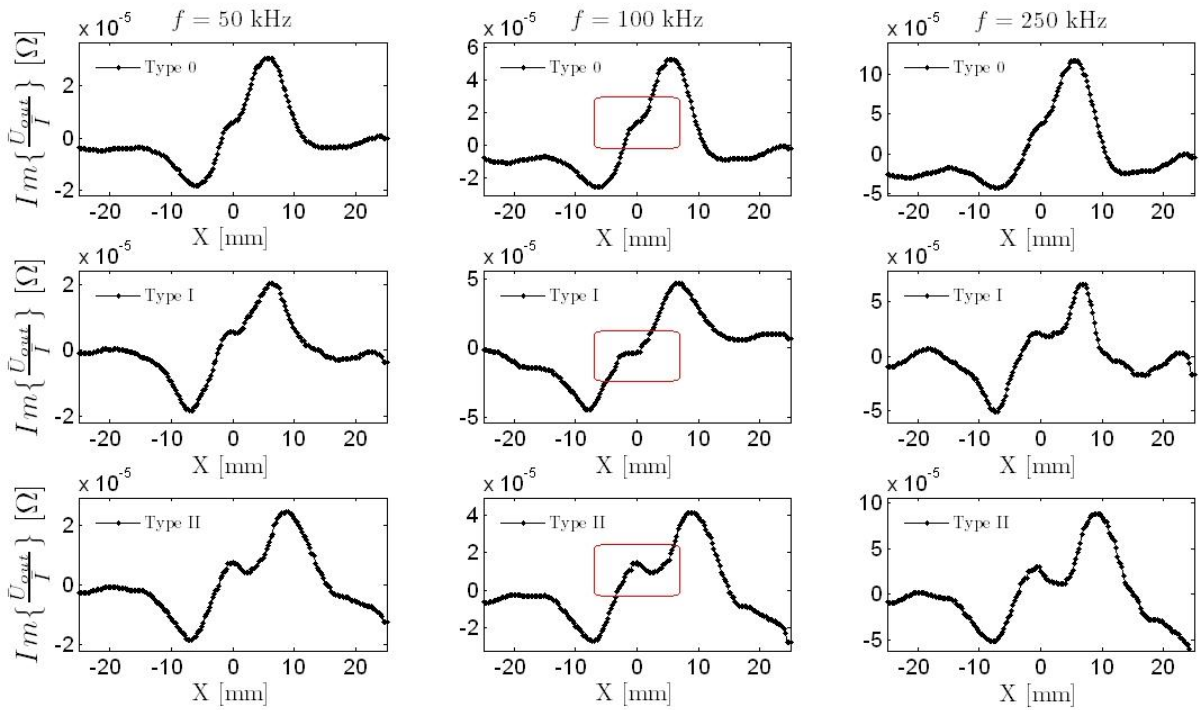
After characterizing a non-defective bead on plate, a set of friction stir welds have been realized on the same aluminum alloy. The welding parameters were chosen in order to produce three distinct types of defects as is shown in Figure 3.19.



**Figure 3.19** - Transversal macrographs of three different FSW defective weld beads.

Defect Type 0 - Oxides alignment, Defect Type I -  $\approx 60 \mu\text{m}$ , Defect Type II -  $\approx 200 \mu\text{m}$ .

The three defects were inspected in same conditions as the bead on plate sample and for the same three frequencies. The imaginary part of  $\bar{U}_{out}/\bar{I}$  for the three types of defects and for the three selected frequencies is shown in Figure 3.20. The presence of defects creates a small perturbation observed in the middle of the sweep, highlighted in red on Figure 3.20. The different types of defects can be detected and there is a very good proportionality between the defect dimension and the observed perturbation on the imaginary part of  $\bar{U}_{out}/\bar{I}$ .



**Figure 3.20** - Results for the FSW weld beads with defect types 0, I and II for 50, 100 and 250 kHz.

To compare the performance of the new probe with the conventional ones, the system was used also with a traditional planar probe. This second probe is composed by a flat spiral coil with 20 windings and 8 mm overall diameter. The results on inspecting the FSW joints when the coil current is a 1 A sine wave with frequencies 100, 250 and 750 kHz are shown in Figure 3.21. Unlike the results achieved with the IOnic probe, there is no characteristic that could be used to conclude about the

presence of defects. With this probe, the material conductivity changes inside the FSW weld bead mask the contribution of the defects making impractical the defect detection.

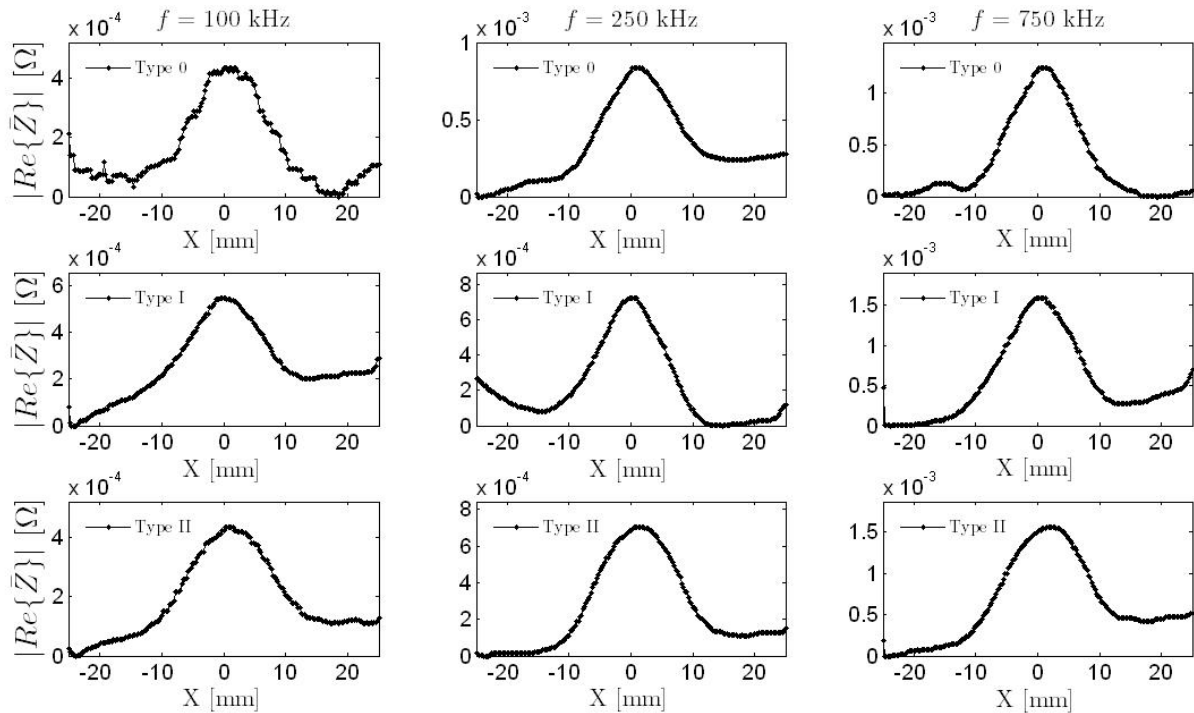


Figure 3.21 - Results for the FSW weld beads with a conventional planar probe.

### 3.5 Ionic concept advantages

The Ionic probe has some advantages when compared to the conventional eddy currents probes:

- Differential based operation resulting on high sensibility and superior lift-off immunity. The probe is almost completely immune to lift-off if the probe remains perfectly parallel with the material;
- Improved contact with test material. The planar design allows the probe to be in close contact with the material (100-300  $\mu\text{m}$ ) enhancing the sensibility for very small defects;
- Deeper eddy currents penetration due to the small distance between the driver trace and the test material;
- The intense eddy currents induced in the material near the driver trace can be taken as advantage to evaluate materials where the flaws tend to follow a specific orientation. Making use of the probe on such conditions may substantially increase those defects detection probability;
- Allow the inspection of the material borders as long as the symmetry axis remains perpendicular to it. It can be also used on non-planar and complex geometry surfaces since the probe can be manufactured on flexible substrates;

- Despite the preferred operation mode is differential, the probe can also perform absolute measurements by making accessible the common terminal of the pickup coils. This will provide information on material parameters such as conductivity, magnetic permeability and thickness.

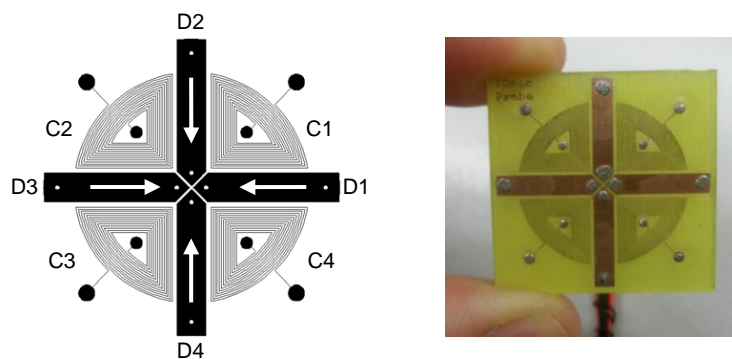
### 3.6 IOnic concept variations

Three concept variations of the IOnic probe have been studied in order to overcome some of the probe limitations or to improve their performance on some inspection applications.

#### 3.6.1 IOnic Plus

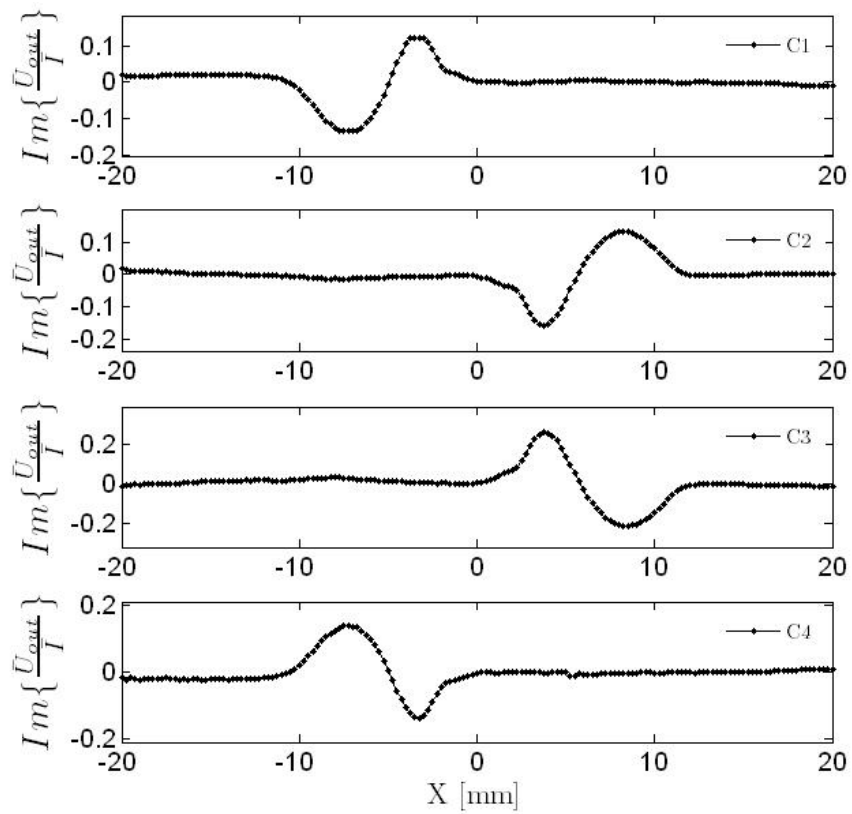
With the original probe, it is very hard to detect defects that appear transversally to the driver trace. In such conditions the defects interact with the originated eddy currents but the magnetic field symmetry along the axis defined by the driver trace remains unchanged. This concept variant was designed to overcome this limitation of the original probe. By modifying of the original morphology, new features and operation modes have been found.

The IOnic Plus probe exhibit four driver traces outlining a cross and four pickup coils, one in each quadrant of the driver traces cross, Figure 3.22. As before, the magnetic field is sensed in the pickup coils which can be read independently or in multiple combinations. This morphology enables multiple operation modes according to the currents flowing in the driver traces and the configuration selected for the pickup coils wiring.



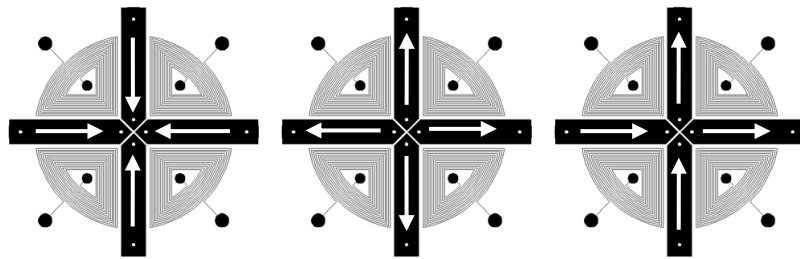
**Figure 3.22** - IOnic Plus morphology and prototype.

In order to validate the probe operation, it was used together with the preliminary NDT system to inspect the standard defect described in Figure 3.9. The probe is positioned so that two of the driver traces are parallel to the defect. The same 1 A amplitude, 500 kHz frequency sine wave is made to flow in the driver traces according with the arrows in Figure 3.22. The results for the output signals from the four pickup coils are shown in Figure 3.23.



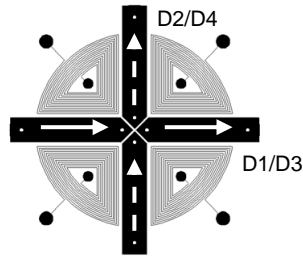
**Figure 3.23** - IOnic Plus standard defect inspection results.

Unlike the IOnic probe where the two pickup coils are wired together, the signals on each pickup coil were independently processed. The presence of the defect can be observed in all the pickup coils output signal even if the probe is rotated by 90°. The results illustrate the static operation of the probe that can be achieved by using the same current on the driver traces. Even in the static operation mode, the driver traces can be wired in several configurations as shown in Figure 3.24 leading to multiple patterns of induced eddy currents.



**Figure 3.24** - IOnic Plus static operation mode configurations.

In addition to this basic operation mode, there is the possibility to introduce variations between the currents flowing in the driver traces. This dynamic operation mode enables to control the induced eddy currents profile by commanding the relative amplitude and phase difference between the currents in the driver traces. To operate the probe, are required two independent current generators for the D1/D3 and the D2/D4 driver traces sets, Figure 3.25. The control of the eddy currents can then be made electronically while inspecting the material.



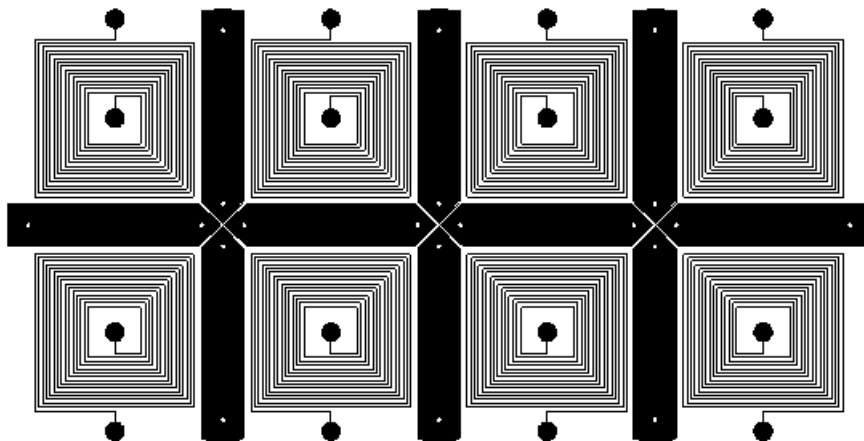
**Figure 3.25** - IOnc Plus driver trace connections for the dynamic operation mode.

The use of this new variant allows an improved defect characterization and accurate localization by introducing some advantages:

- Versatility of the probe operation, allowing creating an output signal from each pickup coil or from their combination;
- The defects localization and morphology can be reconstructed by using the correlation between the four pickup coils output signals;
- The electronic control of eddy currents disposition inside the test material, allows the detection of defects whose morphology follow any direction;
- The multiple response patterns from the several combination of driver traces currents and pickup coils arrangements originate a huge amount of data on each point of the material to inspect;
- Less complex motion and positioning systems and increased inspection speed by removing the need of rotate the probe.

### 3.6.2 IOnc Matrix

This concept variation is based on the matrix repetition of IOnc plus arrangements. This repetition can be made on the two directions of the substrate plane and with a reconfigurable pattern according to the inspection purposes, Figure 3.26. To maximize the sensitive area of the pickup coils, their shape is square. The main advantage resulting from this repetition is the expanded inspection area of the probe and consequently the increase of the inspection speed.



**Figure 3.26** - IOnc Array illustration.

### 3.6.3 IOnic Active

The IOnic probe can be made even more sensitive to small defects by reducing the sensitive area of the probe. However, the number of windings of the pickup coils is limited by the manufacturing capabilities leading to very low amplitude output signals. This concept variation allows overcoming electromagnetic compatibility issues that can arise from the signal transmission between the probe and the acquisition system.

In order to amplify the output signal of the probe, a differential amplifier was used and assembled on the top side of the probe substrate. The differential amplifier used was the AD8351 low noise amplifier set to 20 dB voltage gain. In this conditions, the expected noise spectral density introduced by the AD8351 is about  $2.7 \text{ nV}/\sqrt{\text{Hz}}$ . Besides the good characteristics regarding noise and linearity, this device has been selected because of the single power supply operation and low power dissipation. To set the probe output common mode voltage, the common terminal of the pickup coils is wired to the GND reference of the amplifier.

The probe is printed in the bottom layer of the substrate and the circuit is assembled on the top layer. In Figure 3.27 the bottom view of the manufactured IOnic Active probe inside a Plexiglas enclosure is shown. The six coil windings of the pickup coils have about  $90 \mu\text{m}$  and are separated by the same distance.

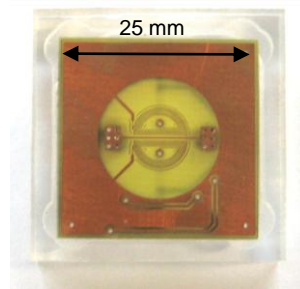


Figure 3.27 - IOnic Active bottom view.

## 3.7 Summary

In this chapter, the new IOnic concept for eddy currents probe has been presented. The electromagnetic phenomena related with the probe operation have been discussed using classic examples of electromagnetism literature. FEM analysis has been used to clarify and corroborate the new concept of eddy currents probe. The experimental validation and application results to FSW specimens presented demonstrate the effectiveness of the probe on the defect detection. In the end of the chapter some advantages of the new approach and concept variations have been introduced.

The potential of the new probe was highlighted by the encouraging results obtained while inspecting FSW joints. However, this preliminary system has some limitations as the narrow frequency operation range and the impossibility to explore new types of stimulus. These reasons lead to the development of a new and improved version of the non-destructive testing system.



# Chapter 4 – ECscan NDT System Hardware

## 4.1 Introduction

To extract the maximum advantage from the new probes, a tailor made electronic system to perform non-destructive testing tasks was developed. This second approach was designed to fully replace the electronic devices employed in the preliminary version by a single and integrated solution, Figure 4.1. ECscan is a reconfigurable solution for eddy currents NDT composed by hardware for high speed signal generation and processing, and dedicated software. The new system takes advantage from the flexibility, repeatability and reliability achieved through the probe signals digital signal processing. ECscan is highly reconfigurable through the use of programmable digital logic devices and the possibility to set several combinations of peripherals cards for signal generation or acquisition. Also, several communication interfaces have been added providing easy connectivity with personal computers and networks.

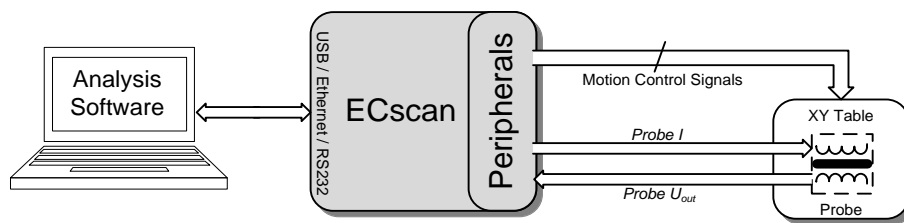


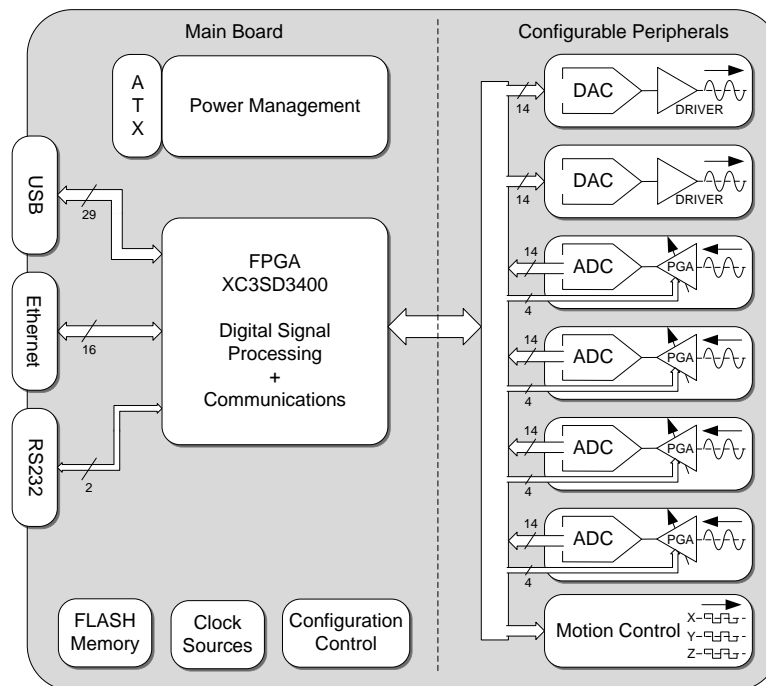
Figure 4.1 - ECscan system Overview.

Regarding hardware, ECscan is an embedded system based on a FPGA device tailored for digital signal processing and memory intensive applications. The main board includes the processing and power management devices, and communication interfaces for Universal Serial Bus (USB) 2.0 High Speed, Ethernet 10/100 and RS232, Figure 4.2. In addition, the main board has non-volatile FLASH memory, used to store software and internal settings, several clock sources and configuration interfaces.

In this innovative system, digital stimulus are generated in the FPGA processing core and then converted to an analog signal that is used to drive the probe. Conversely, the probe output signals are acquired and then processed in the digital domain. Unlike the preliminary NDT system, this new approach enables the generation of numerous stimulus types and the probe output signals processing through a great variety of algorithms. Furthermore, the seven connectors available in the main board can be used to set multiple configurations of peripherals cards to generate or to acquire the signals on the several IOnic probes and concept variants. With this number of connectors and the three types of peripherals cards developed, it is possible to implement a proper combination to operate the IOnic

Plus probe as can be seen in Figure 4.2. In order to easily exchange the peripherals, they are connected to the main board through Single In-Line Memory Module (SIMM) 72 vertical sockets.

The peripheral card responsible for the probe input current generation is composed by a 14 bits Digital to Analog Converter (DAC) followed by an improved probe driver circuit featuring higher output current and an extended frequency operation range. Signal acquisition is achieved with 14 bits high speed Analog to Digital Converters (ADC) connected to Programmable Gain Amplifiers (PGA) where the input signal amplification is controlled by a four bits gain digital code. The frontend of the acquisition operates in the differential mode allowing extracting the maximum advantage from the IOnic Active probe. An additional peripheral was designed to simultaneous control up to three axis on the XY Table.



**Figure 4.2** - Main board functional diagram.

Along this chapter, the design of each ECscan hardware block will be described. The hardware was developed using Altium Protel 2009, Computer Aided Design (CAD) software and the produced schematics are included in the Appendix I.

## 4.2 ECscan Main Board

The main board of ECscan system contains the processing device, power management devices, the communication interfaces and connectors for peripherals. This board aims to provide features that are needed for almost all possible system application. It was specially designed to provide sufficient resources for the seven peripherals that can be connected.

Despite the fact that this board has been designed to be included in the ECscan system, it can be used for prototyping, evaluation and educational purposes. In fact, the board resources can be employed to develop a different system avoiding the complex and time consumer design of a FPGA

processing core. Also, it can be used to implement didactical projects on digital signal processing and embedded systems.

The characteristics of the ECscan Main board are:

- XILINX XC3SD3400A FPGA processing core;
- High Speed USB 2.0 interface;
- Ethernet 10/100 interface;
- RS232 Interface;
- 2 on-board clock sources;
- 7 peripheral connectors providing a total of 198 FPGA IO pins and several power supplies;
- 32 Mb of Inter-Integrated Circuit (I<sup>2</sup>C) FLASH data memory;
- 32 Mb of FLASH program memory;
- Several configuration standard interfaces;
- Status LEDs, Push buttons and Dual In-line (DIL) switches;
- Advanced Technology Extended (ATX) compatible power supply.

#### 4.2.1 FPGA based processing core

A FPGA is a general-purpose integrated circuit containing a matrix of configurable resources that can be used to implement different digital components. Unlike an Application-Specific Integrated Circuit (ASIC), FPGA devices can be reprogrammed even after has been deployed into a system. A FPGA is programmed by loading a configuration bitstream into Random-Access Memory (RAM) inside the integrated circuit. This bitstream is generated by compilation tools which translate the high level abstractions into a low level logical implementation. The bitstreams contain the information to set interconnections between the computational and IO resources of the FPGA allowing them to be wired together into systems.

FPGAs have some advantages for digital signal processing when compared to DSP processors. The performance of FPGAs results from the ability to build highly parallel processing structures. Unlike DSP processors, where performance is tied to the clock frequency and the Arithmetic Logic Unit (ALU) efficiency, FPGA performance is related with the amount of parallelism that can be achieved in a certain DSP algorithm. The increasing speed, high flexibility and performance make FPGAs ideal for high data rate DSP.

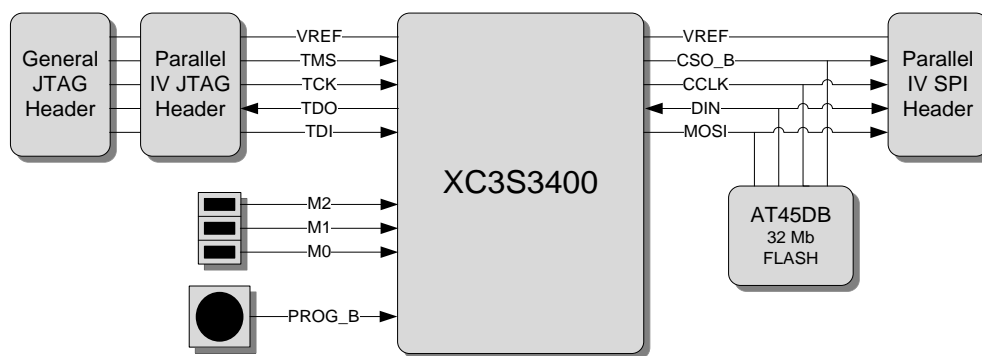
ECscan key device is a XILINX XC3SD3400A FPGA specially tailored for memory-intensive, DSP cost-sensitive applications. To meet this objective, this device has about 2 Mb of integrated RAM and a big number of DSP48A slices. DSP48A slices perform high speed multiply and accumulate operations for 18x18 two's complement operands at 250 MHz, being particularly useful on building DSP structures. The main features of XC3SD3400A device are listed in Table 4.1.

**Table 4.1** - XC3S3400A-4CSG484C FPGA characteristics.

Array (RowxCol)	System Gates	Spartan-3® Slices	DSP48A Slices	BRAM (Kb)	Digital Clock Managers	Max. User IO
104x58	3400 K	23872	126	2268	8	309

The FPGA Input/Output (IO) resources are divided among four banks. In each bank, the voltage levels can be configured by setting their supply voltage from 1.2 V to 3.3 V. One of the banks is used to control on-board resources and the other three are distributed by the peripheral connectors and is set to 3.3 V. The other banks are connected to the peripheral connectors and it is possible to set their voltage levels by changing jumper locations on the board.

The FPGA configuration can be made by a Joint Test Action Group (JTAG) compliant interface or using an SPI Flash memory. Two different JTAG headers have been included, enabling the configuration through a popular XILINX Parallel IV and general JTAG programmers. Atmel AT45DB Serial Peripheral Interface (SPI) Flash device provide 32 Mbits of non-volatile memory for storing the embedded application. This device can be configured using Parallel IV programmers and XILINX proprietary tools. The architecture of the configuration sources is shown in Figure 4.3.



**Figure 4.3** - FPGA configuration sources and control.

Setting the active configuration mode is done by asserting the M[2:0] signals. The logic values for each the configuration selectors can be set changing jumper locations. The configuration logic inside the FPGA reads the state of this input pins and starts the configuration in the selected mode. Configuration modes and respective selection logic values and represented in Table 4.2. Configuration is requested by powering on the FPGA device or asserting the signal PROG\_B which is controlled by a push button. The Power On Reset (POR) is generated using a TPS3106 integrated circuit which supervises the 3.3 V and 1.2 V supplies.

**Table 4.2** - Configuration mode selection.

M[2:0]	Mode	Description
001	Master SPI	Configuration using the on-board SPI FLASH memory
101	JTAG	Configuration through the JTAG chain
111	Slave Serial	Configuration by an external Master

#### 4.2.2 Power Management and Power Distribution Network

Three switching converters ensure the multiple supply voltages needed by the FPGA converting the 5 V available on the ATX connector. Texas Instruments PTH05050 provide up to 95% efficiency and a maximum output current of 6 A. The target output voltage of these converter modules can be set to any voltage over the range 0.8 V to 3.6 V, using a single resistor. This resistor is connected between the ADJ pin and the ground signal and their value is determined by

$$R_{set} = 10000 \times \frac{0.8}{V_{out} - 0.8}. \quad (4.1)$$

Three PTH05050 were set to generate 1.2 V, 3.3 V and another auxiliary supply voltage that can be set between 1.5 V, 1.8 V and 2.5 V by changing a jumper location.

The output stage of PTH05050 can be disabled by controlling the voltage applied on the PWR\_ON pin. To ensure synchronous stabilization of all supply voltages, these converters have a tracking feature. After the PWR\_ON signal is asserted, the output follows the TRACK pin voltage on a volt-per-volt basis until the target voltage is achieved. Connecting the three PTH05050 TRACK pins to the same signal ensures that the voltage absolute maximum ratings between the different FPGA supplies are not exceeded. The TRACK signal is generated by a TPS3825 voltage supervisor which asserts it when the input voltage becomes stable and above 4.5 V, Figure 4.4.

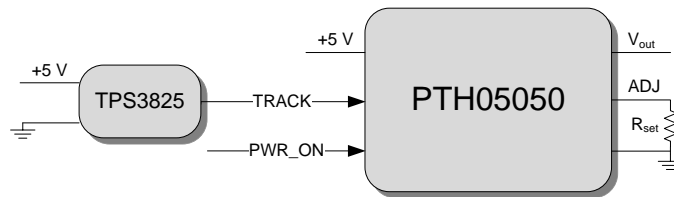


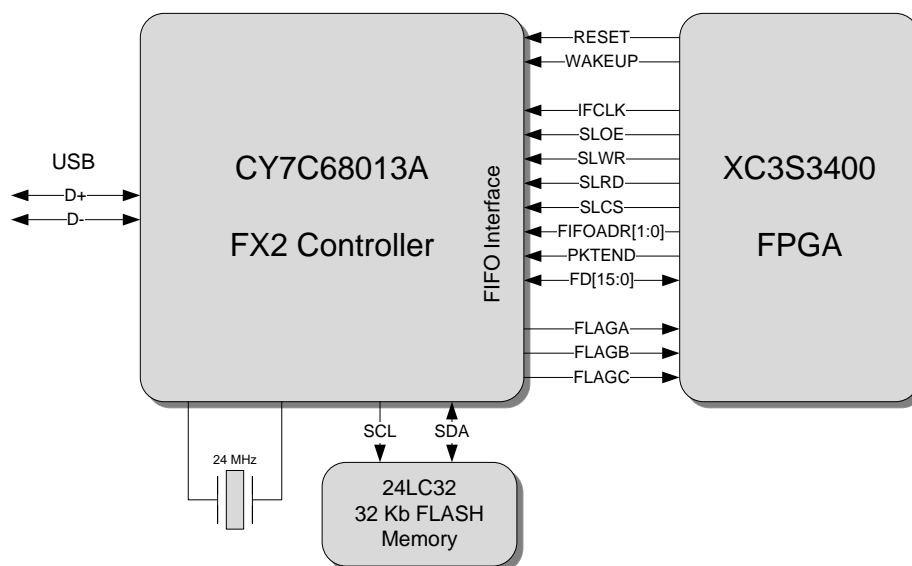
Figure 4.4 - PTH05050 connections and tracking Feature.

In digital devices, transient current demand is the main cause of ground bounce and power supply noise. These two issues are especially critical when developing high-speed digital electronic systems because they can reduce the noise margin for both logic levels. The Power Distribution Network (PDN) concerns the current path from the power supply to the FPGA and includes all the decoupling capacitors or other filtering devices. The design methodology adopted in the FPGA PDN is described in the Appendix II.

#### 4.2.3 USB Interface

The USB protocol is one of the most popular connection methods between personal computers and peripheral devices. The characteristics of plug and play, hot swapping, high compatibility and a relatively high transmission debit, has raised the worldwide production of USB devices to about two billion per year. The initial motivation for developing the USB protocol was the replacement of the numerous low speed communication interfaces found in personal computers. However, USB became common on applications requiring high bandwidth such as video streaming and acquisition systems.

In the ECscan, USB communications are ensured by a Cypress CY7C68013A integrated controller. This chip makes use of Cypress FX2 technology and is a highly integrated, low power USB 2.0 microcontroller. CY7C68013A contains on the same package a transceiver, a serial-parallel conversion mechanism, several programmable interfaces and an enhanced 8051 microcontroller. All the configuration tasks are done by firmware and executed by the 8051 microcontroller while the high speed data processing is handled in hardware. The various interfaces and an architecture that enables multiple operation modes configurable by firmware make the FX2 a quite versatile solution. CY7C68013A controller has eight 512 byte memory blocks that can be used as a First In First Out (FIFO) queue to send and receive data from the USB. During the operation, while some of the eight blocks are controlled by the Smart USB Engine, others are being controlled by the FIFO interface. This particularity allows transmission speeds up to 96 MB/s over the FIFO queue, surpassing the maximum data rate of 60 MB/s on the USB 2.0 High Speed. The FIFO interface can operate in eight or sixteen bits, asynchronous, synchronous with internal or external clock source and in master or slave mode. The signals shared between the FPGA and the CY7C68013A allow the use of the FIFO interface on all the operation modes. In particular, for this application the FIFO will be working in slave synchronous mode with internal clock source. In this configuration the involved signals are represented in Figure 4.5.



**Figure 4.5** - Cypress FX2 USB CY7C68013A to FPGA connections.

USB endpoints are logical units inside the host and the peripherals where the data can be exchanged. Each endpoint can be configured as IN or OUT to send or receive data from the host respectively. The memory block of the FIFO can be configured to form four endpoints of 1024 bytes each. These endpoints can be addressed using the signals FIFOADR[1:0] and accessed through the data bus FD[15:0]. The read and write operations are controlled by the IFCLK, SLOE, SLWR, SLRD and SLCS signals. The PKTEND signal forces the CY7C68013A to commit the data in the addressed endpoint sending it to the host. The three flag signals give to the external logic information about the addressed endpoint state. The function, type and polarity for each signal are described in Table 4.3.

The firmware to be run by the 8051 microcontroller inside the CY7C68013A is stored in the 24LC32 I<sup>2</sup>C memory FLASH. To upload the firmware to the memory flash, a Cypress Semiconductors proprietary tool is used to transmit the data over USB.

**Table 4.3** - CY7C68013A FIFO interface with the FPGA.

Signal	Direction	Active low - L Active high - H	Function
RESET	Output	L	CY7C68013A reset signal
WAKEUP	Output	L	CY7C68013A wakeup signal
IFCLK	Input	H	Interface clock, generated by CY7C68013A with 48 MHz frequency
SLOE	Output	L	Output enable for the FIFO data register
SLWR	Output	L	Slave write strobe
SLRD	Output	L	Slave read strobe
SLCS	Output	L	Slave chip select
FIFOADR[1:0]	Output	H	FIFO address
PKTEND	Output	L	PKTEND strobe
FD[15:0]	Bidirectional	H	Data signals
FLAGA	Input	H	Programmable indication of the FIFO state
FLAGB	Input	H	Full FIFO indication
FLAGC	Input	H	Empty FIFO indication

Beside the power lines, the USB bus includes the signals D+ and D- which form a differential transmission line for the data. To reduce the electromagnetic noise contribution, these signals are transmitted on a twisted pair (with a controlled differential impedance of  $90 \Omega \pm 15\%$ ) inside of a shielding mesh. The PCB design influences the quality of the USB signals more than any other parameter. By this reason, the differential impedance of the PCB tracks for D+ and D- signals should fulfill the USB specifications of  $90 \Omega \pm 15\%$ . The D+ and D- signal were routed as microstrip lines in the PCB top layer. Regarding the PCB layout, the differential impedance seen between the two microstrips can be controlled changing the width W, the distance between the two tracks S, and the distance to the adjacent plane H. This last parameter was set to the thickness of the pre-impregnated coating between the top layer and the internal layer 1 in a standard eight layer PCB. The spacing between the two microstrips was set to the clearance limit achievable in 17  $\mu\text{m}$  copper, 100  $\mu\text{m}$ . The width for the two microstrips was set to 200  $\mu\text{m}$ , as suggested in the Appendix III, leading to a differential impedance of 97.3  $\Omega$ . In Table 4.4 the values considered for the design parameters are listed.

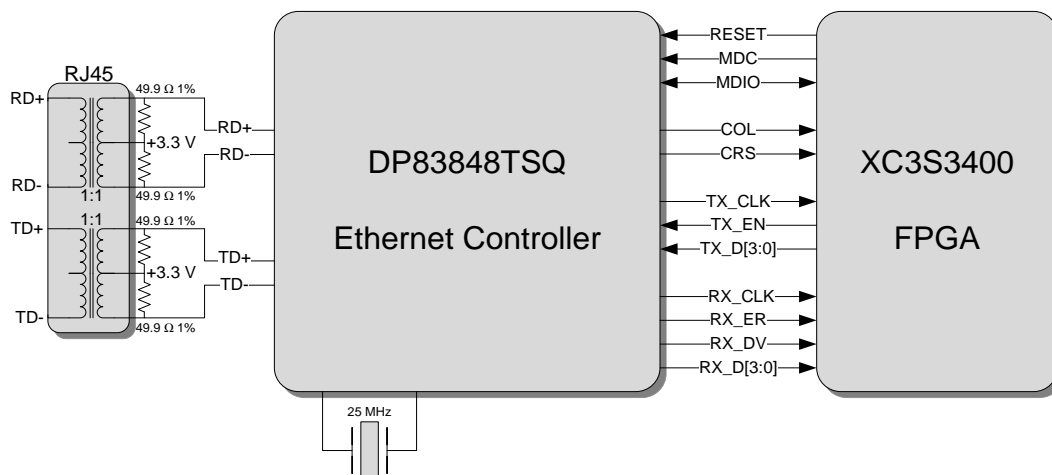
**Table 4.4** - Parameter values for the differential microstrip lines design.

Symbol	Description	Value
$\epsilon_r$	FR4 Dielectric Constant	4.35
T	Copper Thickness	17 $\mu\text{m}$
H	Distance to the adjacent plane	200 $\mu\text{m}$
S	Distance between the two tracks	100 $\mu\text{m}$

#### 4.2.4 Ethernet Interface

Ethernet is a family of computer networking technologies for Local Area Networks (LAN). Ethernet based networks have been in use since 1980, largely replacing old standards as ARCNET and FDDI. The timely standardization of Ethernet by the Institute of Electrical and Electronics Engineers (IEEE) in 1984 (standard 802.3) was a crucial step to their success and widely implementation. Beyond the popularity of Ethernet for local area networking, nowadays it is used under industrial conditions. The main benefits of using Ethernet for industrial control are the relatively high speed, low maintenance costs and reliability. Actually, Ethernet remains one of the lowest cost reliable long lasting solutions when connecting electronic devices over production lines.

The designed Ethernet interface is based on the National Semiconductor DP83848TSQ Physical Layer Transceiver. The upper layers of the communication protocol are implemented inside the FPGA using both dedicated hardware and software. National Semiconductor DP83848TSQ communicates with the logic inside the FPGA through a Media Independent Interface (MII). The MII transfers data using 4-bit words in each direction, clocked at 25 MHz to achieve a maximum of 100 Mbit/s speed. The signals related with the MII interface connected to the FPGA are represented in Figure 4.6.



**Figure 4.6** - National Semiconductor DP83848TSQ to FPGA connections.

MDC and MDIO signals constitute the MII serial management interface and can be used to configure the internal operation mode of the DP83848TSQ integrated circuit. This interface controls the 24 internal registers providing information about the Ethernet status and the ability to enable or disable several communication features. The function, type and polarity for each signal are described in Table 4.5.

The RJ45 connector has internal transformers to interface the Ethernet twisted pairs data lines and an indication LED which is controlled by the transceiver to indicate cable activity. The impedance seen between RD and TD differential signals was matched to the characteristic impedance of the transformer using 49.9 Ω resistors. As indicated in the DP83848TSQ datasheet, the common mode for both RD and TD lines was set to the supply voltage of 3.3 V.

**Table 4.5** - DP83848TSQ interface with the FPGA.

Signal	Direction	Active low - L Active high - H	Function
RESET	Output	L	DP83848TSQ reset signal
MDC	Output	H	MII serial management clock
MDIO	Bidirectional	H	MII serial management data
COL	Input	H	Collision detect indication
CRS	Input	H	Carrier presence indication
TX_CLK	Input	H	Transmitted data clock
TX_EN	Output	H	Transmit strobe
TX_D[3:0]	Output	H	Transmit data
RX_CLK	Input	H	Received data clock
RX_ER	Input	H	Receive error indication
RX_DV	Input	H	Receive strobe
RX_D[3:0]	Input	H	Receive data

#### 4.2.5 Peripheral Connectors

Seven SIMM 72 socket connectors are used to interconnect the main board with the peripherals. To enable the use of several combinations of peripheral cards a common structure for the peripheral connectors was defined. The 72 signals include supply voltages, general IO and clock pins of the FPGA. The number of pins for each type of resource is described in Table 4.6.

**Table 4.6** - Resources on each peripheral connector.

Resource Type	Number
IO	24
Clock	4
GND	26
+1.2 V	2
+1.5 V / +1.8 V / +2.5 V	2
+3.3 V	2
+5 V / +12 V	12

In each socket connector, the resources are placed on the same position. The +12 V and +5 V pins were directly connected to the ATX connector and the low voltage power supplies are generated by the PTH05050 modules.

Up to six peripherals for signal generation or acquisition can be attached to the main board. An auxiliary socket was added to accommodate the peripheral used to generate the motion control signals. This last connector has significantly less IO resources when compared with the ones for the signal generation or acquisition peripherals.

#### 4.2.6 Other Features

The main board also includes the features represented Figure 4.7. The 24LC32 I<sup>2</sup>C FLASH memory can be used to storage configuration settings of the application running on the FPGA. RS232 communications are provided by the MAX3221 integrated circuit. The 50 MHz clock is useful to drive the XILINX soft core processor MicroBlaze and the 125 MHz can be easily doubled achieving the maximum clock rate for DSP48A slices. Some additional features as push buttons, switches and Light Emitting Diode (LED) indicators were included.

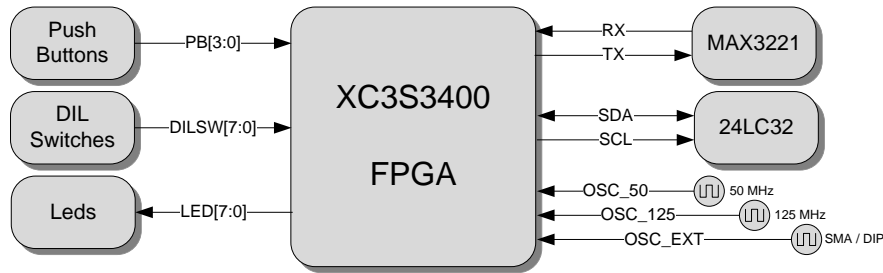


Figure 4.7 - Main board features.

#### 4.2.7 PCB Stack up and Impedance Control considerations

Taking into consideration the most common multilayer PCB structures for manufacturing, a 8 layer PCB stack as represented in Figure 4.8 was adopted. The layer copper thickness determines the minimum track width and clearance achievable. Because of routing, the signal layers copper thickness was set to 17  $\mu\text{m}$ . In each core, the copper thickness on the both layers should be equal leading to the use of 17  $\mu\text{m}$  copper on the GND planes. However, in the power planes 35  $\mu\text{m}$  copper was used to reduce resistance. Components are placed in the top and bottom layers together with the low speed signals routing.

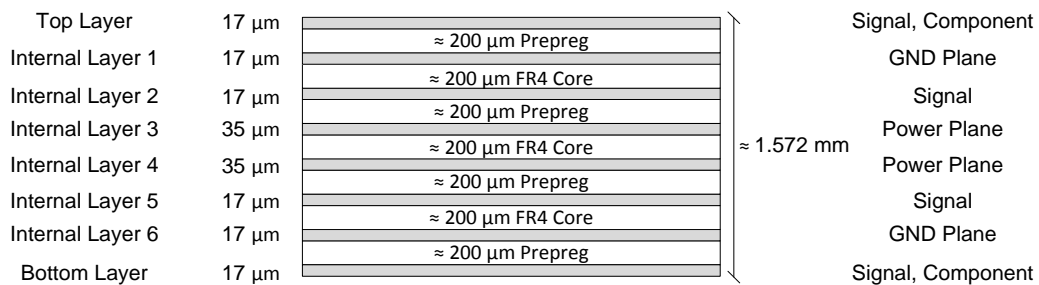


Figure 4.8 - PCB Stackup and Layers.

Since the IO and clock resources of the FPGA are used to interface high speed conversion devices, they were routed as striplines in the internal layer 2 and 5 using the design methodology described in the Appendix III. IO transmission lines are routed to achieve 50  $\Omega$  characteristic impedance. The clock resources transmission lines were designed to meet the 100  $\Omega$  differential impedance specification of the Low Voltage Differential Signaling (LVDS) standard.

## 4.3 IOnic Driver Card

The IOnic Driver Card was designed to generate the probe stimulus. A DAC is used to convert the digital stimulus into an analog voltage signal. This signal is then converted to the probe driver trace current by a transconductance amplifier that can operate in class A or AB to achieve low distortion or low power consumption respectively.

### 4.3.1 Digital to Analog Converter

The Analog Devices AD9707 performs digital to analog conversion at rates up to 175 Mega Samples per Second (MSPS). This converter has excellent dynamic linearity and relatively low power consumption when powered with 3.3 V. Furthermore, its internal temperature compensated reference can be used to set the full scale output current and minimize the external components. The sampling clock is transmitted in LVDS and the input 14 bits digital word is expressed in offset binary format. When inserted in the socket connectors, these peripheral interfaces with the FPGA using the digital signals represented in the Figure 4.9.

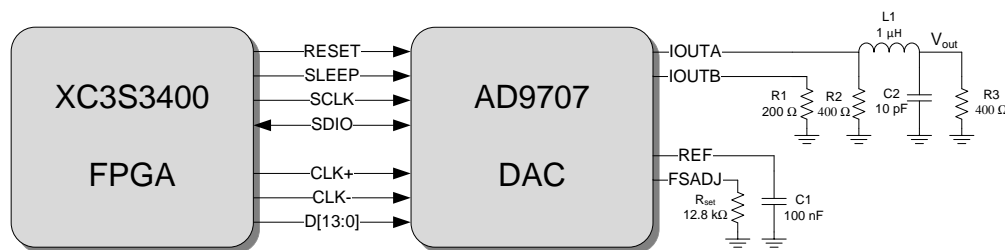


Figure 4.9 - AD9707 DAC to FPGA connections.

SCLK and SDIO form an SPI compliant interface that can be used to configure internal operation parameters of the DAC. The device can enter the power down mode and reduce the power consumption down to 2 mW by asserting the SLEEP pin or changing the internal configuration register. The functions of the several signals to interface the DAC are described in Table 4.7.

Table 4.7 - DAC FPGA interface.

Signal	Direction	Active low - L Active high - H	Function
RESET	Output	L	AD9707 reset signal
SLEEP	Output	H	AD9707 sleep mode activation
SCLK	Output	H	SPI clock signal
SDIO	Bidirectional	H	SPI data signal
CLK	Input	H	LVDS input data clock
D[13:0]	Output	H	Input Data

The output full scale current,  $I_{fs}$ , is adjusted to 2.5 mA and resistors are used to convert the current signal to voltage. Using the internal 1 V reference, the full scale current can be controlled by setting the resistor between the FSADJ pin and the GND reference to

$$R_{set} = 32 \frac{1}{I_{fs}} = 12.8 \text{ k}\Omega . \quad (4.1)$$

Internal reference is decoupled with the 100 nF C1 capacitor. The current output is converted to single-ended complementary voltage signals with R1 and R2 and R3 resistors. Then, the maximum output voltage span is

$$V_{fs} = I_{fs} \frac{R2 \times R3}{R2 + R3} = 0.5 \text{ V} . \quad (4.2)$$

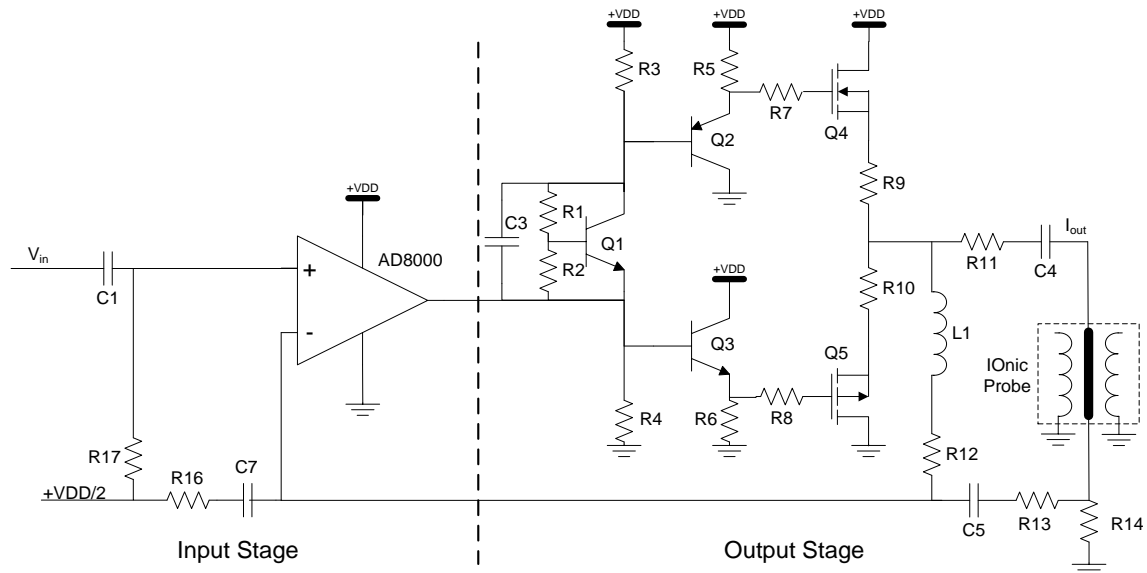
The components L1, C2 and R3 form the DAC output anti-aliasing filter. This second order low pass filter transfer function is

$$T(s) = \frac{R3}{R2 + R3} \frac{\frac{1}{L_1 C_2}}{s^2 + s \frac{L_1 + C_2 R_2 R_3}{L_1 C_2 R_3} + \frac{1}{L_1 C_2}} . \quad (4.3)$$

The filter cut-off frequency was set to about 50 MHz with a quality factor of 0.69 achieving a good transient response while maintaining a relatively low frequency response peak.

#### 4.3.2 Driver Circuit

The probe driver circuit is a high output current transconductance amplifier that is attached to the digital to analog converter. This amplifier is composed by an input stage made up a High performance OPAMP and an output stage, Figure 4.10.

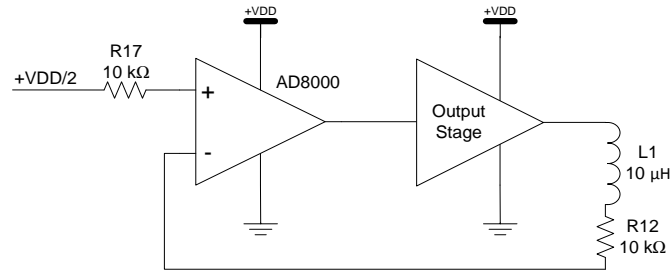


**Figure 4.10** - Driver Circuit.

The input stage comprises an AD8000 OPAMP wired in a non-inverting configuration. Its function is to provide high input impedance, set the steady state voltage level of the output stage at

the middle of the supply voltage and set the dynamic gain. Featuring 100 mA output linear current, a wide operation supply range from 4.5 to 12 V and 1 GHz of Gain-Bandwidth Product (GBW), AD8000 is a good choice for this application.

To understand how the voltage steady state operation point of the output stage is established, the AC path should be ignored, Figure 4.11. In these conditions, the output voltage will follow the input. The inductance L1 is needed to filter the AC component in the output that was set at the middle of the supply voltage.

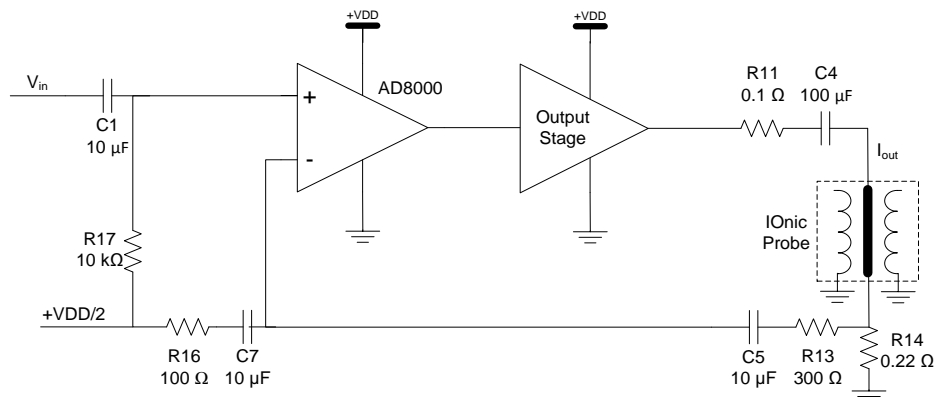


**Figure 4.11** - Input stage and DC feedback.

Additionally, the input stage controls the overall feedback of the transconductance amplifier. As can be seen in Figure 4.12, the probe driver output current is sensed in the 0.22 Ω R14 resistor and used as feedback in the input stage. Capacitors C4, C5 and C7 block the DC component allowing only AC current to flow in the probe driver trace. Hence, the transconductance gain is

$$\frac{I_{out}}{V_{in}} = \frac{1}{R14} \left( 1 + \frac{R13}{R16} \right) \approx 18 \text{ S}. \quad (4.4)$$

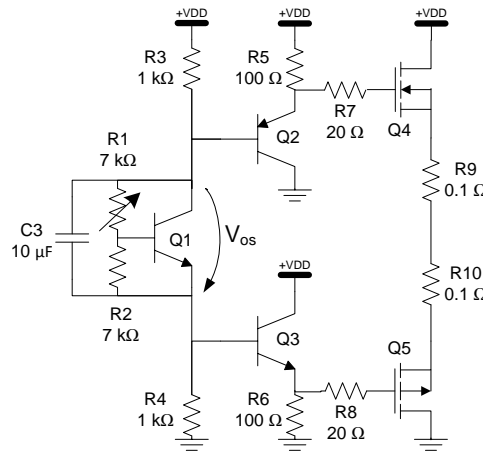
The capacitor C4 should provide very low impedance over the frequency operation range, otherwise it can limit the current supplied to the probe. As the input voltage AC component is added in the positive input of the OPAMP, the AC input impedance is equal to R17. To make the transconductance gain unitary, a voltage divider at the input of the circuit is used.



**Figure 4.12** - Probe driver circuit input stage and AC feedback.

Output current is generated through the output stage which can operate in class A or class AB. The circuit can be powered with any supply voltage from 5 V to 12 V and the operation mode can be

set by changing jumper locations. Biasing is done using the Voltage Base to Emitter (VBE) multiplier circuit composed by R1, R2 and Q1 in Figure 4.13.



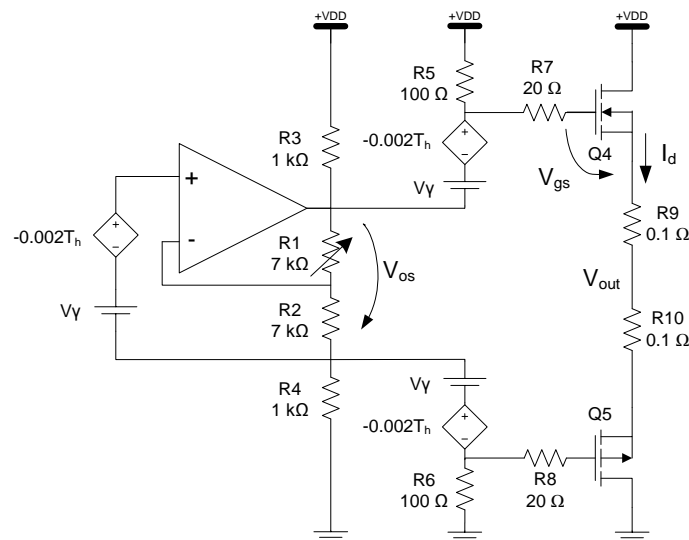
**Figure 4.13** - Output Stage.

Assuming that the base current of the transistor Q1 is negligible, the biasing offset voltage is

$$V_{os} = V_T \left( 1 + \frac{R1}{R2} \right) \quad (4.5)$$

where  $V_T$  is the base-emitter forward biasing voltage of Q1. The control of the bias current on the output transistors Q4 and Q5 is made by setting the resistor R1 and consequently change the VBE multiplier offset voltage. Q3 and Q2 bipolar transistors are used to drive the Metal Oxide Semiconductor Field Electric Transistors (MOSFET) Q4 and Q5 gates.

The VBE multiplier is also responsible for the thermal compensation of the output stage devices. As the base-emitter voltage drop on a bipolar transistor has thermal coefficient of -2 mV/°C, the thermal compensation is implicit on the operation of the VBE multiplier. The thermal compensation model for the output stage is represented in Figure 4.14.



**Figure 4.14** - Output stage thermal compensation mechanism.

All the relations in the system are highly dependent on the proximity of the devices to enable a strong thermal coupling. In the model, the parameter  $T_h$  is the temperature in the heatsink. With the increasing of the heatsink temperature, the  $V_{OS}$  offset voltage decreases leading to a lower biasing current.

To study the amplifier behavior to the ambient temperature, the incremental model for the thermal compensation mechanism in Figure 4.15 derived. As the output is at the middle supply voltage, and assuming that the MOSFETs Q4 and A5 are perfectly matched, the bisection theorem can be applied to the circuit. MOSFETs thermal coefficients depend on the power dissipation. Typically MOSFETs have positive thermal coefficients but after a certain limit of dissipation, their thermal coefficient becomes negative. The MOSFET -1 mV/°C thermal coefficient was extracted from the datasheet evaluating

$$\frac{\Delta V_{gs}}{\Delta T_a}, \quad (4.6)$$

when the drain current is equal to the 500 mA biasing current. From the same point of the MOSFET characteristic was registered the equivalent transconductance  $gm$  equal to 8 S. The thermal resistance represented the thermal path from the transistors silicon to the PCB and in the selected package is about 12 °C/W

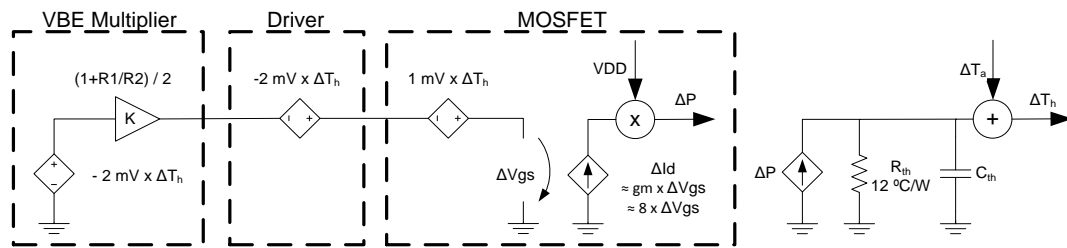


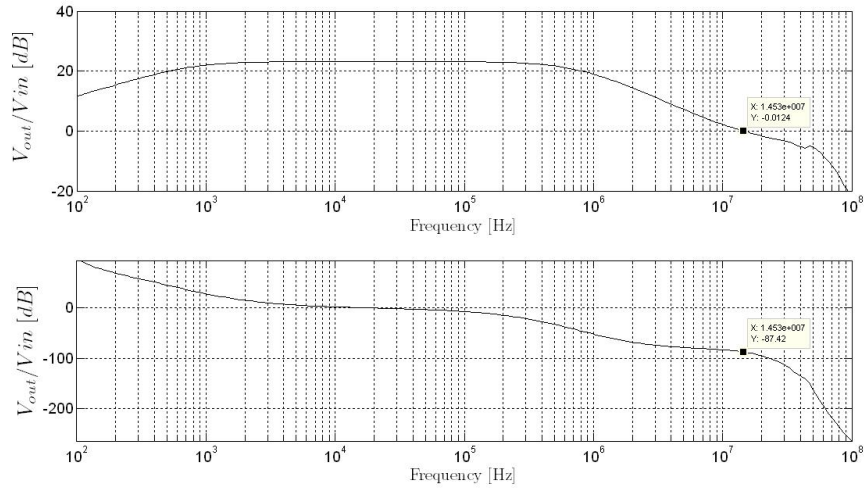
Figure 4.15 - Incremental model for thermal compensation.

Using the previous model, the thermal response to ambient temperature variations despising thermal capacitive effects is

$$\frac{\Delta I_d}{\Delta T_a} = \frac{-1 \times 10^{-3} \left( 2 + \frac{R1}{R2} \right) \times gm}{1 + 1 \times 10^{-3} \left( 2 + \frac{R1}{R2} \right) \times gm \times VDD \times R_{th}}. \quad (4.7)$$

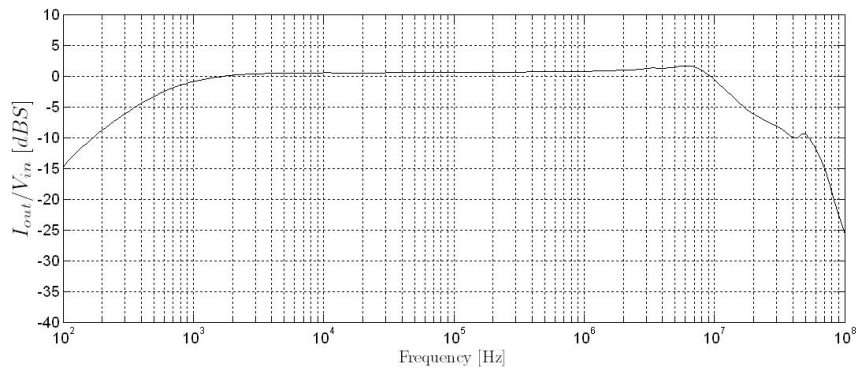
When powered with 12 V and a steady state biasing current of 500 mA, the circuit biasing current thermal coefficient is - 6.2 mA/°C. The thermal compensation mechanism is very important to avoid thermal runaway and damaging of the circuit.

After project and assembly a prototype circuit, the stability of the transconductance amplifier was evaluated by using a Agilent 4395A spectrum analyzer measuring their voltage open-loop response when loaded by the 0.22 sensing resistor, Figure 4.16, where the phase margin observed is about 92.5 °.



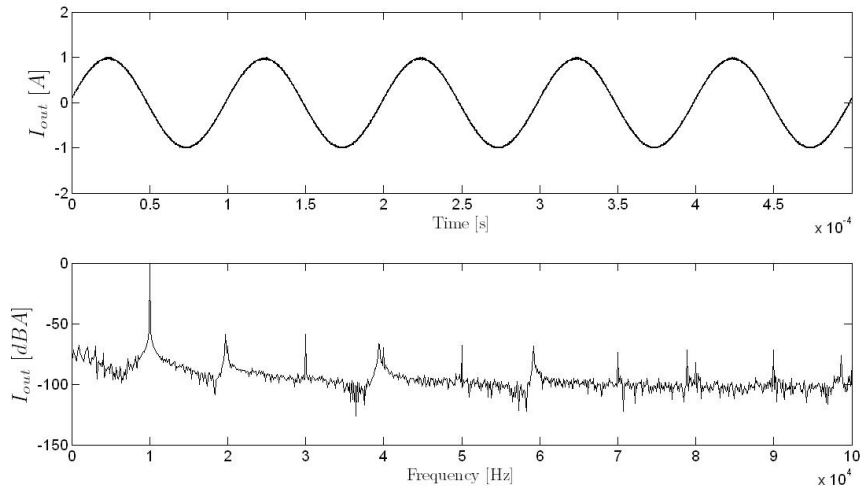
**Figure 4.16** - Probe driver circuit voltage open loop frequency response.

Also, the closed loop was evaluated. Based on the results shown in Figure 4.17, the circuit is able to drive the probe from about 1 kHz to 14 MHz with a very flat frequency response.

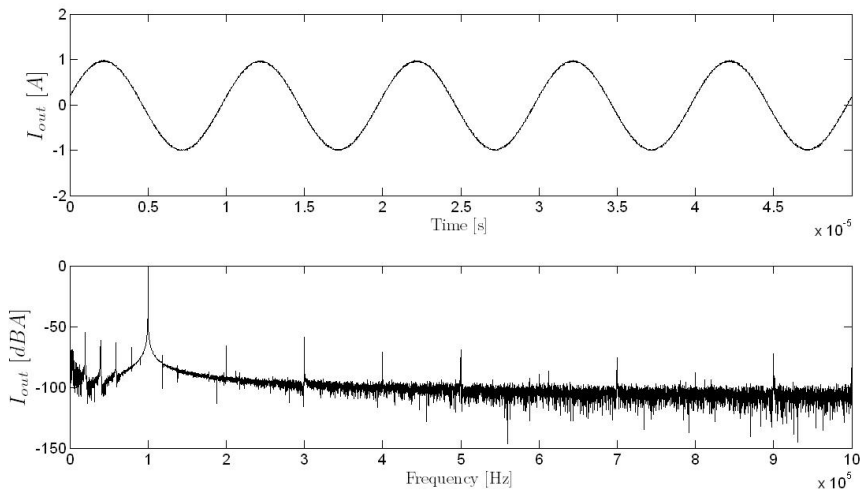


**Figure 4.17** - Probe driver circuit closed loop frequency response.

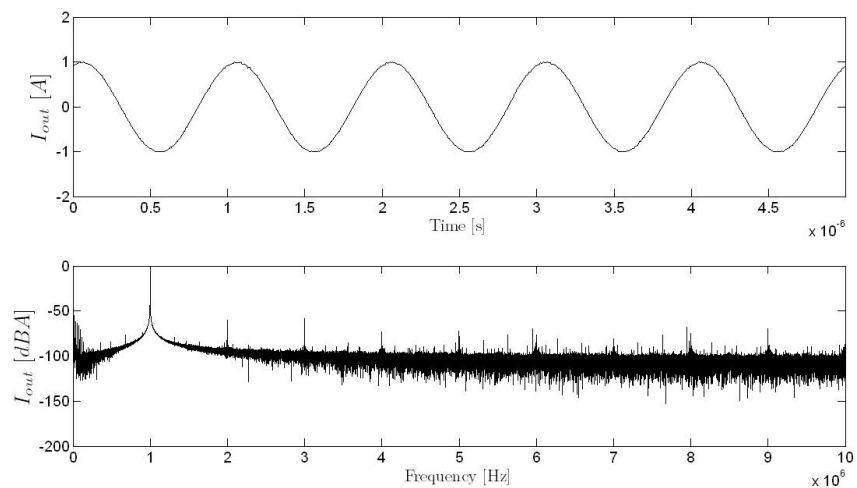
To evaluate the distortion and noise generation by the driver circuit, their response was analyzed. Making use of a TTI TG1010A function generator and a Agilent 54622A 250 MSPS oscilloscope, the voltage across the sense resistor was acquired for 1 A sine waves output currents. These sequences were processed by the Matlab Discrete Fourier Transform (DFT) algorithm and the Total Harmonic Distortion (THD) was calculated. The THD values for the four analyzed frequencies are described in Table 4.8 together with the generator THD extracted from their datasheet. Figure 4.18 to Figure 4.21 shows the output current signal and the respective frequency domain representation for 10 kHz, 100 kHz, 1 MHz and 10 MHz frequencies.



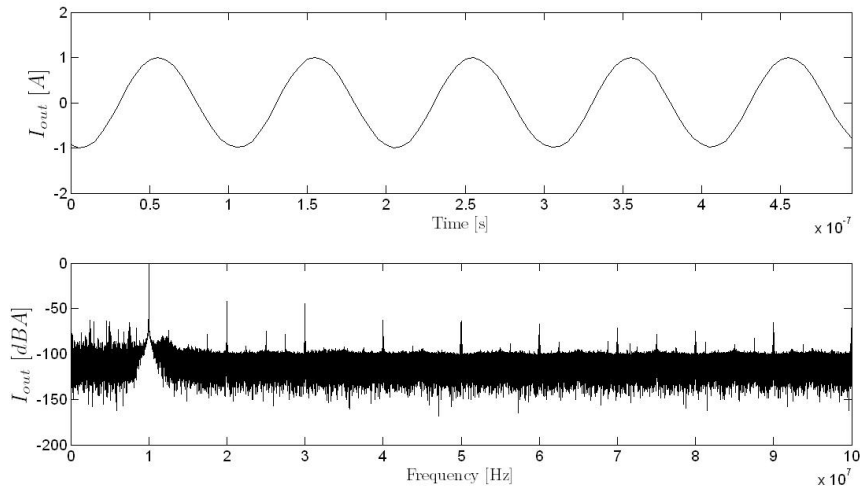
**Figure 4.18** - Probe driver circuit performance for 10 kHz, 1 A amplitude sine wave output current.



**Figure 4.19** - Probe driver circuit performance for 100 kHz, 1 A amplitude sine wave output current.



**Figure 4.20** - Probe driver circuit performance for 1 MHz, 1 A amplitude sine wave output current.



**Figure 4.21** - Probe driver circuit performance for 10 MHz, 1 A amplitude sine wave output current.

The measured THD includes not only the distortion introduced by the driver circuit but also the distortion of the generator output signal. Also, there are spurious components on the generator output voltage that may interfere with the measurement. Thus it is very difficult to conclude about the absolute value of the circuit THD. However, the circuit seems to introduce very low distortion as the measured THD is close to the maximum THD announced by the generator manufacturer.

**Table 4.8** - Probe Driver Circuit THD.

Frequency	Measured THD [dB]	TG1010A THD [dB]
10 kHz	- 51.1	< - 60
100 kHz	- 51.0	< - 60
1 MHz	- 58.2	< - 50
10 MHz	- 31.8	< - 35

## 4.4 IOnic Acquisition Card

The IOnic acquisition card was designed to amplify the probe output signal and to perform their conversion to the digital domain as they can be read by the FPGA. It is composed by an ADC and a PGA.

### 4.4.1 Analog to Digital Converter

The analog to digital conversion is achieved by the 14 bit resolution AD9246 ADC. There are three commercial versions of the circuit with different maximum sampling rates of 80, 105 and 125 MSPS and compatible packaging. In the 125 MSPS version, this converter consumes only 395 mW when powered with a 1.8 V source. Furthermore, the output data register can be configured to generate offset binary, gray code or two's complement codes. The AD9246 features outstanding dynamic specifications achieving an Effective Number of Bits (ENOB) of 11.7 when converting a 10 MHz sine wave. The analog to digital interface with the FPGA can be seen in Figure 4.22. The

internal voltage can be set to 0.5 V or 1 V by leaving the sense pin open or connecting it to the GND reference. This reference controls the input conversion range and is decoupled using the capacitor C1. To achieve maximum dynamic performance, the ADC input should be connected in differential mode.

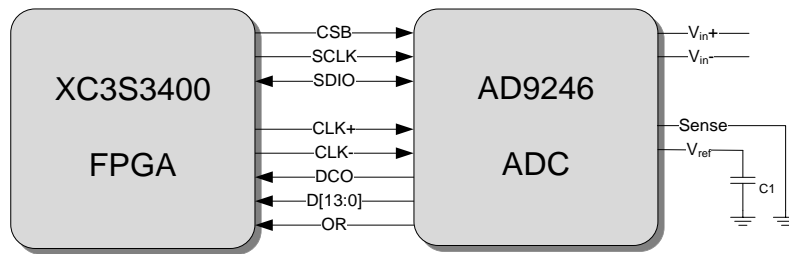


Figure 4.22 - AD9246 ADC to FPGA interface.

AD9246 internal operation mode can be configured by an SPI compliant interface. When a new sample is converted the AD9246 asserts the data clock output, DCO signal. The signal OR indicates that the input voltage has exceeded the maximum of the conversion range. The function of each signal for interfacing the ADC is described in Table 4.9.

Table 4.9 - ADC FPGA Interface.

Signal	Direction	Active low - L Active high - H	Function
CSB	Output	L	Chip Select
SCLK	Output	H	SPI clock signal
SDIO	Bidirectional	H	SPI data signal
CLK	Input	H	LVDS sampling clock
DCO	Input	H	Output data clock
D[13:0]	Input	H	Converted data
OR	Input	H	Over range indication

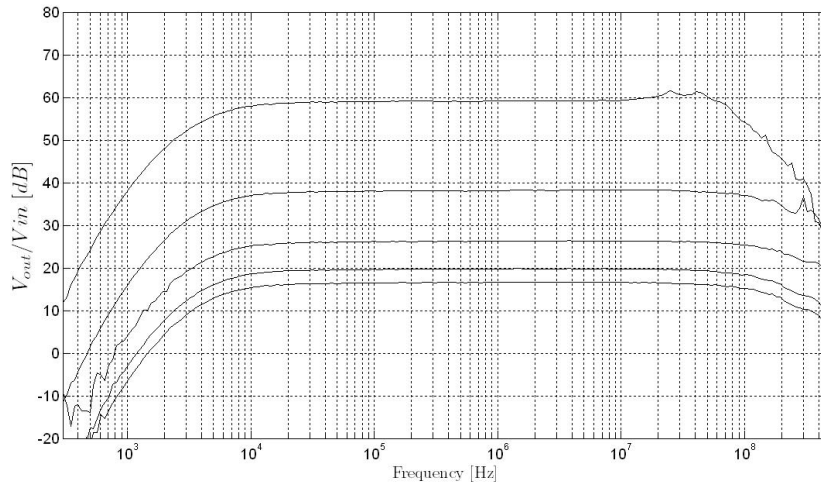
#### 4.4.2 Programmable Gain Amplifier

To extend the input dynamic range, an amplification chain composed by a 20 dB pre-amplifier and a 40 dB maximum digital controlled amplifier was designed. The pre-amplification is achieved with the low noise amplifier AD8351 also used on the IOnic Active probe. Controlled gain is implemented with an AD8369 with gains from -5 dB to 40 dB with 3 dB steps. Unlike conventional programmable gain amplifiers, the AD8369 operation is based on controlling the transconductance of the output stage leading to a constant bandwidth in all the possible gains.

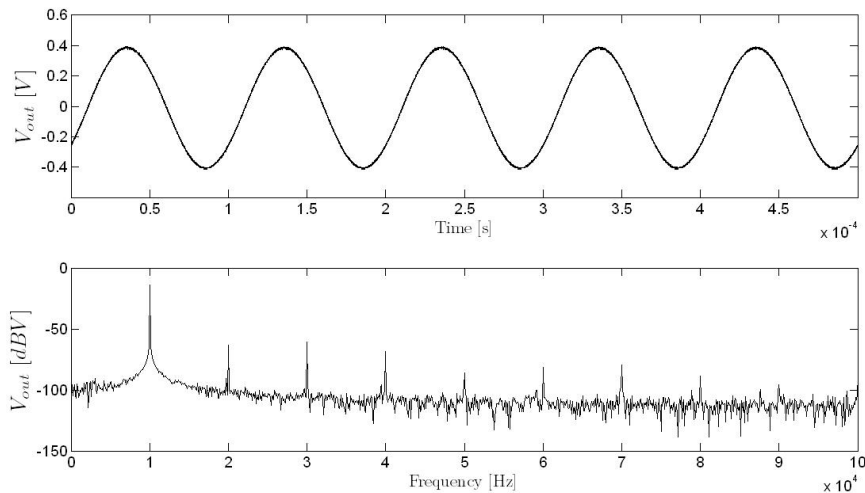
. The frequency response of the programmable gain amplifier was characterized using the Agilent 4395A spectrum analyzer. The overall gain for the tested codes is described in Table 4.10 and the respective frequency response is shown in Figure 4.23.

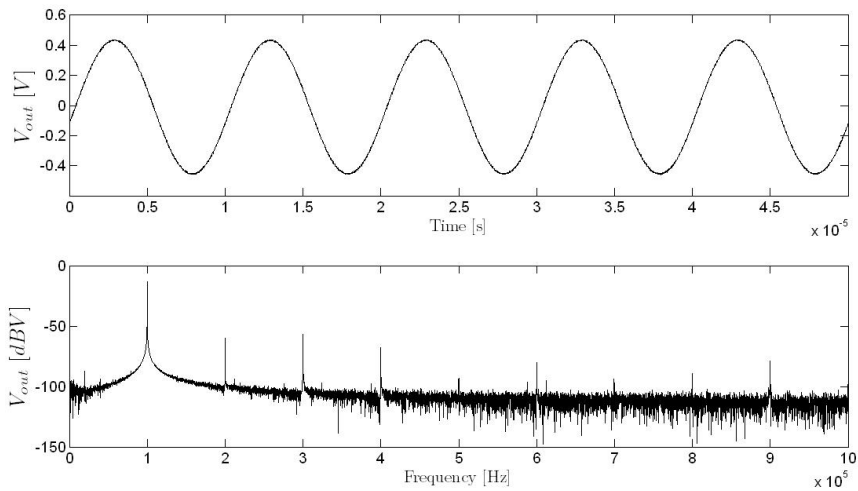
**Table 4.10** - Gain codes and overall gain.

Gain Code	AD8369 Gain [dB]	Overall Gain [dB]
0001	-2	18
0010	1	21
0100	7	27
1000	19	39
1111	40	60

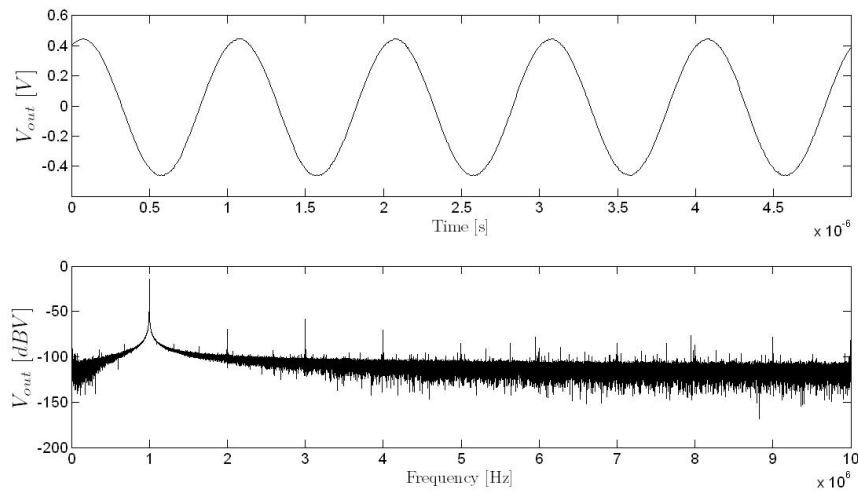
**Figure 4.23** - PGA frequency response for the selected gains.

As can be seen in Figure 4.23, this programmable gain amplifier can be used from 10 kHz to 50 MHz with a very flat frequency response. To study the distortion, the same equipment used to characterize the probe driver was used. Figure 4.24 to Figure 4.27 shows the output voltage signal and the respective frequency domain representation for 10 kHz, 100 kHz, 1 MHz and 10 MHz, 5 mV amplitude input sine waves. The acquired signals were processed by the Matlab DFT algorithm and the Total Harmonic Distortion was calculated. The THD values for the four analyzed input frequencies are described in Table 4.11 together with the generator THD extracted from their datasheet.

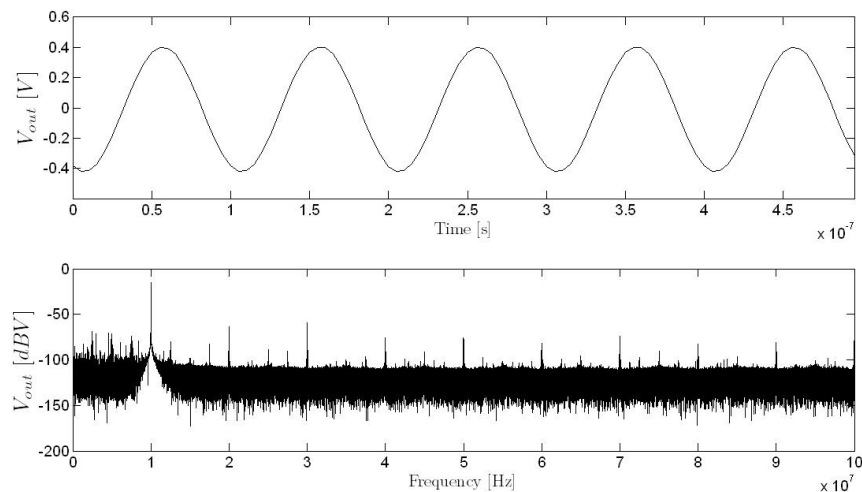
**Figure 4.24** - PGA performance for 10 kHz, 0.5 mV amplitude sine wave input voltage.



**Figure 4.25** - PGA performance for 100 kHz, 0.5 mV amplitude sine wave input voltage.



**Figure 4.26** - PGA performance for 1 MHz, 0.5 mV amplitude sine wave input voltage.



**Figure 4.27** - PGA performance for 10 MHz, 0.5 mV amplitude sine wave input voltage.

THD results for high frequency are close to the generator THD maximums. However, at 10 and 100 kHz the measured THD deviates from the expected results by consulting the devices datasheets.

This may be caused by the very low amplitude on the generator output or some other issue related with the generator.

**Table 4.11** - Programmable gain amplifier THD.

Frequency	Measured THD [dB]	TG1010A THD [dB]
10 kHz	- 44.4	< - 60
100 kHz	- 42.0	< - 60
1 MHz	- 60.4	< - 50
10 MHz	- 48.5	< - 35

## 4.5 Motion Control Card

To enable the control of a XY table, an additional peripheral card was designed. This peripheral has stepper control devices for three different axes. L297 together with L298 integrated circuits can be used to control and drive a wide range of stepper motors. The L297 generates stimulus used by the L298 driver to set the stepper motors phases. With this combination, the system can control unipolar and bipolar step motors with a maximum current per phase of 2 A. Only 5 signals are needed to control the motion on a axis, their function is described in Table 4.12.

**Table 4.12** - L297 stepper motor controller to FPGA interface.

Signal	Direction	Active low - L Active high - H	Function
RESET	Output	L	Chip reset
CLK	Output	H	Step clock
CW/CCW	Bidirectional	H	Clockwise or counterclockwise step
HALF/FULL	Input	H	Half or full step
ENABLE	Input	H	Chip Enable

## 4.6 Budget and Prototyping

Three inquiries for the PCBs production have been requested and the final choice between them was made by selecting the lowest price. The budget of a complete system to operate the IOnic Plus with 2 driver cards, 4 acquisition cards and a motion control card is described in the Appendix IV. The unitary price of each board including the PCB and the components is shown in Table 4.13.

**Table 4.13** - ECscan system overall production cost (without assembly).

Quantity	Item	Unitary Price (€)	Price (€)
1	FPGA Board	336.97	336.97
1	Peripherals Board	50.89	50.89
2	IOonic Driver Card	36.17	72.34
4	IOonic Acquisition Card	96.18	384.72
1	Motion Control Card	62.03	62.03
<b>Total</b>			906.95

By using several high performance integrated circuits, the system becomes a very expensive solution. Furthermore, the four ADCs used contribute with 336.3 € representing about 37 % of the overall production costs. For this prototype the assembly of the integrated circuits will be complete on the IST Taguspark facilities. By this reason the price of assembly operations was not accounted.

The Main board has 220x180 mm dimension and is composed by two PCBs that are attached side by side as shown in Figure 4.28.

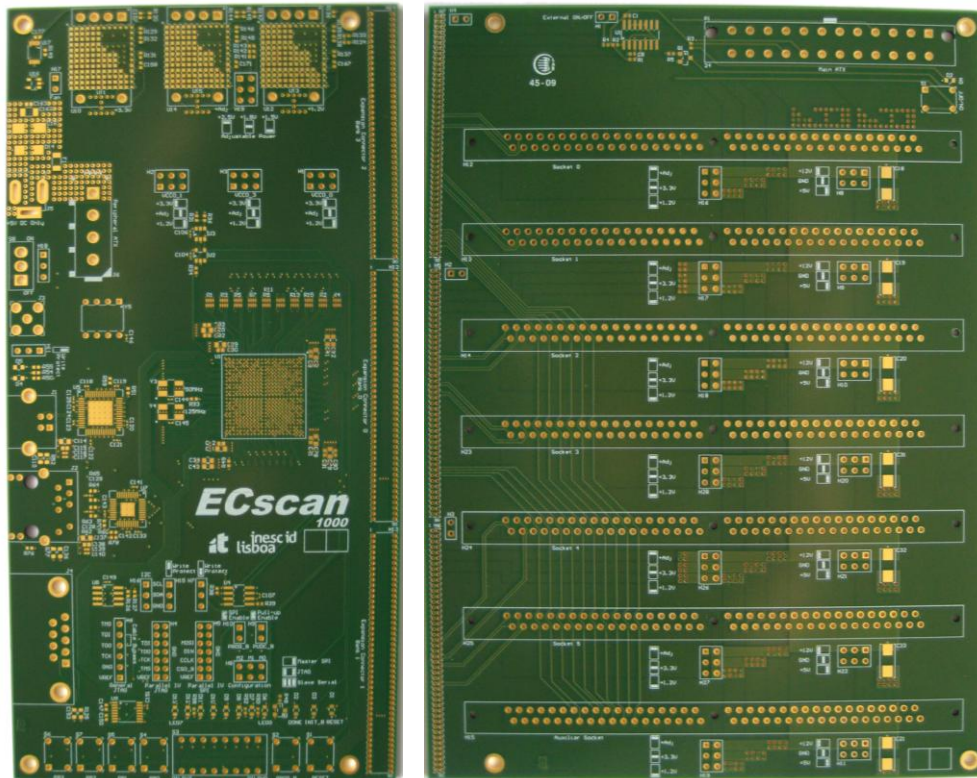


Figure 4.28 - Main Board PCBs.

The IOnic driver card PCB has 108x40 mm and can be seen in Figure 4.29. The exposed copper area highlighted and the four holes at their corners will be used to attach the probe driver circuit heatsink.

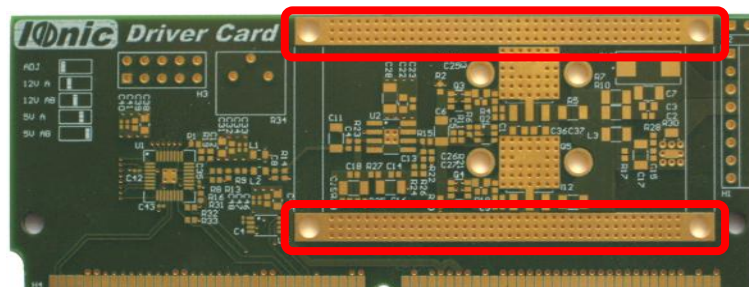
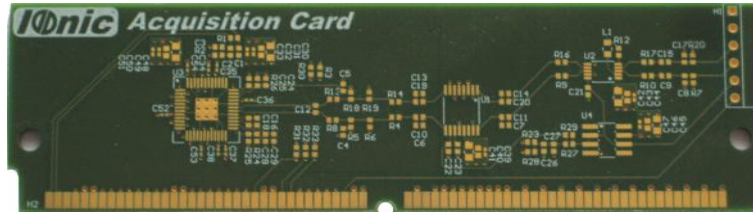


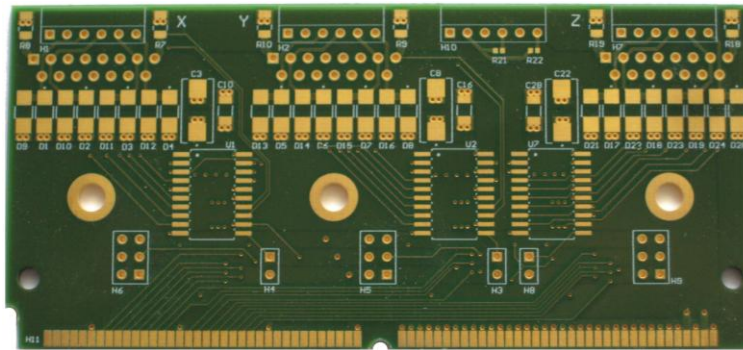
Figure 4.29 - IOnic Driver Card PCB.

An IOnic acquisition card PCB can be seen in Figure 4.30 with external dimension of 108x30 mm.



**Figure 4.30** - IOnic Acquisition Card PCB.

Finally, a motion control card PCB is shown in Figure 4.31 with 108x50 mm external dimension.



**Figure 4.31** - Motion Control Card PCB.

## 4.7 Summary

In this chapter, the development and prototyping of ECscan hardware was described. This new approach enables the use of multiple digital signal processing algorithms and an extended frequency operation range from 10 kHz to 10 MHz, overcoming the limitations found in the preliminary version. The system was made highly reconfigurable through the use of a programmable logic device and an architecture that enables multiple combinations of peripherals for signal generation or acquisition. Furthermore, several communication interfaces has been included making easy the connection of the new system to personal computers and networks. Since the ECscan system hardware is already described, the next step is to describe the embedded software application.

# Chapter 5 – ECscan NDT System Software

## 5.1 Introduction

A software application for the FPGA processing core has been designed. This application is responsible for the digital generation and processing of the probe signals and the control of the sensor position. The central hardware core on this application is the XILINX MicroBlaze soft-core processor set up to configure the probe signals generation and to receive amplitude and phase digital processed data performing the defect detection. The software application on the MicroBlaze communicates with a high level application running on personal computers through one of the included communication interfaces. The high level application will allow the configuration of acquisition parameters, the implementation of powerful visualization modes and post-processing features. The high speed digital signal processing and the communication interfaces control tasks are done upon hardware peripherals attached to the main processor.

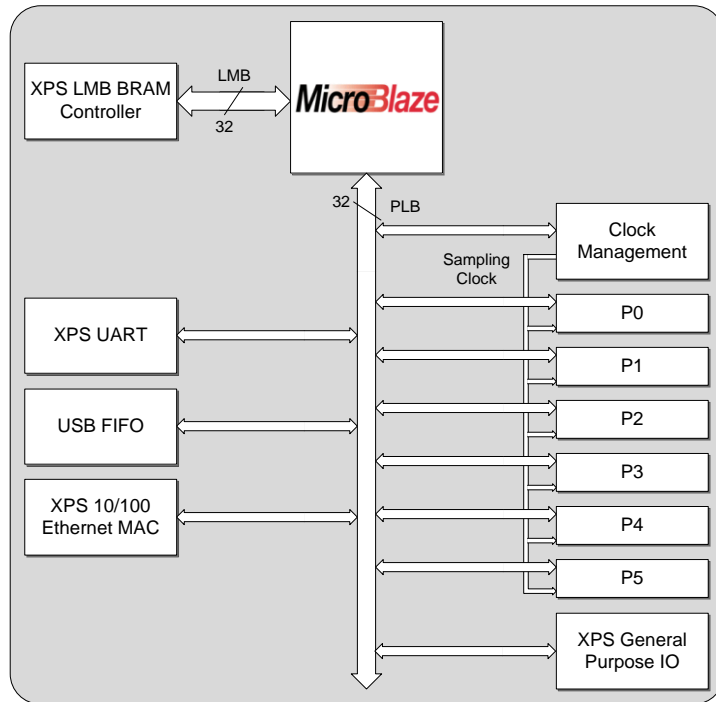
## 5.2 Embedded application development

The main block on the developed application is the XILINX MicroBlaze soft-core processor. The application running on this processor controls the positioning of the probe, the digital generation and processing of the probe signals on the peripherals and the data transmission over the communication interfaces. MicroBlaze is a 32-bit Reduced Instruction Set Computer (RISC) Harvard architecture soft-core processor with an instruction set optimized for embedded applications. This solution supports complete flexibility to select the combination of peripherals, memory and interface features that are need for a certain application. There are two MicroBlaze versions, a 3 pipeline stage area-optimized and a 5 pipeline stage performance optimized. In this application, as the heavy computational tasks will be executed by custom peripherals connected to the main processor, the 3 pipeline stage version of MicroBlaze was chosen.

High speed digital signal processing tasks and the control of the communication interfaces is ensured by hardware peripherals connected to the main processor by a XILINX Peripheral Local Bus (PLB), Figure 5.1. To configure or exchange data with the peripherals, the application running in the main processor accesses their internal registers which are mapped on the PLB bus. XILINX development tools offer a great number of Intellectual Property (IP) cores that can be used together with the MicroBlaze processor avoiding the need to build all the peripherals used on a certain application. From this group, this application makes use of:

- LMB BRAM Controller - Controls the read and write operations on a configurable size memory block build with BRAM cells;
- XPS UART - Provide RS232 communications using the MAX3221 transceiver;

- XPS 10/100 Ethernet Media Access Controller (MAC) - Used to control and communicate with the DP83848TSQ over the MII interface. This core provides addressing and channel access control mechanisms over the Ethernet network;
- XPS General Purpose IO - IO resources to control the stepper motors controllers in the Motion Control Card.



**Figure 5.1** - Embedded application software blocks.

To complete the application, it was necessary to develop the following three cores:

- USB FIFO Core - Interfaces the CY7C68013A USB 2.0 controller FIFO enabling the embedded application to communicate over the USB bus;
- Signal Generator Core - It consists on a digital data synthesizer set to generate the IOnic Driver Card DAC signals. This core enables the configuration of the output signal waveform as also their frequency, amplitude and phase delay;
- Signal Processor Core - Process the IOnic Acquisition Card ADC output signals generating information about the amplitude and phase of the probe signals.

The peripherals cores P0 to P5 in Figure 5.1 can be configured as Signal Generators or Signal Processors in order to match a certain combination of peripheral cards.

### 5.2.1 USB FIFO Core and CY7C68013A firmware

The USB FIFO is a finite state machine that is controlled by four internal registers available through the PLB bus. Their function is to control the CY7C68013A FIFO interface signals to enable

the MicroBlaze software application to send and receive data over USB. The core hardware is described in the VHDL entities described in Table 5.1.

**Table 5.1** - USB FIFO Core Entities.

Entity	Included In	Function
usb_fifo_core	-	Top level entity
plbv46_slave_single	usb_fifo_core	Provides standardized slave interface between user_logic entity and the PLB Bus.
soft_reset	usb_fifo_core	Generates the software reset for the user_logic entity.
user_logic	usb_fifo_core	Contains the peripheral internal registers and the user hardware.
usb_fifo	user_logic	Implements all the FIFO management tasks.

All the described entities except usb\_fifo were generated using the development tools and provide the hardware needed to interface the PLB bus. The usb\_fifo contains all the hardware to interface the CY7C68013A FIFO and is included in the Appendix V. The interface between the PLB bus and the usb\_fifo entity is ensured by the following internal registers:

- Control Register - Controls the read and write operations on the FIFO;
- Status Register - Peripheral and FIFO status flags;
- Data IN Register - 16 bits data word to be write in the FIFO;
- Data OUT Register - 16 bits data word read from the FIFO.

As the PLB is set to 32 bits wide, only the 16 less significant bits are implemented in the Data IN and Data OUT registers. The function of each bit on the control and status register is described in Table 5.2 and Table 5.3 respectively.

**Table 5.2** - USB FIFO Core control register.

Bit	Type	Name	Function
4-31	R/W	U	None
3	R/W	PKTENDGO	Send packet to host
2	R/W	OUTGO	Read FIFO data word
1	R/W	INGO	Write FIFO data word
0	R/W	U	None

Legend: U - Unimplemented Bit R - Readable W - Writable

**Table 5.3** - USB FIFO Core status register.

Bit	Type	Name	Function
5-31	R	U	None
4	R	DATAOUTV	New data word available from FIFO
3	R	PKTENDRDY	Packet sent confirmation
2	R	OUTRDY	FIFO read confirmation
1	R	INRDY	FIFO write confirmation
0	R	CONNECTED	USB bus connected indication

Legend: U - Unimplemented Bit R - Readable W - Writable

To configure the FX2 platform, an application for the 8051 microprocessor inside the CY7C68013A was developed. The principal function of this application is to set the USB endpoints configuration, initialize the FIFO memory and the FIFO interface. After these tasks are accomplished, the 8051 microprocessor becomes idle waiting for packets committed over the control endpoint. All the data exchanged between the FPGA and the host computer is processed by the FX2 dedicated hardware. In order for the host computer be able to distinguish the developed peripheral, the Peripheral Identifier (PID) and the Vendor Identifier (VID) are set to 0x4605 and 0x0220 and stored together with the 8051 application in the EEPROM connected to the CY7C68013A.

A device driver was developed to host computers using the Cypress proprietary driver cyusb.sys. The driver was changed to match the PID and VID codes referred before and used together with a prototype C# application to communicate with the MicroBlaze application.

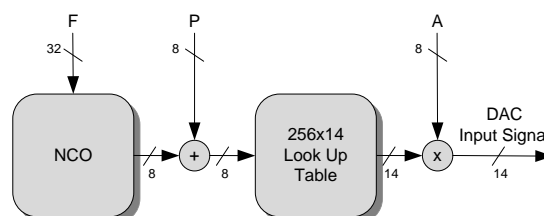
### 5.2.2 Signal Generator Core

The aim for this hardware core is to generate the digital signals to be converted by the IOnic Driver Card ADC. Signal Generator is implemented by the entities described in Table 5.4.

**Table 5.4** - Signal Generator Core Entities.

Entity	Included In	Function
signal_generator_core	-	Top level entity
plbv46_slave_single	usb_fifo_core	Provides standardized slave interface between user_logic entity and the PLB Bus.
soft_reset	usb_fifo_core	Generates the software reset for the user_logic entity.
user_logic	usb_fifo_core	Contains the peripheral internal registers and the user hardware.
signal_generator	user_logic	Implements the digital generation and control of the output signal.

The signal\_generator entity contains logic that implements the data digital synthesizer on Figure 5.2 and is included in the Appendix VI. The Numerically Controlled Oscillator (NCO) is built with a DSP48 slice configured as an accumulator. NCO output is then added with a phase increment and the result is used to address a 14 bits wide Read Only Memory (ROM). This ROM acts as a look up table to create a sine wave whose amplitude is controlled with the last multiplier. In order to control the relative phase of several signal generator cores, the same reset signal is shared between all the signal generators in the application.



**Figure 5.2** - Signal Generator logic.

The frequency, phase and amplitude of the output sine wave is controlled by internal registers F, P and A respectively, according to the relations

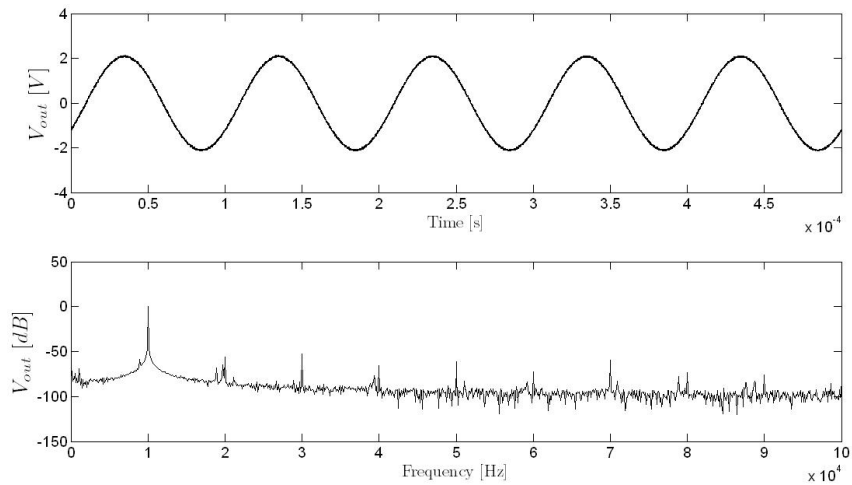
$$f_o = \frac{F}{2^{32}} f_{clk} , \quad (4.1)$$

$$P_o = \frac{P}{2^8} 360 , \quad (4.1)$$

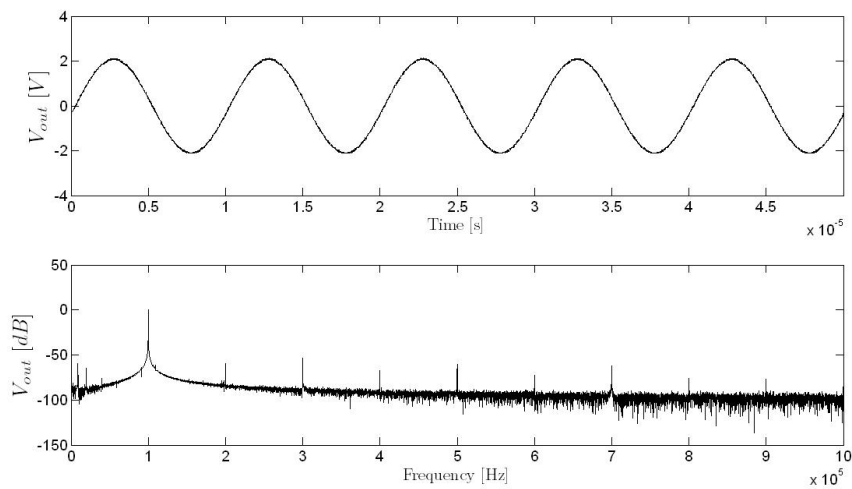
and

$$A_o = \frac{A}{2^8} 2 . \quad (4.1)$$

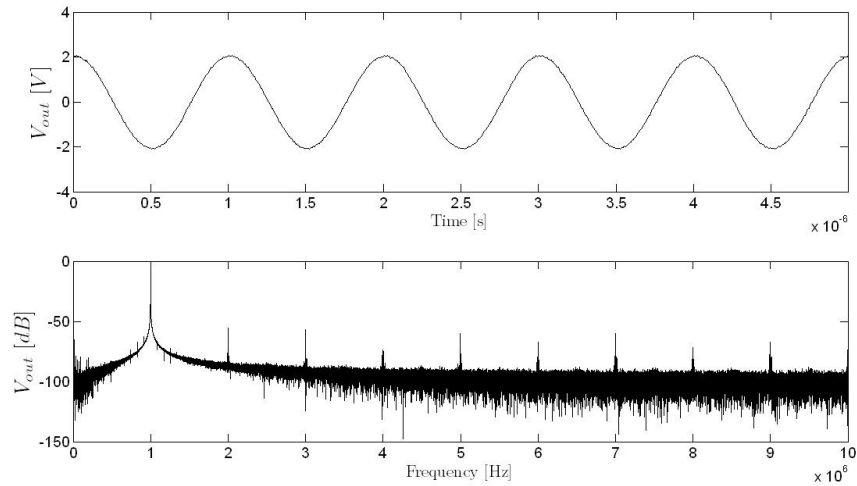
Using an XtremeDSP IV evaluation kit, which contains a XILINX FPGA featuring DSP48 slices and two ADC/DAC pairs, the signal generator output was verified. The DAC device is a 14 bits AD9772A with sampling frequency set to 125 MHz. Figure 5.5 to Figure 5.4 shows the output signal and the respective frequency domain representation for a 10 kHz, 100 kHz, 1 MHz and 10 MHz sine waves.



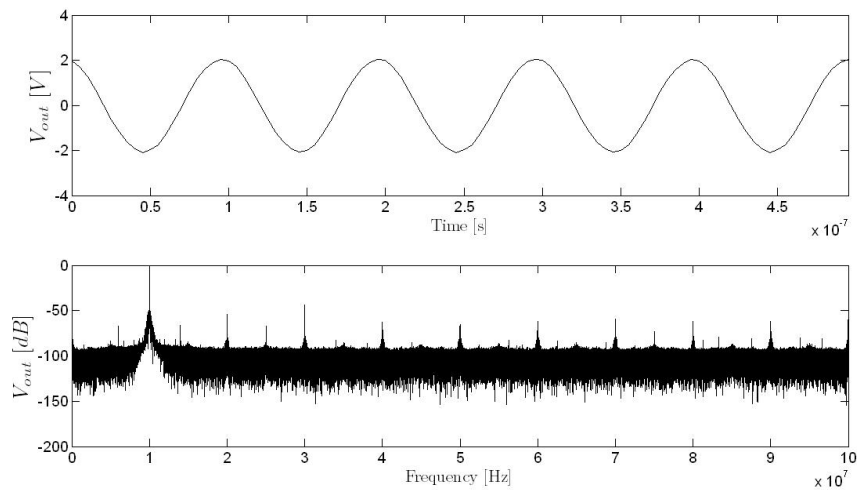
**Figure 5.3** - 10 kHz, 2 V amplitude sine wave synthesized by the signal generator core.



**Figure 5.4** - 100 kHz, 2 V amplitude sine wave synthesized by the signal generator core.



**Figure 5.5** - 1 MHz, 2 V amplitude sine wave synthesized by the signal generator core.



**Figure 5.6** - 10 MHz, 2 V amplitude sine wave synthesized by the signal generator core.

The converting device used to achieve these results is different from the one included in the IOnic driver cards. However, the results with the chosen ADC should very similar as the sampling frequency and the bit number remain the same.

## 5.3 Summary

In this chapter, the ECscan software application has been described. It is composed by the XILINX MicroBlaze soft-core processor and some peripherals repository. The application became complete with the development of an additional core for USB communications and two cores to generate and process the probe signals. The number of cores on each type can be configured to match a certain combination of peripheral cards.

## Chapter 6 - Conclusions

This work presented the study, modeling and validation of a new concept of eddy currents probe together with the development of dedicated electronic systems to meet their new requirements. To accomplish the proposed objectives, it was necessary to develop knowledge in areas from mechanical technology, electromagnetism and embedded systems, extending the scope of the presented dissertation. From all the activities and discussions, the following conclusions were registered.

Eddy currents non-destructive testing can be used to perform a great number of characterization measurements. Eddy currents remain the preferred method for inspecting metallic welds and there are several advantages associated with this practice. This non-destructive method has been successively improved and today it is being supported by advances on multiple scientific areas.

Advances on mechanical technology justify the constant demand for improved non-destructive testing techniques. Today, by their metallurgical characteristics, FSW is presented as one of the greatest challenges on NDT technology. Their consolidation and industrial application requires the development of techniques able to detect the very subtle defects taking influence over the integrity of the welded structures.

When inspecting FSW specimens with the IOnic probe, it is verified that the presence of defects generates a distinctive characteristic on the output signals which is very easy to interpret. The verified characteristic is proportional to the dimension of the three tested defects in all the frequencies used. Based on the presented results, this new concept leads to a very sensitive and also effective probe able to detect micro size defects.

IOnic probe operation can be understood using simple electromagnetism examples. Nevertheless, the FEM was useful to verify eddy currents behavior in the test material and to predict the probe response to the standard defect. The FEM models were corroborated by experimental validation using the preliminary version of the NDT system.

The preliminary NDT system was able to handle the probe during the experimental validation and was applied to the inspection of FSW specimens under industrial conditions. Nevertheless, to explore all the IOnic probe potential a new and improved system was necessary. The second NDT system, introduces the use of digital generation and processing of the probe signals supported by a FPGA based processing core and conversion devices.

The ECscan system was developed with the purpose of being highly reconfigurable allowing operation with the several probes configurations. This was achieved through a special architecture that enables multiple combinations of peripherals for signal generation or acquisition and the characteristics of the processing core. Furthermore, the new approach will allow exploring several digital signal processing algorithms.

Almost all the future work suggestions are focused on further development of the proposed system and probe concept. However, there are some issues regarding the electromagnetic phenomena behind eddy currents that could be accessed:

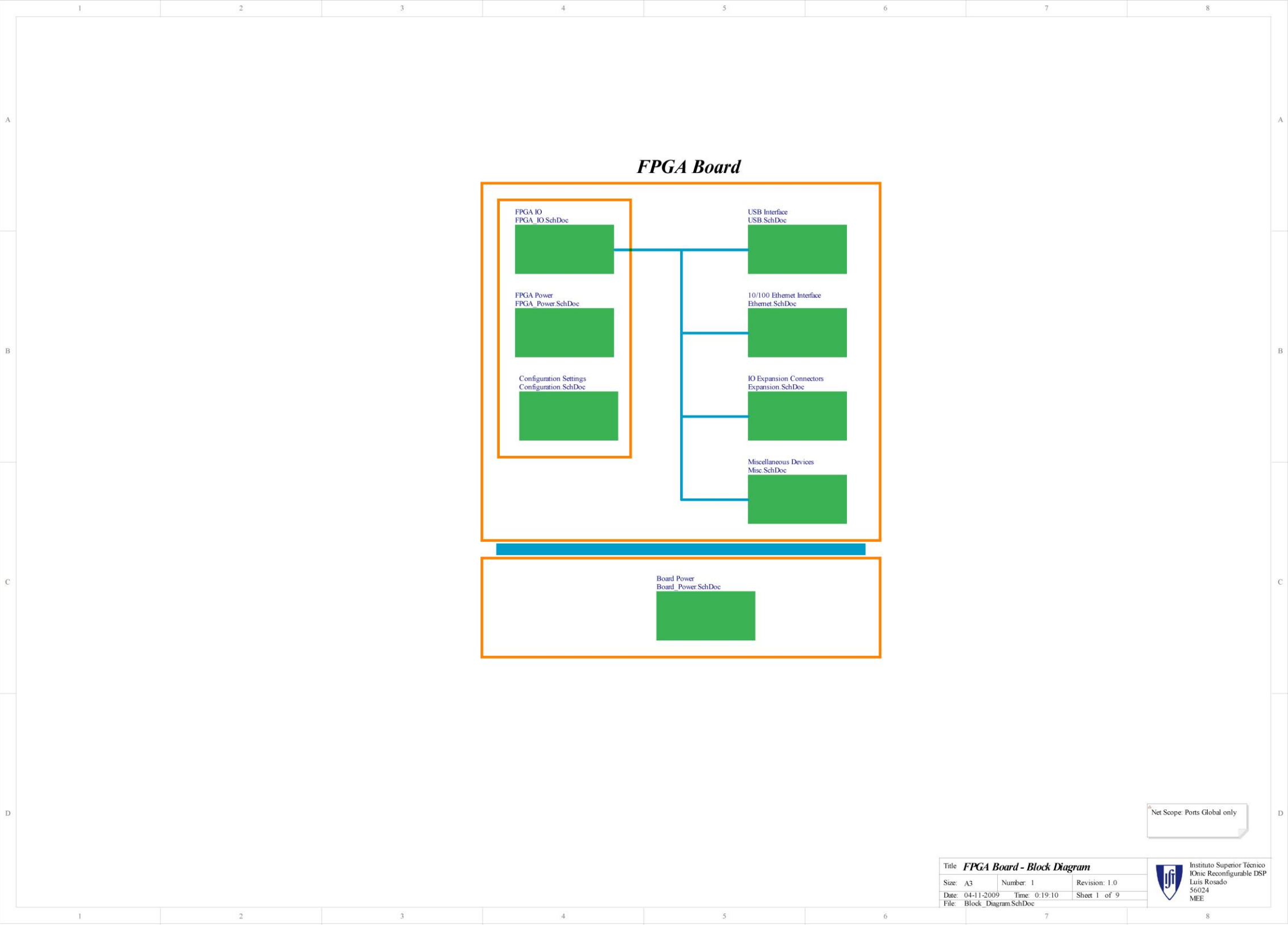
- Perform a more intense research regarding the physical principles of eddy currents non-destructive testing. Specifically, it would be interesting to study the eddy currents density taking into account the relation between frequency and the superficial density;
- Model and study the IOnic Plus and IOnic Array with a similar approach followed in the case of the IOnic concept. By doing this, it will be possible to understand the eddy currents disposition when varying the amplitude and phase difference between the multiple driver traces;
- Continue the prototyping of the ECscan system and develop new stimulus and analysis algorithms. The new system enables the implementation of multi-frequency and pulsed eddy currents and to explore a multitude of new stimulus patterns;
- Design a convenient probe shielding and enclosure, cabling and a standard connection method for the multiple IOnic probes that can be used with the ECscan;
- Develop personal computers software to communicate with the system enabling powerful data visualization modes and post-processing features;
- Study a new probe concept based on solid-state magnetic field micro sensors (Magnetic Tunnel Junctions, Spin Valves and GMR) or micro coils arrays. By using this type of sensors it should be possible to improve spatial resolution and sensibility for micro size defects.

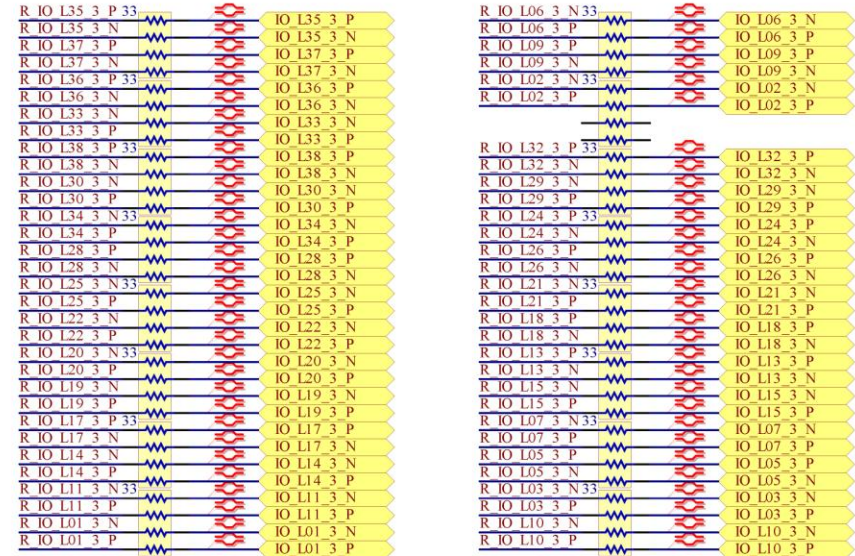
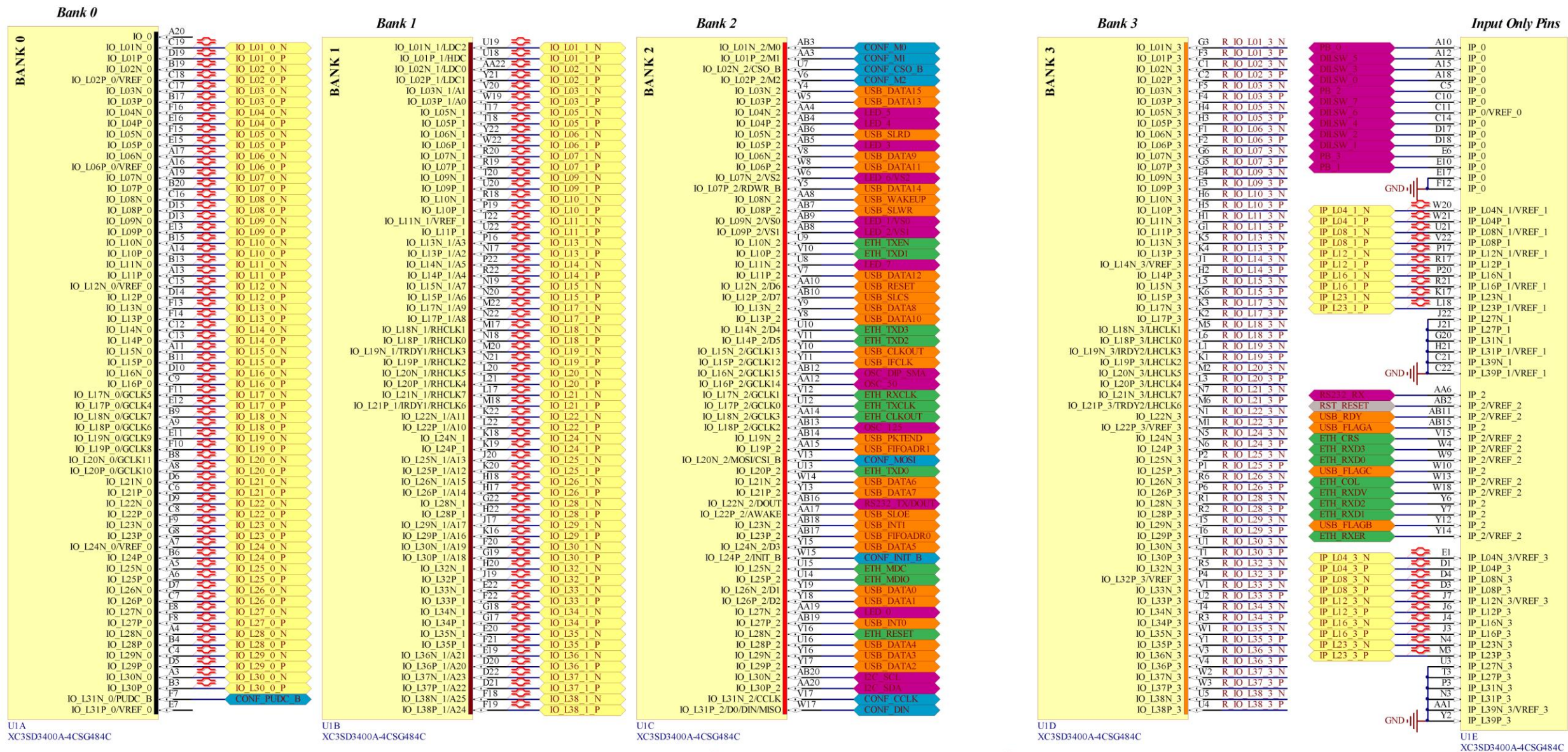
## References

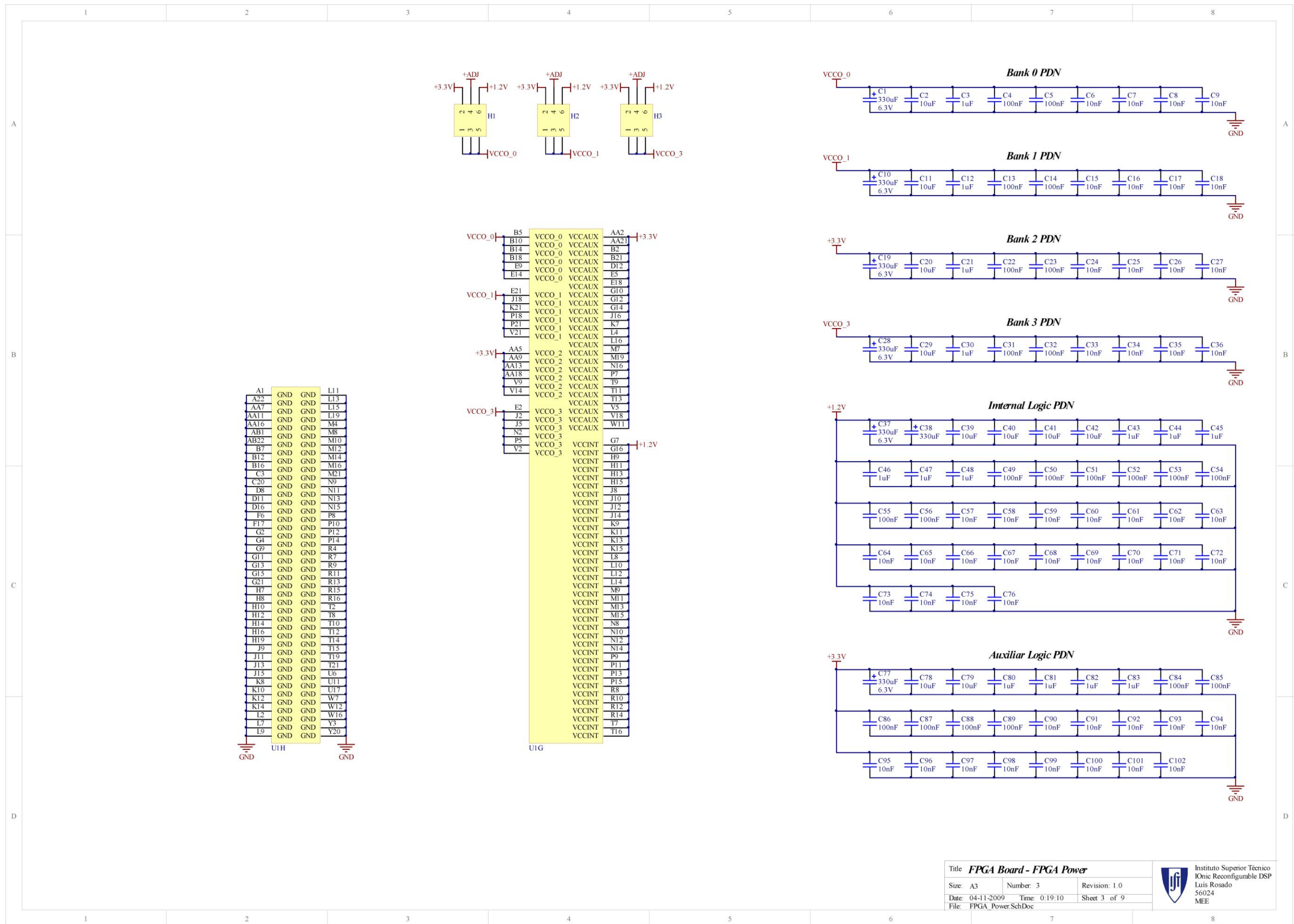
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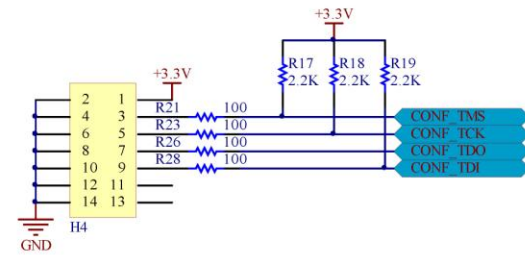
Appendix I - ECscan System Schematics



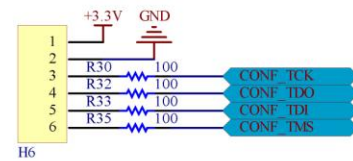




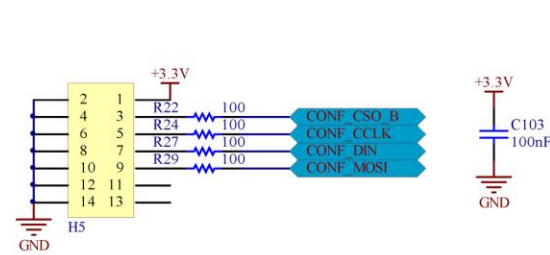
**Parallel IV JTAG Connector**



**General JTAG Connector**

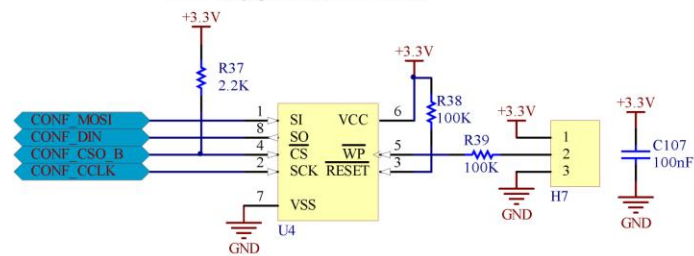


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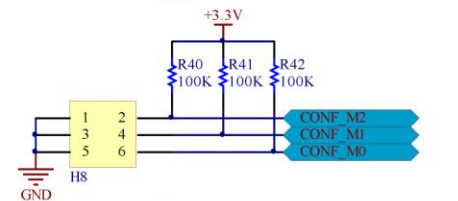


Route CCLK Line with stubs shorter than 12.5 mm. 50 Ohms characteristic Impedance

**SPI Configuration EEPROM**

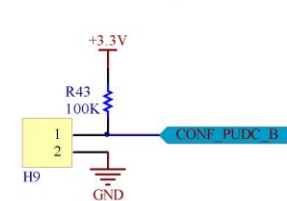


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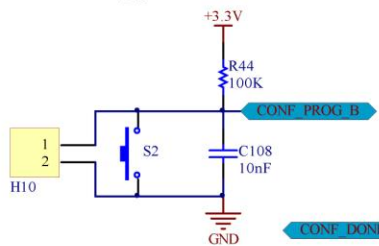
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010	Master BPI Mode	No
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100	Reserved	-
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110	Slave Parallel Mode	No
111	Slave Serial Mode	Yes

**IO Pull-up E/D**

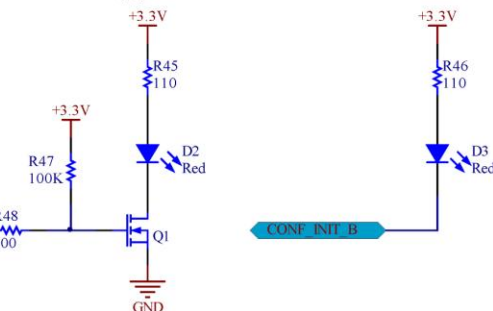


Enable all IO internal pull-ups

**Configuration Control**

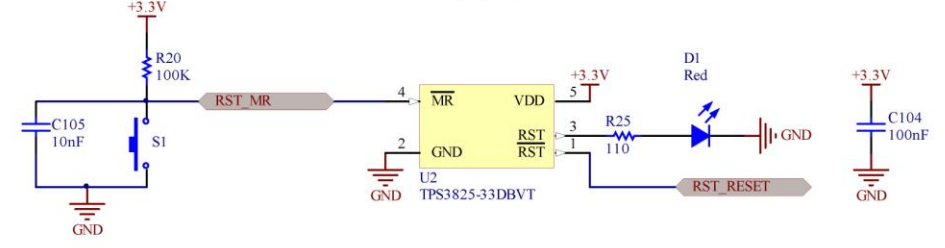


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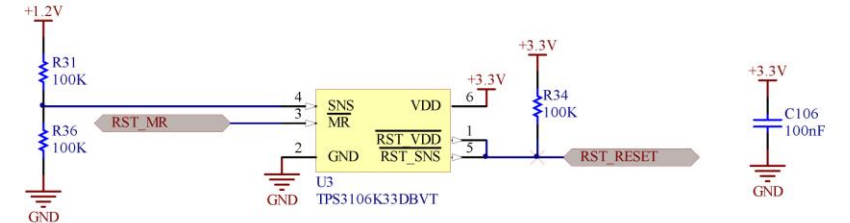


Disable suspend feature

**Reset Generator**



**Alternative Reset Generator**



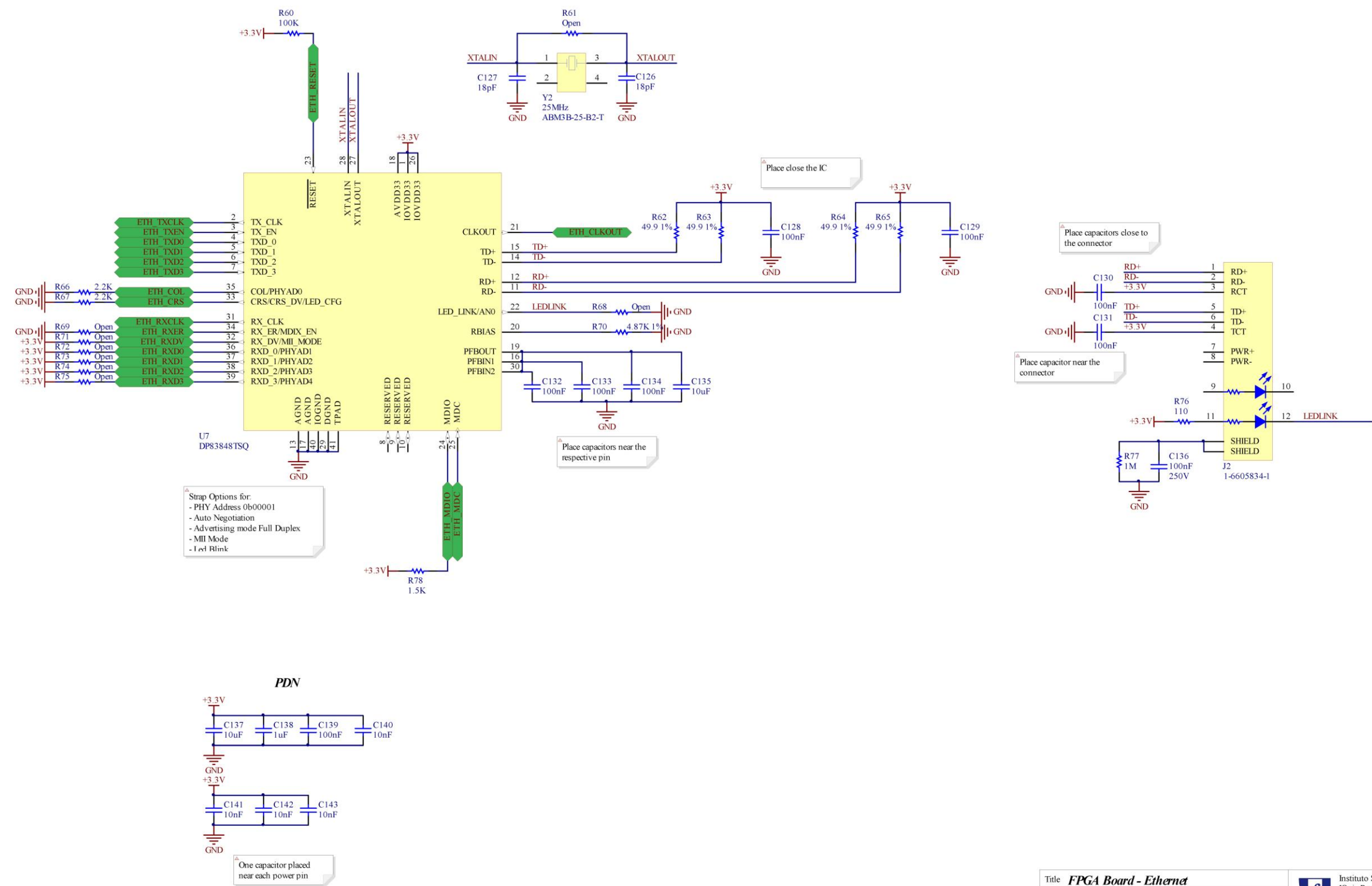
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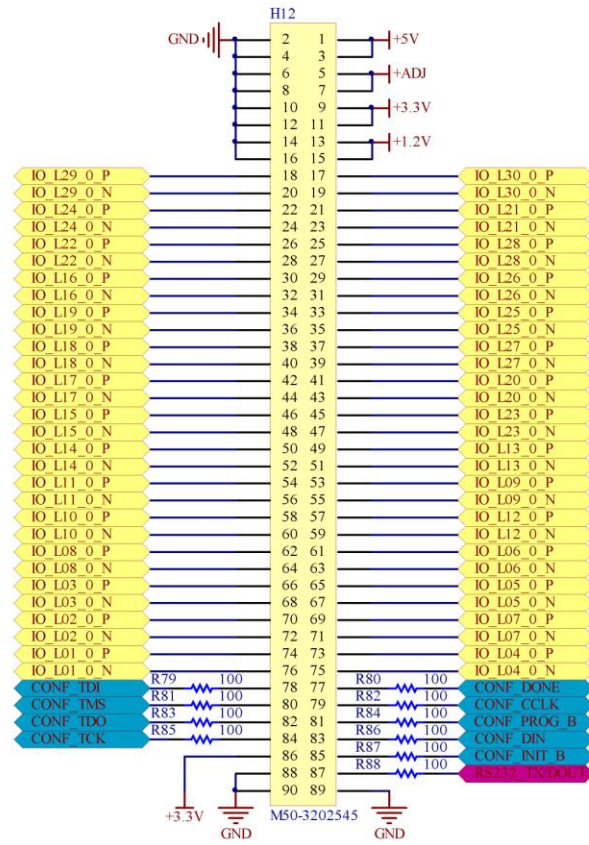
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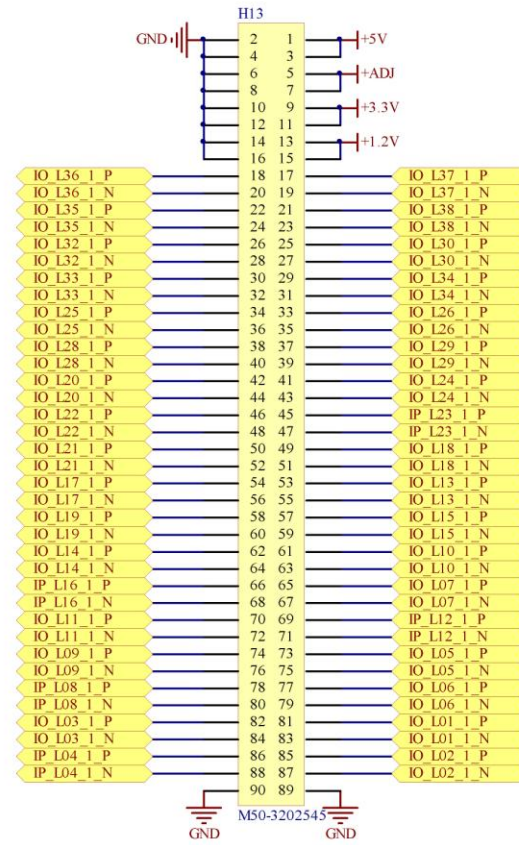


Route CCLK Line with stubs shorter than 12.5 mm. 50 Ohms characteristic Impedance

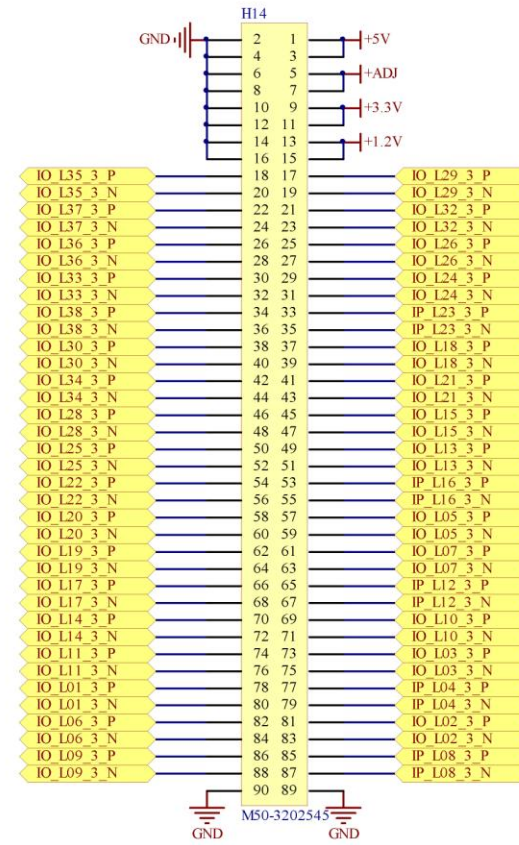
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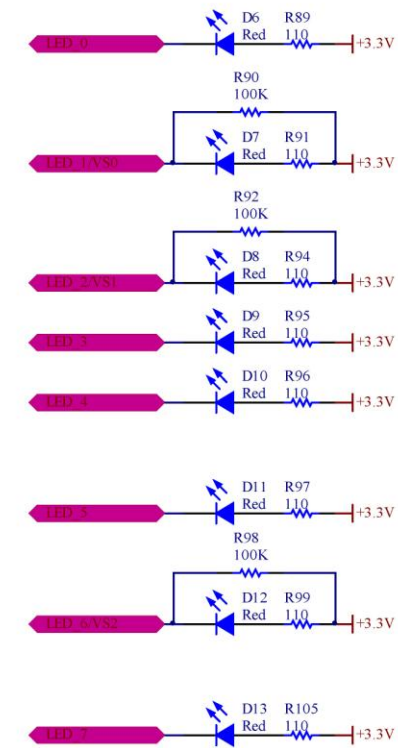
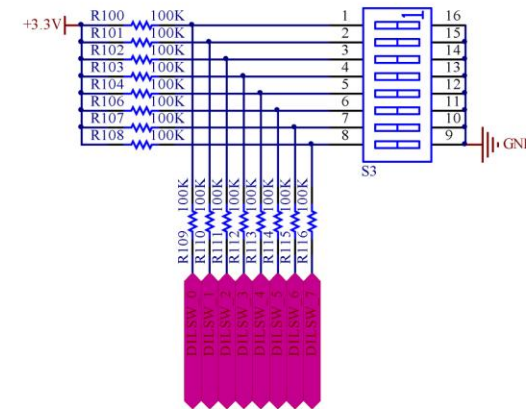
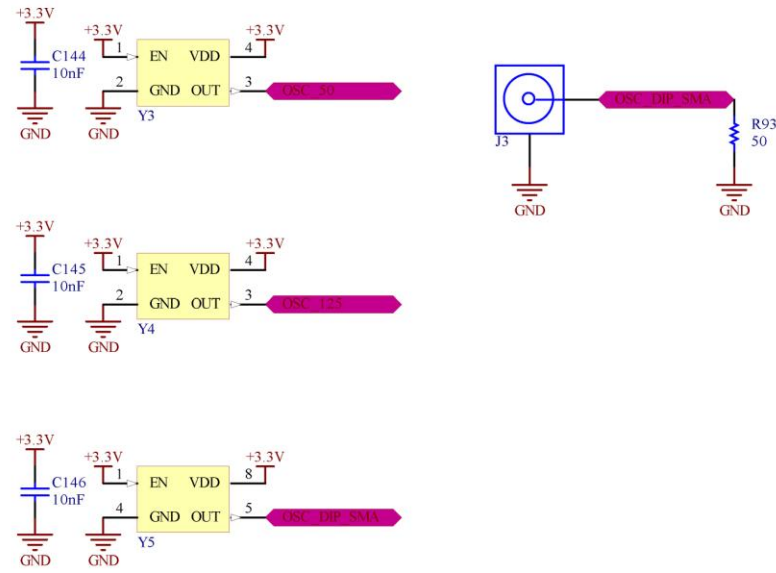
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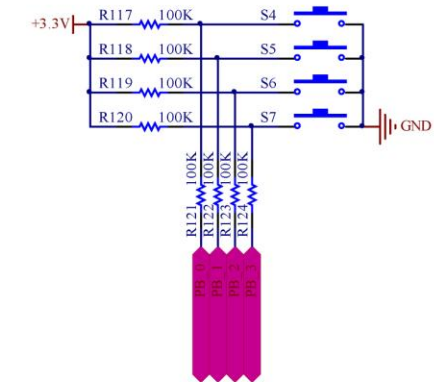
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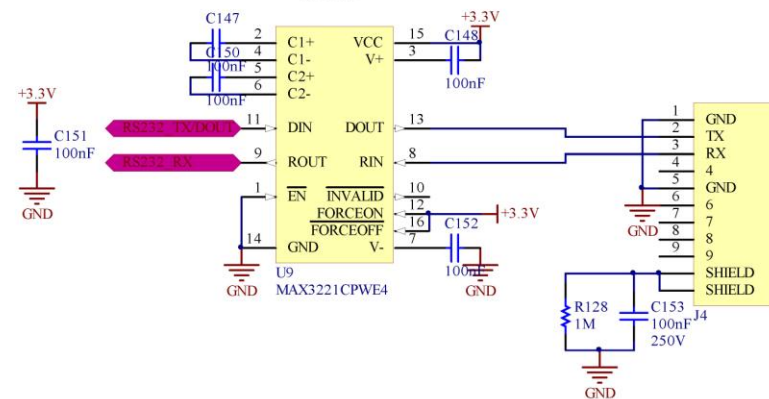
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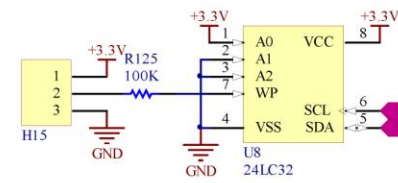
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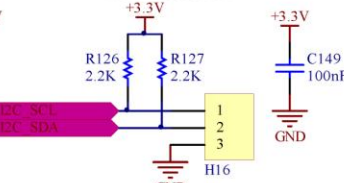
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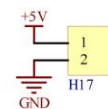
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### I2C Connector

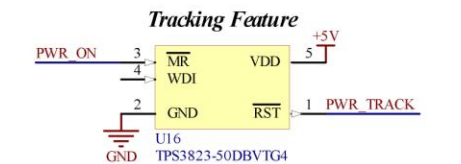
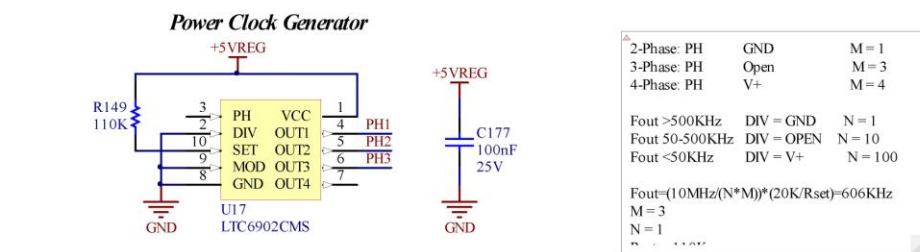
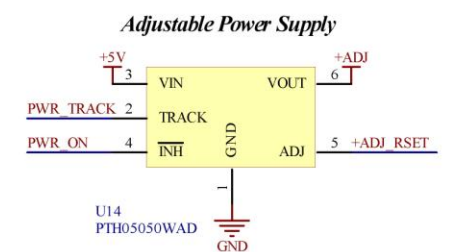
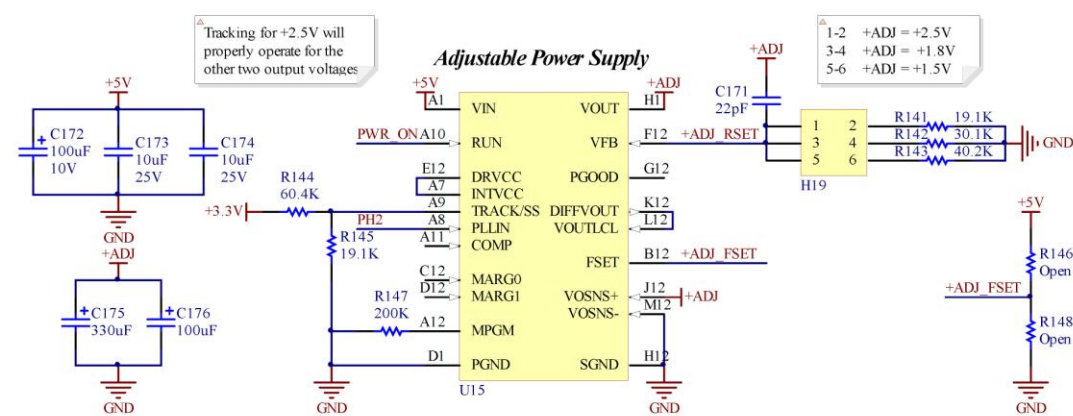
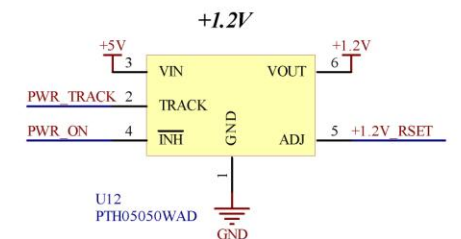
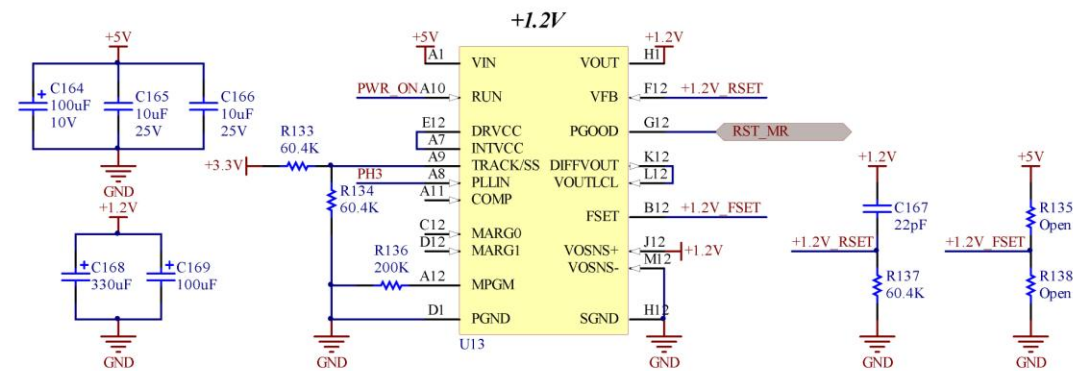
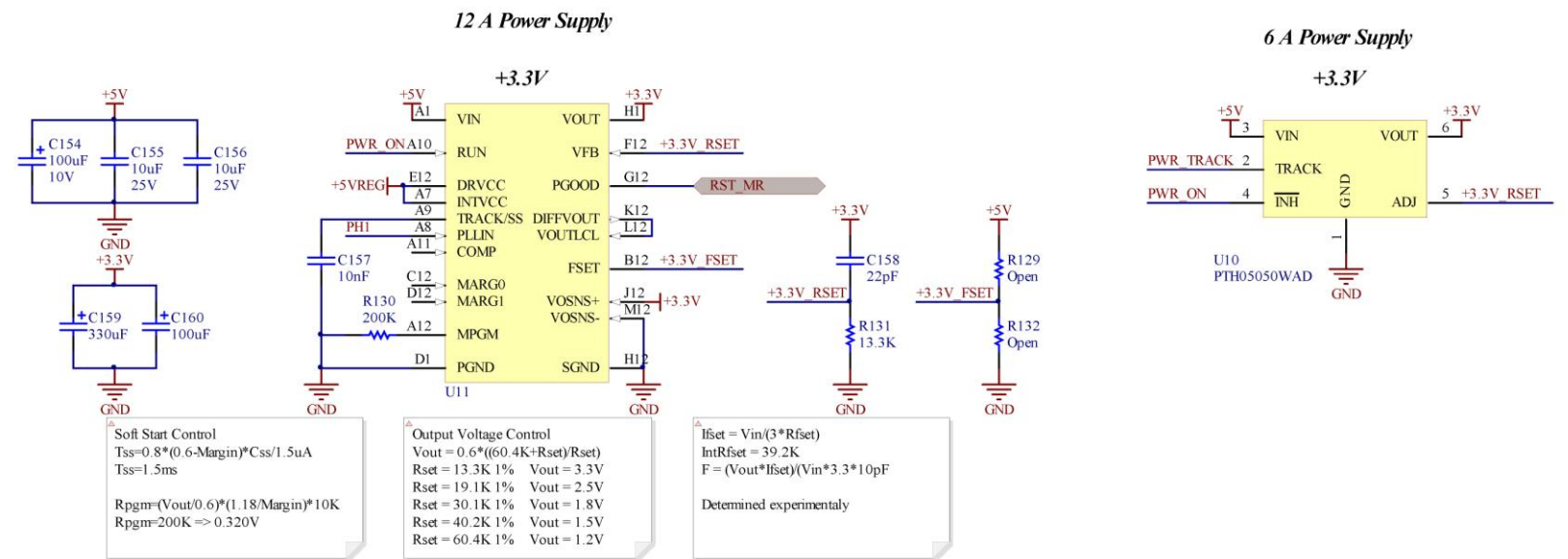
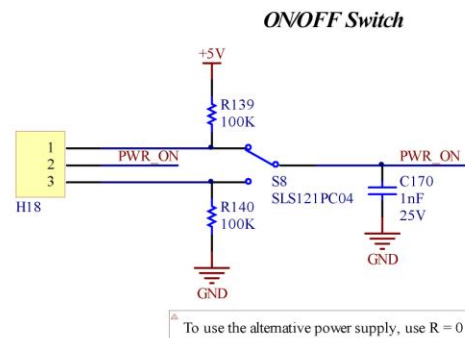
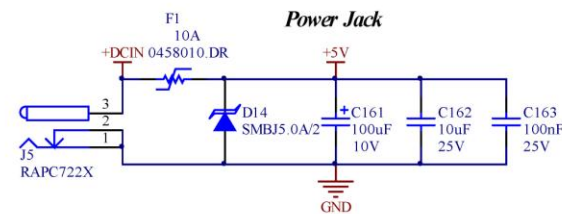


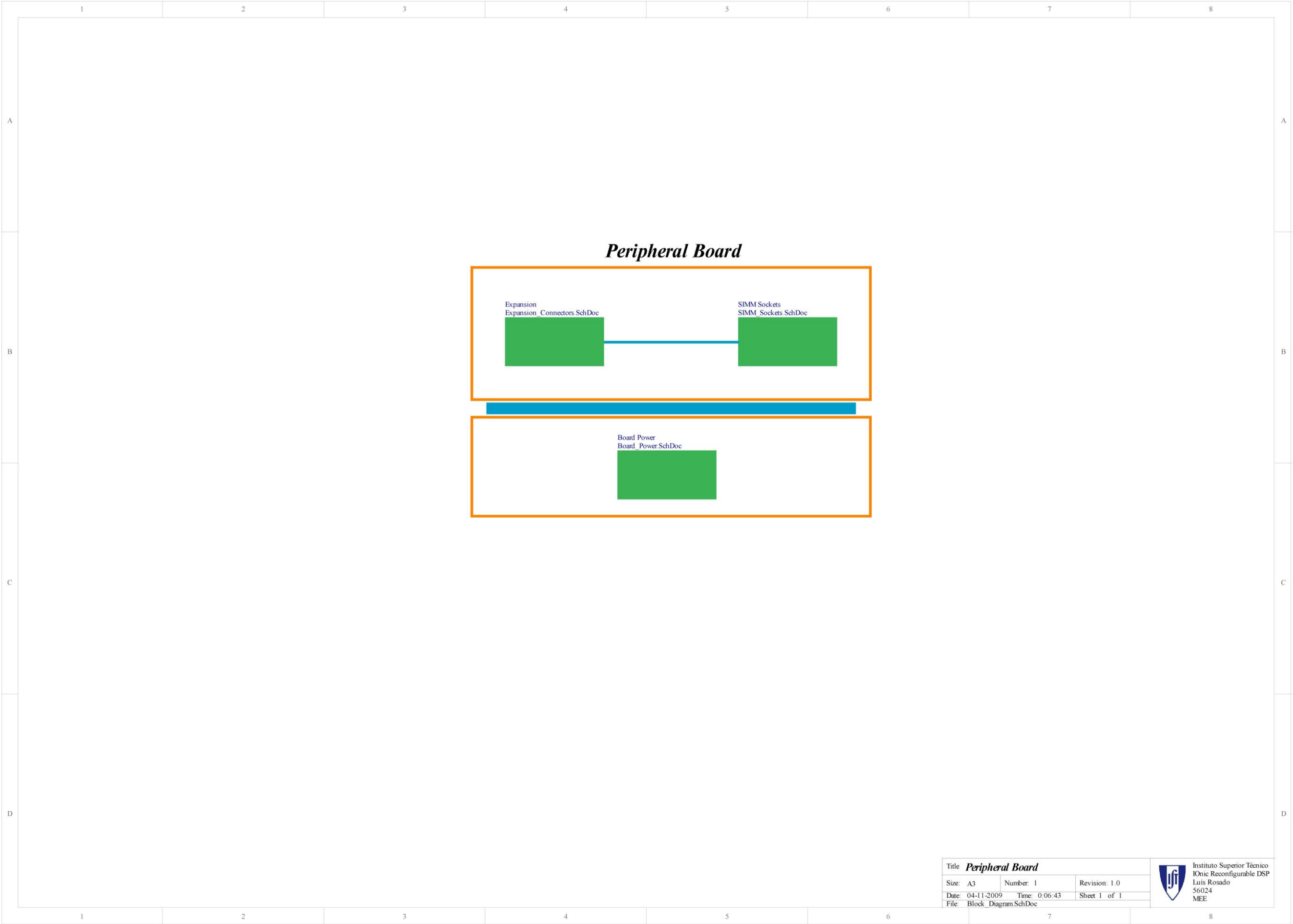
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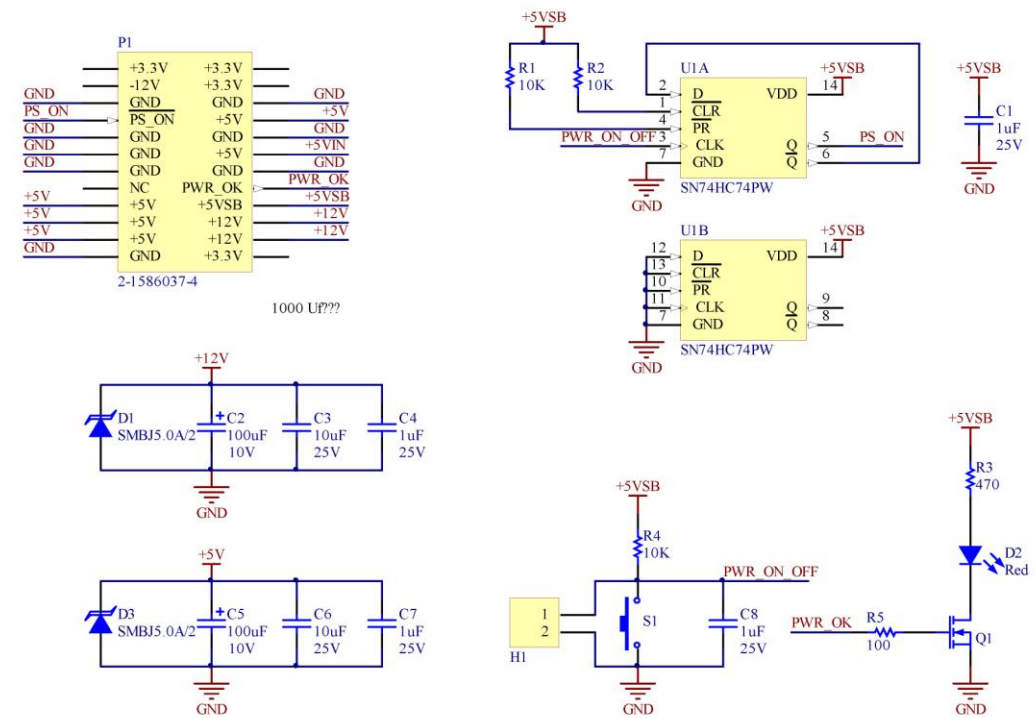
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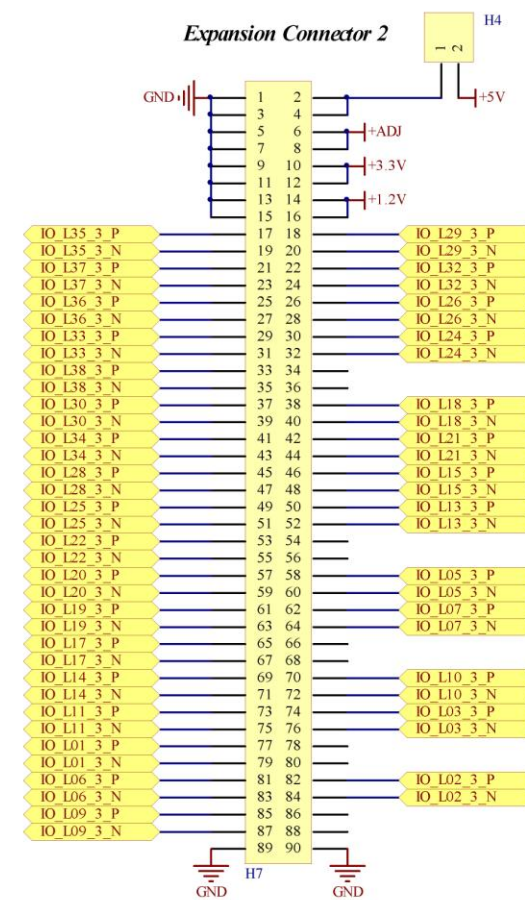
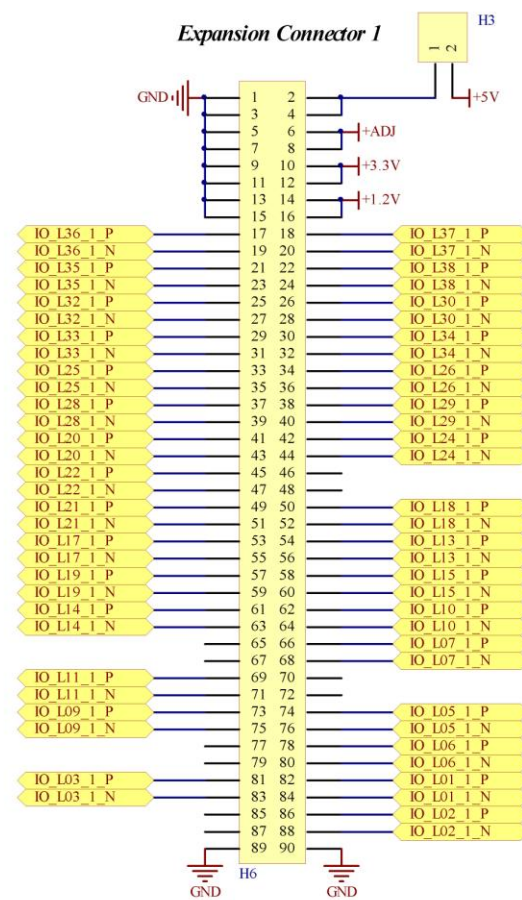
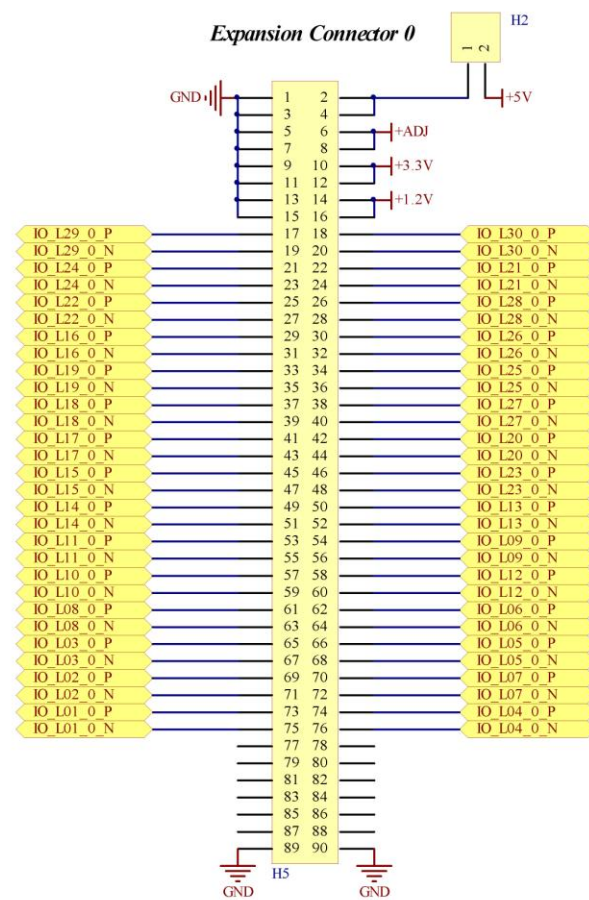
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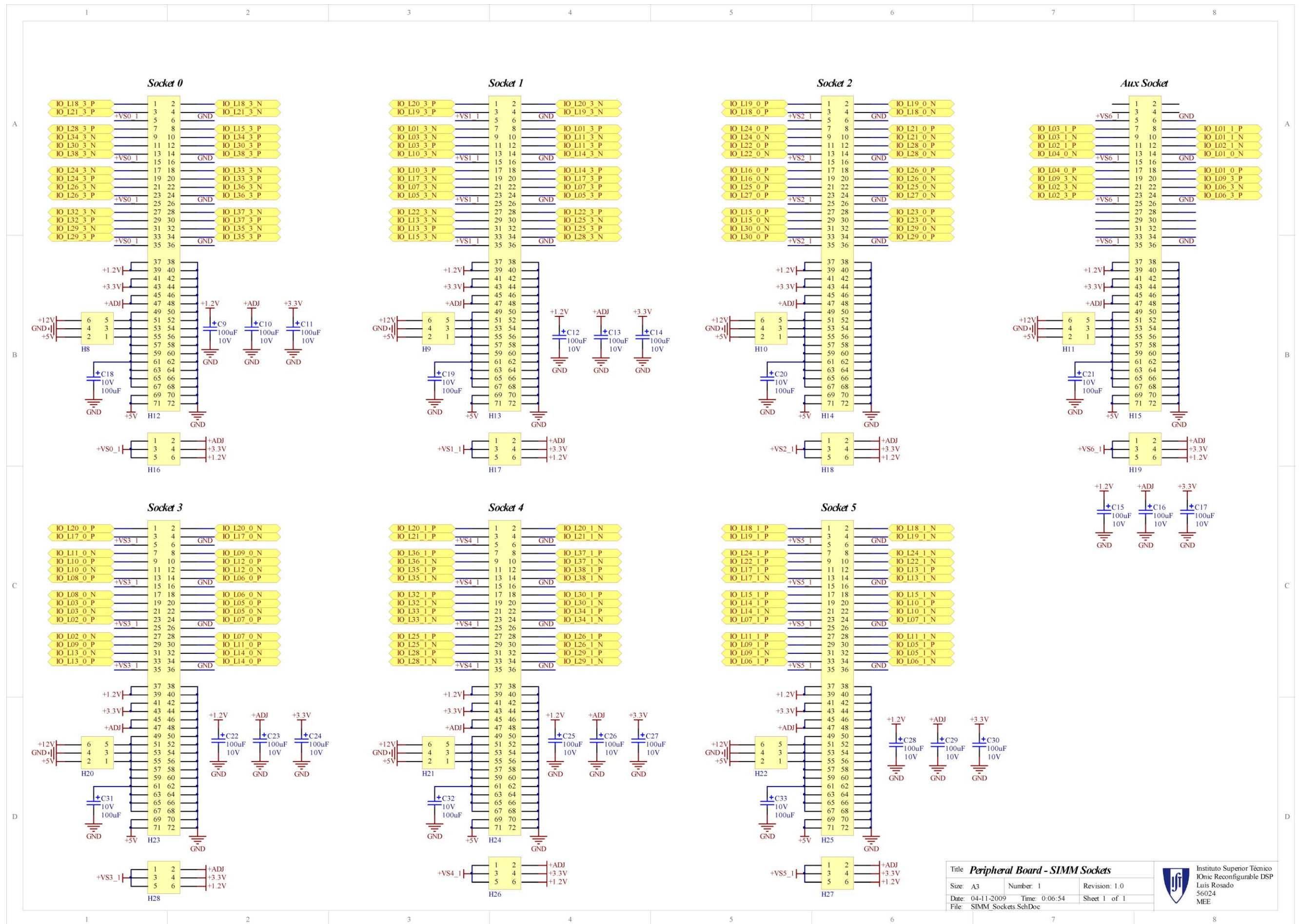


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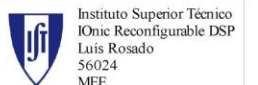


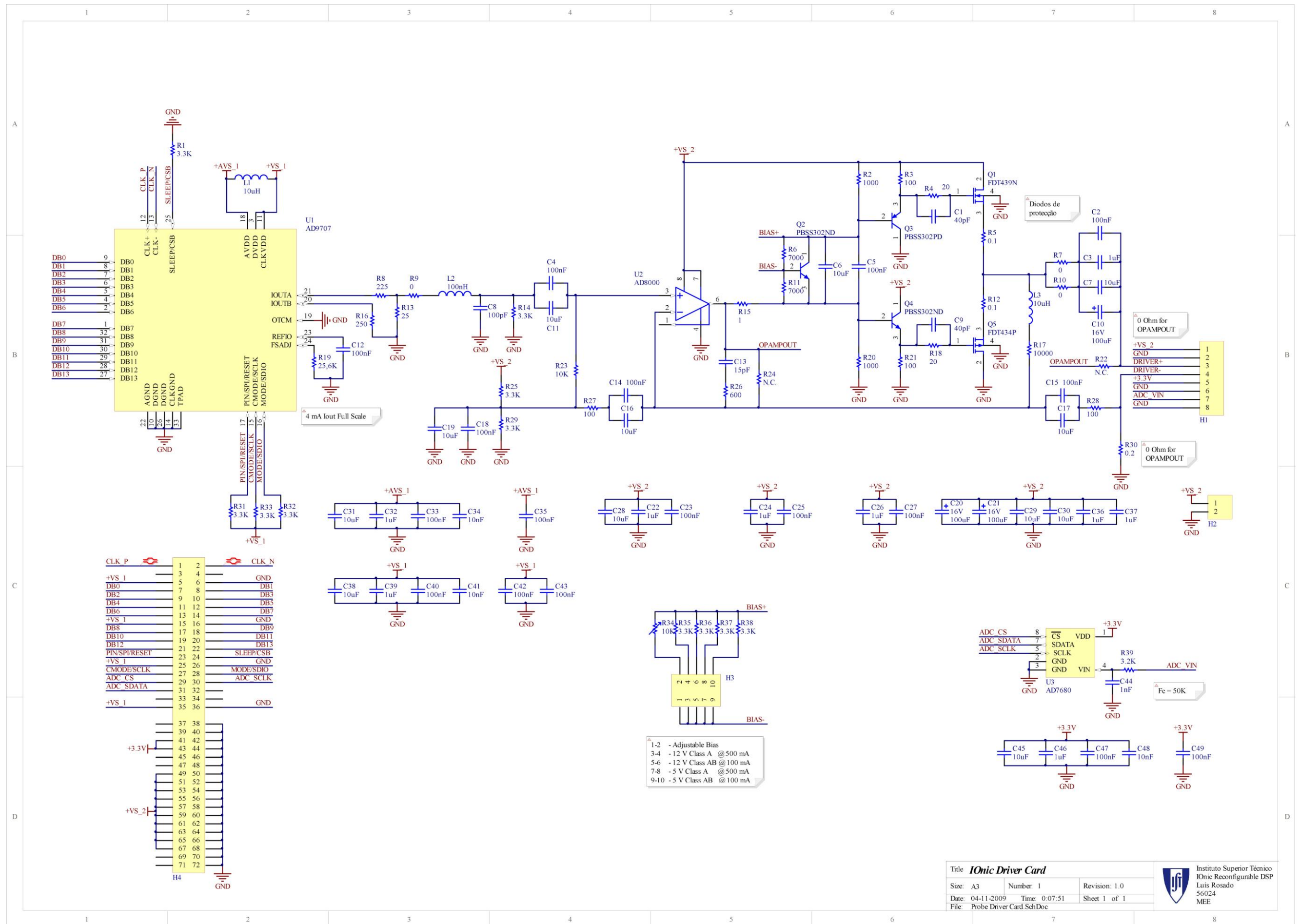
Instituto Superior Técnico  
 IOnic Reconfigurable DSP  
 Luis Rosado  
 56024  
 MEE

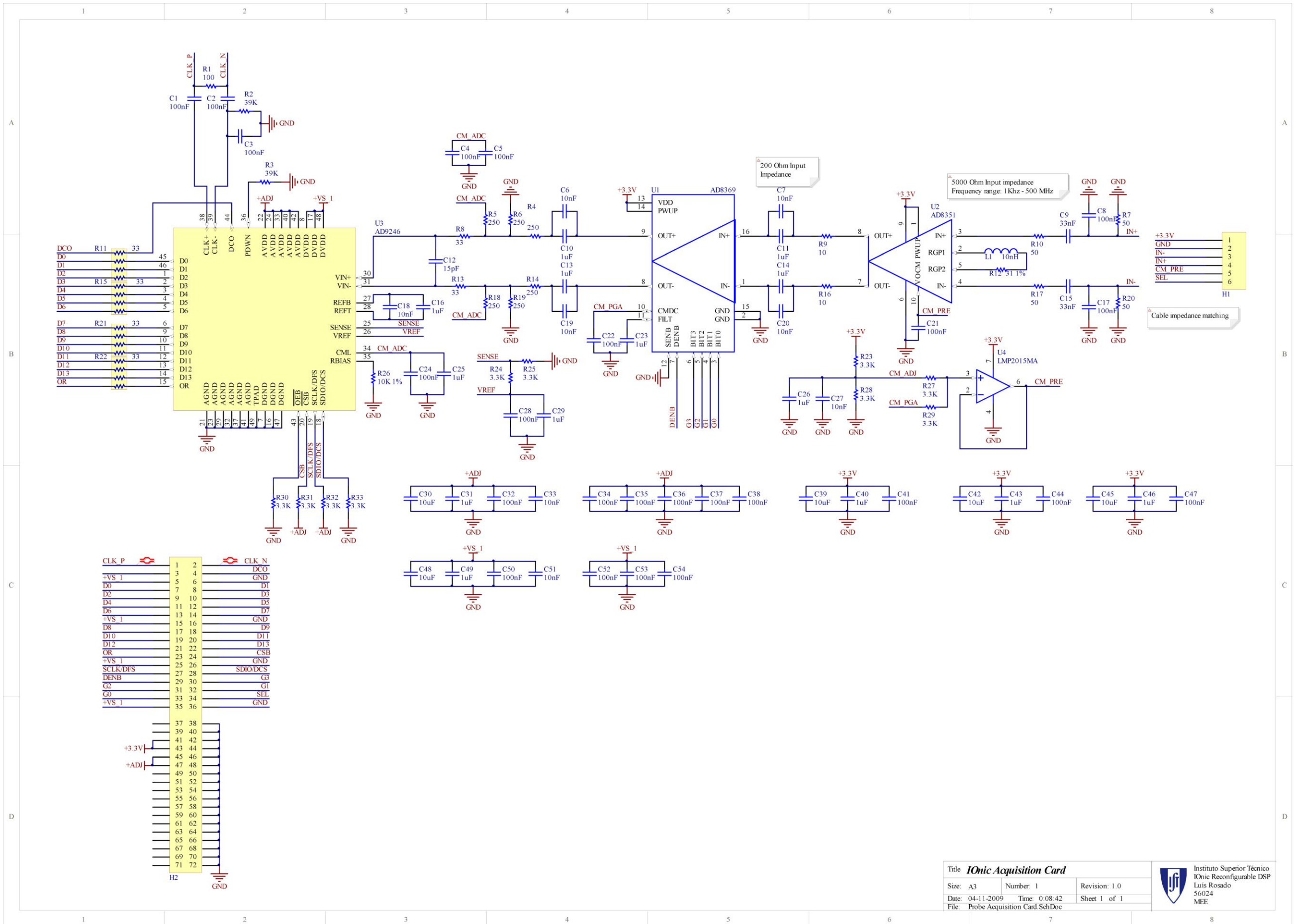


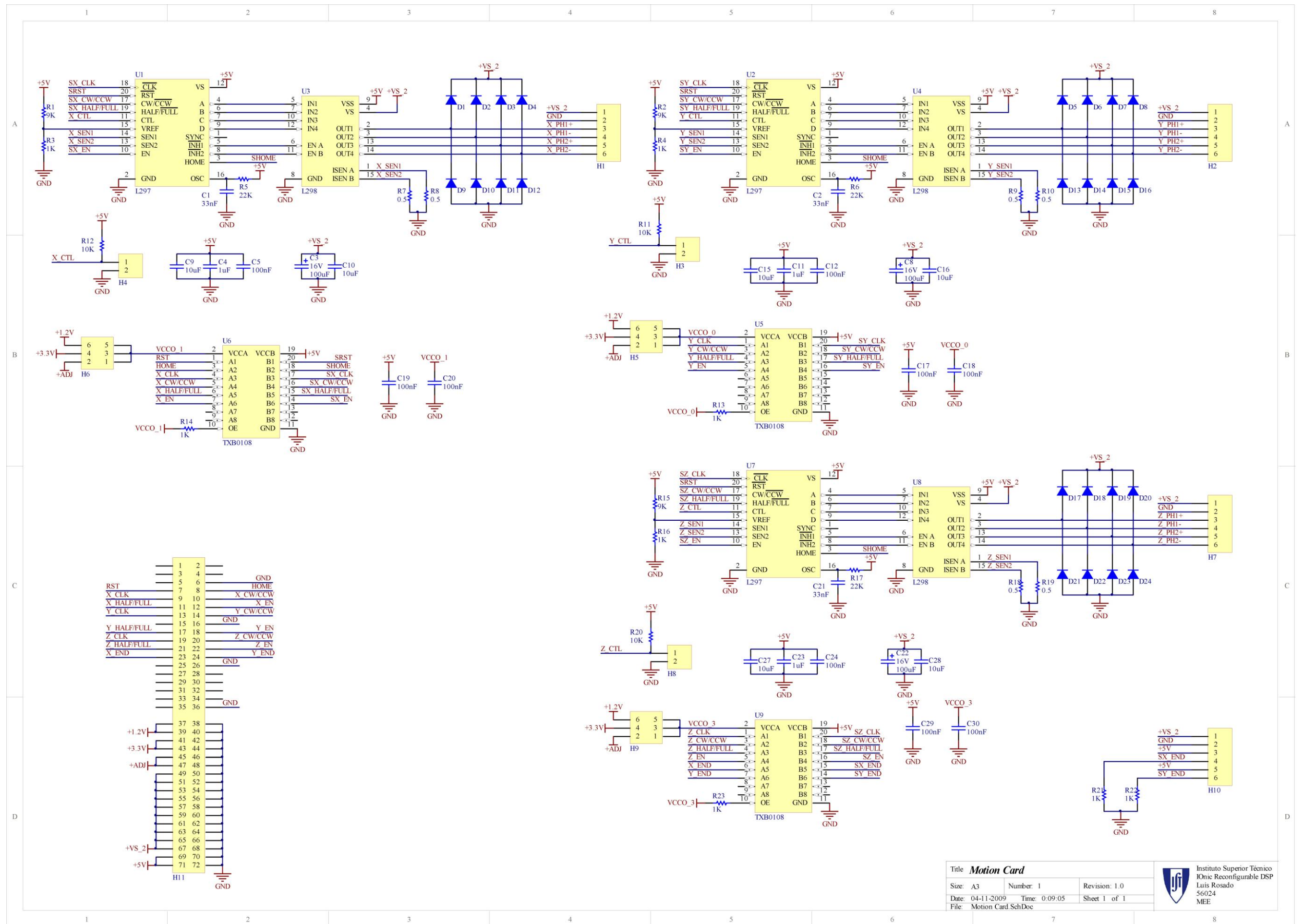


Title <b>Peripheral Board - SIMM Sockets</b>		
Size: A3	Number: 1	Revision: 1.0
Date: 04-11-2009	Time: 0:06:54	Sheet 1 of 1
File: SIMM_Sockets.SchDoc		





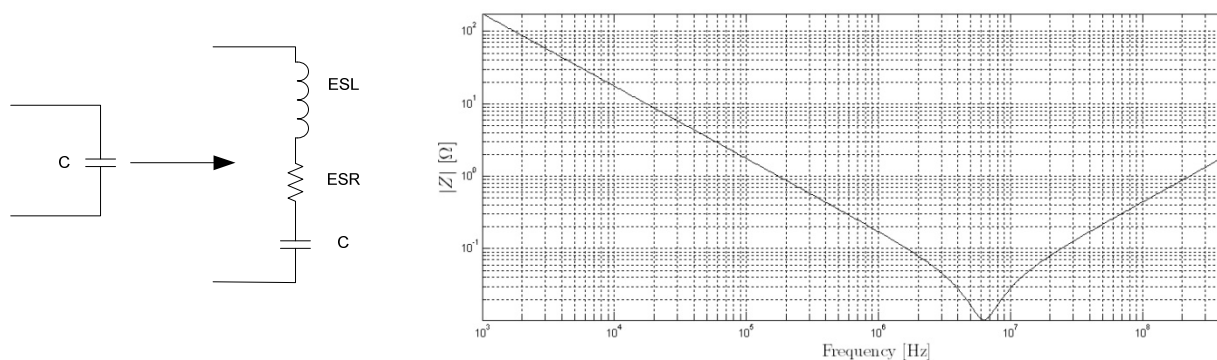




## Appendix II - Power Distribution Network Design

Since FPGAs can implement very different applications and simultaneously use several clock sources, it can be very intricate to predict how their transient current demand will be. For this reason, the PDN for FPGA devices is designed in a conservative worst-case way. Although this decision leads to the use of a great quantity of decoupling capacitors, it is widely accepted and effective.

The multiple capacitors in a PDN act as local energy storage elements reducing the supply voltage noise originated by transient currents. Capacitors can exhibit several parasitic effects such as series resistance (ESR) and inductance (ESL). These effects reduce the frequency range where the capacitor can be used for decoupling purposes and can be modeled as shown in Figure 1.



**Figure 1** - Capacitor Model and the resulting impedance profile.

Furthermore, the capacitors placement and footprint should be considered to minimize the inductance introduced between the capacitor and the FPGA pins. For 0603, 0402 and 0201 standard footprints and a full stack via it usual to take into account a 0.8 nH mounting parasitic inductance. Then, the self resonance frequency for the capacitor attached to the FPGA pins can be computed as

$$f_r = \frac{1}{2\pi\sqrt{(ESL + L_{mount})C}} \quad (1)$$

The capacitors position is related with their self resonance frequency. High self resonance frequency capacitors position is critical and they must be placed as close as possible to the FPGA device, typical under it in the bottom layer. This position improves the mounting inductance by reducing path length between the capacitors and the FPGA pins close to the PCB thickness. High value capacitors and consequently low self resonance frequency are less significant.

To improve the frequency range where the PDN is effective, several capacitor values should be employed. Actually, by doing this is possible to maintain low PDN impedance over a wide frequency range. The chosen capacitance values are not critical but they should cover several magnitude orders. Tailoring the design suggestions from the FPGA supplier described The selected capacitors and the relative percentage between them is described in Table 1. To achieve a relatively flat impedance profile, the quantity of capacitor is roughly doubled for every decade of capacitance decreasing.

**Table 1** - Capacitor Value Percentages for a Balanced Distribution Network.

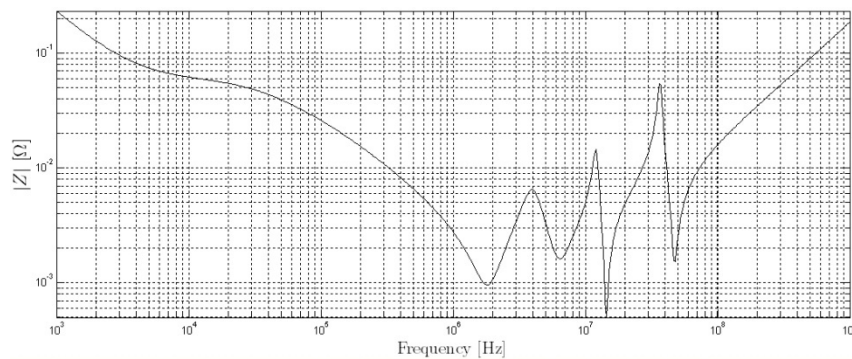
Capacitance Value	Quantity Percentage [%]	Package	Voltage Rating [V]	Dielectric Type
330 $\mu$ F	3 %	C	6.3	Tantalum
10 $\mu$ F	8 %	0603	6.3	X5R
1 $\mu$ F	14 %	0402	6.3	X5R
100 nF	25 %	0201	6.3	X5R
10 nF	50 %	0201	10	X7R

The overall number of capacitors for a certain supply voltage is made equal to the matched FPGA pins. The quantities of each capacitor employed are represented in Table 2 and were found through the use of the relative percentage described before.

**Table 2** - Decoupling capacitor per each supply voltage.

Supply Voltage	Description	Pins	330 $\mu$ F	10 $\mu$ F	1 $\mu$ F	100 nF	10 nF
VCCINT	Internal Logic	38	2	4	6	9	18
VCCAUX	Configuration Logic	25	1	2	4	6	12
VCCO0	IO Bank 0	8	1	1	1	2	4
VCCO1	IO Bank 0	8	1	1	1	2	4
VCCO2	IO Bank 0	8	1	1	1	2	4
VCCO3	IO Bank 0	8	1	1	1	2	4

Capacitors models were obtained from KEMET manufacturer and used together with a Simulation Program with Integrated Circuit Emphasis (SPICE) to compute the impedance profile of the FPGA internal logic PDN. The mounting inductance was considered 0.8 nH for all the capacitor below 100 nF. The impedance profile is presented in Figure 2 where it is possible to observe a absolute value impedance below 0.1  $\Omega$  from 10 kHz to about 600 MHz.

**Figure 2** - PDN impedance.

# Appendix III - Microstrip and Stripline Design

## Microstrip Design

For the microstrip line design is considered the configuration of the Figure 1. The characteristic impedance for each line can be computed as

$$Z_0 = \frac{60}{\sqrt{0.475\epsilon_r + 0.67}} \ln \left( \frac{4H}{0.67(0.8W + T)} \right) \quad (1)$$

where  $\epsilon_r$  and H are the dielectric constant and thickness of the medium, W the width of the trace and T the conductor thickness.

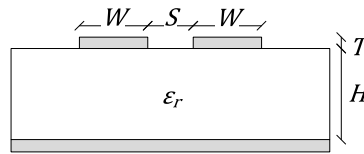


Figure 1 - Side view of two coupled microstrip lines.

The differential impedance between the two coupled microstrip lines is

$$Z_{dif} = 2Z_0 \left( 1 - 0.48e^{-0.96\frac{S}{H}} \right), \quad (2)$$

The last equation is valid for W, H and S values that respect the relations

$$0.1 < \frac{W}{H} < 2 \quad 0.2 < \frac{S}{H} < 3. \quad (3)$$

## Stripline Design

Striplines are designed in the configuration of Figure 2. The characteristic impedance for each line is

$$Z_0 = \frac{60}{\sqrt{\epsilon_r}} \ln \left( \frac{4H}{0.67\pi(0.8W + T)} \right) \quad (4)$$

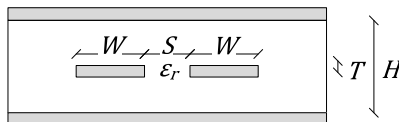


Figure 2 - Side view of two coupled striplines.

The differential impedance between the two coupled striplines is

$$Z_{dif} = 2Z_0 \left( 1 - 0.374e^{-2.9\frac{S}{H}} \right), \quad (5)$$

The last equation is valid for W, H and S values that respect the relations

$$\frac{H - T}{2W} > 1 \quad \frac{H}{4T} > 3. \quad (6)$$



## Appendix IV - ECscan System Budget

**Table 1 - FPGA Board production costs per unit.**

Quantity	Code	Reference	Description	Value	Unitary Price (€)	Price (€)
1	1671099	XC3SD3400A-CSG484C	FPGA		90.23	90.23
1	9471596	MCDS08	DIP Switch. 8 Position. SPST		0.97	0.97
1	8457239	TPS3825-33DBVT	1 channel voltage supervisor		0.73	0.73
1	8457034	TPS3106K33DBVT	2 channel voltage supervisor		2.78	2.78
2	7472358	87758-1416	Header, 14-pin. 2 mm pitch		1.3	2.6
1	9551107	SMBJ5.0A/2	Transient Voltage Suppressor		0.57	0.57
39	1657913	02016D104KAT2A	Capacitor	100nF	0.073	2.847
10	1679287	T495C337K006ZT	Polarized Capacitor	330uF	1.18	11.8
1	1663748	LTC6902CMS	Multiphase oscillator		5.39	5.39
65	1657919	0201ZC103KAT2A	Capacitor	10nF	0.057	3.705
3	1650770	251R14S4R7BV4T	Capacitor	100nF	0.101	0.303
1	1641047	FXO-HC536R-50	Surface mount quartz crystal		3.83	3.83
1	1640934	MJ/30/30/40/12PF	Surface mount quartz crystal		2.37	2.37
4	1612040	RR0510R-49R9-D	Resistor	49.9 1%	0.018	0.072
1	1611816	ABM3B-25-B2-T	Surface mount quartz crystal		0.97	0.97
1	1608727	RAPC722X	Power supply connector		1.51	1.51
1	1602447	DP83848TSQ	10/100 Ethernet Transceiver		5.61	5.61
1	1538963	FXO-HC535R-125	Surface mount quartz crystal		16.15	16.15
1	1527547	CPF0603F4K87C1	Resistor	4.87K 1%	0.46	0.46
1	1467959	2N7002MTF	N-Channel MOSFET		0.085	0.085
7	1463372	TMK316F106ZL-T	Capacitor	10uF	0.153	1.071
1	1455042	AT45DB321D-SU	SPI serial EEPROM		3.43	3.43
3	1432275	NOJC107M006RWJ	Polarized Capacitor	100uF	1.39	4.17
1	1308876	2411 03	USB B connector		0.48	0.48
16	1288253	C0402C105K9PAC	Capacitor	1uF	0.076	1.216
13	1288201	C0603C106M9PAC	Capacitor	10uF	1.01	13.13
1	1284349	1-6605834-1	Ethernet connector		6.61	6.61
1	1269133	CY7C68013A-56LFXC	USB microcontroller		15.9	15.9
1	1248990	5-1814832-1	SMA Connector		1.83	1.83
1	1234683	TPS3823-50DBVTG4	1 channel voltage supervisor		1.34	1.34
1	1197660	SLS121PC04	SPDT slide switch		0.81	0.81
3	1103286	PTH05050WAD	DC/DC converter module		10.79	32.37
6	1099537	M50-3202545	Connector 40-pin, 1.27mm pitch		7.97	47.82
1	1099294	8LCM009S-304B	D9 Connector		0.63	0.63
1	1053614	MAX3221CPWE4	RS-232 Transceiver		1.49	1.49
4	197180	TAJC107K010R	Polarized Capacitor	100uF	1.32	5.28
1	148086	350211-1	ATX Power Connector		2	2
					<b>Components (€)</b>	292.55
					<b>PCB (€)</b>	44.42
					<b>Total (€)</b>	336.97

**Table 2 - Peripheral Board production costs per unit.**

Quantity	Code	Reference	Description	Value	Unitary Price (€)	Price (€)
2	1463372	TMK316F106ZL-T	Capacitor	10uF	0.153	0.306
2	9551107	SMBJ5.0A/2	Transient Voltage Suppressor		0.57	1.14
3	1022319	M50-3902542	Connector 90-pin, 1.27mm pitch		3.77	11.31
7	1101360	5822021-4	Connector 72-pin. dual row		1.83	12.81
1	8116130	2-1586037-4	ATX Power Connector		1.07	1.07
1	1467959	2N7002MTF	N-Channel MOSFET		0.085	0.085
1	9591680	SN74HC74D	Dual D-type flip-flop		0.49	0.49
					<b>Components (€)</b>	27.21
					<b>PCB (€)</b>	23.68
					<b>Total (€)</b>	50.89

**Table 3 - IOnic Driver Card production costs per unit.**

Quantity	Code	Reference	Description	Value	Unitary Price (€)	Price (€)
9	1463372	TMK316F106ZL-T	Capacitor	10uF	0.153	1.377
3	1457493	T491D107K016AT	Polarized Capacitor	100uF	0.86	2.58
3	1288201	C0603C106M9PAC	Capacitor	10uF	1.01	3.03
3	1288253	C0402C105K9PAC	Capacitor	1uF	0.076	0.228
7	1657913	02016D104KAT2A	Capacitor	100nF	0.073	0.511
3	1657919	0201ZC103KAT2A	Capacitor	10nF	0.057	0.171
1	1463450	BKP1608HS101-T	IND	10uH	0.038	0.038
1	1612117	LK1608100K-T	IND	10uH	0.081	0.081
1	1471058	FDT439N	N-Channel MOSFET		0.68	0.68
2	1510741	PBSS302ND	NPN Transistor		0.32	0.64
1	1510742	PBSS302PD	PNP Transistor		0.32	0.32
1	1611577	FDT434P	P-Channel MOSFET		0.63	0.63
2	8067589	RL1206FR-7W0R1L	Resistor	0.1	0.21	0.42
1	1399746	SR732BTDR200F	Resistor	0.2	0.2	0.2
1	1438929	AD9707BCPZ	14 Bits, 175Msps DAC		15.38	15.38
1	8397546	AD7680ARM	16 Bits, 100Ksps ADC		5.67	5.67
<b>Components (€)</b>						31.95
<b>PCB (€)</b>						4.22
<b>Total (€)</b>						36.17

**Table 4 - IOnic Acquisition Card production costs per unit.**

Quantity	Code	Reference	Description	Value	Unitary Price (€)	Price (€)
14	1288253	C0402C105K9PAC	Capacitor	1uF	0.076	1.064
5	1288201	C0603C106M9PAC	Capacitor	10uF	1.01	5.05
13	1657913	02016D104KAT2A	Capacitor	100nF	0.073	0.949
2	1657919	0201ZC103KAT2A	Capacitor	10nF	0.057	0.114
1	1274202	AD9246BCPZ-125	14 Bits, 125Msps ADC		84.05	84.05
1	1542530	LMP2015	Precision OPAMP		1.72	1.72
<b>Components (€)</b>						92.94
<b>PCB (€)</b>						3.24
<b>Total (€)</b>						96.18

**Table 5 - Motion Control Card production costs per unit.**

Quantity	Code	Reference	Description	Value	Unitary Price (€)	Price (€)
3	1457493	T491D107K016AT	Polarized Capacitor	100uF	0.86	2.58
6	1463372	TMK316F106ZL-T	Capacitor	10uF	0.153	0.918
24	1459147	MURA120T3G	Fast Diode		0.31	7.44
3	1467714	L297D	Stepper Motor Controller		7.92	23.76
3	1366570	L298HN	Dual Full Bridge Driver		5.2	15.6
3	1494945	TXB0108	Voltage Shifter		2.11	6.33
<b>Components (€)</b>						56.62
<b>PCB (€)</b>						5.41
<b>Total (€)</b>						62.03

**Table 6 - Prototyping Costs.**

Prototyping Costs (€)	
Main Board	875
Others	438
<b>Total</b>	<b>1313</b>

**Table 7 - ECscan (with 2 Driver Cards and 4 Acquisition Cards) production costs.**

Quantity	Item	Unitary Price (€)	Price (€)
1	FPGA Board	336.97	336.97
1	Peripherals Board	50.89	50.89
2	IOnic Driver Card	36.17	72.34
4	IOnic Acquisition Card	96.18	384.72
1	Motion Control Card	62.03	62.03
<b>Total (€)</b>			906.95

# Appendix V - USB\_FIFO VHDL description

```

-----
-- usb_fifo.vhd - entity/architecture pair
-----
--
-----
-- Filename:          usb_fifo.vhd
-- Version:           1.00.a
-- Description:       Slave Fifo Interface for CY68013A
-- Date:              09-08-2009
-- Authors:           Luis Rosado
-- VHDL Standard:     VHDL'93
-- Notes:             OUT - From host to peripheral
--                   IN - From peripheral to host
-----

-- User Libraries
-----
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

-- Entity Definition
-----
entity usb_fifo is
port(
    reset                : in std_logic;           -- Peripheral reset signal
    ingo                  : in std_logic;           -- Send IN data
    outgo                 : in std_logic;           -- Get OUT data
    pktendgo              : in std_logic;           -- Commit a packet
    connected             : out std_logic;          -- Connected Signal
    inrdy                 : out std_logic;           -- IN data sent
    outrdy                : out std_logic;          -- OUT data received
    pktendrdy             : out std_logic;          -- Packet committed
    dataoutav             : out std_logic;           -- OUT data available
    dataout               : out std_logic_vector(0 to 31); -- Data from host to uBlaze
    datain                : in std_logic_vector(0 to 31); -- Data from uBlaze to host
    slavereset            : out std_logic;           -- CY7C68013A Reset signal
    slavewakeup           : out std_logic;           -- CY7C68013A Wake Up signal
    slavesetup            : in std_logic;           -- CY7C68013A Setup signal
    slaveclkout           : in std_logic;           -- CY7C68013A Clock signal (dummy)
    slaveflaga            : in std_logic;           -- CY7C68013A FIFO programmable flag
    slaveflagb            : in std_logic;           -- CY7C68013A FIFO full flag
    slaveflagc            : in std_logic;           -- CY7C68013A FIFO empty flag
    slavefifoadr          : out std_logic_vector(0 to 1); -- CY7C68013A Endpoint pointer
    slavepktend           : out std_logic;          -- CY7C68013A Pktend signal
    slaveoe               : out std_logic;          -- CY7C68013A Interface Output Enable
    slavewr               : out std_logic;          -- CY7C68013A Interface Write Enable
    slaverd               : out std_logic;          -- CY7C68013A Interface Read Enable
    slaveclk              : in std_logic;           -- CY7C68013A Slave FIFO Clock
    slavedatain           : out std_logic_vector(0 to 15); -- Master FIFO Interface Output Buffer
    slavedataout          : in std_logic_vector(0 to 15); -- Master FIFO Interface Input Signal
    masteroe              : out std_logic;          -- Master FIFO Interface Output Enable
);
end entity usb_fifo;

-- Behavioral Description
-----

```

architecture behavioral of usb\_fifo is

```

type      statetype is (setup, idle, write1, pktend1,
                        read1, read2, to_in, to_out);
signal    state          : statetype;
constant  oe             :std_logic := '0';
constant  od             :std_logic := '1';
signal    masteroe_o     : std_logic;
constant  fifoout        : std_logic_vector := "00";
constant  ffoin          : std_logic_vector := "10";
type      inoutmodetype is (outmode, inmode);
signal    inoutmode      : inoutmodetype;
signal    ingo_i         : std_logic;
signal    outgo_i        : std_logic;
signal    pktendgo_i     : std_logic;

begin
    dataout(0 to 15) <= (others => '0');
    masteroe <= masteroe_o;
    slaveoe  <= not masteroe_o;

---
-----
slave_fifo_interface : process(slaveclk, reset) is
begin
    if reset = '1' then
        dataout <= (others => '0');

        slavedatain <= (others => '0');
        dataoutav <= '0';
        slavereset <= '0';
        slavewakeup <= '1';
        slavewr <= '1';
        slaverd <= '1';
        slavepktend <= '1';
        inrdy <= '0';
        pktendrdy <= '0';
        outrdy <= '0';
        connected <= '0';
        slavefifoadr <= fifoout;
        masteroe_o <= od;
        inoutmode <= outmode;
        state <= setup;
    else
        slavereset <= '1';
    end if;

---
-----
    if slaveclk'event and slaveclk = '1' then
        ingo_i <= ingo;
        outgo_i <= outgo;
        pktendgo_i <= pktendgo;

        case state is
            when setup =>
                if slavesetup = '1' then
                    state <= idle;
                    connected <= '1';
                end if;
            when idle =>
                if ingo_i = '1' then

```

-- FSM state list  
-- FSM state signal  
-- Master output enable boolean value  
-- Master output disable boolean value  
-- Drive masteroe  
-- OUT FIFO address  
-- IN FIFO address  
-- Mode list  
-- Mode signal  
-- IN data ready to send  
-- Check for OUT data  
-- Commit a packet

-- Unused bits of output register  
-- To avoid output collision

-----  
-- ASSYNCHRONOUS RESET  
-----

-- Reset state  
-- Setup all outputs to default value

-- Reset CY7C68013A

-- OUT mode by default

-- Next state

-- Stop resetting CY7C68013A

-----  
-- FINITE STATE MACHINE  
-----

-- Rising edge active  
-- Trigger new control signals

-- STATE SETUP  
-- Wait until CY68013A is fully configured

-- STATE IDLE  
-- Send IN data

```

        if inoutmode = outmode then                                -- IN mode?
            state <= to_in;                                         -- Get IN mode configuration
        else
            if slaveflagb = '1' then
                slavewr <= '0';
                slavedatain <= datain(16 to 31);
                state <= write1;
            end if;
        end if;
    else
        if pktendgo_i = '1' then                                    -- Commit IN packet
            if inoutmode = outmode then                            -- IN mode?
                state <= to_in;                                     -- Get IN mode configuration
            else
                slavepktend <= '0';
                state <= pktend1;
            end if;
        else
            if slaveflagc = '1' then                                -- If '0' FIFO is empty
                if outgo_i = '1' then
                    slaverd <= '0';
                    state <= read1;
                end if;
                dataoutav <= '1';
            else
                dataoutav <= '0';
            end if;
        end if;
    end if;

    when write1 =>                                                  -- STATE WRITE1
        slavewr <= '1';
        inrdy <= '1';
        if ingo_i = '0' then
            inrdy <= '0';
            state <= to_out;
        end if;

    when pktend1 =>                                                 -- STATE PKTEND1
        slavepktend <= '1';
        pktendrdy <= '1';
        if pktendgo_i = '0' then
            pktendrdy <= '0';
            state <= to_out;
        end if;

    when read1 =>                                                  -- STATE READ1
        dataout(16 to 31) <= slavedataout;
        slaverd <= '1';
        outrdy <= '1';
        state <= read2;

    when read2 =>                                                  -- STATE READ2
        if outgo_i = '0' then
            outrdy <= '0';
            state <= idle;
        end if;

    when to_in =>                                                  -- STATE TO_IN
        slavefifoadr <= fifo_in;
        masteroe_o <= oe;
        inoutmode <= inmode;
        state <= idle;

    when to_out =>                                                 -- STATE TO_OUT
        slavefifoadr <= fifo_out;
        masteroe_o <= od;
        inoutmode <= outmode;

```

```
        state <= idle;

    end case;

    end if;
end process slave_fifo_interface;
end architecture;
```

## Appendix VI - Signal\_generator VHDL description

```
-----
-- signal_generator.vhd - entity/architecture pair
-----
--
-----
-- Filename:          signal_generator.vhd
-- Version:           1.00.a
-- Description:       Digital data synthesizer with PLB interface
-- Date:              10-08-2009
-- Author:            Luis Rosado
-- VHDL Standard:     VHDL'93
-- Notes:             Preliminary version
-----

-- User Libraries
-----
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

Library UNISIM;
use UNISIM.vcomponents.all;

-----
-- Entity Definition
-----
entity signal_generator is
generic(
    MASTER_SLAVE      : integer range 0 to 1      := 1      -- Master/Slave mode
);
port(
    reset_masterin     : in std_logic;            -- Peripheral reset signal
    reset_slavein      : in std_logic;            -- Peripheral reset signal
    reset_slaveout     : out std_logic;            -- Peripheral reset signal
    clk                : in std_logic;            -- DDS input clock
    dds_on              : in std_logic;            -- DDS ON control
    frequency           : in std_logic_vector(31 downto 0); -- Frequency control input
    phase              : in std_logic_vector(7 downto 0);  -- Frequency control input
    amplitude           : in std_logic_vector(7 downto 0); -- Frequency control input
    dacmod0             : out std_logic;
    dacmod1            : out std_logic;
    dacdiv0            : out std_logic;
    dacdiv1            : out std_logic;
    clkout              : out std_logic;           -- Output Clock
    dacout             : out std_logic_vector(13 downto 0) -- DDS
);
end entity signal_generator;

-----
-- Behavioral Description
-----
architecture behavioral of signal_generator is

-- acc_dsp48 component
component acc_dsp48
port (
    b: IN std_logic_VECTOR(31 downto 0);
    clk: IN std_logic;
```

```

        sclr: IN std_logic;
        q: OUT std_logic_VECTOR(31 downto 0));
end component;

-- Synplicity black box declaration
attribute syn_black_box : boolean;
attribute syn_black_box of acc_dsp48: component is true;

-- rom_8x256 component
component rom_8x256
    port (
        a: IN std_logic_VECTOR(7 downto 0);
        clk: IN std_logic;
        qspo: OUT std_logic_VECTOR(13 downto 0));
end component;

--- Synplicity black box declaration
attribute syn_black_box of rom_8x256: component is true;

-- mul_dsp48 component
component mul_dsp48
    port (
        clk: IN std_logic;
        a: IN std_logic_VECTOR(13 downto 0);
        b: IN std_logic_VECTOR(7 downto 0);
        p: OUT std_logic_VECTOR(21 downto 0));
end component;

-- Synplicity black box declaration
attribute syn_black_box of mul_dsp48: component is true;

-- Signal declarations
signal reset      : std_logic;
signal acc_out    : std_logic_vector(31 downto 0);
signal phase_out  : std_logic_vector(7 downto 0);
signal rom_out    : std_logic_vector(13 downto 0);
signal amplitude_out : std_logic_vector(21 downto 0);

begin
-- set low pass filter response and no zero stuffing
dacmod0 <= '0';
dacmod1 <= '0';
-- optimum settings for sampling rate
dacdiv0 <= '1';
dacdiv1 <= '0';

MASTER : if (MASTER_SLAVE = 1) generate
reset <= reset_masterin;
end generate MASTER;

SLAVE : if (MASTER_SLAVE = 0) generate
reset <= reset_slavein;
end generate SLAVE;

reset_slaveout <= reset;

dds_on_control : process(dds_on)is
begin
if dds_on = '1' then
    dacout <= not(not amplitude_out(21) & amplitude_out(20 downto 8));
else
    dacout <= "10000000000000";
end if;
end process dds_on_control;
clkout <= clk;

ACC_DSP48_I : acc_dsp48

```

```

port map (
    b => frequency,
    clk => clk,
    sclr => reset,
    q => acc_out);

phase_register: process (clk) is
begin
if clk'event and clk = '1' then
    phase_out <= acc_out(31 downto 24) + phase;
end if;
end process phase_register;

ROM_8X256_I : rom_8x256
port map (
    a => phase_out,
    clk => clk,
    qspo => rom_out);

MUL_DSP48_I : mul_dsp48
port map (
    clk => clk,
    a => rom_out,
    b => amplitude,
    p => amplitude_out);
end architecture;

```



## Appendix VI - Signal\_generator VHDL description

```

-----
-- signal_generator.vhd - entity/architecture pair
-----
--
-----
-- Filename:          signal_generator.vhd
-- Version:           1.00.a
-- Description:       Digital data synthesizer with PLB interface
-- Date:              10-08-2009
-- Author:            Luis Rosado
-- VHDL Standard:     VHDL'93
-- Notes:             Preliminary version
-----

-- User Libraries

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

Library UNISIM;
use UNISIM.vcomponents.all;

-----
-- Entity Definition
-----
entity signal_generator is
generic(
    MASTER_SLAVE      : integer range 0 to 1      := 1      -- Master/Slave mode
);
port(
    reset_masterin      : in std_logic;           -- Peripheral reset signal
    reset_slavein       : in std_logic;           -- Peripheral reset signal
    reset_slaveout      : out std_logic;          -- Peripheral reset signal
    clk                 : in std_logic;           -- DDS input clock
    dds_on              : in std_logic;           -- DDS ON control
    frequency           : in std_logic_vector(31 downto 0); -- Frequency control input
    phase               : in std_logic_vector(7 downto 0);  -- Frequency control input
    amplitude           : in std_logic_vector(7 downto 0);  -- Frequency control input
    dacmod0             : out std_logic;
    dacmod1             : out std_logic;
    dacdiv0             : out std_logic;
    dacdiv1             : out std_logic;
    clkout              : out std_logic;          -- Output Clock
    dacout              : out std_logic_vector(13 downto 0) -- DDS
);
end entity signal_generator;

-----
-- Behavioral Description
-----
architecture behavioral of signal_generator is

-- acc_dsp48 component
component acc_dsp48
port (
    b: IN std_logic_VECTOR(31 downto 0);
    clk: IN std_logic;

```

```

        sclr: IN std_logic;
        q: OUT std_logic_VECTOR(31 downto 0));
end component;

-- Synplicity black box declaration
attribute syn_black_box : boolean;
attribute syn_black_box of acc_dsp48: component is true;

-- rom_8x256 component
component rom_8x256
    port (
        a: IN std_logic_VECTOR(7 downto 0);
        clk: IN std_logic;
        qspo: OUT std_logic_VECTOR(13 downto 0));
end component;

--- Synplicity black box declaration
attribute syn_black_box of rom_8x256: component is true;

-- mul_dsp48 component
component mul_dsp48
    port (
        clk: IN std_logic;
        a: IN std_logic_VECTOR(13 downto 0);
        b: IN std_logic_VECTOR(7 downto 0);
        p: OUT std_logic_VECTOR(21 downto 0));
end component;

-- Synplicity black box declaration
attribute syn_black_box of mul_dsp48: component is true;

-- Signal declarations
signal reset      : std_logic;
signal acc_out    : std_logic_vector(31 downto 0);
signal phase_out  : std_logic_vector(7 downto 0);
signal rom_out    : std_logic_vector(13 downto 0);
signal amplitude_out : std_logic_vector(21 downto 0);

begin
-- set low pass filter response and no zero stuffing
dacmod0 <= '0';
dacmod1 <= '0';
-- optimum settings for sampling rate
dacdiv0 <= '1';
dacdiv1 <= '0';

MASTER : if (MASTER_SLAVE = 1) generate
reset <= reset_masterin;
end generate MASTER;

SLAVE : if (MASTER_SLAVE = 0) generate
reset <= reset_slavein;
end generate SLAVE;

reset_slaveout <= reset;

dds_on_control : process(dds_on)is
begin
if dds_on = '1' then
    dacout <= not(not amplitude_out(21) & amplitude_out(20 downto 8));
else
    dacout <= "100000000000000";
end if;
end process dds_on_control;
clkout <= clk;

ACC_DSP48_I : acc_dsp48

```

```

port map (
    b => frequency,
    clk => clk,
    sclr => reset,
    q => acc_out);

phase_register: process (clk) is
begin
if clk'event and clk = '1' then
    phase_out <= acc_out(31 downto 24) + phase;
end if;
end process phase_register;

ROM_8X256_I : rom_8x256
port map (
    a => phase_out,
    clk => clk,
    qspo => rom_out);

MUL_DSP48_I : mul_dsp48
port map (
    clk => clk,
    a => rom_out,
    b => amplitude,
    p => amplitude_out);
end architecture;

```

