INSTITUTO SUPERIOR TÉCNICO
Universidade Técnica de Lisboa

PMU Test Platform

Nuno de Burgos Simas do Canto Brum

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Juri

President: Prof. José Costa Freire

Director: Prof Marcelino Santos

1st Reader : Prof Carlos Beltran Almeida

2nd Reader : Prof Jorge Guilherme

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Acknowledgments

Nowadays Power Management is present in any electronic appliance and its performance is bound to influence the system autonomy, consumption and lifetime. From a Making a good and reliable Power Management Circuit requires a intensive testing at design prototypes.

The key performance figures for a power management design are: Efficiency, Accuracy, Line Regulation, Load Regulation, Line Transient, Load Transient, PSRR, Output Noise, Startup-up/Power-Down Time, Power Consumption, Over-Current protection and current protections. In order to have a thorough analysis of these parameters, is only feasible if there is a test platform that allows a fast characterization of these parameters.

This project proposes a solution for the automation of the characterization of Power Management Units. It provides programmable regulated supplies and two load types, which allow to set the operating point of the PMU. It also provides measuring channels of both input and output voltages as well as input currents. The output current is set by the built-in load.

Designed as a test Platform, it provides an interface to a daughterboard where the DUT is to be installed. This allows that the reuse of the platform for several PMU prototypes, only requiring for that purpose that a basic daughterboard to be built, containing the DUT and the necessary passive components for its operation.

The document also presents details about the physical implementation of the platform, such as PCB construction, critical lines and grounding schemes.

Resumo

Circuitos de Gestão de potência existem em qualquer dispositivo electrónico. A performance do circuito de gestão de potência é critical para o desempenho do sistema no que respeita a autonomia, consumo e tempo de vida.

Para fazer um Circuito de Gestão de potência que seja bom e confiável requer um intensivo período de testes em protótipos. Nesta fase, são testados diversas figuras de performance do dispositivo, tais como: Eficiência, Precisão, Regulação de Alimentação, Regulação de Carga, Transiente de Alimentação, Transiente de Carga, PSRR1, ruído na saída, tempos de reacção, consumos e protecções de sobre-carga de corrente.

Obter uma caracterização que percorre todos os pontos de operação, só é exequível se existir uma plataforma que permita a aquisição rápida de medidas. Este projecto propõe exactamente um sistema de teste para PMUs, providenciando para esse efeito, fontes de alimentação reguladas programáveis, e dois tipos cargas electrónicas para ajustar o ponto de operação do circuito de teste. Também estão incluídos canais de medida de tensão para os nós de entrada e saída e para a corrente no nó de entrada.

Desenhada para ser uma plataforma de teste, tem um interface para uma daughterboard onde se irá instalar o Dispositivo a Testar.

Este documento também apresenta alguns detalhes acerca da implementação física da plataforma, tal como o PCB, linhas criticas e esquema de massas.

Finalmente, são apresentados os resultados de caracterização de uma unidade de gestão de potência contendo um BandGap, um DC/DC e um LDO.

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1. Introduction

Nowadays Power Management exists in almost every electronic appliance. Be it an aeroplane, a satellite, a car, a cell-phone, or even a computer mouse there is a power management unit.

The demands for having cleaner energy, more autonomy and higher integration and less consumption translate directly into a need to generate more energy, to store more energy, and spend less energy.

In a system that needs several DC voltage levels to operate, and that needs to generate those voltages from a single power source, be it mechanical, or chemical or from the power grid, a good power management system is paramount for its efficiency and consumption requirements.

For having a good and reliable power management circuit, needs an exhaustive development phase coupled with an intensive prototype testing.

This project is a Test Platform for the test of DC to DC Circuits. The motivation for this project, the existing solutions and problems are described. Then the objectives and specifications for this project are detailed and enumerated the challenges that need to be surpassed.

It discusses the architecture of the project and the implementation details. Finally, it is presented the a test report of a power management IP testchip.

1.1. Motivation

A fundamental characteristic of a DC/DC converter is the energy transfer efficiency from one voltage node to the other. This efficiency highly depends on the operating conditions of the device. For a given DC/DC converter, the variables that influence efficiency are: the Supply Voltage; the Output Voltage; the amount of energy being transferred to the load; the temperature of the device, the switching frequency and the mode of operation in which the DC/DC is working.

A typical case for a test of a DC to DC converter, is where 5 input voltages are considered, with 15

different load currents, with 15 Output voltages, 2 switching frequencies, in 2 modes of operation and 3 different temperatures (max.; min. and room) will yield roughly 13500 tests.

Each test involves 2 voltage and 2 current measurements in order to calculate the Power Converter Efficiency[1]. Moreover, this test has to be repeated over a reasonable[2] number of samples to account for the dispersion of the technology process in which the component was manufactured and to evaluate possible yield problems.

The traditional setup resorts to GPIB connected instruments controlled by a Lab View executive application running on a Personal Computer. Accounting for the set of conditions, settling, integrating measurements, processing time and latency in the control bus, it takes about 1 second per acquisition. This is not affordable in today's semiconductor industry, because it would mean that the development cycles would be paced by laboratory validation and device characterization.

A possible answer to speed up the process would be to have an analog ATE to make this characterization, but there are several problems to that approach:

- cost of access to an ATE is prohibitive for an R&D activity: 3 to 4.5M$ for an ATE. Depreciation, maintenance costs and operation costs of the equipment in a 24h per day, yields about 4.5 cents /second.

- a specific load-board would have to be designed for the task and an ATE software program would have to be developed, characterized (and debugged), which again represents an additional cost. Part of this process is mandatory to be performed on the actual ATE, which increases its impact on costs

The aim of this project is to develop a Power Management Test Platform that provides a generic interface to a Power Management Test Chip (DUT[3]) internal settings and additionally has auxiliary circuitry needed to test the performance of the DUT. This auxiliary circuitry extends in function the connected monolithic instruments, and will enable reduction of the characterization time.

This Power Management Test Platform will have a direct application on the characterization of Power Management IPs and it can also be used as a demonstration unit to potential buyers.

1 Efficiency (η) of power converters is expressed as Pout/Pin, hence (Vout*Iout)/(Vin*In)

2 Depends on the statistical error wanted to achieve. About 40 samples is generally accepted.

3 DUT, i.e. Device Under Test´

1.2. Objectives

The objective of this Power Management Test Platform is twofold. It can serve as: a.) debug and characterization tool for the major key parameters of a Power Management circuit and b.) speeding up the characterization process.

The key parameters that can be characterized are:

- Efficiency (η) – ratio between the output power and the input power which is specially relevant in DC/DC converters. In mathematical form it can be expressed as $\eta=P_{OUT}/P_{IN.}$
- Accuracy – the absolute difference between the expected output voltage and the measured voltage in a given condition.
- Load regulation – the variance of the output voltage across different output loads. This is a quasi static measurement that establishes $\nabla vout(Iload)$
- Line regulation – the variance of the output voltage to changes in the input voltage This is is a quasi-static measurement that establishes $\nabla vout(Vinput)$.
- Line transient – dynamic measurement that captures the response time of the Power converter to a change in the input voltage.
- Load transient – dynamic measurement that captures the response time of the Power converter to a change in the output current.
- Power Supply Rejection Ratio (PSRR) – the output voltage immunity of a power converter to stimuli present on the supply or on the voltage input. This is a dynamic performance value that is dependent on the stimuli spectral components.
- Output Noise – the RMS noise level of a given output. Typically IC manufactures give the noise power in integrated in a band between 10Hz and 100kHz.
- Start-up-time – the time that the Power Management circuit takes from power down state till to functional state within performance limits.
- Enable/Disable time – the time response to the IP to Enable/Disable signal
- Power Consumption – the quiescent current being used by the Power Management IPs for it's own operation.

- Over-current Protection – the trip-point of the over-current protection circuits built-in in the power management IP (if any).

- Current Limit and/or Fold-back – The voltage/current fold-back profile of the power management IP (if any).

1.3. Organization of this Document

The following chapter briefly describes the architecture of the Power IC test platform. Next, chapter 2 details the components that build the platform and the implementation issues that arise from its physical implementation. On chapter 3 is analyzed the implementation of the control application at Application Level (PC) and at Firmware level (micro-controller).

On chapter 4 the test methodologies are reviewed and its application to the measurements defined as objectives for this platform.

In Chapter 5 are presented the test results of Management Testchip using test and automation methodology proposed in this document on a fast prototyping board. Hardware bring-up delays hindered the usage of the platform for this purpose.

Chapters 6 and 7 analyze what are the future steps and final considerations about this project execution. The following annexes complement the information given in this document. There can be found the bibliography, schematics and source code used for this project.

2. Architecture

A generic test environment for a Power Circuit is depicted in Figure 1.

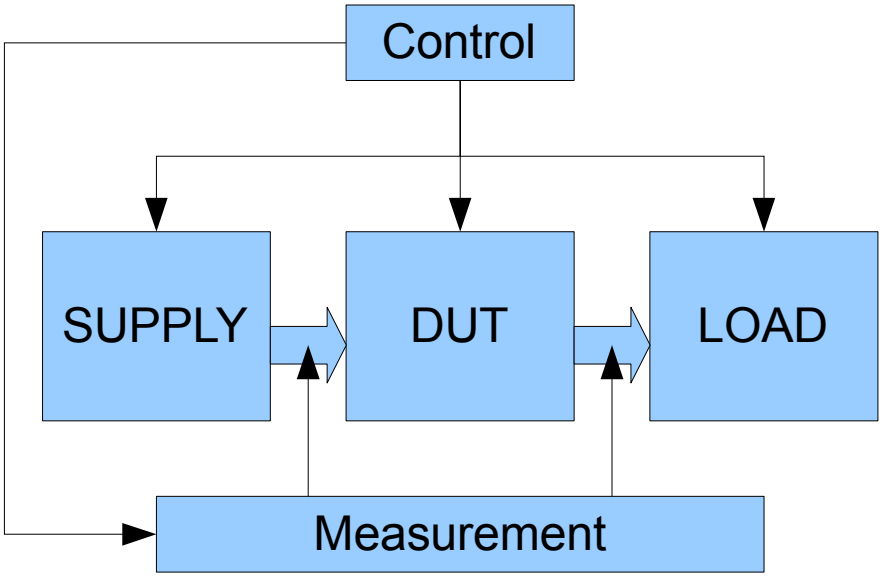


Figure 1: Generic Power Circuit Test Environment

The supply block provides all the voltage inputs to the device under test (DUT). On the load side, are the circuits that sink current. These can be either electronic loads or resistive loads. The control block, is responsible for the interface with the DUT, and also for changing the supply and sink settings.

In measurement block, are the circuits that measures voltage on both inputs (supplies) and outputs (loads) of the DUT. The current is measured in the input node. Current is measured at the input node of the DUT. At the output, the current is established by the loads.

3. System Design

In order to use the same platform for the characterization of several test chip, the same architecture that is used in commercial ATE was used here. It consists of a common platform where all controls; supplies; loads and measuring circuits are implemented (left side of Figure 2), and a load board where the DUT is installed (right side of Figure 2). The load-board (a.k.a. daughterboard) is only a simple design where the DUT installed together with the interface connector and the passive components needed for the PMU operation (decoupling and switched capacitors, switching inductors, etc...).

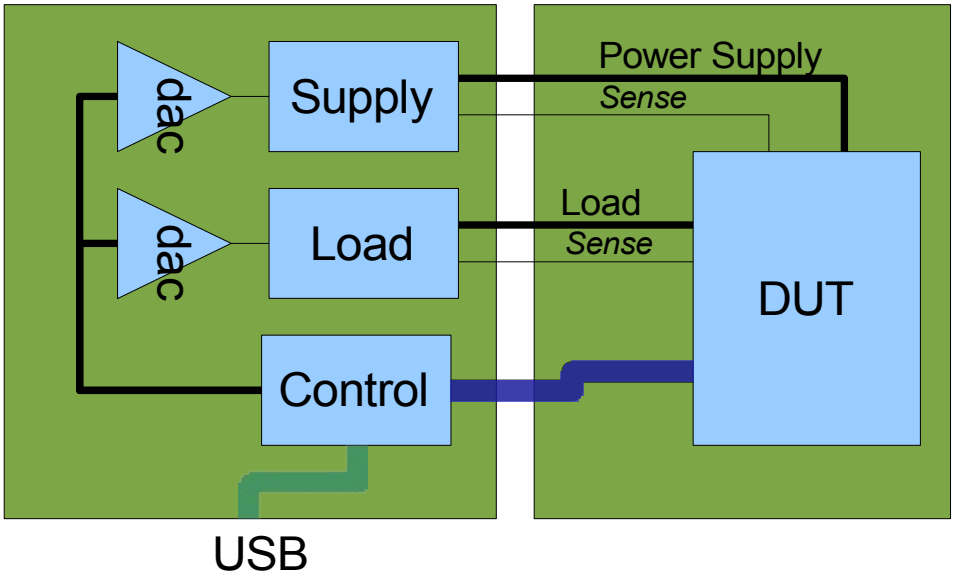


Figure 2: Platform Configuration

Taking into account that peak currents can achieve the order of 1A, to overcome the IR drop effect in power lines, sense lines are used. In sense lines no current will pass, thus allow the Motherboard supplies to compensate for the IR drop in the supply and load power lines.

3.1. Supplies

The supply of the Device Under Test must comply to a list of requirements: It needs to have a very low output impedance, be able to supply up to 250mA of current and yet have a low noise floor. The target is to have a noise floor below the -90dBm. For the current application, voltages as low as 1V and as high as 5.1V are required.

Dynamically, it should be able to react very quickly to load changes and conversely, be able to change output value quite fast. Additionally, it must be stable over a diverse set of output impedance's.

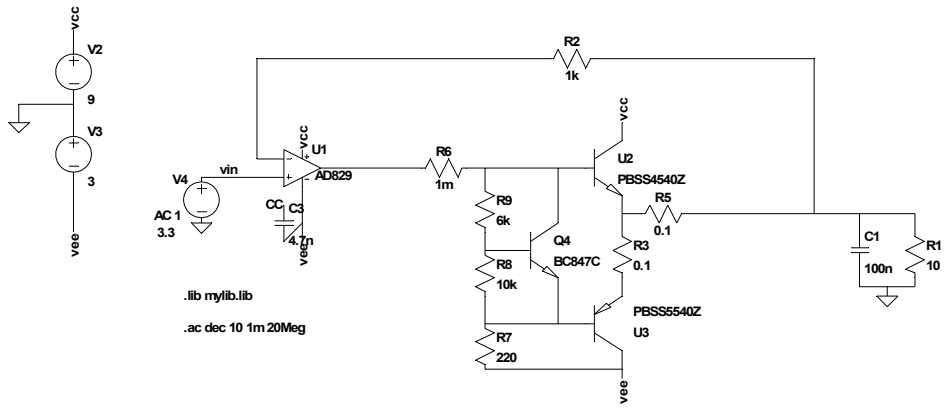


Figure 3: Power Supply Circuit

The solution found for the power supply is presented in Figure 3. The circuit is essentially a Power Buffer, based on an Low Noise, High Speed Operational Amplifier (U1), a VBE multimeter (R9,R8 and Q4), and the classical output of a Class A/B driver (U2 and U3).

The Operational Amplifier was chosen for being a very fast one, but still having a very low noise, which is critical for maintaining the Power Supply output with minimal output noise. The need for a very fast amplifier is to be able to make PSRR tests. The simulated bandwidth of the circuit from input (V4) to load (R1//C1) is shown in Figure 4.

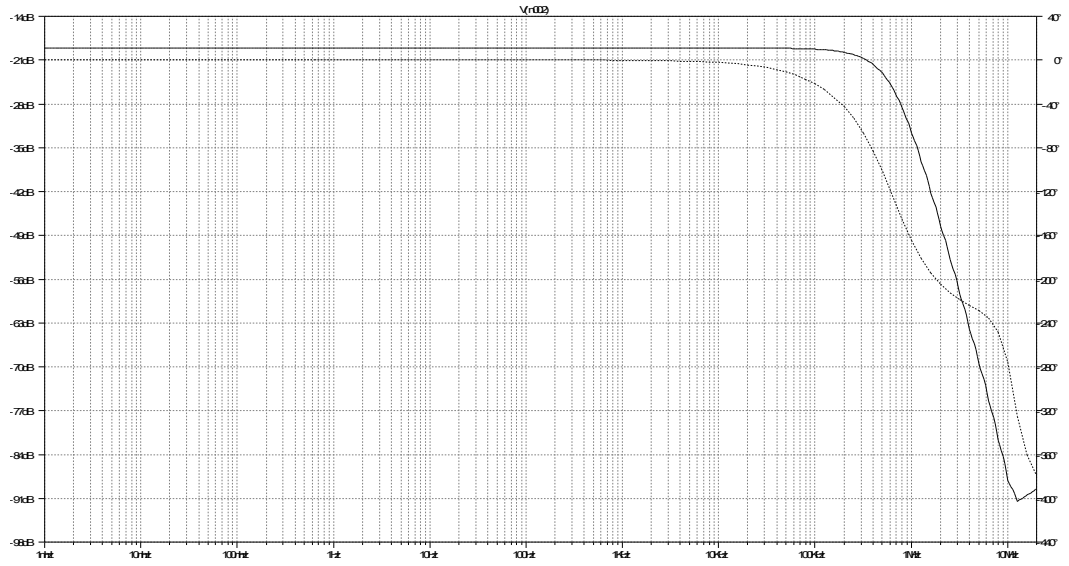


Figure 4: Power Supply Bandwidth

The stability open gain simulation is presented in Figure 5.

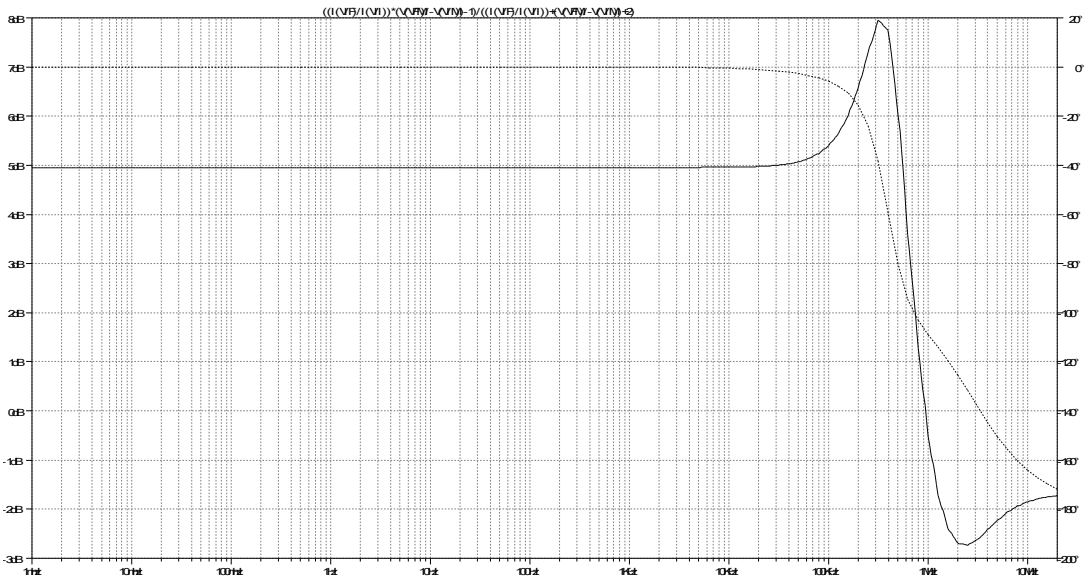


Figure 5: Open Loop Transfer Function

The simulation circuit for open loop simulation is presented in the Figure 6.

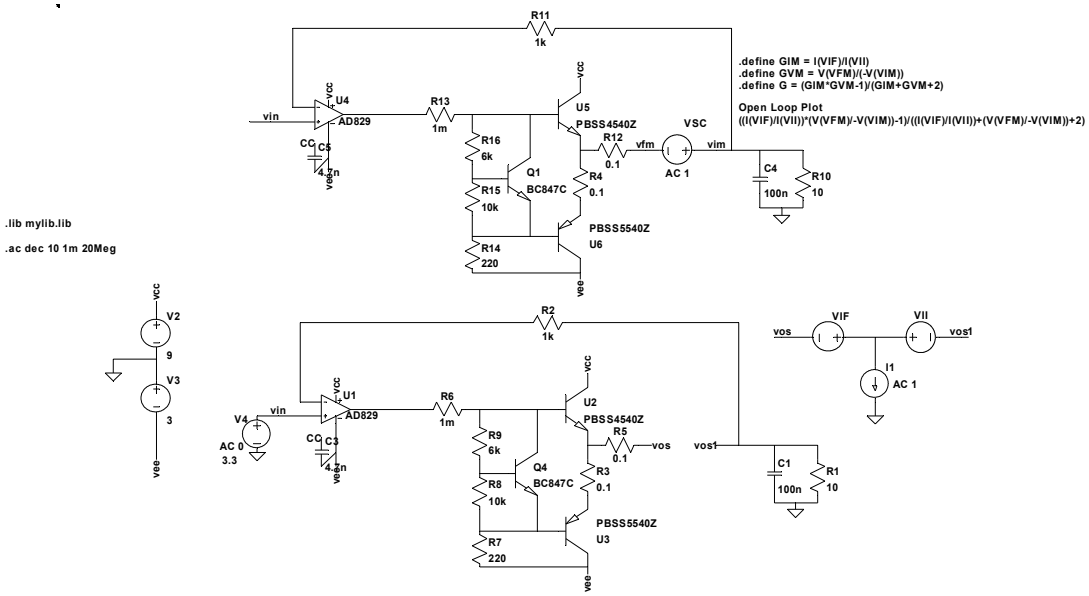


Figure 6: Open Loop Simulation Schematic

For open loop analysis it was opted to follow the method described in [1] have a two similar circuits. The open loop transfer function is obtained without opening the loop, but using two identical circuits, in which one is used to calculate the open loop voltage gain (top of Figure 6) and other to calculate the open loop current gain (bottom of Figure 6).

This design is embedded into the schematic in Figure 7 for reader's convince. It can also be found on Annex A page 11.

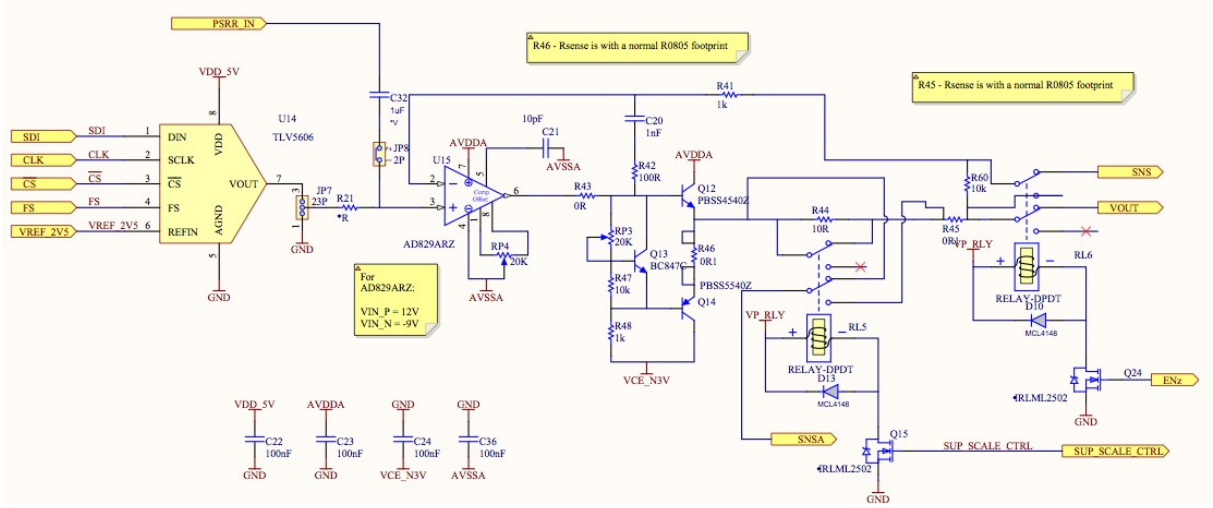


Figure 7: DUT Power Supply

The IC in the left side of the schematic is a SPI controlled 10 bit DAC from Texas Instruments. This DAC will serve to set the voltage in the Power Supply in case JP7 is set in position 2-3. The reference VREF_2V5 is given by a dedicated IC in another schematic sheet and defines the half-scale point of this DAC. The reference IC was tuned to give 2.6V so that the full scale of the DAC is 5.1V

The Texas Instruments DAC is limited to 1.25MHz Sample Rate. There is no anti-aliasing filter in front in order to minimize output settling time in static measurements.

For PSRR measurements, the PSRR_IN port is used to input the PSRR AC stimuli, being the DC given by the DAC. In this case the C32 and R21 form an high-pass filter pole from the PSRR_IN port to OPAMP input.

Another alternative is to supply the DC+AC stimuli directly into the OPAMP positive reference using JP7 pins 2-1 as an input connector.

The quiescent current of the Class AB can be tuned by the potentiometer RP3 in the VBE multiplier can be tuned by the potentiometer RP3. Since this power amplifier is going to be working most of the time supplying current[4], the output stage is unbalanced, being the output resistor R46 only used for sinking current. Transistors Q12 and Q14 must be assembled next to each other to maximize the thermal coupling. This is done to make sure that the transistors keep matched and avoid thermal drift of the Class A/B.

The feedback loop of the OPAMP in default operation (both relays in default state), is connected to a sense point placed as close as possible to the DUT in order to compensate for the IR drop that will exist on power lines. Resistor R60 exists for the case when the Daughter-board is not connected, and insures that a loop path always exists. When the daughterboard is inserted, it will surely have a significantly lesser resistance, and thus the impedance of R60 is negligible.

There are two series resistors (R44 and R45), that serve as current sense resistors. The sensing

4 Only for PSRR tests that the Class A/B capabilities are used.

points are the ports SNSA and VOUT. While in default operation R44 is shorted by RL5, so the sensing voltage is proportional to (V_{SNSA}-V_{OUT}) *R45.

Take notice that the sensing point is also switched by RL5, so that the parasitic resistance of R44 shunt does not interfere with the measurement.

When RL5 is energized then, the sensing voltage is proportional to (V_{SNSA}-V_{OUT}) *(R44+R45).

The R45 resistor is a 0.1Ohm resistor with a 0.1% accuracy, but this does not avoid that calibration procedures need to be done prior to usage as current sensing.

Relay RL6 at the most right side of the schematic, serves to place the circuit output into high impedance.

Another aspect that is worth mentioning here, is the presence in the schematic of the R41, R42 and C20 network in the feedback loop. R42 and C20 do not exist in the original design and placed here only as a safeguard and will not be assembled at the board's birth. There can be a significant contribution to phase shift introduced by a long distance from Power Supply to DUT, and specially from decoupling capacitors that normally exist near the DUT. This may degrade the stability of the original circuit, and thus we may need to introduce a these components in order to make the circuit stable.

3.2. Loads

For this project two kinds of loads were considered. The first one is a simple programmable current sink with a sink range from 0 to 200mA in 1024 linear steps (195.3uA per step), and the other is a resistive load.

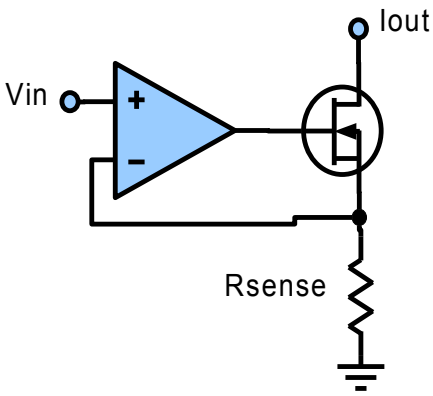


Figure 8: Current Sink Conceptual Drawing

3.2.a) Current Sinker

The Current sinker design follows the topology defined in Figure 8. The virtual shunt created by the OPAMP, sets the voltage across the 0.1Ohm resistor Rsense, thus establishing a sink current on the output transistor.

Figure 9 illustrates the current sinker implementation. It uses the same DAC that was used for the DUT Power Supply for rationale purposes. It is important from a design point of view to minimize the number of different items in a BOM. Also the reference that it uses is shared with other circuits including the Power Supply, but for this circuit it is divided by two by R51 and R54.

The output of the DAC is further divided by the relation of R52 and R55 and used as positive input for the OPAMP.

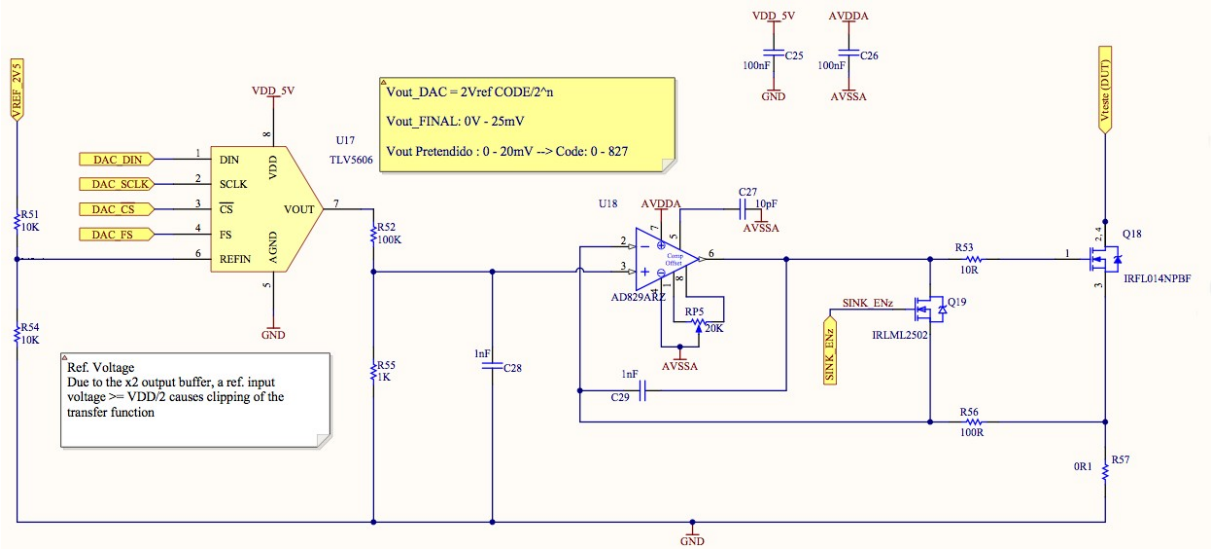


Figure 9: Current Sinker

The output current of this circuit is given by:

$$I_{SINK} = \frac{\left[\left(\frac{R55}{R55+R52}\right)\times\frac{DAC_{CODE}}{2^n}\times 2\times\left(\frac{R54}{R51+R54}\right)\times VREF\right] - Voff_{OPAMP} + R56\times Ibias_{OPAMP}}{R57} \quad (1)$$

With R54= 10kOhm ; R51= 10Ohm ; R55= 1kOhm ; R52= 100Ohm ; R57=0.1Ohm VREF=2.6V and n=10

$$<=> \quad I_{SINK} = \frac{\left(\frac{1}{101}\times\frac{DAC_{CODE}}{1024}\times 2\times\left(\frac{1}{2}\right)\times VREF\right) - Voff_{OPAMP} + 100\times Ibias_{OPAMP}}{0.1} \quad (2)$$

$$<=> \quad I_{SINK} = \frac{\left(\frac{DAC_{CODE}}{1024\times 101}\times 2.6\right) - Voff_{OPAMP} + 100\times Ibias_{OPAMP}}{0.1} \quad (3)$$

$$<=> \quad I_{SINK} \approx 251.39\times 10^{-6}\times DAC_{CODE} - 10\times Voff_{OPAMP} + 1000\times Ibias_{OPAMP} \quad (4)$$

Since this is to be used for measurement, the final circuit needs to be characterized so that the residual current associated with the OPAMP offset and bias are determined as well as the gain error associated with the component tolerances.

The resolution step of the current sink is given by the LSB value and is only dependent of 2.6V reference tolerance and resistor tolerances. Even if assuming 1% resistor errors, the accuracy will be about 4 times less than 1mA.

Stability Analysis

Stability analysis in open loop was analyzed using the Figure 10. In the circuit on the bottom of Figure 10 we apply the stimuli in voltage mode in the output. The bottom circuit only serves to bias the transistor, and its limited in bandwidth by capacitor C1. The source of transistor M1, <<vr>> is applied to the open loop identical circuit in the top through a voltage dependent voltage source. The open loop transfer function is taken as the ratio between Vz and Vr and it is shown in Figure 11. Since there is already a signal inversion in the transfer function, margins are calculated towards 0º. Hence, there is about 80º phase margin and 70dB of gain margin.

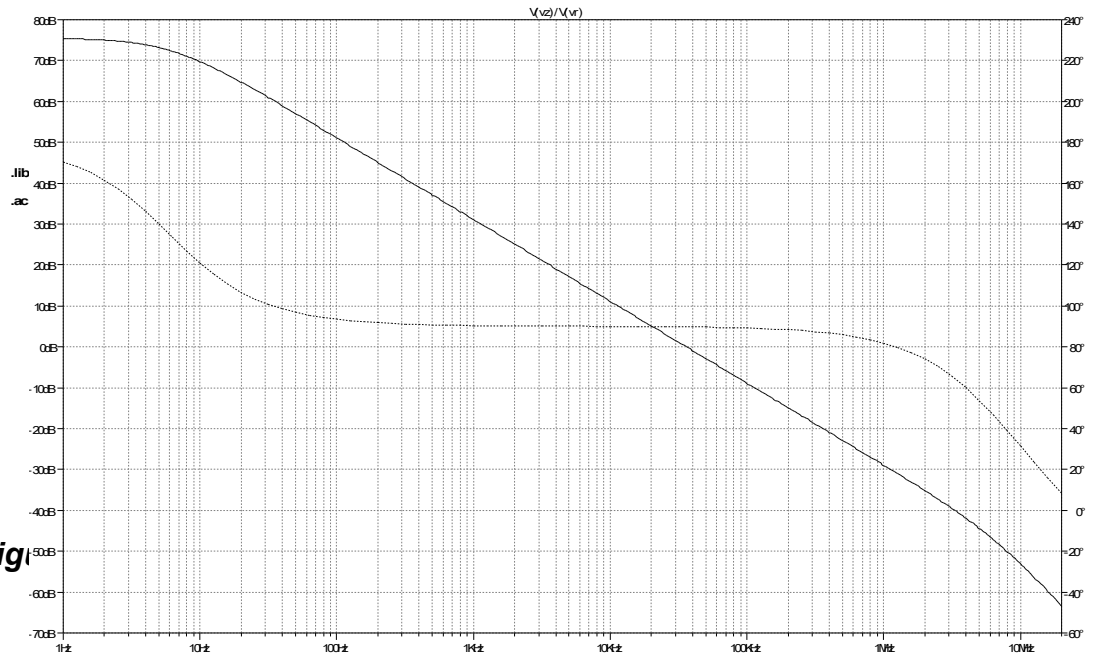


Figure 11: Current Sink Stability

3.2.b) Resistor Load

The purpose of this circuit, as was stated in the project analysis, is to make an automated characterization of the fold-back current of DC/DCs.

Normally this test is done with an actual resistor, which value is slowly being decreased and forcing the DC/DC to supply more current. When the DC/DC reaches the maximum current, it will cease to regulate, and the output voltage will drop to an unregulated voltage. Since the voltage drop means a drop in current, and the DC/DC will fall into a certain point for a given output resistor.

Going on the opposite direction, i.e. increasing the output load resistor, will cause the current to decrease, and at a given point the DC/DC will be able to resume regulation.

The current fold-back test traces Vout/Iout curve in both directions, and determines the trip resistance where the DC/DC ceases to regulate, and afterward determines the resistance where the DC/DC will start regulating again.

Doing this test using an actual resistor, is hard to automate, so, it we designed a circuit that emulates the resistor behavior. One of the difficult specifications for this resistor emulator, is the frequency bandwidth. An actual resistor has theoretically infinite bandwidth, while an resistor emulator has a bandwidth limited by the bandwidth limitation of its components. For this test, the bandwidth should be at least significantly higher (>>10x) than the DC/DC response time.

The electronic load was initially conceived as illustrated in Figure 12.

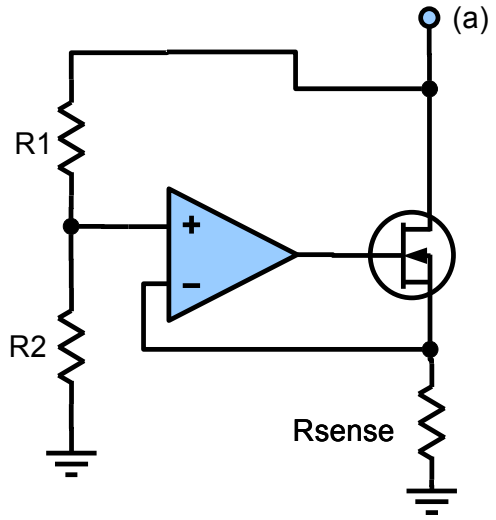


Figure 12: Electronic Load

The current at the input port is given by the following equation:

$$Ia = \left(\frac{R2}{R1+R2} \cdot \frac{1}{Rsense} + \frac{1}{R1+R2} \right) \times Va \quad (5)$$

or

$$Ia = \left(\frac{R2}{Rsense} + 1 \right) \times \left(\frac{1}{R1+R2} \right) \times Va \quad .(6)$$

Since the R2 >> *Rsense*, then the equation is simplified and the equivalent input impedance of the circuit is given by:

$$Za = \frac{R1+R2}{R2} \times Rsense \quad \Leftrightarrow \quad Za = \left(\frac{R1}{R2} + 1 \right) \times Rsense \quad (7)$$

By changing R1 we have a linear relation with the equivalent Za. This was the first approach, unfortunately the programmable potentiometer that we needed was not available at the supplier, and the alternatives had problems with the maximum frequency.

The backup plan for this circuit is illustrated in Figure 13.

This solution has the advantage that can have a much higher resolution that would be obtained with a potentiometer. With a off-the-shelf potentiometer a typical resolution is of about 8 bits, and with a DAC, resolutions can be as much as 10 or 12 bits.

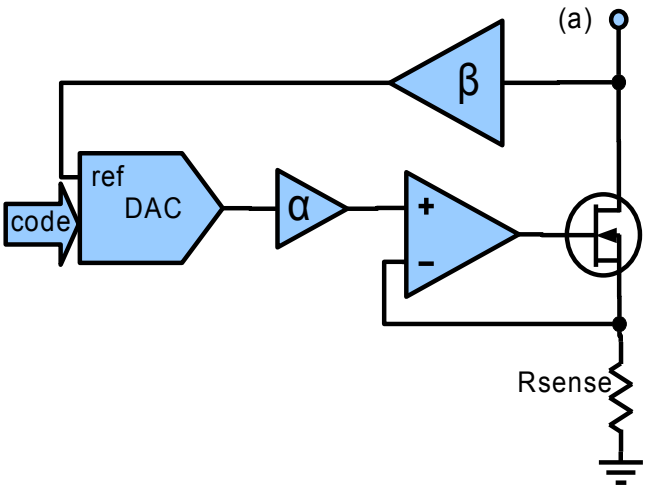


Figure 13: Resistive Load (Backup Solution)

Another advantage of using a DAC is the fact that the bandwidth response from ref to output is much higher than the potentiometer. Also, price-wise, the DAC is less expensive than the Potentiometer.

The 100K 8 bit potentiometer had a 40KHz bandwidth and the 10K has a bandwidth of 400KHz, whilst the DAC used in the design has a reference to output bandwidth of 1.3MHz.

Considering that the output voltage for the TLV5606 DAC is given by the following formula.

$$V_{DAC} = 2 \times V_{REF} \times \frac{DAC_{CODE}}{2^{10}} \quad (8)$$

the current sinking into port (a) is

$$I_a = \frac{\frac{2 \cdot V_a \cdot \alpha \cdot \beta \cdot DAC_{CODE}}{2^{10}}}{Rsense} = \frac{2 \cdot DAC_{CODE}}{2^{10} \cdot Rsense} \times V_a \quad (9)$$

hence the equivalent resistor is given by

$$Z_a = \frac{2^{10} \cdot Rsense}{2 \cdot \alpha \cdot \beta \cdot DAC_{CODE}} \quad (10)$$

The factors α and β are present in the circuit in order to match the input voltage into the DAC range of operation. The selected DAC is the Texas instruments TLV5606 has a vref range of operation from 0 to VDD, but by equation (8), in order to avoid clipping it is recommended that the reference be kept below VDD/2.

Since this is a closed loop control, there is need to analyze the stability of circuit. This was not possible till the moment since we couldn't find any spice model of the DAC transfer function. In alternative, we are going to implement the circuit and have provisions to improve stability by trial and error.

The major inconvenience of this circuit comparing with the first solution is that the setting code appears at the denominator of the function. This means that the resistor resolution is higher in big equivalent resistances and in smaller resistances the resolution is lower.

For the current circuit application that it is good enough to have resolution in smaller resistances.

3.3. On-board instrumentation

As seen in the project analysis document, it was decided to include at the board voltage and current measurement capabilities for both supply and load. Also, provision must exist so that the external instruments can be used for calibration and for DUT characterization, in case higher accuracy is needed.

3.3.a) Supply side

For the supply side the foreseen solution for voltage and current measurement is presented in Figure 14.

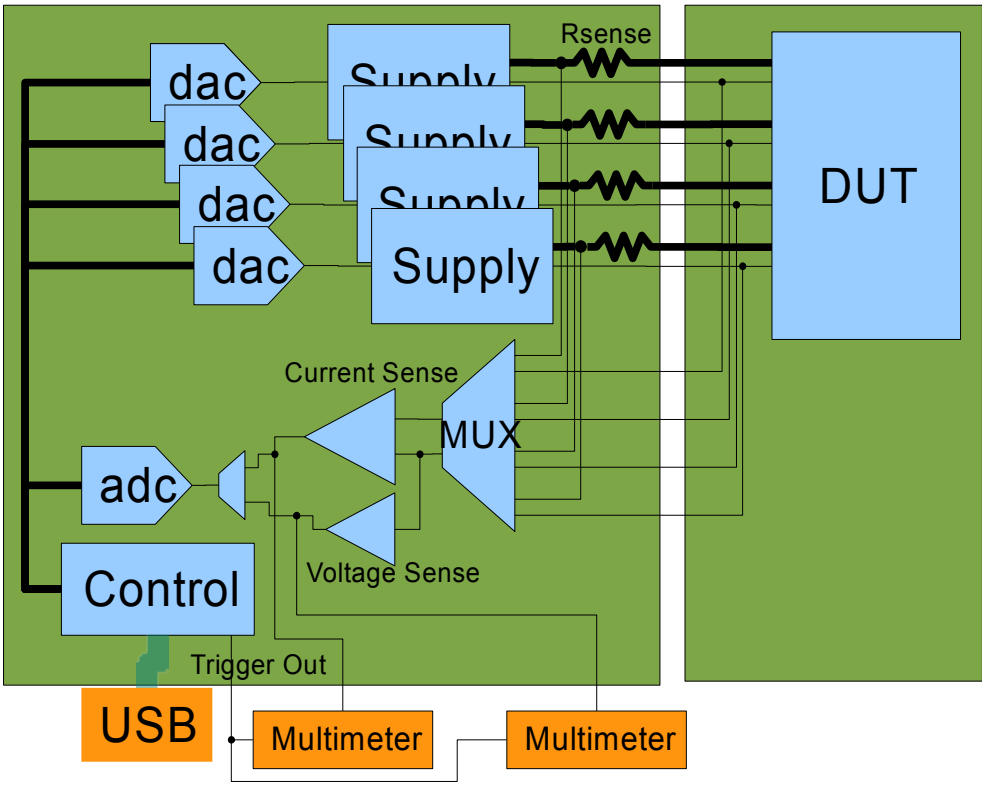


Figure 14: Supply Current and Voltage Measurements (Conceptual View)

The current is calculated based on the voltage drop in the sense resistor present in each supply schematic. An instrumentation operational amplifier (OPAMP) is used with adjustable gain (x10, x100) is used to convert the resistor voltage drop into a single ended signal. The output voltage is then buffered by a second OPAMP in order to keep both sense lines in a high impedance node.

Schematic for this circuit is on page 10 of Annex A (PMU Tester Schematics).

The MUX used is the ADG407BNZ (U10), a two way 8-to-1 analog multiplexer from Analog Devices. The first 5 inputs are used for sensing current and voltage from the built-in power supplies. The remaining inputs are going to be discussed later. This analog multiplexer has a typical RON about 80Ohms, which are relatively low when comparing with the input impedance of the Op-amps.

For current measurement, the INA141UAE4 instrumentation OPAMP is used. This instrumentation OPAMP has two preset gains that are being controlled by relay RL4. Combining this gain with the configuration of the sense resistor of the power supply we achieve dynamic range of 60dBA (x1000).

Table 1: Current Sensing configurations

OPAMP (Gain)	Power Supply Sense	I to V
10x	0.1Ohm	1A/V
10x	10.1Ohm	9.9mA/V
100x	0.1Ohm	100mA/V
100x	10.1Ohm	990uA/V

For voltage reading the AD8595 (U12) is used (Substitute schematics) in a voltage follower configuration just to buffer for the ADC input which is known to generate some noise due to sampling and hold operation.

Both voltage and current sense are then converted into digital domain by an on-board 10bit ADC, or by external multimeter. To speed-up acquisition, the external instruments should be placed in “trigger mode”, and the acquisition be controlled by the platform micro-controller.

Due to precision tolerances of the sense resistors and the non negligible resistance on the power lines and the offset of the buffers, a calibration must be done per channel.

This calibration procedure is the following:

1. First the 2.5V reference that used for all supplies must be trimmed. This reference is generated by the LT1009CZ#PBF, a trimmable reference IC present on page 6 of the Schematics. Since the specification for maximum voltage is 5.1V and the TLV5606 DACs used in power supplies have the full scale in 2x their reference, the reference must be trimmed to 2.55V by usage of potentiometer RP1.
2. Secondly the voltage readings of the ADC must be calibrated. Please note in page 10 of schematics that the 2.5V reference that is used for all power supplies is connected to the 8th

input of the multiplexer in order for its value to be read and determine the offset error of the ADC.

3. Reading the value of each supply with corresponding DAC set to half scale (same voltage as its reference), allows to determine the DAC + Power Buffer reading offset.
4. Then repeating this operation for all the supply voltage settings, generates data that allows to determine the gain errors of the A/D converter[5].
5. Last, a known load must be placed in the DUT side, and a current reading must be done by the platform. Repeating this operation for two or more loads, will allow to calculate by linear regression, the gain and offset of the measuring function.

A major requirement is that all the blocks have a monotonic behavior, and that the resolution of the calibrating instrument, be at least two times superior to the on-board SAR ADC.

Once the calibration is done, the error compensation of the current reading can be done by the micro controller on-the-fly during data acquisition.

Final notes on page 10 of the schematic:

- All the Power Supplies DACs as well as Current-Sink and Load DACs are controlled by an SPI interface. In order to save pins, the SPI interfaces share the SDI and SCLK pins and only CS (chip select) is independent. The SCLK is a very critical line, reflections on this line, it will cause malfunction of the DAC operation. The SCLK is routed passing through all the DACs in daisy-chain, and to avoid reflections, this net is terminated and the impedance of the trace be controlled so it matches the termination. R37 and R38 make in parallel an termination of 75Ohm. The capacitor in series make this termination only visible in AC, so there is no DC current even if clock is stopped.
- There are two inductor beads that are used to filter the Analog Supply. These inductors block high frequency noise that come from micro-controller digital operation and that could affect output noise of the Power Supplies.
- The reference of the Instrumentation OPAMP is equal to the negative reference of the 10bit ADC used to make current measurements. The smaller the difference between positive and negative references of the ADC the better voltage resolution int the ADC reading. Two resistor dividers R35;R36 and R64;R65 allow to change the ADC VREFN and VREFP respectively. The current resistor values set VREFN to 0V and VREFP to 5.4V[6]. If there isn't a need to read voltages as low as 0V, or has high as 5.4V there is a real benefit in changing

5 This correction assumes that the DAC has the announced linearity. It should be verified by experimental measurements.

6 VREFP = [R65/(R65+R64)]*AVDD = [15k/(10k+15k)]*9V = 5.4V

these two relations. For the first usage of this platform, the minimum voltage that needs to be read is a bit less than 0.8V (DC/DC output) and the the maximum is 5.1V (DC/DC input).

3.3.b) Load side

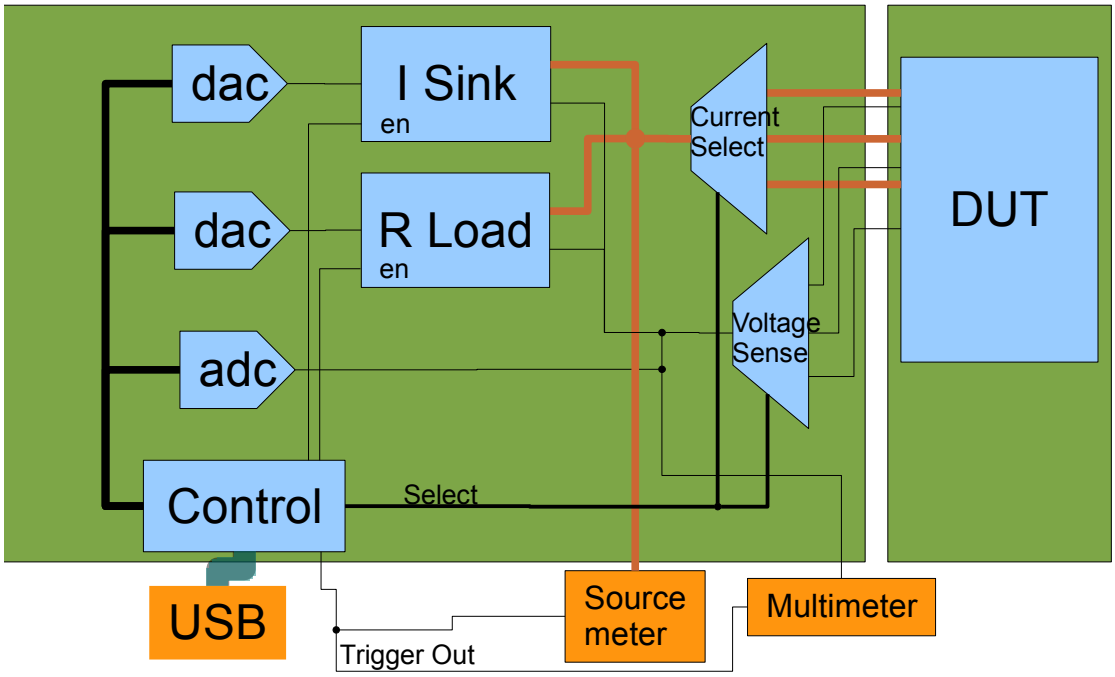


Figure 15: Load Voltage and Current Measurement (Conceptual View)

For the load side the foreseen solution is presented in Figure 15. Since only one Power Management IP is to be tested at one time, we have a current select block and a sense select block that configure which IP is going to be subject to test. The output select is done by two channel dual pole single throw relays, being one channel reserved for the sense signal and the other for the power signal.

The selected output voltage of the IP is read by the built-in ADC passing through the MUX also used for the supply voltage measurements seen on page 11 of Annex A.

Once the output is selected there are 3 possible testing options: a Current Sink; an Electronic Resistor Load; or an external test equipment. All these three testing options are tied together in the same node. To disable their sinking function both Current Sink and Electronic Resistor have independent enable pins. The external source meter usually has a disable function, so, it is possible to select which sinking element is being used.

If the on-board load circuits are used (R-Load or I-Sink), it is assumed that the current established in the DUT output is the one defined by the load circuit setting. In order to insure this, calibration of the load circuits is needed prior to its use.

The calibration procedure starts with the calibration of the output voltage measurement circuit. This requires a circuit to impose the voltage output instead of the DUT like for example a source meter or precision power supply. If none is available, a practical solution is to loop the supply output directly to the load output, and provide that voltage and current are monitored by an external calibrated multimeter.

The calibration of the R-Load and I-Sink must be done separately, but the procedure is the same. Sweep the current setting or the resistance setting respectively if for the I-Sink or the R-Load, and measure the current being sinked. For the R-Load this sweep must be repeated for several input voltages, because the current being sinked is also a function of the input voltages. For the I-Sink, although this is not the case, is recommended to test the sink function in the maximum and minimum input voltages.

3.4. Printed Circuit Board

The DUT is not directly attached to the platform printed circuit board (PCB). Instead it is attached to a mezzanine (a.k.a. piggyback) daughter card. The platform provides to the daughter card 5 independent supplies and 3 selectable output loads, so it can accommodate PMU testchips with up to 3 Power Management IPs. Since the load circuits are shared between outputs, only one can be tested at one time.

3.4.a) Layer Stacking

It is recommended that at least the daughterboard PCB be designed with a minimum of 4 layers, in order to achieve the optimum environment for the DC/DCs operation. Rationale for this is that switched power management devices demand very high current surges and specially in DC/DCs, the low resistance path between input and output capacitors as well as for the coil, are critical factors for the resulting efficiency. As such, the advised layer configuration is to have two signal layers, and two ground/supply planes.

The chosen PCB structure is depicted on Figure 16. The top and bottom layers are signal layers and the internal planes are ground and supply rails. This offers two advantages[7] for our project:

7 There are some known disadvantages to this approach, as it is more prone to emit radiation and conversely to absorb interference.

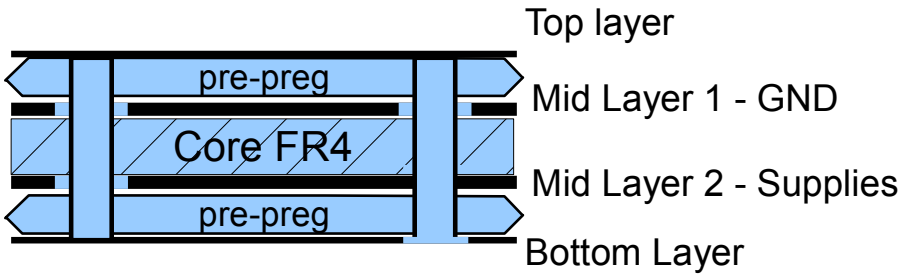


Figure 16: PCB Layer Stacking

- Easier Debug – Being the signal layers the external ones, it offers better access to probe signals and
- Trace Impe “microstrip”) have half of the medium air as the die is results that the trace impedance circuit (IC) signal outputs have limited current drive, offering a lower impedance for the driver to “see” is <u>often</u> beneficial. Often is underlined here, because there are a few situations where a low impedance is desirable, but for these cases there is the option of enlarging the trace widths.
- Better EMI performance – Without any ground planes, supplies and ground rails must be routed as normal trac For better EMI performa current loops like the one in Figure 17 should be avoided. ey not only pick up RF ise from aerials, they also will emit electromagnetic inter nce. Using a complete s plane, will act as a shield and protect signals, specially long es from acting as antenna

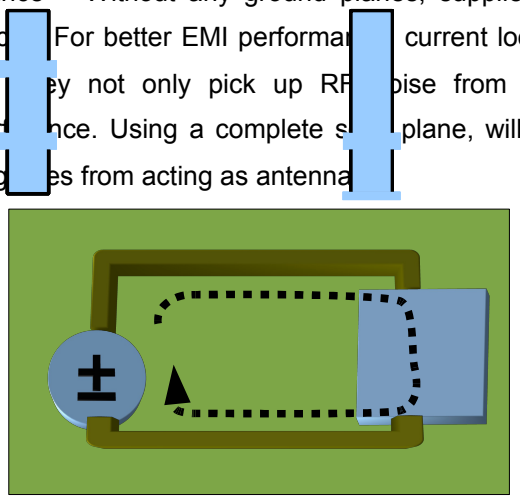


Figure 17: Current Loop

For single or double sided boards, it is advised to route ground and supply rails side by side or one on top of the other, so the area of the loop is minimized. See Figure 18.

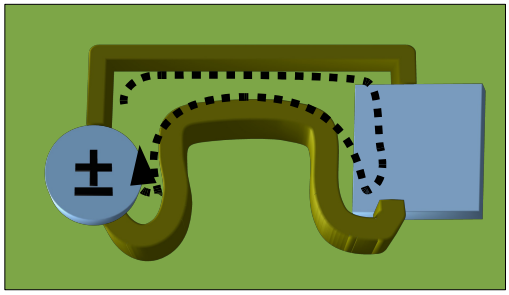


Figure 18: Minimizing Current Loops

3.4.b) Grounding Scheme

Choosing between having a common ground or alternatively separate analog and digital grounds at PCB level have been subject to many discussions, in papers and technical forums.

The main rationale for separating analog and digital grounds is to avoid that the noise generated by the digital grounds affects the performance of highly sensitive analog circuits. This approach is good but has a few handicaps. In some situations if extra care is not taken, it may even cause greater disturbance to the critical signals.

For example, If there is a digital circuit is operating next to an analog circuit, and has some controls that need to cross the boundary between analog and digital areas like is depicted in Figure 19. With this configuration the return path makes a loop that will lead to a bad EMI performance and will degrade noise margins at the digital signals.

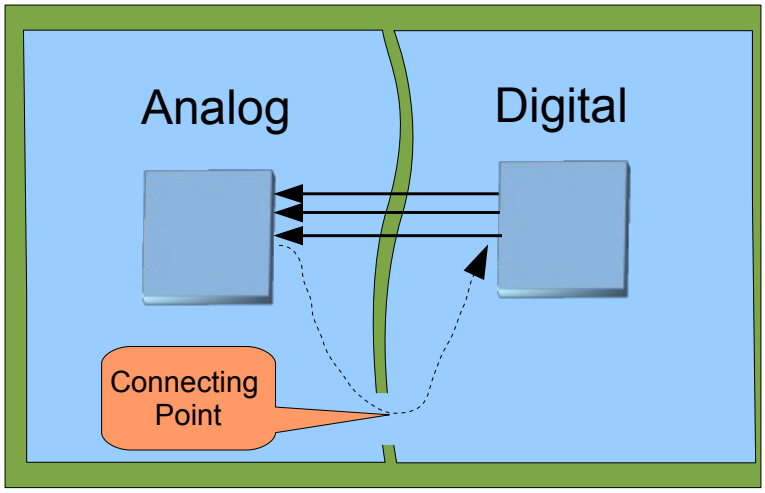


Figure 19: Separate Ground Issues

The solution of having a single plane doesn't have these problems, but there are a few issues that must be taken into consideration. Take for example the situation illustrated in Figure 20.

There are two digital blocks that communicate between each other and the lines are routed over a analog section of the circuit. In this configuration the Analog section will be perturbed by the digital signals toggling and by their return path which shares a common ground.

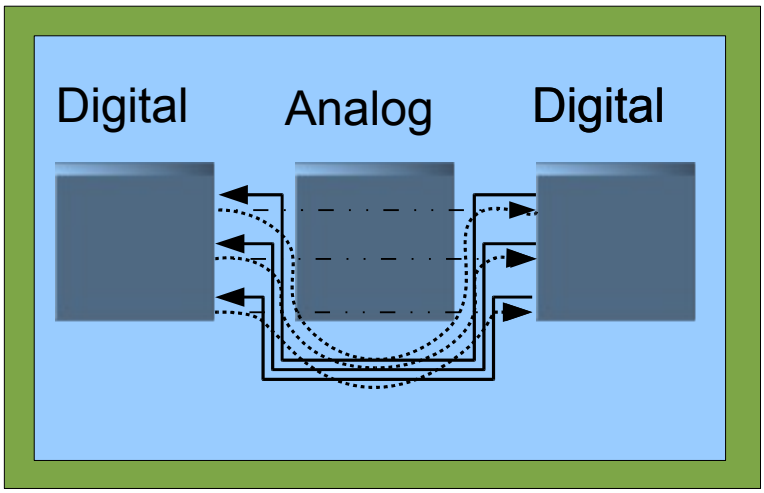


Figure 21: Return Path in a common ground

In Figure 21 it is shown the case where the digital signals are routed in order to avoid the analog section. What happens in this case is that the return path of those signals will choose the least impedance path. Which means that near DC, least impedance return path is the shortest path, passing through the analog section. But, if the signals are of high frequency, then the least impedance return path will pass as close as possible to the matching trace.

The best is to simply keep analog and digital areas separated and avoid having signals crossing boundaries. In Figure 22 it is described what is believed to be the best practice.

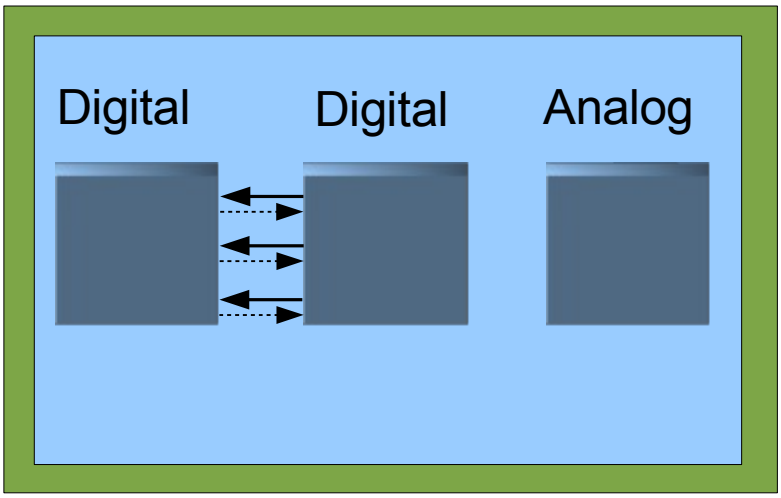


Figure 22: Best Solution for a Common Ground

3.4.c) Decoupling Supplies

Although all the domains preferably share the same ground, in what concerns supplies, they are going to be separated. Digital and Analog Supplies even if at the same voltage level, will have their own dedicated voltage regulator. A good LDO operating with enough dropout margin, insures decoupling of

low frequency (LF) noise.

For HF the option is to place 100nF(X5R) and 100pF(C0G/NP0) Ceramic Capacitors per each supply pin, and 10uF for each Supply Line. For each analog supply, a ferrite bead in series before the regulator input capacitor will improve even more the noise rejection in VHF.

NOTE: All the capacitors should comply and not exceed the DUT application note or datasheet, so that the measurements are a fair representation of the DUT under normal operation.

3.4.d) Routing

There are two major concerns on the layout of this platform:

- High Speed Signal Integrity and
- IR- Drop in Power Lines

High speed signals or any signal that has fast rise/fall times are affected essentially by :

- Impedance mismatches in their path causing reflections
- Cross talk between traces. Specially relevant they run in parallel long distances[8] which is not a problem for this platform since there aren't high speed data buses .[9]
- and attenuation, which is not a problem for our platform since the operating frequencies are too small for attenuation to become a concern

Characteristic Impedance

Every time there is a change in the impedance of a transmission line, part of the signal energy passes through and part of the energy is reflected back to origin. The amount of energy reflected back is given by a reflection coefficient.

Reflection coefficient is given by

$$\Gamma = \frac{Z - Z_O}{Z + Z_O} \quad (11)$$

, where Z_O is the trace impedance where the signal is circulating and Z the equivalent impedance seen from the signal at the intersection point. When transmitting digital signals toggling at high frequencies, and with long propagation delays, if large reflection coefficients exist, then it may happen that reflections can distort the signal above the allowed noise margins thus causing bit errors.

8 Let define long when the distance is on the order of magnitude of the wavelength of higher frequency component of the signal with enough spectral power that can cause problems.

9 In case there is the need of routing in parallel, the thumb rule is to keep them apart at least 3 times the trace width.

As a thumb rule, there is a need to have special cares about reflections when the following inequality is true [2] and [3].

$$2 \cdot Tpd < \frac{Tr}{10} \quad (12)$$

where *Tpd* is the propagation time and *Tr* the rise or fall time of the signal.

Propagation delay is dependent on the velocity of a signal on a given material which is given by:

$$v = \frac{v_o}{\sqrt{\varepsilon_r}} \quad (13)\ [3]$$

where the ε_r is the dielectric constant.

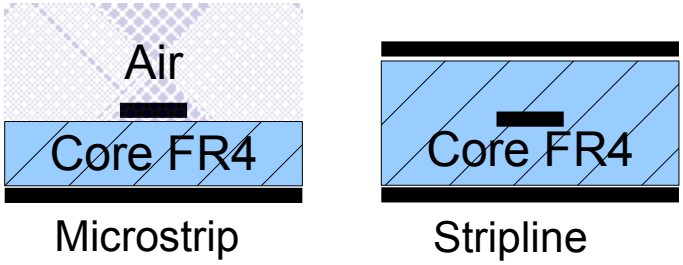


Figure 23: Microstrip and Stripliness

Signal velocity depends on where the trace is routed. For a Microstrip line, both air and substrate dielectric influence its propagation delay, whereas on a Stripline, it is essentially dominated by the dielectric of the core.

Roughly the propagation delay for Microstrip

$$Tpd = 85 \cdot \sqrt{0.475\,\varepsilon_r + 0.67} \quad \text{ps//in (14)[3]}\ ^{10}$$

and for Stripline is

$$Tpd = 85 \cdot \sqrt{\varepsilon_r} \quad \text{ps/in (15)[3]}\ ^{11}$$

The PCB substrate FR4 has a ε_r of 4.5 and thus computing the propagation delays :

Tpd= 142.423 ps/in for a microstrip and

Tpd = 180.312 ps/in for a stripline.

The rise and fall time reported on our micro-controller datasheet for an I/O port is typically 10ns. In case propagation delays are higher than 500ps, then line impedance matching becomes necessary.

So, 500ps propagation delay corresponds according to the formulas above to :

10 This is an approximation. For more accurate other factors must be taken into consideration, such has the distance to ground/supply planes, the geometry of the trace, the residual solder resist on top of the traces for the microstrip case, etc... More information can be found on [2]

Distance microstrip = 500/142.423 in = 3.5in = 8.9 cm

Distance stripline = 500/180.312 in = 2.77 in = 7.04 cm

For this platform the clock lines and USB differential pairs are identified as critical. Data lines are not considered critical because the system is designed to be clock synchronous, giving to data lines a setup time of about half clock period, which is more than enough for all reflections to be damped by non {-1;1} reflection coefficients and being clamped by IC inputs protection diodes to GND and VCC.

Since the SPI clock has a fan-out of 8 DACs, it was decided to use a daisy chain connection type and a parallel termination resistor at the far end as illustrated by Figure 24. [11]

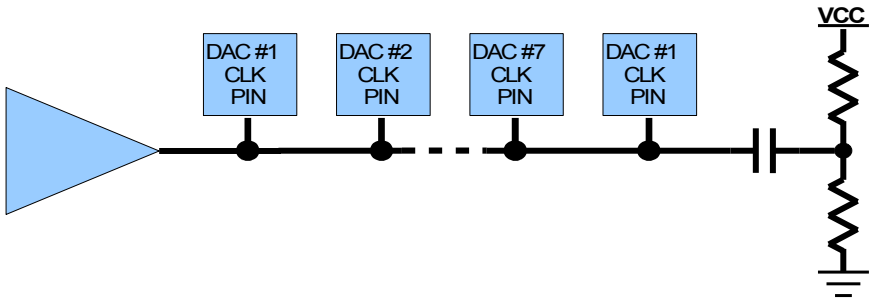


Figure 24: Daisy Chain CLK routing

The parallel of the two resistors on the termination side should match the characteristic impedance of the PCB trace. The series capacitor near to the resistor pair, is not essential for the impedance matching. It is there to kill the DC current flowing through the driver. The capacitor must be calculated in such that the time constant given by Zo.C be more than 10 times bigger than the clock period, otherwise the termination will not be effective.

For calculating the characteristic impedance of the traces first the board stack-up dimensions must be defined. In Figure 25 is the board build-up obtained from EUROCIRCUITS which is the elected PCB manufacturing provider for this platform. The dimensions of the stack-up are in Figure 26.

11 It was not possible to use the source termination resistor, since this is more appropriate for point to point communication.

Figure 25: PCB Layer Stacking (from EUROCIRCUITS)

In order to meet the 1.55 mm standard stack-up, two layers of prepreg of 100um were removed from the stack-up.

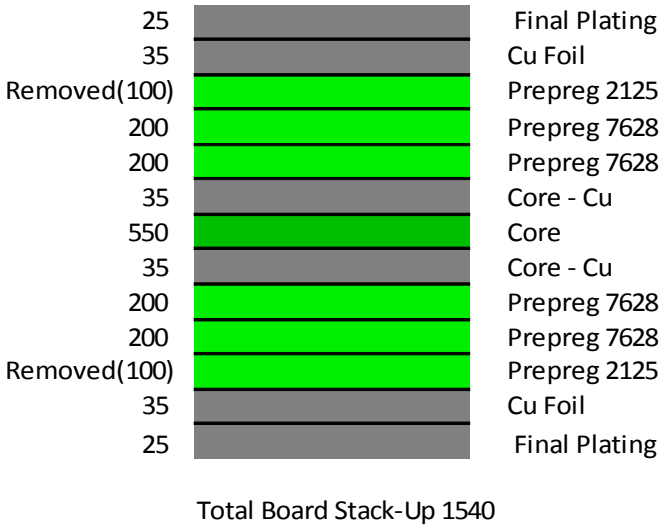


Figure 26: Board Stack-up Dimensions

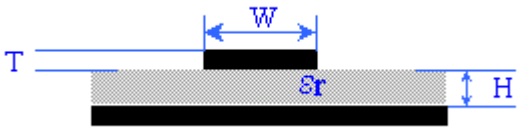


Figure 27: Microstrip Dimensions

For the trace impedance calculations we used:

$$Z_O = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \cdot \ln\left(\frac{5.98\mathrm{H}}{0.8\mathrm{W} + T}\right) \quad (16)[5]$$

where H, W and T are the dimensions as shown in Figure 27.

For microstrip lines we have calculated the characteristic impedance for several trace widths. See Table 2.

Zo(Ohm)	W(um)	T(um)	H(um)	Er	W(mils)
92.58	150	60	400	4.5	5.91
85.4	200	60	400	4.5	7.87
79.42	250	60	400	4.5	9.84
74.3	300	60	400	4.5	11.81
69.82	350	60	400	4.5	13.78
65.84	400	60	400	4.5	15.75
59	500	60	400	4.5	19.69
53.26	600	60	400	4.5	23.62
48.32	700	60	400	4.5	27.56
43.98	800	60	400	4.5	31.5
40.1	900	60	400	4.5	35.43
36.61	1000	60	400	4.5	39.37

Table 2: Characteristic Impedance

It is advised that the clock lines be routed with the smallest width possible so that the termination resistors in Figure 24, not be too small and cause excessive consumption. It was chosen for to set the width for 200um which is the minimum for EURICIRCUITS class 5.

USB Lines

For differential signals of USB lines, it is critical that a good impedance matching is obtained. If there are reflections on these lines, given the bit frequency of 480Mbps and the typical long cables that are used to connect to the PC, it will be disastrous.

The differential lines of USB as defined by the USB.ORG institution has to be 90Ohms.

The differential impedance for a microstrip is given by:

$$Z\,diff = 2 \cdot Zo \cdot (1 - 0.48\, e^{-0.96\mathrm{S}/H}) \quad (17)[5]$$

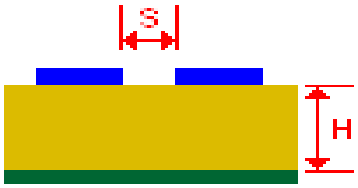


Figure 28: Differential Microstrip

being the Zo calculated as the single ended microstrip and S the separation between traces.

In Table 3 it is shown the differential impedance for several track widths (W) and separations (S).

Table 3: Differential Impedance

ZoDIFF(Ohm)	S(um)	Zo(Ohm)	W(um)	T(um)	H(um)	Er	W(mils)
120.07	200	85.4	200	60	400	4.5	7.87
104.46	200	74.3	300	60	400	4.5	11.81
92.57	200	65.84	400	60	400	4.5	15.75
90.43	300	59	500	60	400	4.5	19.69
91.44	400	56.02	550	60	400	4.5	21.65
91.12	500	53.26	600	60	400	4.5	23.62
89.88	600	50.71	650	60	400	4.5	25.59

As can be seen the further the traces are apart more loose is the coupling between the lines and the differential impedance becomes more dependent of the single ended impedance. In order to improve noise immunity of the differential pairs the separation between pairs should be minimum.

In order to keep the EUROCIRCUITS manufacturing in class 5, both W and S must be higher than 200um, which makes the option of having S=200um and W=400um the preferred one.

4. Board Control

All operation of the Board will be controlled by a PC by means of a USB or Ethernet interface. The test instructions are streamed into the controller, which will acknowledge their reception and execute them sequentially in a FIFO strategy.

The schematic page of the controller is on page 2 of Annex A. The micro controller used is the PIC18F8622 from MicroChip™. This controller features:

- Program Memory Type .....Flash
- Program Memory (KB) 64
- CPU Speed (MIPS) 10
- RAM Bytes 3,936
- Data EEPROM (bytes) 1024
- Digital Communication Peripherals .....2xA/E/USART + 2xMSSP(SPI/I2C)
- Capture/Compare/PWM Peripherals .....2 CCP, 3 ECCP
- Timers .....2 x 8-bit, 3 x 16-bit
- ADC .....16 ch, 10-bit
- Comparators 2
- Temperature Range (C) .....-40 to 85
- Operating Voltage Range (V) .....2 to 5.5
- Pin Count 80

The main task of this PIC is basically to stream into actions the commands that are coming from the PC and send back to the PC measurements that are made in the board.

The built-in USART interface of the PIC18F8622 will be used in tandem with USB to RS232 Transceiver. The USB-RS232 transceiver used is the FT323R from FTDI Technologies ™ , which provides serial port emulation drivers for all major OS platforms: Linux; Mac OS X (10.4 and later) ; Windows (2000 and later) and Windows CE (4.2 and later).

This approach will eliminate the need of developing a board driver, and for the first debugs, any available Hyper-Terminal application can be used.

The baudrate on the FT232R can be configured by software and is obtained by the division of a 3MHz clock. There are 8 sub-integer pre-scalers in the baudrate generator so the final frequency is given by

$$baudrate = \frac{3\text{MHz}}{divisor} \quad (18)$$

where $divisor$ can be n + 0, 0.125, 0.25, 0.375, 0.5, 0.625, 0.75, 0.875; and n is an integer between 2

and 16384 (214).

divisor = 1 and *divisor* = 0 are special cases. A *divisor* of 0 will give 3 MBaud, and a *divisor* of 1 will give 2 MBaud. In these two cases, sub-integer divisors are not allowed.

On the PIC18F8622 side, there is an automatic baudrate configuration mode. When this mode is enabled, it requires that the first byte received be a 55h (ASCII "U" character), so that the baudrate generator be automatically configured.

The baud generator is generated from the internal clock oscillator tuned at factory to 8MHz. The formula to baudrate is:

$$baudrate = \frac{8\text{MHz}}{p \cdot (n+1)} \quad (19)$$

where p = {16 or 4} and n is 16bit register or, alternatively p=64 and n is 8bit register.

Using the automatic baudrate configuration sequence, can set it safely to 57.6KBaud. If more throughput is needed, then it should be configured manually. Since there are several factors that affect the mismatch between the two baud-rate generators[12], the best 10 top matches between the PIC18F8622 and FT232R presented in Table 4. These configurations should be tried experimentally and checked for BER performance.

Table 4: Baudrate Configurations

Baudrate	FT232R	PIC18F8622
2MBaud	N=1	P=4, N=0
1MBaud	N=3.0	P=4, N=1
666.666KBaud	N=4.5	P=4, N=2
500KBaud	N=6.0	P=4, N=3; P=16 N=0
400KBaud	N=7.5	P=4, N=4
333.333KBaud	N=9.0	P=4, N=5
285.714KBaud	N=10.5	P=4, N=6
250KBaud	N=12.0	P=4, N=7; P=16 N=1
222.222KBaud	N=13.5	P=4, N=8
200KBaud	N=15.0	P=4, N=9

12 Accuracy of the oscillators, phase noise in the division, temperature frequency drift, pin and ground noise.

4.1. Communication protocol

The devised protocol for the communication between the PC and the board control is very simple. It is based on a ASCII encoding for commands being the arguments passed in DECIMAL-ASCII format. This allows in an early stage using an hyper terminal as controlling application.

The command format is fixed and follows the following sequence of ASCII characters

command	*space*	*id*	*space*	*Comma separated parameters in ascii format*

As a first step, the commands will have direct action on the the micro-controller pins, leaving up to the application to make all the sequence of operations needed to control the board.

Once all the routines are tested and debugged at application level, the more critical routines can be implemented in the micro-controller. This *modus operandi* will minimize the time spend debugging the board control routines given the fast development cycle of python.

Afterward, it will be easy to translate python instruction sequences to micro-controller C code, than to code and debug them directly on the micro-controller.

Table 5 presents the list of commands implemented in the micro-controller.

Table 5: Microcontroller commands

command	*id*	*parameters*	*description*
SET	LOAD_SEL	000-111	000 – No DUT IP is selected 001 – LDO is selected for load test 010 – DC/DC is selected for load test 100 – Charge Pump is selected for load test
SET	LOAD_EN	00-11	MSB – Enables/Disables Current Sink LSB – Enables/Disables Resistive Load
SET	MEAS_SEL	000-111	Selects the measuring channel
SET	SUPP_EN	00000-11111	Controls the Power Supply Enable, one bit per supply
SET	SW_PASS	0-1	1 – Bypasses the load current monitor point 0 – The load current monitor is used.
SET	DUT_CP_CLK	0-1	Enables the 555 oscillator for Charge Pump
SPI	CS	0-7, 99	0-7 Asserts the SPI_CS[n] 99 Deasserts all the SPI_CS[0:7] pins
SPI	ADDR	0-255	Configures the SPI address
SPI	W_WR	0-1	Initiates an SPI Read (0) or Write (1) sequence
SPI	W_VAL	0-255	Configures the SPI write value
SPI_RET			Ask for a the last SPI read value
RST			Initiates a soft reset to the micro-controller
WRITE	*address*	0-255	Writes to the micro-controller internal register
READ	*address*		Reads from micro-controller internal register

4.2. PC Application

In the application on the PC side, the opted solution will be to use Python language for the test scripts.

4.2.a) Why Python ?

Python is a pure Object-Oriented Language created in the early 90's by Guido van Rossum under an open source development. Since then it has gained acceptance from the community of programmers assuming today the place between the top 10 programming languages[13].

With Python a good level of abstraction is achieved, resulting in a more comprehensive and compact code. Typically 3 to 10 fewer lines then C/C++/Java. Since it is an interpreted language, the development cycle is faster. No need for compiling and linking, just save file and run.

Python installation comes already with an extensive library package that covers all the essential needs of a programmer, enabling him to concentrate on the task at hands.

13 Source http://www.tiobe.com/index.php/content/paperinfo/tpci/index.html

Also, 3rd party libraries can be found on internet that complement the built-in library package. The fact that libraries needed for test automation are readily available for use with Python together made it a very good option for this project. The 3rd party libraries found useful for this project are:

- pyVisa – Defines an object that represents a Instrument, and methods that establish all the communication protocol. This requires that a VISA software be installed in the PC in order for this library to work. The one used is NI-VISA from National Instruments
- D2xx – A python wrapper for the D2XX.DLL library to access the FTDI USB Controllers.
- pyParallel and pySerial – Libraries to access PC I/O port addresses, namely for the Parallel port and serial port addresses. It depends on a Application called GIVEIO.EXE.
- NumPy – Mathematical library that implements all major algebraic and mathematical functions, making python as an alternative to MatLAB for vector and matrix processing.
- MySQL – Python Interface to a MySQL database
- SQLAlchemy – Class Foundation Library that implements a object oriented interface to SQL structures.
- wxPython – Python wrapper for the WXWidgets, an open source and multi-platform GUI foundation class.

4.2.b) DUT Interface

To take advantage of the object oriented capabilities of Python, a structure of objects was created to map the entities that are involved in communication.

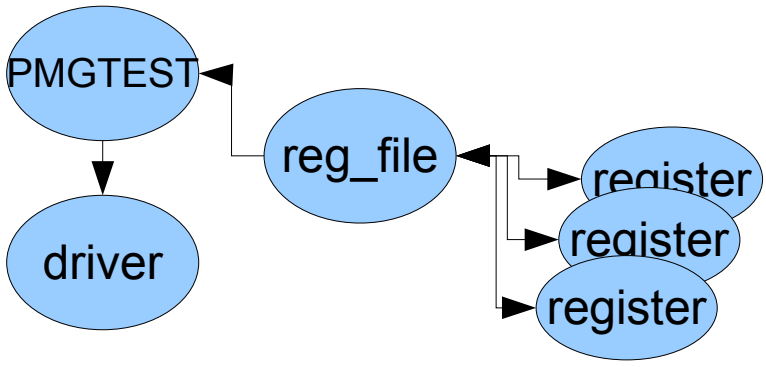


Figure 29: DUT Interface Classe Relation

The arrows in the diagram shows the reference pointers between objects. This class structure allows for each object to have self contained methods.

For example, by invoking the register method write(data), the operation write will be done transparently to the user without having to worry about address and data bit locations, communication channels or protocols. All of this is resolved by calls to the respective methods of each object pointers.

Follows a very high-level description of class attributes and methods. Not all methods are described below, class constructors and destructors, auxiliary functions and attributes as well as others that are python implementation specific are not described here.

OBJECT : driver

Responsible for the serial or parallel communications. Derived from available class at D2XX or pyParallel.

METHODS:

- *write(command)* – sends *command* to the *port*
- *read*() - return: the data available at the *port*

ATTRIBUTES:

- *port* – pointer to communication port (COM or LPT)

OBJECT : PMGTEST

Responsible for the communications with the board and to the DUT register map.

METHODS:

- *write(command)* – sends *command* to the *driver*
- *read*() - return: the data available at the *driver*
- *writereg(address, data)* – writes into DUT register at *address* the contents of *data*.
- *readreg(address)* – returns: data contained in DUT *address*.

ATTRIBUTES:

- *driver* – pointer to driver class instantiation

OBJECT : registerfile

This class library manages the access to the DUT register map. The resister information is read from a CSV file, so that the creation of register objects is automated. Registers pointers are stored in this class and indexed by their names.

METHODS:

- *writereg(address, data)* – writes into register at *address* the contents of *data*.
- *readreg(address)* – returns: data contained in *address*.
- read_csv(filename) – reads a CSV file containing the register map information and

creates a register instantiation per register found in the file.

- *load_contents*(filename) – reads from a file preset values for DUT registers and writes them to the DUT.
- *save_contents*(filename) – writes to a file the current values of the DUT.

ATTRIBUTES:

- *driver* – pointer to PMGTEST class instantiation
- *reg_dict* – dictionary of pointers to register class instantiations. A dictionary is a built-in structure of python that indexes object references. In this implementation, the indexation is made by register names.
- *reg_shadow* – shadow of the register map in the PC. It acts as a cache in read-op-write sequences.
- *shaddow_read* – boolean variable that sets the usage of the shadow register.

OBJECT : register

This class library manages the access to DUT register.

METHODS:

- *write(value)* – writes into register the argument *value*.
- *read()* – returns: data contained in the register.

ATTRIBUTES:

- *driver* – pointer to resisterfile class instantiation
- *address* – is an integer representing the address in the board
- *mask* – is an integer in which the binary encoding represent the active bits.
- *lsb* – this is used for registers that occupy more than one address location. It should contain the LSB (Least Significant Bit) in a given address.

4.2.c) Instrument Drivers

The pyVisa library already defines a class called Instruments with the following methods and attributes:

OBJECT : Instrument

This class manages communication with a VISA resource.

METHODS:

- *write(command)* – sends a command to the VISA resource pointed by *resource_address*
- *read()* – returns: answer from VISA resource pointed by *resource_address.*

ATTRIBUTES:

- *resource_address* – VISA address of the instrument.
- *timeout* – timeout to be used in read and write operations.

For each equipment used, was created a class derived from the above class and that defines the functions needed from the instrument. In Table 6 is the list of drivers implemented.

Table 6: Test Equipment Drivers

Equipment	Model Used	driver
Source Meter	Keithley KT2420	drvKT2420.py
Oscilloscope	Tektronix TDS3054	drvTekScope3000.py
Spectrum Analyzer	Rohde & Schwarz FSEA30	drvFSEA30.py
Multimeter	Keithley KT2700	drvKT2700.py

As an example there it is shown here the source meter Instrument class.

OBJECT : sourcemeter

This class manages communication with a Keithley 2420 sourcemeter

METHODS:

- *set_comp(value)* – sets the compliance to *value.*
  Writes to Instrument (":SENS:CURR:RANG "+str(value)+
  ";SENS:CURR:PROT "+str(value) + ";")
- *set_value(value)* – sets the output to *value*
  Writes to Instrument(":SOUR:VOLT:RANG 10;:SOUR:VOLT:LEV " + str(value) + ";")
- *setup(source, sense)* – sets the source and sense mode of the source meter, being

source and *sense* = {“VOLT”;”CURR”}

Writes to the Instrument(":SENS:FUNC "+ *sense* +"; :SOUR:FUNC "+ *source* +";")

- *get_measures( )* – reads the instrument the sensing voltage and/or current

  Writes to the Instrument(":READ?") and reads from the Instrument

- *output(state)* – Enables and Disables the output of the source meter

ATTRIBUTES:

- *comp_value* – output compliance value
- *output_value* – output value
- *sense_s* – sense mode: (Voltage or Current)
- *source_s* – source mode: (Voltage or Current)

4.2.d) Test Automation

Once the DUT interface and Instrument drivers were development, the test scripts were written. As an example, here is a test script developed for the characterization of the DC/DC.

```
from PMGDUT import *    # import class library PMGDUT
import time             # importing a time library
from myutils import sweep           # auxiliary function from

import sourcemeter      # importing the sourcemeter class driver
import drvE3631A        # importing a power supply class driver

      ## Instantiating two source meter
sm1 = sourcemeter.Keithley2420("GPIB0::21::INSTR")
sm2 = sourcemeter.Keithley2420("GPIB0::24::INSTR")

## Configuring the source meters for voltage source
sm1.setup(sense="CURR", source="VOLT")
sm2.setup(sense="CURR", source="VOLT")

      ## Setting Vin and compliance
sm1.set_value(3.3)
sm1.set_comp(0.5)

      ## Setting the Load conditions to 10mA
sm2.set_value(0)
sm2.set_comp(0.01)

      ## Enabling the two source meters
sm1.output(1)
sm2.output(1)
time.sleep(0.5)   # Wait for 500ms

pmu = PMGTEST()   # Instatiating the Power Management Class
regfile = RegisterFile() # Instantiating the RegisterFile Class
regfile.load_csv("DUTREGS.csv") # Loading the register map information
regfile.shaddow_read=True     # enable the shadow memory feature
```

```
pmu.add_RegFile(regfile)      # Link the registers to the PMGDUT object
pmu.board_reset()             # Resets the board

pmu.regs.bgenable=1           # This block writes to registers
pmu.regs.cpenable=0
pmu.regs.ldoenable=0

pmu.regs.dcdcvprog=4          # Config for Vout=0.8V
pmu.regs.inttrim=0x1B
pmu.regs.vlxrevdet=1
pmu.regs.pwrdwn=0
pmu.regs.deftrim=0

#pmu.regs.testdig=1

#pmu.PORIN(1)

fout = file("DCDC4_EffSweep.csv",'w')     # opens file for data output
fout.write("vin_set, vprog, iout, vin_meas,vin_curr, vout_meas, vout_curr,
                                  deftrim\n")       # write header
try:
            ## Sweeps from 5.1 down to 2.0 with 0.4 steps
    for vin in sweep(5.1,2.0,0.4):
        sm1.set_value(vin)                # sets sourcemeter output value
        for vprog in (0,8,16,24,31):      # iterates this series
            pmu.regs.dcdcvprog=vprog      # programs the dcdcvprog register
            for deftrim in range(4):      # iterates from 0 to 3
                pmu.regs.deftrim=deftrim
                iout_list = [ x for x in sweep_log(1e-3, 200e-3, 2)]
                #iout_list = (10e-3, 50e-3)
                for iout in iout_list:
                    sm2.set_comp(iout)
                    time.sleep(0.2)
                    meas1=",".join([str(x) for x in sm1.get_measures()])
                    meas2 = ",".join([str(x) for x in sm2.get_measures()])
                    fout.write(str(vin)+','+ str(vprog) +
                                        ','+ str(iout) +','+ meas1 +
                                        ','+ meas2 + ',' + str(deftrim) +
'\n')
                sm2.set_comp(0.02)
                time.sleep(0.2)
        time.sleep(0.2)

finally:
    fout.close()
```

4.2.e) Storing Test Data

As was stated before in the motivation chapter, the characterization of Power Management components produce a lot of data that has to be manipulated. The most commonly used office tools cannot be used for this purpose since they cannot handle more than 65535 rows of data. Dividing data into chunks is simply not practical and will be an obstacle when retrieving information from several sources.

The adopted approach will be to use databases for the storage and statistical analysis of information. Open solutions like MySQL provide a good and reliable way to store this data and there are already tools readily available.

5. Test Environment

In an earlier chapter was a brief discussion of the measurements that characterize a Power Management IP. In this chapter it will be explained the methodology of test for each measurement.

5.1. Static Measurements

It is defined as static measurements the ones that have no dependency with time, e.g. once the conditions are set, and given a settling time, the voltages and tensions at input and output nodes of the DUT will not change through time. Surely from this are excluded long term factors such as noise and ageing factors.

As was mentioned earlier, static measurements can be done by the test platform without the need of external instrumentation, *i.e.* once the supplies, loads and measurement channels are duly calibrated.

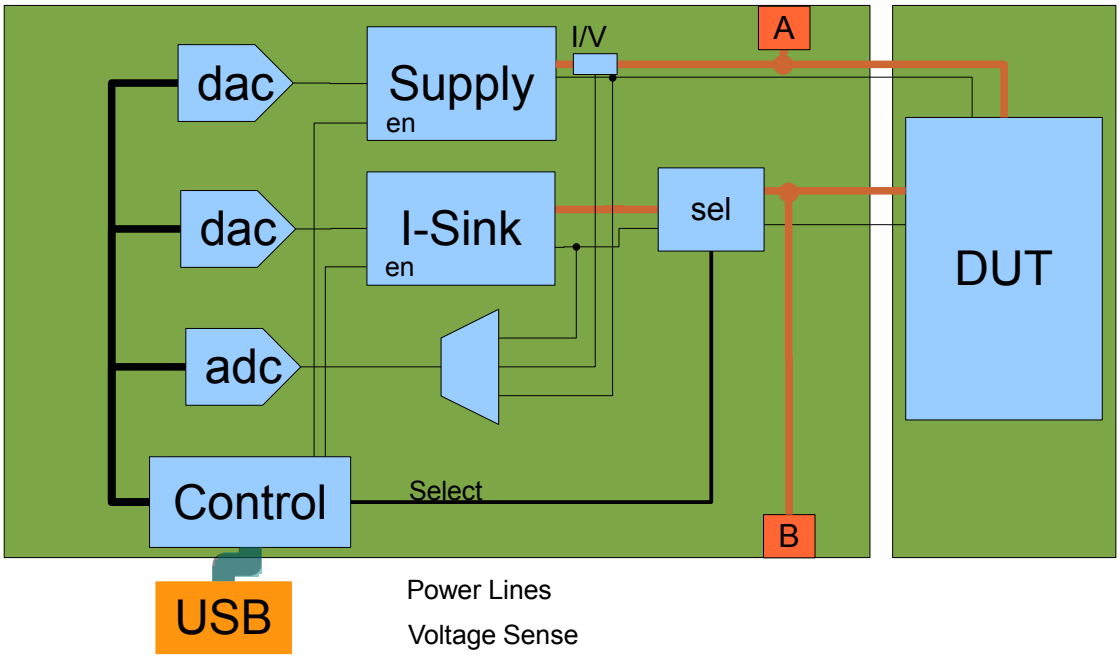


Figure 30: Dynamic Tests (Conceptual View)

In Figure 30 is presented a conceptual view of using the Test platform in Static Measurement

Connectors A and B will serve for calibration purposes and for characterization of the DUT itself in case case is needed.

5.2. Dynamic Measurements

Transient tests are defined as the ones that evaluate a system time response of a given stimuli. From the list of tests enumerated in 1.2. (Objectives), the dynamic tests are: Load Transient, Line Transient, Start-up and Enable/Disable Time.

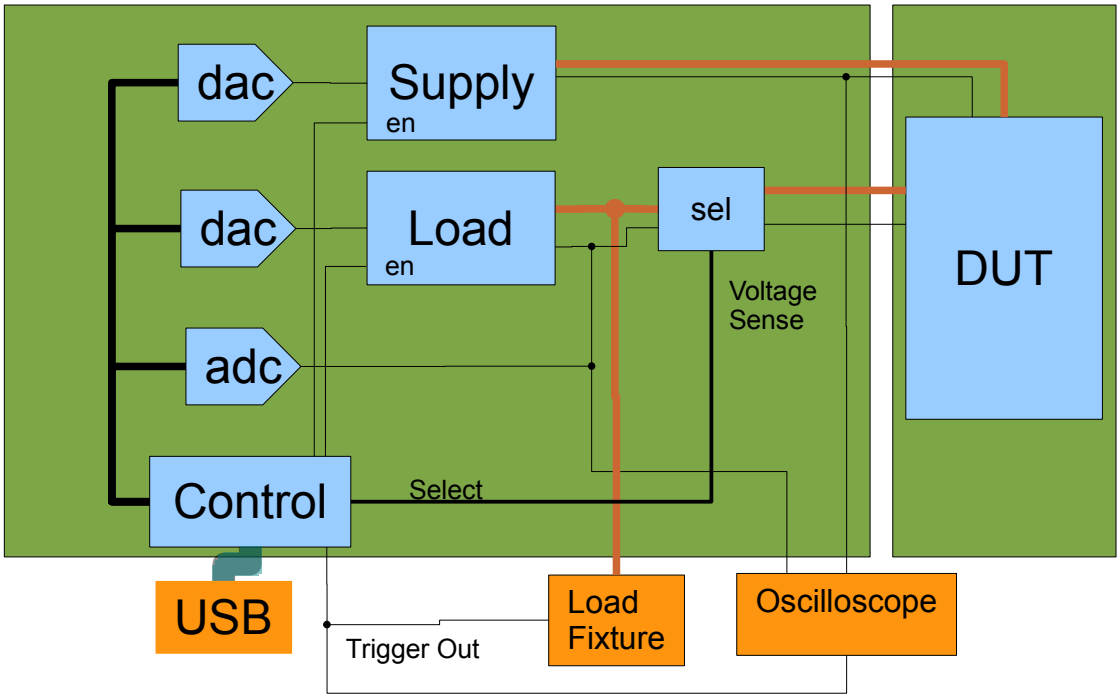


Figure 31: Dynamic Tests (Conceptual View)

In Figure 31.the generic configuration for Dynamic tests is presented

Since the response over time of a given stimuli is wanted, an oscilloscope is needed to perform this test. A triggering system is needed to activate the time base of the oscilloscope. For that purpose, a trigger output will be used.

This trigger has the advantage over the traditional solution of using the built-in oscilloscope triggering system because sometimes, the trigger can be a very complex signal such as a I2C transaction or an SPI command. Using the real-time controller to generate the trigger surpasses this problem.

It is recommended that the Oscilloscope for such measurement is a Digital-Phosphor Oscilloscope (DPO) with at least 500MHz bandwidth. A current probe is highly recommended, specially while debugging DC/DC Converters.

5.3. Frequency Domain Measurements

These tests are the ones that evaluate the system performance on frequency domain. Basically there are two tests in this category: Output Noise and Power Supply Rejection Ratio.

5.3.a) Output Noise

This test requires an equipment with a good spectrum analyzing module. It can either be a Spectrum Analyzer; a Network Analyzer or an Audio Precision. Key requirements is that it has a noise floor below -100dBm.

The configuration for this test is a very simple one, basically just connect the Spectrum Analyzer to the output of the IP using a series decoupling capacitor. The capacitor value must be high enough in such that the high pass filter resulting from the series capacitor and the input impedance of the Analyzer (50Ohm or 75Ohm), has a low cut-in frequency.

$$F_{cutin} = \frac{1}{2 \cdot \pi \cdot R \cdot C} \quad (20)$$

With a value of 220uF, given a 50Ohm input impedance, results in a cut in frequency of ~14.46Hz. Please note that this capacitance, if made with a single capacitor, it is necessarily a polarized one, and thus special attention should be taken for it to be placed in the correct polarity.

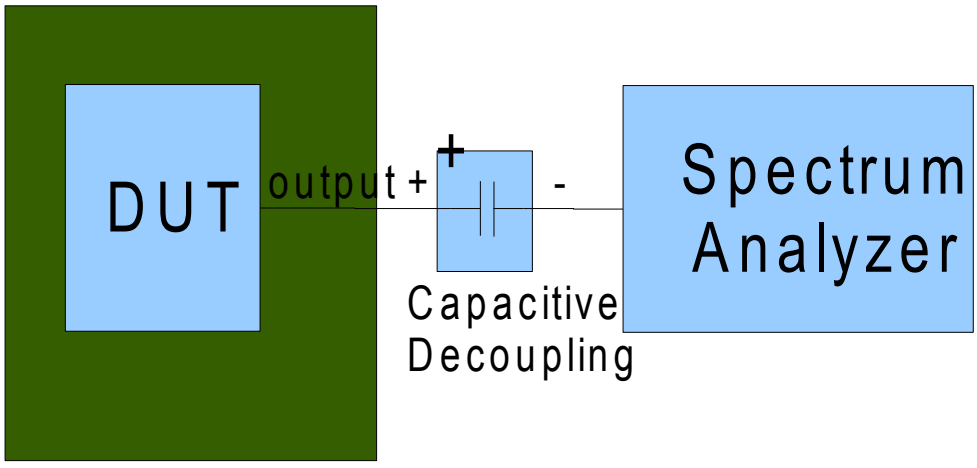


Figure 32: Output Noise Test Setup

The plus terminal should be in the higher potential, like is depicted in Figure 32.

5.3.b) PSRR

Measuring of PSRR is one of the most difficult tasks to do in an LDO characterization. It implies superimposing an AC component top of the DC supply. As seen in [6], this can be done either by capacitive coupling, or a magnetic coupling, or by a combining AC + DC by means of a power driver.

Magnetic coupling has losses at low frequency, and the capacitive at high frequencies, so the option that seems more appropriate is the last one, similar to the one used in [7].

Figure 33. illustrates the usage of the Test platform for PSRR testing.

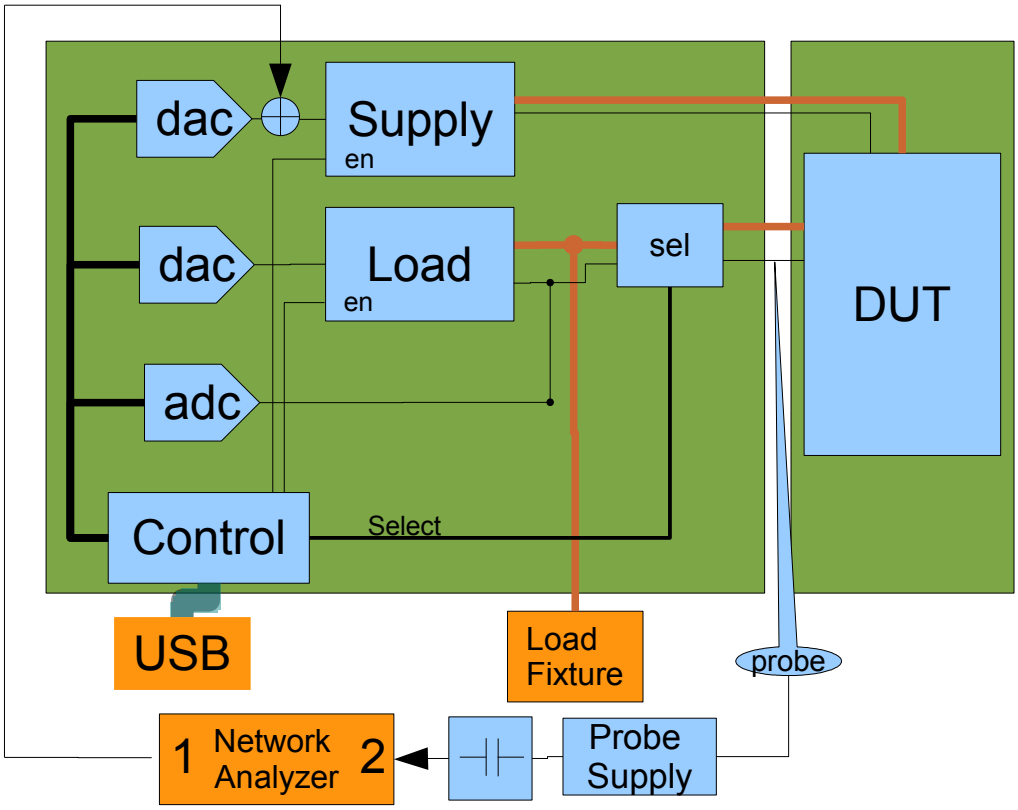


Figure 33: PSRR Test Setup

The AC source to be used will be supplied by Port 1 of Network Analyzer and the port 2 will be connected to the output of the LDO, passing through a DC blocker circuit and an active oscilloscope probe with a probe supply module. The frequency band in where the PSRR can be measured is mostly limited by Power Supply bandwidth.

The PSRR test must be done ratio-metrically. Since the frequency response of the Power Supply is not ideal, a first test must be done probing the DUT voltage input, and a second run probing the supply output. The PSRR measurement is the ratio between the first and the second measurement. If a Network analyzer is not available, the tests can also be done with a Spectrum Analyzer and a function generator for the stimuli generation.

5.4. Equipment Needs

In this table are described all instruments that will be needed not only for the Power Management Characterization phase but also for the Platform development.

Table 7: Equipment Needs

Instruments	Description
Power Supply	The platform will be supplied with a DC Voltage. Power Budget is not yet finished, but, a +/-15V DC Supply with 3A gives already enough margin.
Oscilloscope	It is essential piece of equipment, for the debug and characterization. The minimum requirements for this oscilloscope is to have at least 200MHz bandwidth (ideally 500MHz or higher) and be a digital phosphor oscilloscope. For debugging the very fast transients existing in switched converters are only visible with a high bandwidth oscilloscope.
Current Probe	A 20MHz or more current probe with good resolution and withstanding up to 3A currents.
GPIB Controller	IEEE 488.2 GPIB-Bus Controller. This is needed to automate the data acquisition of laboratory equipment.
Network Analyzer or Spectrum Analyzer or Audio Precision SYS-II	Needed for the Frequency Domain Measurements, as described in section 4.3.Frequency Domain Measurements.
Temperature Machine	For the full characterization of the DUT
PC	For controlling the test environment and developing the platform.
Probe Supply	For PSRR tests

6. Test Report

6.1. Fast prototyping Board

Since the Power Management Test Platform was not ready when the testchip arrived, due to urgency on getting test results, a small test board with no supplies, no loads and only with the essential to control the testchip was made.

The schematic for this small board is on Annex B. In the schematic is included the testchip, the needed decoupling and charge pump capacitors and the coil for the DC/DC operation. The power is supplied externally by means of connectors.

The control is made through a parallel port, and the digital clock is supplied by an 555 oscillator circuit.

This board will allow to test all the basic functions of the testchip, however there are a few limitation that need to be taken into account.

- Due to the reduced number of available power supplies, it was opted that all IP supplies (DC/DC; Charge Pump and LDO) share the same power supply. This will limit the possibility of making power down consumptions and will affect the DC/DC Efficiency measurements.
- It will require to have external measurement capabilities, which in the case of the Charge Pump and DC/DC will mean that two source meters will be needed.
- The prototyping board was designed to be handcrafted using available resources, so, it was made from a one sided copper coated prototyping board. This does not offer the ideal solid ground attachment and ideal decoupling placement for the characterization of Power Management IP. Specially the DC/DC efficiency and LDO PSRR may be affected by board limitations.

In Annex B the board Layout can be found.

6.2. Band-Gap

Specifications

Values obtained from corners analysis: V_{IN}= {3.1V ; 5.1V}, I_{LOAD}= {1µA ; 10µA}, T_A= {-40°C ; +125°C},
MOS = {cmoswp ; cmosws ; cmoswo ; cmoswz} and Res ={reswp ; resws}.
Typical conditions: V_{IN}= 3.3V, I_{LOAD}= 1µA, T_A=25°C and bgtrim<2:0> = "000", unless otherwise specified.

Table 8: Band-Gap Specifications

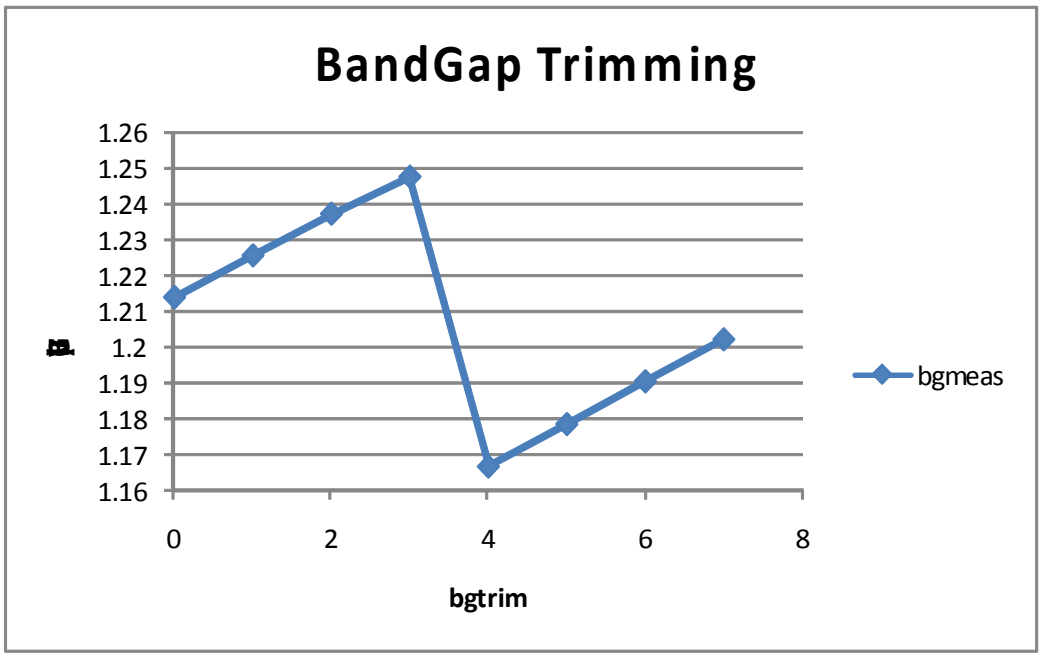
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VBG	Output Voltage		1189	1216	1252	V
TC_{VBG}	Temperature Coefficient	-40°C ≤TA≤ +125°C		32		ppm/°C
$\Delta_{VBG}/\Delta_{VIN}$	Line Regulation	3.1V ≤ VIN≤ 5.1V	0.46	0.56	654.00	µV
$\Delta_{VBG}/\Delta_{ILOAD}$	Load Regulation	1µA ≤ I_{LOAD}≤ 10µA	44.82	56.72	574.67	µV
V_{NOISE}	Output Voltage Noise	10Hz ≤ f ≤ 100kHz	104.8	131.6	159.7	µVrms
$PSRR_{1kHz}$	Power Supply Rejection Ratio	f = 1kHz, CLOAD= 0pF	-113.3	-110.6	-57.6	dB
$PSRR_{100Hz}$	Power Supply Rejection Ratio	f = 100kHz, CLOAD= 0pF	-71.7	-69.2	-55.5	dB
$PSRR_{1MHz}$	Power Supply Rejection Ratio	f = 1MHz, CLOAD= 0pF	-65.4	-62.5	-47.4	dB
ts	Start-Up Time	CLOAD= 0pF	7	14	22	µs
ten	Enable Time	CLOAD= 0pF	8	17	22	µs
IL_{MAX}	Maximum Load Current				15	µA
IQ	Quiescent Current	bgivref grounded	10.7	16.8	30.2	µA
IPD	Power-Down Current	bgivref grounded	0.26	0.27	146.50	nA

Test Measurements

Table 9: BandGap Test Summary

SYMBOL	TEST	COMMENTS	MIN	TYP	MAX	UNIT
VBG	T01	Bgtrim=0 Bgtrim=1 Bgtrim=2 Bgtrim=3 Bgtrim=4 Bgtrim=5 Bgtrim=6 Bgtrim=7		1.213814 1.225453 1.237068 1.247404 1.166607 1.178437 1.190346 1.202069		V
TC_{VBG}	T03	To be Done	-	-	-	ppm/°C
$\Delta_{VBG}/\Delta_{VIN}$	T04	3.1V ≤ VIN≤ 5.1V bgtrim = 0			98	µV/V
$\Delta_{VBG}/\Delta_{ILOAD}$	T05	To be Done	-	-	-	µV/µA
V_{NOISE}	T08	To be Done	-	-	-	µVrms
PSRR	T9	To be Done	-	-	-	dB
ts	T10	To be Done	-	-	-	µs
ten	T11	To be Done	-	-	-	µs
ILMAX	T13	To be Done	-	-	-	µA
IQ	T14	To be Done	-	-	-	µA
IPD	T14	To be Done	-	-	-	nA

T01 – Bandgap trimming



6.3. LDO

6.3.a) Specifications

Values obtained from corners analysis:

VIN = {3.1V ; 5.1V}, I_{LOAD} = {0mA ; 50mA}, TJ = {-40°C ; +125°C},

MOS = {cmoswp ; cmosws ; cmoswo ; cmoswz} and Res ={reswp ; resws}.

Typical conditions: VIN = 3.3V, I_{LOAD} = 50mA, TA=25°C, VEN=VIN, COUT=4.7µF and the reference voltage is given externally, unless otherwise specified.

Table 10: LDO Specifications

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIN	Input voltage range		3.1	3.3	5.1	V
VREF	Bandgap reference voltage		-	1.22	-	V
VOUT	Output voltage		2.32	2.37	2.44	V
	Output voltage accuracy(1)	TJ=25°C, nominal	-2.2	-	2.2	%
		0µA ≤ I_{LOAD} ≤ 50mA, 3.1V ≤ VIN ≤ 5.1V, –40°C ≤ TJ ≤ 125°C	-2.4	±2.2	2.6	%
VDO	Dropout voltage VIN=VOUT – 100mV	I_{LOAD} = 50mA	55	84	123	mV
TC	Temperature coefficient of the output voltage	I_{LOAD} = 50mA	-	0.7	2.2	ppm/°C
I_{LOAD}	Output current		0	-	50	mA
ICL	Output current limit		-	184	340	mA
IQ	Ground pin current	I_{LOAD} = 50mA	36.6	54	89.3	µA
IPD	Power-down current		-	0.45	3530	nA
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation (2)	3.1V ≤ VIN ≤ 5.1V	0.09	0.11	0.13	%
$\Delta V_{OUT}/\Delta I_{LOAD}$	Load regulation (2)	0µA ≤ I_{LOAD} ≤ 50mA	0.71	1.01	1.41	%
V_{NOISE}	Output noise voltage	10Hz ≤ f ≤ 100kHz	18.3	21.1	24.2	µVrms
PSRR	Power supply rejection ratio I_{LOAD} = 50mA	f = 100Hz	88	119.3	121.7	dB
		f = 1kHz	88	118.4	119.1	dB
		f = 100kHz	80.6	87.5	95.3	dB
		f = 1MHz	58.5	70.2	79.4	dB
ts	Start-up time VOUT=0~90%	I_{LOAD} = 50mA	55.9	70.7	81.7	µs

6.3.b) Test Results

Table 11: LDO Test Summary

SYMBOL	TEST	COMMENTS	MIN	TYP	MAX	UNITS
ts	T01				100	us
$\Delta V_{OUT}/\Delta V_{IN}$-T $\Delta V_{OUT}/\Delta V_{IN}$-P	T02	Iout = 50mA Vin = 3.1V → 5.1 (tran < 1us)			5 2	ms V
		Iout = 50mA Vin = 5.1V → 3.1 (tran < 1us)			0 0	ms V
$\Delta V_{OUT}/\Delta_{ILOAD}$-T $\Delta V_{OUT}/\Delta_{ILOAD}$-P	T03	Vin = 5V Iout = 50mA → 1mA (tran < 1us)			30 30	us mV
		Vin = 5V Iout = 50mA → 1mA (tran < 1us)			20 30	us mV
V_{OUT}	T04	Accuracy	2.34	2.36	2.37	V
$\Delta V_{OUT}/V_{IN}$	T05	Line Regulation	-0.61	-	0.4	%
$\Delta V_{OUT}/I_{LOAD}$	T06	Load Regulation	-1.38	-	0.30	%
IQ	T07	Not possible with current setup	-	-	-	mA
IPD	T08	Not possible with current setup	-	-	-	nA
ICL	T09	Not possible with current setup	-	-	-	mA
TC	T10	To be Done	-	-	-	ppm/°C
PSRR	T11	Vin = {3.1V, 5.1V} ; Freq < 100kHz ; VAC={0.1V; 0.2V; 0.4V)	55.7		115.5	dB
V_{NOISE}	T12	Integrated from 10Hz ≤ f ≤ 100kHz			Note1	µVrms
VDO	T13	I_{LOAD} = {1mA; 10mA, 50mA}	167.1	-	259.1	mV
IMAX	T14	Maximum Current				

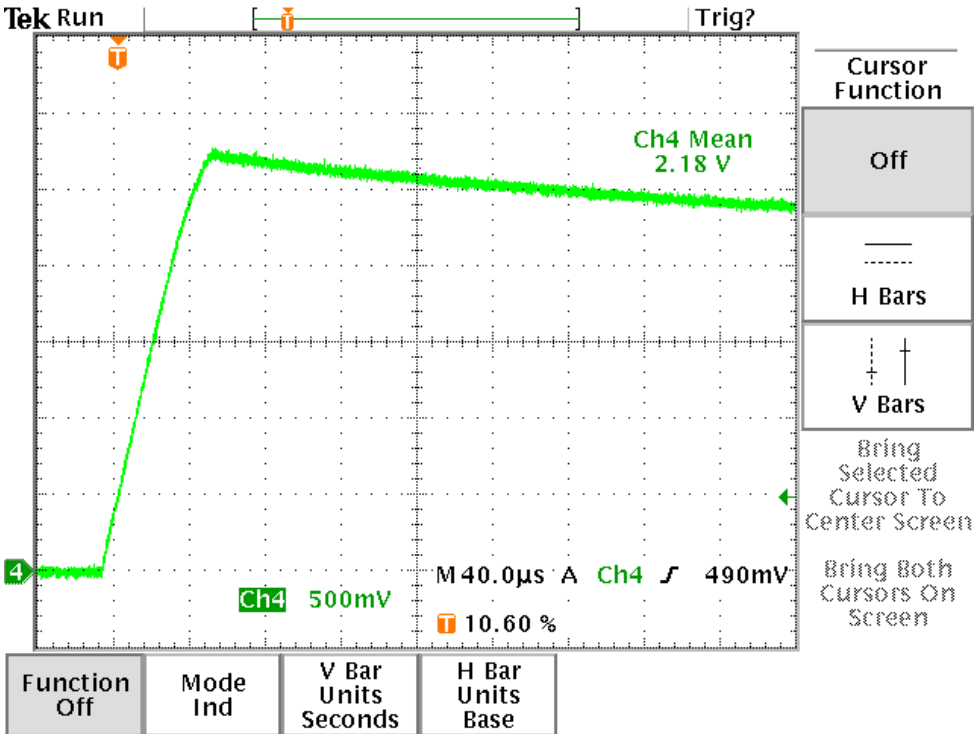
Comments:

T02 fails because the supply is faster than the LDO. Cannot modulate rising time in the available equipment. This test should be repeated using a function generator to control the Vin rise/fall time.

Note1 – The Output noise was measured with a Spectrum analyzer and it has a high spectral power in the 10Hz to 10KHz band. In order to have a better measurement an audio analyzer such as an Audio Precision should be used. Excluding the referred band the LDO has a noise level below 15uVrms

T01 – LDO Start-up

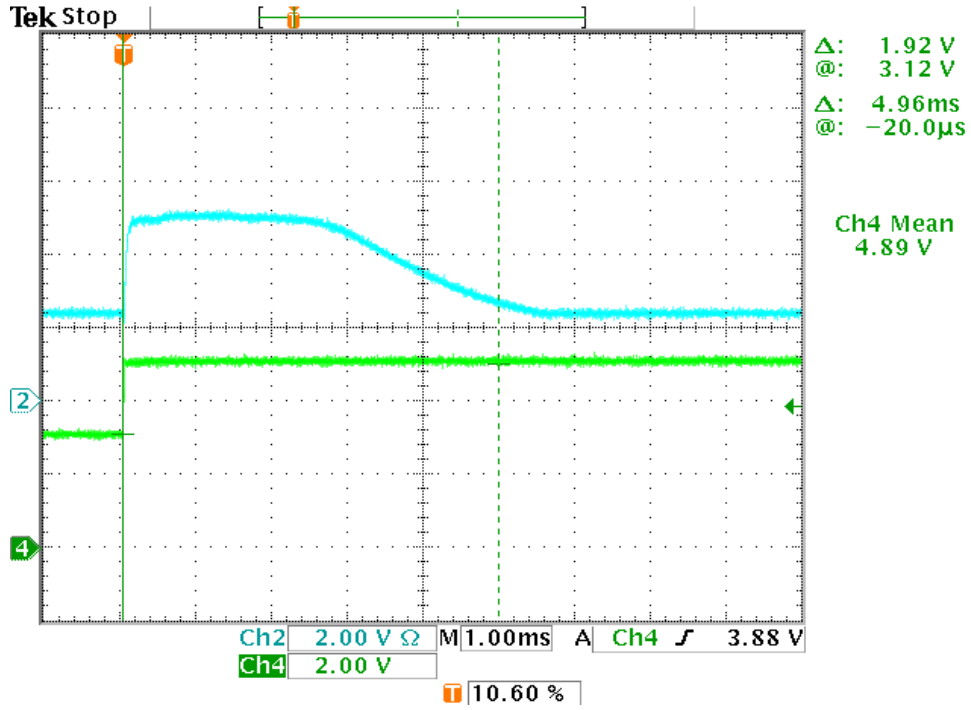
Conditions: Vin= 3.3V ; Enable LDO



CH4: LDO Output

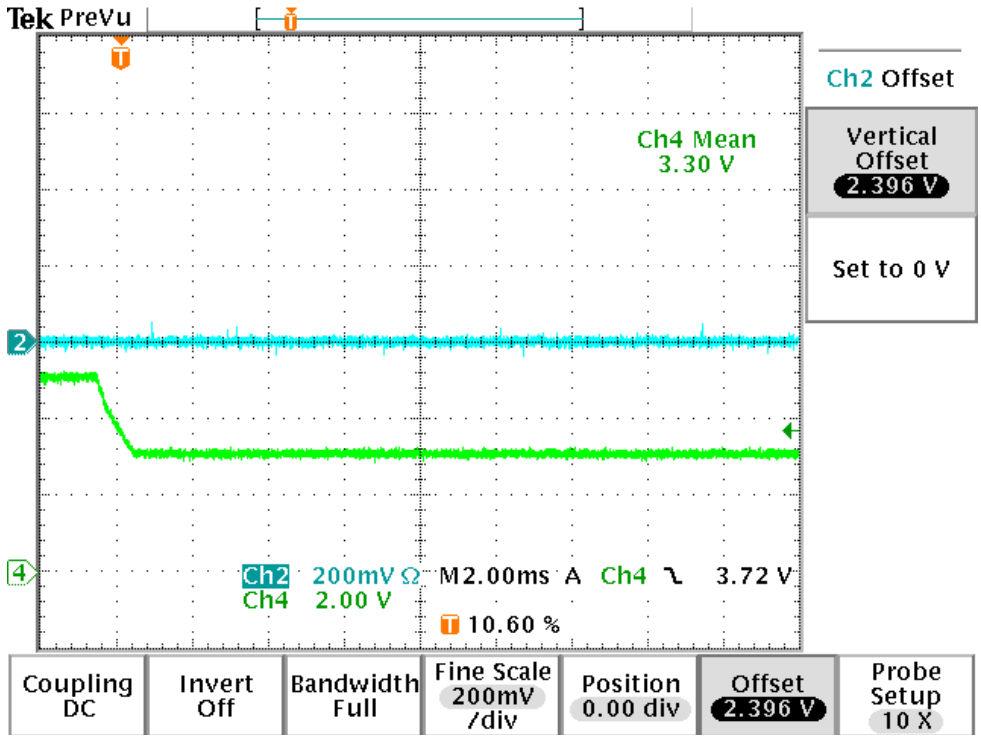
T02 – Line Transients

Condition: Vin from 3.1V to 5.1V



CH2: Vin ; CH4: LDO Output (V_{OUT})

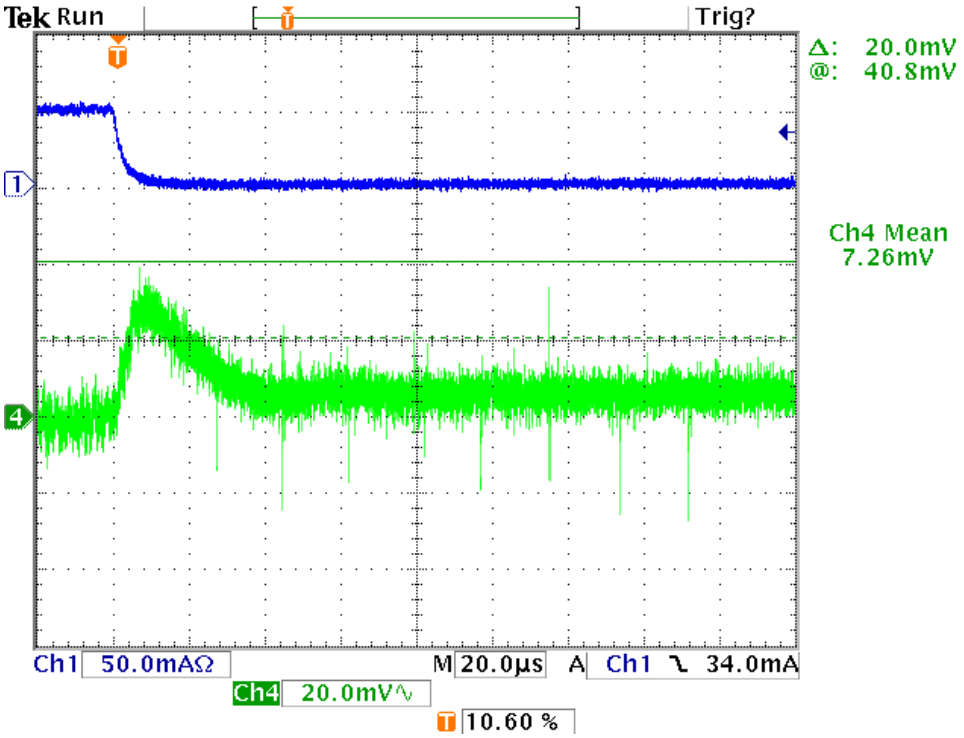
Condition: Vin from 5.1V to 3.1V



CH2: Vin ; CH4: LDO Output (V_{OUT})

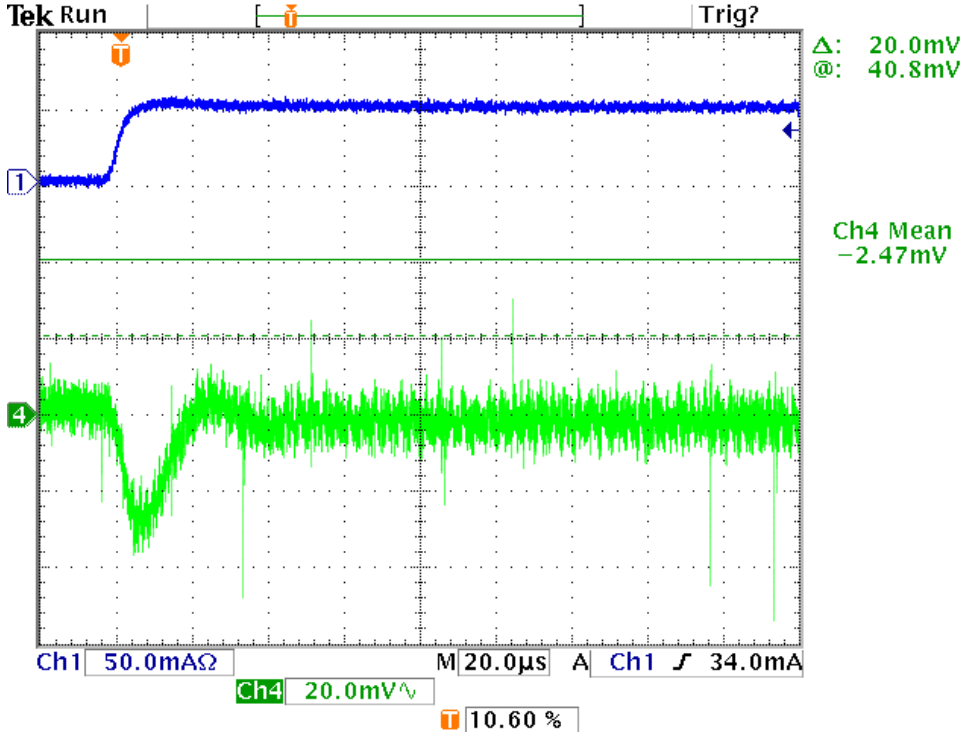
T03 – Load Transients

Conditions: IOUT from 50mA to 1mA



CH1: Output Current ; CH4: LDO Output (Vout)

Conditions: Load transient from 50mA to 0mA

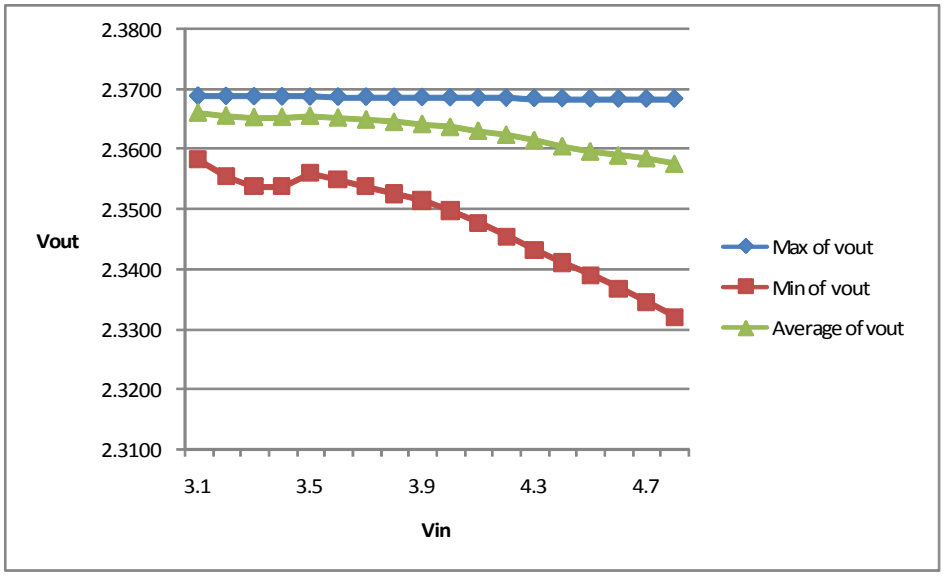


CH1: Output Current ; CH4: LDO Output (Vout)

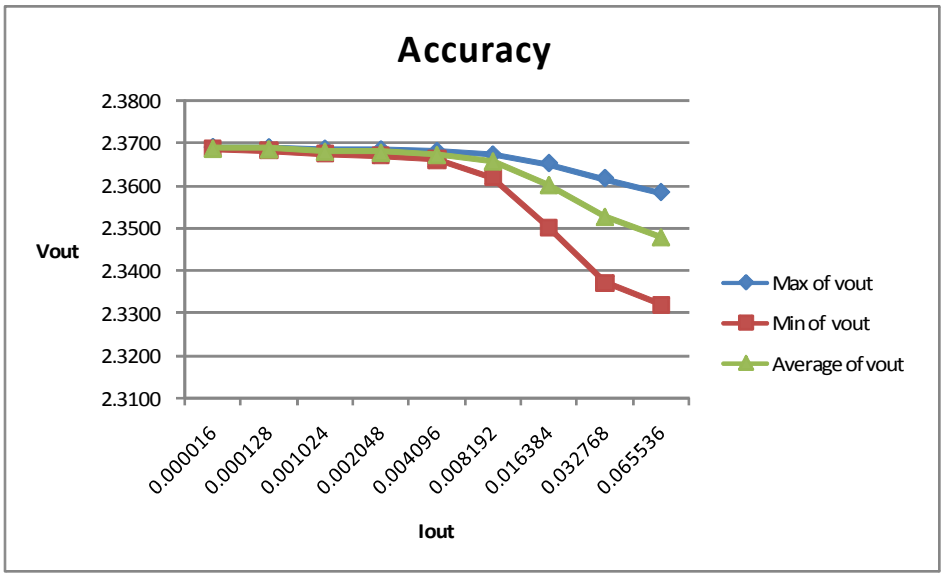
T04 – Accuracy

Conditions: Vin = [3.1V : 4.9V] ; Iout = {1mA; 2mA, 4mA; 8mA; 16mA; 32mA; 64mA; 128mA}

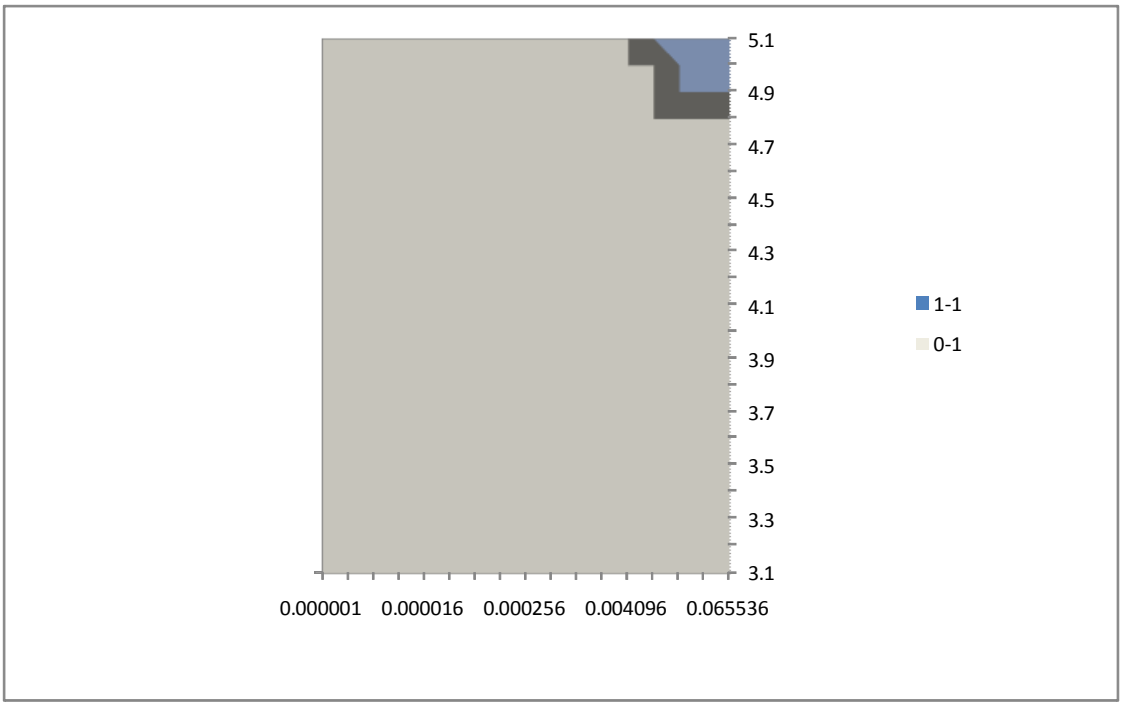
NOTE : Some points were removed from the plot specially with VIN in [4.5 V: 5.1V] and Iout =[32mA : 128mA]. See Area in plot # 3. In these points the testchip failed due to overheating. Package for this testchip has insufficient thermal dissipation, specially in socketed environment. Corners over temperature could reveal more about this problem.



Output Voltage Dependency on Output Current

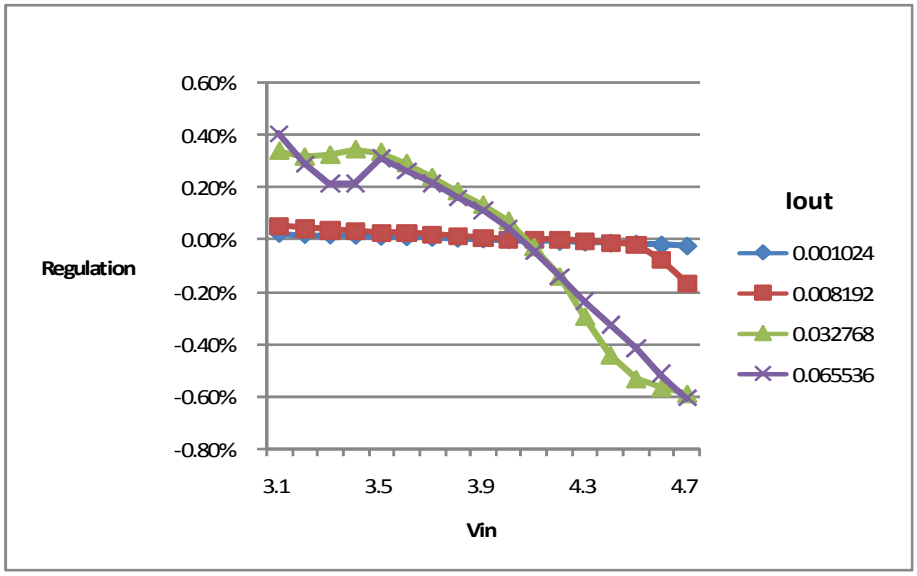


Plot #3 Discarded Data due to overheating of the Testchip



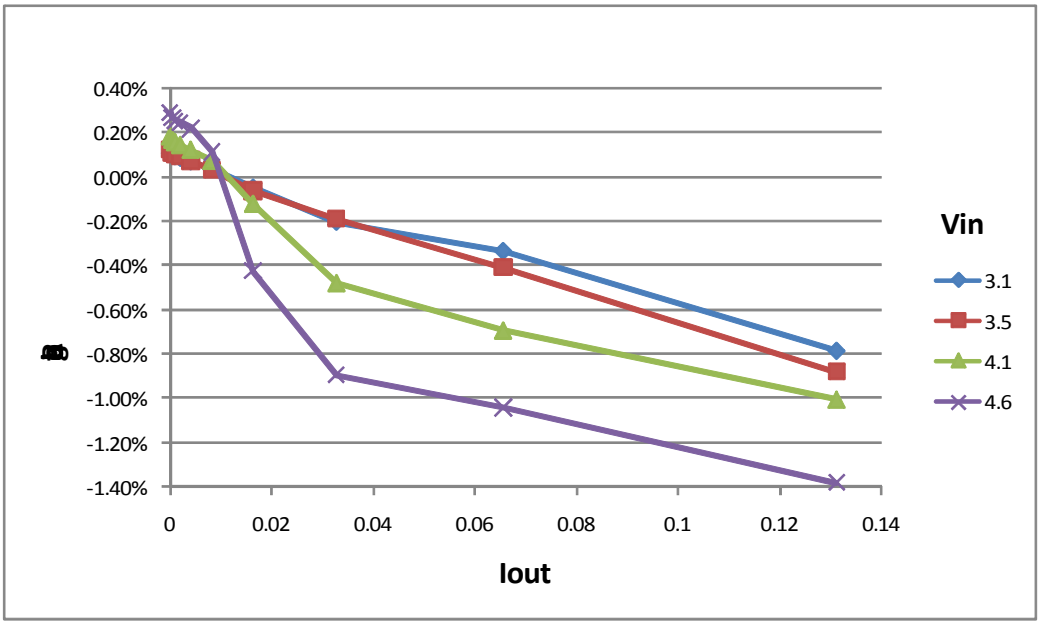
T05 – Line Regulation

Regulation of LDO across Input Values for several output currents

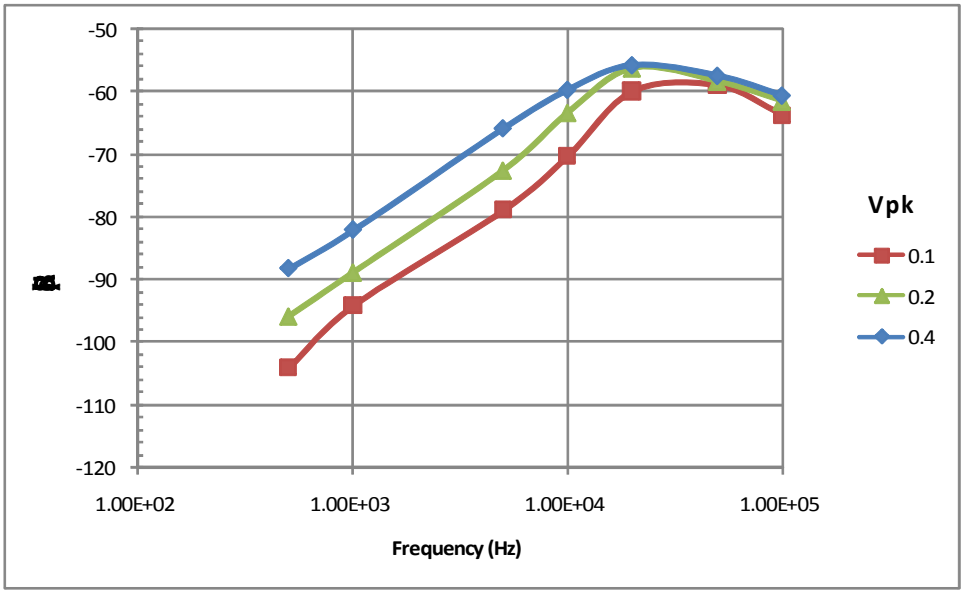


T06 – Load Regulation

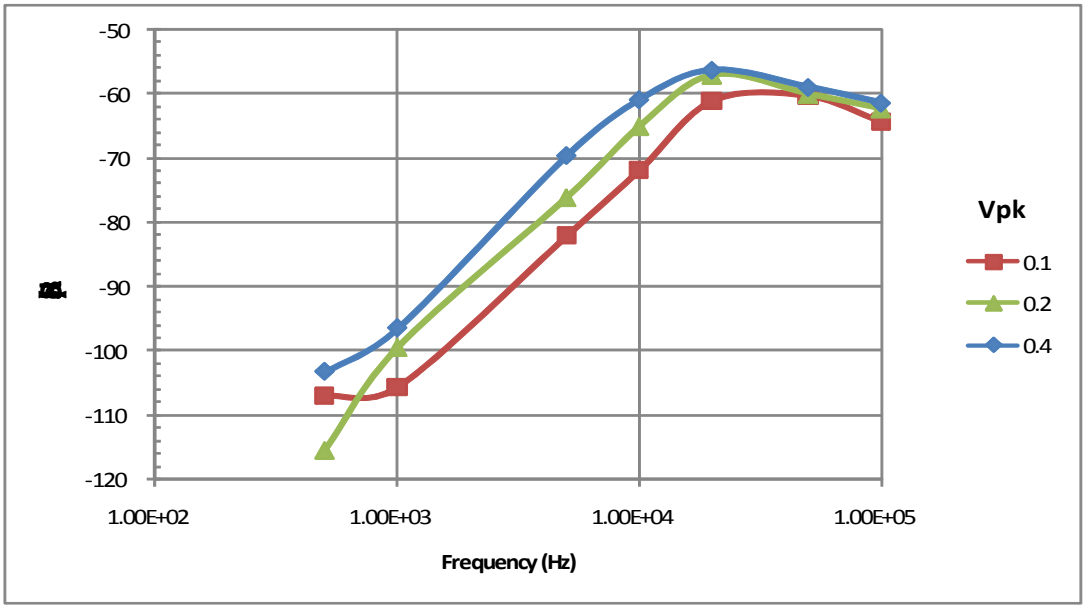
Regulation of LDO across Ouput current for several Input voltages



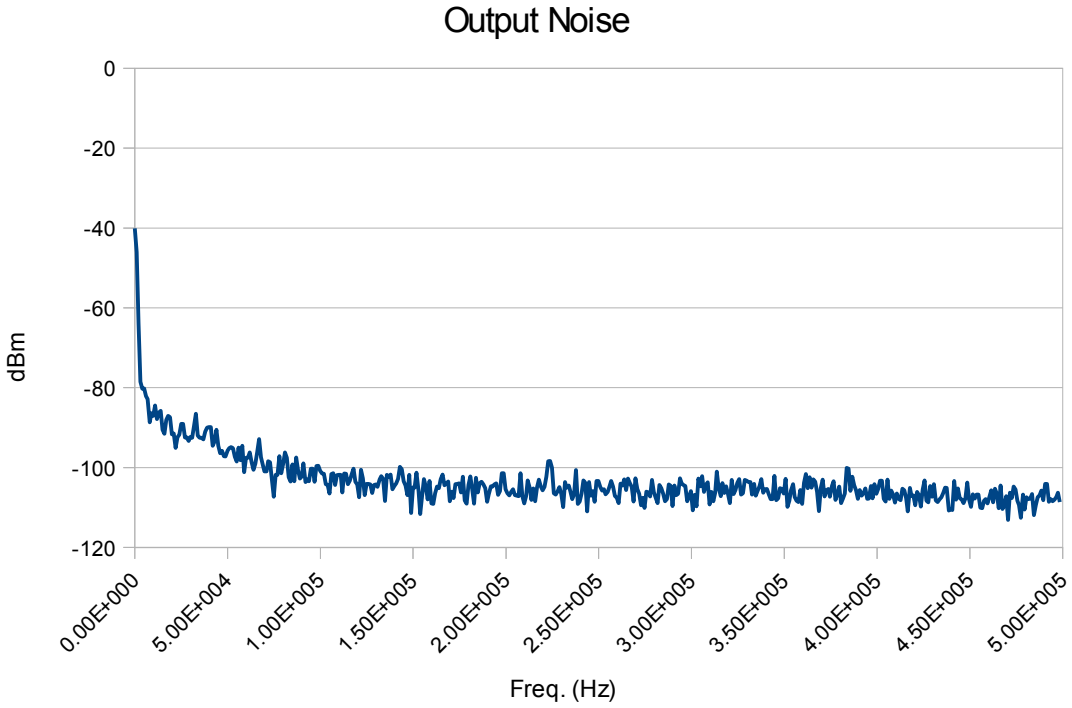
T11 – PSRR



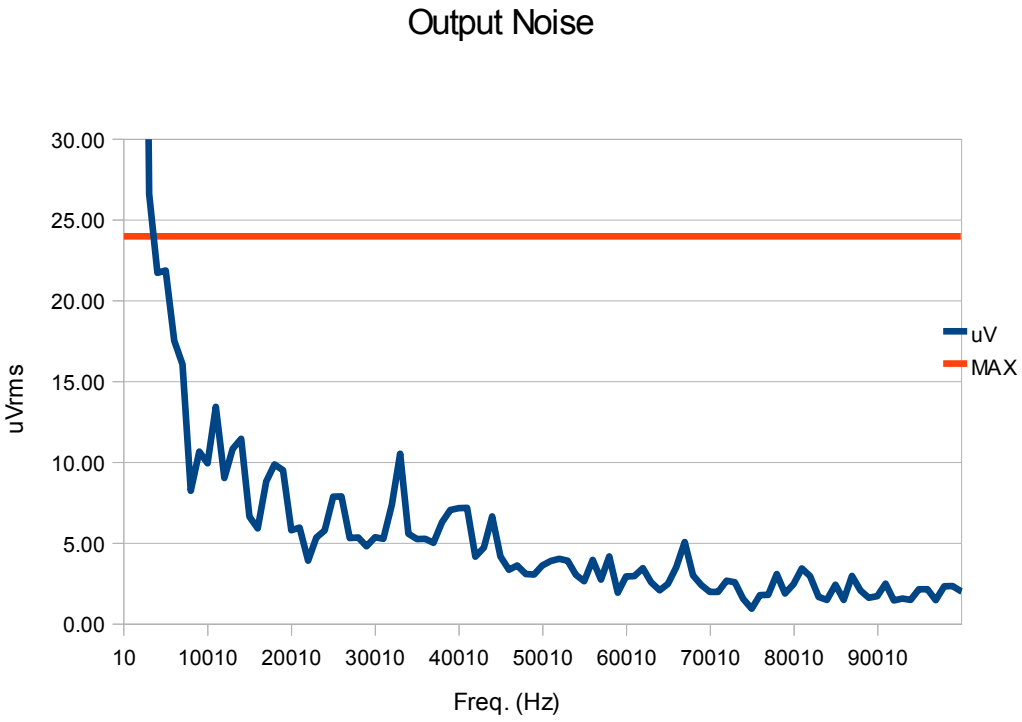
PSRR with 5.1V input



T12 – Output Noise

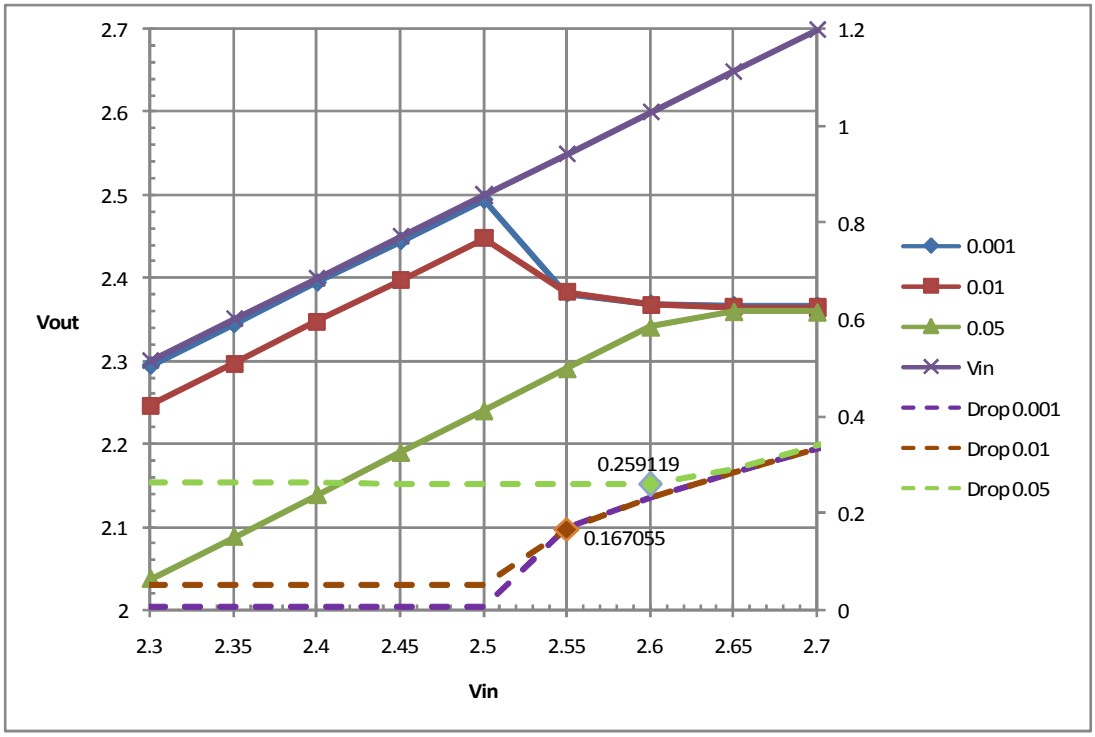


The Equivalent plot converted to uVrms in the frequency range between 10Hz and 100kHz is shown below together with the theorical calculated maximum. The measurement was taken with the series capacitor so, the near DC large component is thought to be due to an offset on the Spectrum Analyzer internal 50Ohm Termination resistor.


Output Noise
30.00
25.00
20.00
15.00
10.00
5.00
0.00
uVrms
10
10010
20010
30010
40010
50010
60010
70010
80010
90010
Freq. (Hz)
uV
MAX

T13 – Voltage Drop

Conditions: ILOAD = {1mA; 10mA; 50mA}



In horizontal axis is the voltage input (VIN), also represented by the most higher line on top (“purple”).

In solid lines is represented the LDO output (VOUT) for the different load currents. The scale for the voltage outputs is on the left side.

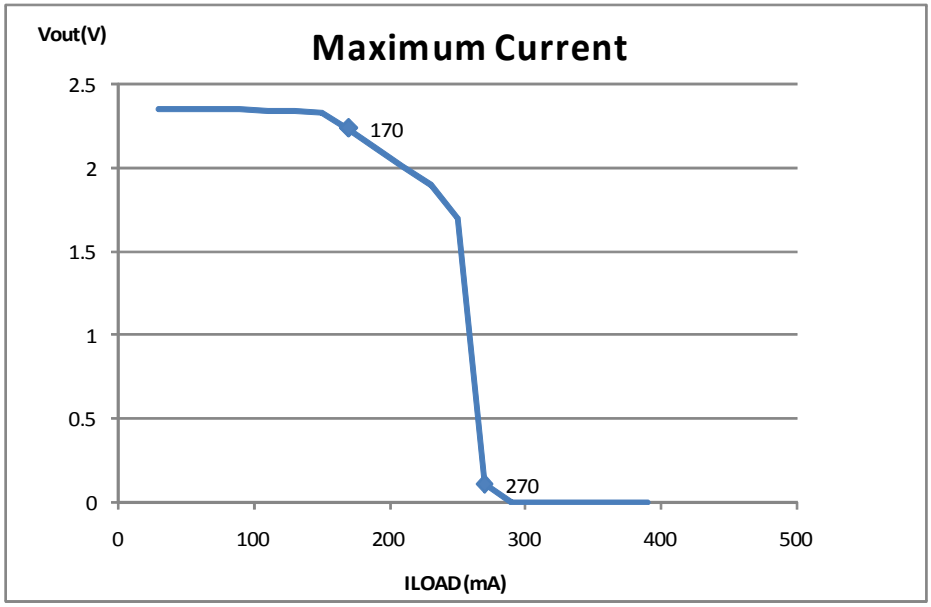
The dashed lines represent the LDO drop (VIN-VOUT) for the several load currents. Please refer to the scale on the right side of the plot for the LDO Drop readings.

T14 – Maximum Current

Conditions:

Vin = 3.1V

Iout = [3mA ..390mA]



LDO looses regulation at 170mA load and shuts down at 270mA.

6.4. DC/DC

6.4.a) Specifications

VIN = [1.8V ; 4.5V], VO = [0.8V ; 3.9V], ILOAD = [0mA ; 180mA],
TA = [-40°C ; +125°C], minimum (VIN - VO) = 500mV.

Typical conditions:

VIN = 3.3V, VO =1.2, ILOAD = 100mA, CX=4.7uF, LX=1uH, TA=25°C, trim<5:0> = “011011”, vprog<4:0> = “00100”, bmax<1:0> = “00” and bmin<1:0> = “00”, unless otherwise specified.

Table 12: DC/DC Specification

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ts	Start-Up Time	ILOAD = 0mA, VIN=4.5V	32	42	110	µs
IPD	Power-Down Current	PWRDN=1		6.8		nA
IQSLEEP	Quiescent Current	I_{LOAD}=1mA, en=0		5		µA
IQFAST	Quiescent Current	I_{LOAD}=100mA,en=0		85		µA
IQEN	Quiescent Current	en=1		2.12		mA
ILXH	Inductor Pulse Max Current Integrator and Refs Trimmed			400		mA
ILXL	Inductor Pulse Min Current Integrator and Refs Trimmed			0		mA
VO	Output Voltage Selection	I_{LOAD}=100mA	0.8	1.2	3.9	V
IOM	Maximum Output Current			180		mA
VOR	Output Voltage Ripple Peak to Peak,	I_{LOAD}=100mA		26.0		mV
$\Delta V_{OUT}/V_{IN}$	Line Regulation	1.8V ≤ VIN ≤ 4.5V		259.3		µV/V
$\Delta V_{OUT}/\Delta V_{IN}$-PK	Line Transient Voltage Peak	VIN from 1.8V to 4.5V		44		mV
$\Delta V_{OUT}/\Delta V_{IN}$-T	Line Transient Peak Period	VIN from 1.8V to 4.5V		4		us
$\Delta V_O/I_{LOAD}$	Load Regulation	10mA ≤ I_{LOAD} ≤ 100mA		-128.9		µV/mA
$\Delta V_{OUT}/\Delta I_{LOAD}$-PK	Load Transient Voltage Peak	I_{LOAD} from 10mA to 100mA		435		mV
$\Delta V_{OUT}/\Delta I_{LOAD}$-T	Load Transient Peak Period	I_{LOAD} from 10mA to 100mA		1		ns
η	Efficiency	I_{LOAD} {1mA;10mA:100mA} (VO;VIN) = {(1.2V;3.3V) ; (1.2V;4.5V) ; (2.2V;3.3V) ; (2.2V;4.5V) ; (3.9V;4.5V)}	73.9	81.4	93	%

6.4.b) Test Results

Table 13: DC/DC Test Summary

Symbol	Test	Condition	MIN	TYP	MAX	Units
ts	T01	Not Done				µs
IPD	T02	Not Done				nA
IQSLEEP	T03	Not Done				µA
IQFAST	T04	Not Done				µA
IQEN	T05	Not Done				mA
VO (Accuracy)	T06	V_{IN}={3.1;5.1} I_{LOAD}= [1mA...64mA] All settings where: Vout < Vin-500mV	-12.16		76.4	mV
IOM	T07	Not Done				mA
VORipple	T08	Not Done				mV
$\Delta V_{OUT}/V_{IN}$	T09	Iout =[1mA...128mA], Vprog = {0;8;16;24;31} ; Vin = {3.1; 3.5; 3.9; 4.3; 4.7; 5.1}; deftrim = 0 and Vout < Vin-500mV	-2.67		2.04	%
$\Delta V_{OUT}/\Delta V_{IN}$-PK	T10	Not Done				mV
$\Delta V_{OUT}/\Delta V_{IN}$-T						ms
$\Delta V_O/I_{LOAD}$	T11	Iout =[1mA...128mA], Vprog = {0;8;16;24;31} ; Vin = {3.1; 3.5; 3.9; 4.3; 4.7; 5.1}; deftrim = 0 and Vout < Vin-500mV	-3.32		4.80	%
$\Delta V_{OUT}/\Delta I_{LOAD}$-PK	T12	Not Done				mV
$\Delta V_{OUT}/\Delta I_{LOAD}$-T						ms
Output Ripple	T14	Not Done				mV
η	T15	Iout =[1mA...128mA] Vprog = {0;8;16;24;31} ; Vin = {3.1; 3.5; 3.9; 4.3; 4.7; 5.1}; deftrim = 0 and Vout < Vin-500mV NOTE #2	40.06 #1		82.04	%

Notes:

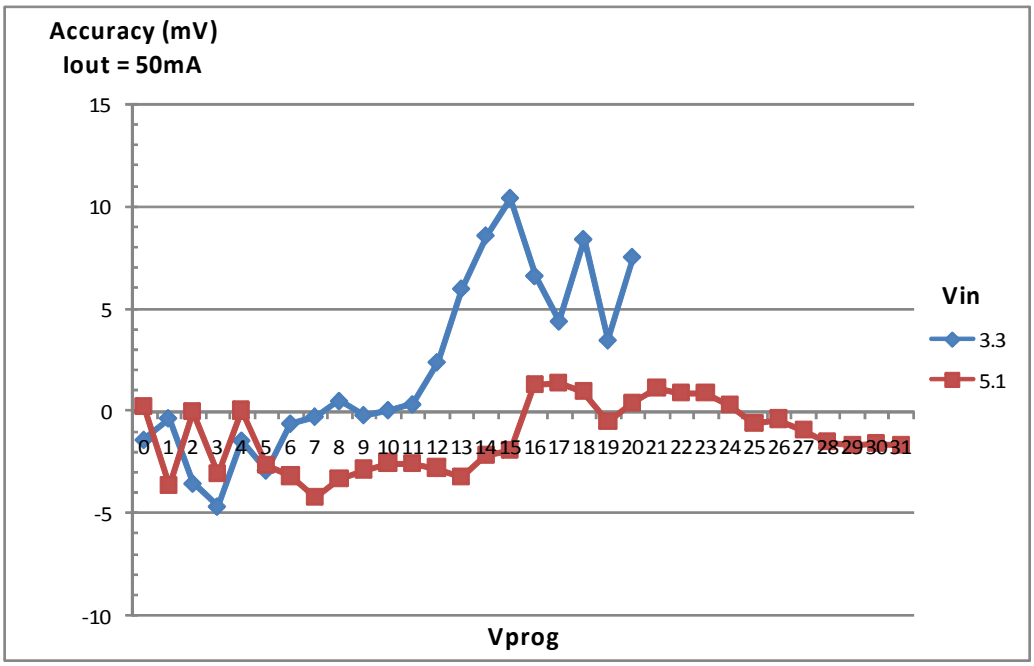
#1 Minimum 32mA Current Load for minimum efficiency.

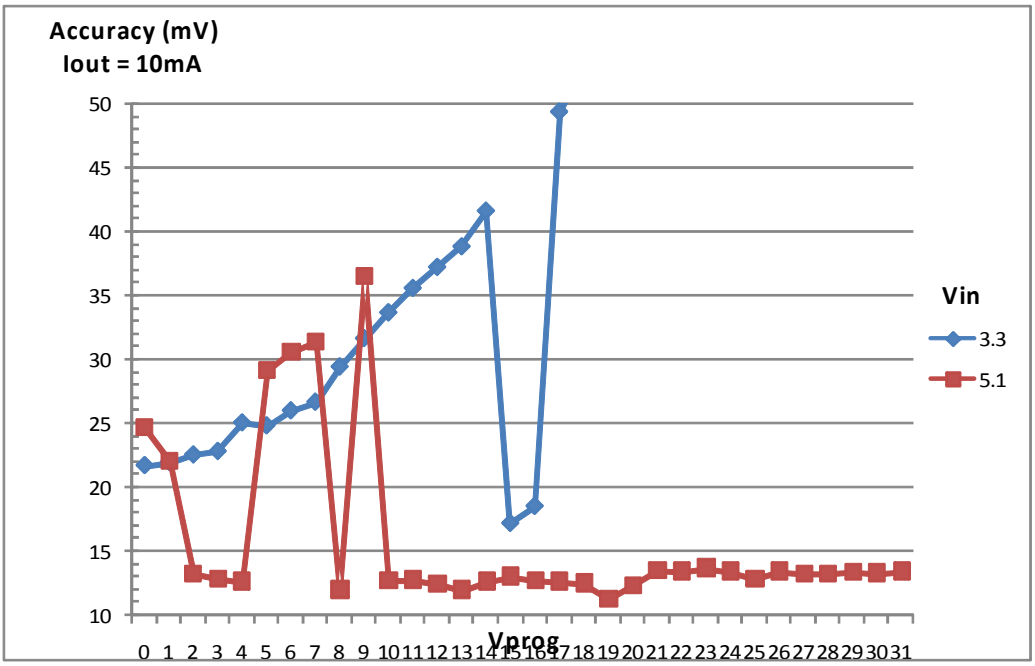
#2 The efficiency levels are affected by the fact that Vin supply is shared in the fast prototyping board with the LDO and ChargePump supply, and also the interface stage of the parallel port.

T06 – Accuracy

Conditions: Vin = {3.3; 5.1} ; Vout = 0.8 + vprog*0.1 ; Vout ≤ Vin – 500mV Iout = {10mA; 50mA}

Accuracy = Vout - 0.8 + vprog*0.1





T09 – Line Regulation

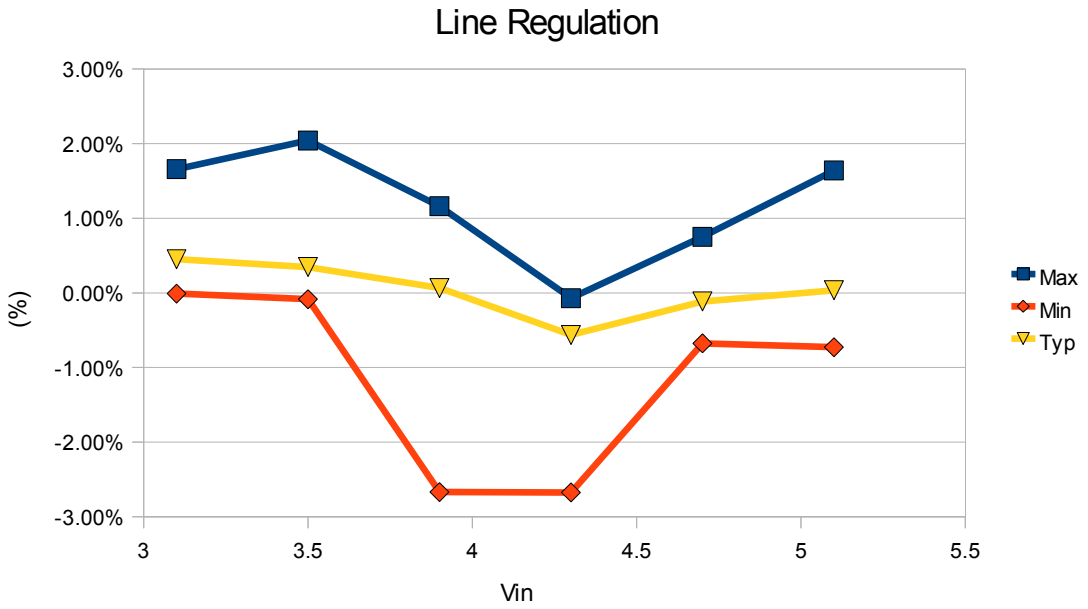
Conditions:

Iout =[1mA...128mA],

Vprog = {0;8;16;24;31} ; Vin = {3.1; 3.5; 3.9; 4.3; 4.7; 5.1};

deftrim = 0 and

Vin – 500mV >= 800mV + vprog*0.1



Regulation calculated as the variation of Vout across a series for a given Iout and vprog.

T11 – Load Regulation

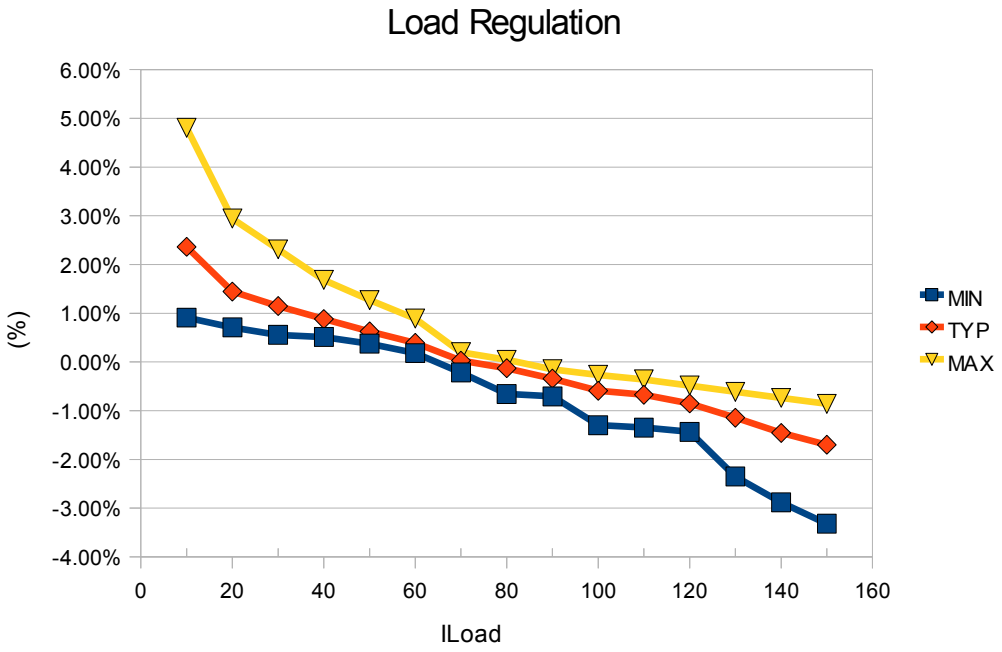
Conditions:

Iout =[1mA...128mA],

Vprog = {0;8;16;24;31} ; Vin = {3.1; 3.5; 3.9; 4.3; 4.7; 5.1};

deftrim = 0 and

Vin – 500mV >= 800mV + vprog*0.1



T15 - Efficiency

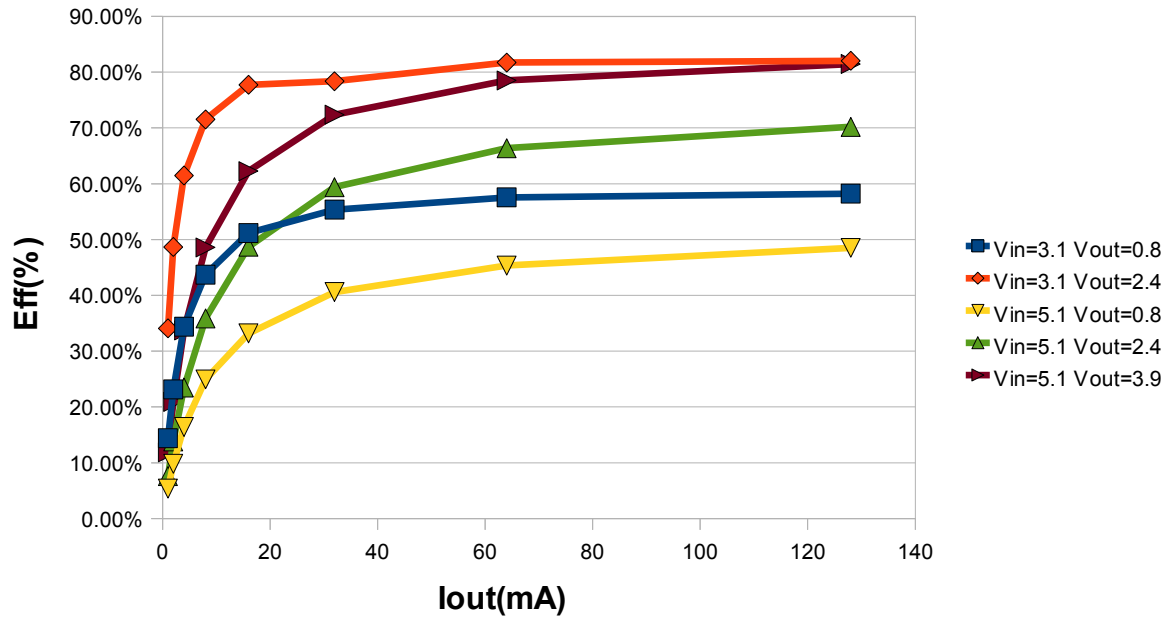
Conditions:

Iout =[1mA...128mA],

Vprog = {0;8;16;24;31} ; Vin = {3.1; 3.5; 3.9; 4.3; 4.7; 5.1};

deftrim = 0 and

Vin – 500mV >= 800mV + vprog*0.1



NOTE : This efficiency levels are affected by the fact that VIN line is shared with the LDO; Charge Pump and the interface stage of the parallel port.

7. Conclusion

The nature of this project make it very multi-disciplinary. It covers several fields such as : Power Converters; Test and Measurement; Board Level System Design; Software Development and Database Management. The 13 years of experience working in the electronics field, were, in this author opinion, were an essential asset for the definition of solutions here implemented. Nonetheless, the project still required an extensive research.

For unforeseen delays on the manufacture and of the test platform, the initial statement of work wasn't complied and back-up solution had to be found to make the tests that were initially proposed.

With the prototyping board, the proposed test procedures where validated and automated using only application level test scripts.

For the static measurements, the test fixtures that were designed couldn't be used, so two source meters were used. Using an USB to GPIB controller, 100ms per test case was achieved.

The PSRR measurements were also automated, a Spectrum Analyzer together with a function generator and a Power Buffer circuit that was built for a former project of the author. A Spectrum Analyzer

Automating the transient test proved to be much more difficult. Setting the Vertical and Horizontal scales of an oscilloscope using the pyVisa library proved to be quite easy, however, developing the algorithm that calculates the optimal Vertical and Horizontal scales depending on the test condition would take more time than the available and thus was not done.

In order to continue this work, the following steps must be completed.

- Populate and bring up test platform board
- Rewrite the PMGDUT object class to match the new test platfrom
- Repeat the tests that were limited or which performance was degraded by the use of the fast prototype board.
- Install an MySQL server and use available controlling objects to include in test scripts data commit to SQL tables.

8. Literature Review

At board system design the best source of guideline information are IC Manufacturers Applications Notes and Design Recommendations. Also much useful information is found on discussions of electronics newsgroups. Searches done in the scientific and academic universe did not produce many relevant references, specially in what concerns Test and Characterization of Power Management IPs.

Given the diverse source of information collected for this project, the references are categorized by the different areas.

For Power Management concepts, we highlight [8] since it has a good tutorial for the reader that is not familiar with Power Management components, namely DC/DC converters.

[9] Establishes all terms and definitions used in the Power Management Test and Characterizations and exemplifies a typical Test Setup for DC/DC converters.

Application Notes [10] [11] and [12] give some insight on choosing the right components for DC/DC converters and [13] give a design tip to avoid oscillations at the Voltage Input of DC/DC converters.

[14] its old but still really a good source of practical information on the operation of DC/DC. Very nuts and bolts kind of application note, written with a good sense of humor as is usual in all Jim Williams Application Notes.

These two next references [15] and [16] are focused on decoupling capacitors. Not only for DC/DCs but also for digital circuits.

The [17] approaches the subject of the load transient circuits and test problems.

For the PSRR Measurement, we highlight two references: [6] although not intended primarily to the Power Management IPs, it gives some conceptual ideas for the PSRR measurement in Section 3. [7] gives some more solutions to for the PSRR measurement.

For the on-board Instrumentation and Calibration, [19] gives a comprehensive overview of Instrumentation Amplifier technology and application, and [20] gives the complementary background.

For PCB Design, [21] is a primer on ground bouncing problems related to the usage of DC/DCs and [22];[23]and[24] approaches the problem of ground return path..Article [25] is in favor of separate grounds. It is presented here just for the sake of curiosity for the reader.

On [26] the parasitic effects on high frequency applications are analyzed. Although at first sight a Power Management doesn't appear to suffer much from high frequency effects, in reality the fast rise and fall times make these effects quite noticeable.

The [27] presents a short summary of tips to improve PCB Layout Quality in what respects electromagnetic interference (EMI).

[5] Is not exactly an application note, but an essential tool for any PCB designer for the calculation of PCB traces impedance. It isn't as accurate as the SI8000 impedance calculator, but this one is free and is enough for the needs of the current project.

[29] Provides all the information for the implementation of the Test Database.

9. References

[1] Dr. R. D. Middlebrook in International Journal of Electronics, volume 38, number 4, 1975

[2] Howard Johnson High Speed Signal Propagation: Advanced Black Magic

[3] Howard Johnson, “High Speed Digital Design”, Prentice Hall, 1993

[4] Brian D. Butler, “Propagation Delay Measurements with TDR in the Manufacturing Environment” by Introbotics Corporation; Albuquerque, New Mexico
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[5] PCB Trace Impedance Calculator
http://emclabinfo.com/emc_calc/emccalc.htm
http://www.referencedesigner.com/tutorials/si/si_01.php

[6] Kim Madsen and Tomas Soerensen, "PSRR for PurePath Digital™ Audio Amplifiers" June-2005
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[7] David Karpaty, Charles H Small and Fran Granville, “Perform PSRR testing with analyzers having no dc-bias ports”
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[8] Robert W. Erickson, “DC-DC Power Converters”
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[9] “DC/DC CONVERTER”
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http://www.gaia-converter.ca/content/application_notes/terminologyandbasic.pdf

[10] “T8xC5121 DC/DC Guidelines”
Good design Tips for choosing components for their DC/DC
http://www.atmel.com/dyn/resources/prod_documents/doc4216.pdf

[11] “DC/DC Inverter” (Application Information)
Good Design Tips for Choosing components for DC/DC and recommended Layout

http://focus.ti.com/lit/ds/symlink/tps63700.pdf

[12] Christophe Vaucourt, "Choose the best inductor, capacitor for DC/DC converters in portables"
Texas Instruments
http://www.embedded.com/columns/technicalinsights/188500678?_requestid=475827

[13] Robert Kollman, "Power Tip #3: Damping the input filter"
Texas Instruments
http://www.powermanagementdesignline.com/howto/210500098

[14] Jim Williams, “Switching Regulators for Poets - A Gentle Guide for the Trepidatious"
Linear Technology 1987
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[15] Tamara Schmitz and Mike Wong, "Choosing and Using Bypass Capacitors"
Intersil, August 3, 2007
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[16] Mark Alexander, "Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors"
Xilinx February 28, 2005
http://www.xilinx.com/support/documentation/application_notes/xapp623.pdf

[17] Jim Williams, "Load Transient Response Testing for Voltage Regulators
Practical Considerations for Testing and Evaluating Results"
Application Note 25
Linear Technology October 2006
Advises for the Load Transient Testing
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11. Glossary

ATE – Automatic Test Equipment

BER – Bit Error Ratio

DC/DC – DC to DC converter.

Dropout – Voltage Difference between the input and the output of a Power Management Unit.

DUT – Device Under Test

IP – Intellectual Property

LDO – Low Dropout Regulator

Loadboard – Interface Board between DUT and ATE

Microstrip – trace on the surface of a PCB

PCB – Printed Circuit Board

Piggyback – Board that is attached parallel to a bigger mother board

PSRR – Power Supply Rejection Ratio

SQL – Structured Query Language

Stripline – trace buried between layers of a PCB

Testchip – Integrated Circuit that is a test vehicle for a set of IPs

12. Annex A – Platform Schematics

13. Annex B – Prototype Board Schematics

14. Annex C – Daughterboard Schematics