Submarine Cable Power Transmission using DC High-Voltage Three-Level Converters

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Abstract – This paper is about multilevel converters used in High Voltage Direct Current (HVDC) systems. Multilevel converters are useful to reduce voltages applied to semiconductors and to reduce total harmonic distortion (THD) in voltage output but here is presented the study of short-circuit faults in the operation of three, five and seven-level architectures of diode-clamped converters operated as three-level converters. The converters work as inverters placed in one end of a direct link with 500 kV supplying an inductive and monophasic load. The active semiconductors chosen are insulated gate bipolar transistors (IGBTs) and are forced to work in short-circuit situation individually to study, in Simulink environment, the converter behaviour working with this faults. Is expected to reduce short-circuit currents with the increase of levels in the converter.

Index Terms – Multilevel converters, Diode-Clamped Converters, Three-level converters, HVDC systems, short-circuit faults.

I. Introduction

HVDC systems appear as an alternative to the common alternate current (AC) network grids at high voltage levels in power systems bearing in mind some special features as reducing costs, losses and environmental concerns. HVDC systems needs to interact with the successful AC networks once they are wide spread, hence at least two converter stations, AC to DC and DC to AC, are needed and represent an important part of these systems, together with a DC cable link. This technology arises later due to necessity of reliable and economic power electronic devices working with high voltage but is now also wide spreading facing the opportunities where it can compete with AC networks.

An HVDC system is mainly used in interconnection of networks, to reinforce both power systems assuring more balanced power transmission between them, and also to transport energy through long distances (approximately 600 km or more) due to a reduced cost when compared with AC transmission[1]. The cost of converter stations is the most expensive in the investment for an HVDC system and that is the main reason to only use this technology for long distances in overhead lines. The less known submarine cable power transmission is much more adequate to DC systems and is also recognition of HVDC once the use of AC underground or undersea cables were limited to small distances due to their time variant inherent characteristics.

Two different technologies exist for converter stations. The first one is based in line-commutated current source converters (CSCs) using thyristors while the other uses force-commutated voltage source converters (VSCs) with gate turn-off thyristors (GTOs) or IGBTs and they are discussed in [2].

Multilevel converters are part of VSCs family once they respect voltage input and output features and among several topologies the diode-clamped converter is selected for simulation. This paper is organised as follows: diode-clamped converters are briefly introduced in Section II and simulation results for their operation are discussed in Section III; Section IV presents short-circuit faults in the converters and a summary of results achieved is presented in Section V.
II. Multilevel Converters

The development of multilevel converters grows in parallel with the increasing industry needs of higher power equipments in last decades. Also its development is also related with new concepts of electronic conversion, new control systems and new power semiconductors.

Their concept is based in several lower voltage DC sources interacting with power semiconductors to perform power conversion by synthesizing a staircase voltage waveform. The commutation of switches allows the addition of the multiple DC voltage sources reaching a higher output voltage while semiconductors withstand only small voltages (specifically the rating of the DC source to which they are connected). DC voltage sources can be series connected capacitors, batteries or renewable energy sources and the voltage at their terminals is

\[ u_{ci} = \frac{U_{dc}}{(n - 1)} \]  

where \( U_{dc} \) is a nearly constant voltage which represents the maximum voltage drop in the DC side. Also the arrangement of power semiconductors in the converter is made to enable each of them to withstand the same voltage seen in (1).

Three major topologies are well established one [3] [4] [5], namely: diode-clamped, capacitor-clamped and cascaded multicell with separate DC-sources.

The diode-clamped converter is selected to represent a possible VSC in an HVDC system.

II.1. Diode-Clamped Converter

From major topologies, the diode-clamped converter was introduced first by Nabae et al in 1981 [6] and constantly studied in other literatures [7] [8]. The inverter appears as the sequence of a two-level inverter where semiconductors are placed in series to withstand higher voltages. The possible voltage outputs referenced to zero are \( U_{dc} \) and 0. The three-level converter arises with two addition diodes and two capacitors limiting maximum voltage applied in semiconductors to \( \frac{U_{dc}}{2} \) with architecture seen in Figure 1. The middle point between capacitors is defined as neutral point and both diodes connected to it allow current to flow in a new working level achieved in the converter \( \frac{U_{dc}}{2} \) using adequate command signals.

![Figure 1 – Three-level converter.](image)

The extension of this converter topology to \( n \)-levels requires \( (n - 1) \) capacitors and \( 2(n - 1) \) active switches. To assure bidirectional behaviour in current allowing inductive loads to work properly, each switch identified as \( S_j \) is placed together with an anti-parallel diode as shown in Figure 2.

![Figure 2 - Generic multilevel diode-clamped converter.](image)

The \( n \)-level converter to keep the same reverse voltages applied to all, also requires extra
number of clamping diodes. For example in a five-level converter, supplying \( u_1 = U_{dc} \) with all upper switches turned on \((S_1 - S_4)\), the first diode of each column withstands \( U_{dc}/4 \), \( 2U_{dc}/4 \) and \( 3U_{dc}/4 \) respectively. So in order to balance their voltages some additional diodes are placed in series increasing the number of these semiconductors in quadratic proportion. The number of clamping diodes for each phase of converter is \((n-1) \times (n-2)\). The architectures are usually designed to establish maximum voltages in semiconductors to specific capacitors. From top of converter to bottom, IGBTs turned OFF mirrors the voltage of capacitor in the same order. For example in state 2, \( S_1 \) mirrors \( C_1 \), \( S_2 \) mirrors \( C_2 \), \( S_5 \) mirrors \( C_3 \) and \( S_6 \) mirrors \( C_4 \). The same for diodes where \( D_{xj} \) mirrors the voltage in \( C_j \) (\( x \) is the number of the column of diodes and \( j \) the number of the diode/capacitor).

III. Operation of Diode-Clamped Three-Level Converters

The study is made using Simulink software available in Matlab and to simulate a more realistic working environment, non ideal features are introduced in semiconductors as forward voltage, current tail time, current 10% fall time and snubbers. Also to introduce differences between the same type of semiconductors, resistances are placed in parallel with every single one of them with randomly selected values. All these resistances present the same magnitude order of \( M \Omega \). Three, five and seven-level converters are operated for three output levels using a simple sinusoidal pulse width modulation (SPWM) [9] [10] but creating a signal with half wave symmetry to eliminate even order harmonics.

The active semiconductors chosen are IGBTs with conduction resistances of \( 0.1 \Omega \), the DC bus is represented by a DC source with \( 500 \text{ kV} \) \( (U_{dc}) \), capacitors of \( 10000 \mu \text{F} \) and parasitic resistance of \( 0.1 \Omega \). The source simulates the ideal voltage immediately established after rectification in a converter station. The cable is represented only by a resistance with \( 6 \Omega \) which follows a DC reactor [11], usually placed to smooth current, with \( 500 \text{ mH} \). The load is an \( RL \) branch, with \( R = 10 \Omega \) and \( L = 100 \text{ mH} \) to illustrate reversibility in the converter.

III.1. Three-Level Converter

The three-level converter is the basic cell of diode-clamped converters and operated to supply a monophasic load as seen in Figure 1, load voltage achieves three levels \( (250 \text{ kV}, 0 \text{ and } -250 \text{ kV}) \) and current follows, almost, a sinusoidal evolution with a peak value rounding \( 6 \text{ kA} \). To simplify levels identification, they are presented along the paper as state 1, 2 and 3 concerning \( 250 \text{ kV}, 0 \text{ and } -250 \text{ kV} \) applied to load respectively.

The contribution of each capacitor to load is presented in Figure 3 and is noticed that DC bus supplies a nearly constant current due to cable impedance.

![Figure 3 – Capacitors and load currents in three-level converter.](image)

So, capacitor \( C_1 \) contributes during state 1 and \( C_2 \) during state 3. Each one of them is charged with \( 250 \text{ kV} \). Load current orientation influences if capacitors charge or discharge in these states. In state 2 capacitors slowly charge due to DC cable current.

Voltage sharing in all semiconductors respects the ideal concept once the maximum absolute voltage they withstand is, approximately, \( 250 \text{ kV} \).

III.2. Five-Level Converter

In the five-level converter the number of semiconductors increases to eight IGBTs with eight anti-parallel diodes and twelve clamping diodes arranged in three columns with four diodes each. Also these columns are connected to each other as a diode network [12] as a completion of their series connection to limit and balance
voltages of different clamping diodes. The number of capacitors increases to four and each presents 125 kV through its terminals where neutral point is the inner point between $C_2$ and $C_3$. So, capacitors $C_1$ and $C_2$ contribute to state 1 while $C_3$ and $C_4$ are responsible for state 3, while during state 2 capacitors do not intervene. As this converter is controlled as a three-level converter IGBTs are grouped and are operated simultaneously. The groups are arranged with two adjacent semiconductors. With this control load voltage and current are the same as for the three-level converter despite some more voltage drops in more semiconductors.

The problem for these converters can be the voltage sharing between semiconductors but through simulation is observed, in Figure 4 and Figure 5, a decent result either for diodes and IGBTs. The current circulation in the diode network only exists through diodes in the second column. This column is the one clamping the neutral point and current flows in the diodes during state 2 as seen in Figure 6.

Figure 4 – Voltage in diode network in five-level converter.

Figure 5 – Voltage in IGBTs in five-level converter.

So, the diode network in a five-level converter operated as a three-level converter is extremely useful in voltage sharing or else great voltage differences between semiconductors would exist.

III.3. Seven-Level Converter

The seven-level converter as no different features than the previous one except for the voltage withstand by each semiconductor which is smaller. Capacitors $C_1$, $C_2$ and $C_3$ constitute now the voltage in state 1 while $C_4$, $C_5$ and $C_6$ constitute state 3. This way the neutral point is between $C_3$ and $C_4$. The voltage in each capacitor and consequently the ideal maximum absolute voltage withstand by semiconductors rounds 83.3 kV.

Figure 6 - Currents in diode network in five-level converter.

Figure 7 - Voltage in diode network in seven-level converter.

Despite the ideal consideration, equal voltage distribution is more complicated to achieve than for the five-level case but results are still much better than without network once voltage differences present some boundaries and no semiconductor withstands more than 100 kV in the worst case.
In state 2 the current circulates through the column of diodes clamping the neutral point, which is the third column. In this architecture diode network presents five columns with 6 diodes each.

**IV. Short-Circuit faults in Diode-Clamped Three-Level Converters**

Short-circuit faults are taken separately for each IGBT, i.e. only one IGBT is short-circuited for simulation. These faults are represented by a change in the semiconductor command signals from $S_j = 0$ to $S_j = 1$ and the ones happening in states 1 or 3 are referred to smaller conduction duties implying slower discharge.

**IV.1. Three-Level Converter**

In Table 1 are represented all possible short-circuit faults, which cause discharge of one capacitor and short-circuit current, in a three-level converter for each state.

<table>
<thead>
<tr>
<th>State ID</th>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$S_3$</th>
<th>$S_4$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0→1</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0→1</td>
<td>1</td>
<td>1</td>
<td>0→1</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0→1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

So, in this case, all semiconductors can create such short-circuit current due to the arrangement of a smaller impedance path seen by the capacitor when a series connection of three IGBTs (two regular and one short-circuited) occurs. This architecture arranges a path using three IGBTs and one diode no matter which IGBT is short-circuited. So short-circuit current highest peak is approximately

$$I_{cc} = \frac{250}{5r_{on}} = 500\,kA, \quad (2)$$

assuming voltage in capacitors ideal, 250 kV and considering $r_{on}$ as conduction resistances in semiconductors and as the parasitic resistance in the capacitor. Both present the same value in simulations taken. This short-circuit value is extremely high and immediately destroys all semiconductors in the converter. With the increase of levels is expected this value to reduce.

The influences in load behaviour, for short-circuit in IGBT 1, are observed in Figure 8. The discharge of $C_1$ forces the other capacitor to charge and assume entirely the voltage difference created achieving one new steady state. Load voltage is then practically compound by two levels, 0 and $-500\,kV$. This also perturbs load current due to its inductive nature.

![Figure 8 - Capacitors and load voltage with short-circuit fault in IGBT 1 of three-level converter](image)

With this voltage changing in capacitors the semiconductors now present different voltages applied both adjacent IGBTs and clamping diodes.

**IV.2. Five-Level Converter**

In Table 2 is presented which semiconductors cause the discharge of one capacitor and in which state.

<table>
<thead>
<tr>
<th>ID</th>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$S_3$</th>
<th>$S_4$</th>
<th>$S_5$</th>
<th>$S_6$</th>
<th>$S_7$</th>
<th>$S_8$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0→1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0→1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0→1</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0→1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Only four IGBTs, the same number as for three-level case, are identified as causers of short-circuit currents while the converter totals eight. The IGBTs that do not discharge any capacitor, do not affect load voltage or current behaviour. Despite being a positive feature for load, this situation is not entirely acceptable to some semiconductors because short-circuiting one IGBT implies a voltage trade-off with other...
semiconductors where in the worst case they need to withstand twice the voltage they are used to. The only case this not happen is for the edge IGBTs, $S_1$ and $S_6$ that place $D_{11}$ and $D_{25}$ directly in anti-parallel with $C_1$ and $C_4$ during all states withstand the rated value. This happens for diode network but obviously the adjacent IGBT feels all voltage difference now withstand twice the usual voltage. So only if semiconductors are oversized concerning maximum voltage applied, short-circuit fault in one of these IGBTs is not considered a problem. In Figure 9 is presented the simulation result for short-circuit in IGBT 3 where is visible the increase of voltage in $D_{14}$ and consequently reduction in $D_{13}$. Also now $D_{31}$ and $D_{32}$ withstand some voltage while before short-circuit they ideally withstand zero.

Looking for short-circuit currents, now a path arranged by a series connection of the usual IGBTs and the short-circuited one includes five IGBTs and three diodes. With ideal voltage of 125 kV in a capacitor the short-circuit current highest peak is

$$I_{cc} = \frac{125}{9} \approx 139 \text{ kA}.$$  (3)

The peak value is 3.6 times smaller than for the three-level converter. The difference exists primarily due to the voltage in the capacitor which is reduced in half and also to the higher number of semiconductors in the path.

Concerning load, the result is better because output voltage never loses any of three-level. One capacitor discharges but two are responsible for positive and negative output voltage levels. For example discharging $C_2$, with short-circuit of $S_2$, state 1 is achieved through the remaining voltage in $C_1$. Still, $C_1$ trends to assume the voltage difference created by the discharge supplying load with the usual 250 kV in state 1. The evolution is presented in Figure 10 where is visible the discharge of $C_2$ and trend of other capacitors after an initial balance where all charge the voltage difference created.

![Figure 10 - Capacitors and load voltage with short-circuit fault in IGBT 2 of five-level converter.](image)

In Figure 11 is presented the loop created and current circulation during discharge of $C_2$.

![Figure 11 - Discharging loop in five-level converter with short-circuit fault in IGBT 2.](image)

The voltage unbalance in semiconductors also exists due to the voltage differences created with the discharge and consequent charge of other capacitors.

**IV. 3. Seven-Level Converter**

In seven-level converters the same number of IGBTs creates short-circuit currents, four. Obviously the others do not influence load
behavior also but settle some differences in voltage balancing in semiconductors. The edges IGBTs do not repeat the five-level behavior because adjacent diodes to the one affected feel also that voltage trade-off. This is also result of a more complicated voltage balancing in the diode network. In this architecture with an ideal voltage of $83.3$ kV in a capacitor and a path with seven IGBTs and five diodes, short-circuit current highest peak is

$$I_{cc} = \frac{83.3}{13} \approx 64.98 \text{ kA}.$$  \hspace{1cm} (4)

The value is more than two times smaller than (3) and almost eight times smaller than (2). Also with more capacitors used to perform a level, the discharge of one provokes a smaller influence in load voltage and consequently current. In this case losing the voltage from one capacitor, is still possible to achieve in minimum $2 \times 83.3$ kV to perform the level. Anyway, the discharge is not instantaneous and during it other capacitors start to balance voltage distribution in capacitors followed by the trend.

The four IGBTs that create this discharge are the ones placing in series seven IGBTs during one state. They are $S_5, S_6, S_7$ and $S_10$ and are the last semiconductors of each group arranged to work as a three-level converter. The lower IGBTs this way are counted from the bottom of the converter once the converter is symmetric. The symmetry in operation is not entirely valid for short-circuit events because new voltage distributions are not necessarily equal for upper and lower IGBTs placed symmetrically in converter.

IV.4. n-Level Converter

The n-Level Converter represents the extension of this study to all traditional architectures of diode-clamped converters. All short-circuit currents are caused by the series arrangement of the regular IGBTs connection and a short-circuited one. Only four IGBTs create such situation and within the group of semiconductors arranged to control the converter with three-levels is always the last one. The lower part of converter starts the counting from the bottom. The IGBTs are specifically $S_{(n-1)/2}, S_{n-1}, S_n$ and $S_{(3n-1)/2}$ discharging respectively $C_{(n-1)/2}$ (during state 2), $C_{n-1}$ (during state 3), $C_1$ (during state 1) and $C_{(n+1)/2}$ (during state 2).

Short-circuit current in n-level converters decreases according to

$$I_{cc} = \frac{U_{dc}/(n-1)}{2(n-1)r_{on}} = \frac{U_{dc}}{2(n-1)^2r_{on}}$$  \hspace{1cm} (5)

disregarding parasitic resistance from the capacitor.

Short-circuit currents simulated are extremely offensive to semiconductors in converter but concerning just load voltage applied, the higher number of capacitors for each level allows a more steady output voltage in the converter. Even with one capacitor discharged, is seen the trend of the other capacitors in same level charging the voltage difference. This way load voltage is only slightly perturbed.

For standard values of current ratings in IGBTs, approximately 1 kA, the number of levels in converter to create a short-circuit current highest peak round 1 kA is

$$1 \text{ kA} = \frac{500 \text{ kV}}{2(n-1)^2r_{on}} \Rightarrow n = 51.$$  \hspace{1cm} (6)

This result is taken considering load impedance is always bigger than the alternative path created with short-circuited IGBT. Even though with 51 levels semiconductors would need to withstand 10 kV while the maximum available usually rounds 6.5 kV. Architecture to respect this voltage rating has a number of levels bigger than 77.

With destructive values of short-circuit currents but yet capable of being interrupted by fuses or circuit breakers is advised. The use of fuse in the semiconductor short-circuited is complicated because it creates an open circuit turning impossible load current to flow adequately. It only flows through the anti-parallel diode. This solution is than not acceptable to maintain converter output behaviour. Another solution which does not opens load current usual circulation is to place a circuit breaker in the connection between capacitors and diode network except in neutral point. This way short-circuit current is eliminated and load is supplied properly whit no open circuit in its current circulation. This solution do not solves voltage unbalancing existing in semiconductors that still is a recurrent problem.

V. Conclusions

This paper presents the influence of short-circuit faults in IGBTs during the operation of
diode-clamped converters with different number of levels sets and controlled as three-level converters in high voltage conditions.

It is possible to conclude that with architectures designed for higher number of levels, the short-circuit currents created are smaller and always only 4 IGBTs can cause such anomalies no matter the number of levels. The other IGBTs when short-circuited force other semiconductors, diodes and IGBTs, to withstand some extra voltage in worst cases but never more than twice they ideally withstand. Also a trade-off exists when voltage in diode network is changed due to all inner connections between columns, so when some diodes withstand more voltage, others necessarily withstand less. The load is not considerably affected by short-circuit faults in the converter. Faults without discharge of capacitor have no influence at all in load. Faults discharging one capacitor create a small voltage difference in load voltage that is smaller with the increase of levels. Also capacitors responsible for the same output level trend to assume the voltage difference created, keeping load voltage operation equal.

To abridge, short-circuit currents can be reduced by the use of higher levels architectures, as also the perturbations observed in load in this occasions. Only four IGBTs in topology can cause such short-circuit currents when operated as three-level converters. Short-circuit currents are extremely elevated and need to be eliminated. The best solution found is to use a circuit breaker placed in the connection between the capacitor discharging and diode network, except neutral point. Other IGBTs have no influence in load behaviour but create automatically voltage unbalance in some semiconductors with the worst case possible forcing a semiconductor to twice the usual voltage.

Some possible future works in the scope of this paper are the study of architectures with a higher number of levels using the same diode network basis and verify the voltage sharing existing. Identify, if possible, solutions to voltage unbalance in semiconductors with short-circuit faults. Study open circuit faults for other IGBTs to identify problems and possible solutions in the operation of converters in such conditions and study some approaches to face voltage unbalance in capacitors. At last short-circuit situations for three-phase cases and interconnect two converters thru a DC cable and them to respective AC networks to simulate a more complete HVDC system.

REFERENCES


