A 100 mA Fractional Step-Down Charge Pump with Digital Control

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ABSTRACT

A switched capacitor step-down DC-DC converter (charge pump) is proposed. High efficiency is achieved by combination of fractional conversion ratios (different step-down modes of operation), output voltage sensing and pulse skipping based digital control techniques. Two control techniques were implemented with automatic change between modes and their results are discussed and compared. The power module has 9 switches, implemented with 14 power transistors, and a current limit circuit to mitigate the in-rush current in startup phase. This circuit has been designed in AMS C35B4 (0.35um) CMOS process.

The charge pump was designed to provide a maximum load current of 100mA. The peak-to-peak output voltage ripple is less than 20mV with two 3uF flying capacitors and one 22uF output capacitor. Peak and average efficiencies, with maximum load current, are about 75% and 67%, respectively.

Keywords: charge pump, DC-DC converter, self adaptive, digital control, current limiting, load transient, efficiency.

1. INTRODUCTION

In recent years, inductorless switched capacitor DC-DC converters have become more attractive in comparison to typical inductor based DC-DC converters due to their simple control, good cost/efficiency relation, high power density, low EMI and fast development time. A charge pump DC-DC converter is a simple and low cost solution to convert unregulated battery voltage to a constant regulated voltage in integrated circuits. Different conversion ratios can be implemented in a step down charge pump and the efficiency achieved is strongly dependent on the \textit{vout/vin} versus the conversion ratio relation. Limiting the number of external flying capacitors to two, there are four possible modes of operation that correspond to different conversion ratios: 1/3, 1/2, 2/3 and 1/1. The main purpose of this work is to show that, by self adapting the operation mode to the load current and input voltage, charge pumps can exceed inductor based DCDC converters efficiency, especially for light loads, while presenting lower area and lower retargeting costs.

Several methods are used nowadays to regulate output voltage in charge pumps, each with advantages and disadvantages.

Constant frequency control\footnote{[1]} with two sequenced phases of operation is used with a transconductance amplifier that compares the output voltage with a voltage reference and controls the amount of charge injected in the flying capacitors. The output capacitor is charged when the output voltage is too low. This control scheme has a well defined noise frequency spectrum that can be filtered, but has poor efficiency with light loads.

Current mode control\footnote{[2, 3]} can be implemented with a current sensing circuit, usually a series sensing resistor, with large power loss, or with a current sensing transistor in parallel with the power transistor that demands additional circuitry. This kind of control is used with duty cycle close to conversion ratio to achieve low output voltage ripple in high load conditions.

Pulse skipping\footnote{[4]} is used with constant switching frequency and constant duty cycle with charge and discharge modes of operation. The charge pump operates on charge mode when the output voltage drops below a pre-determined threshold voltage, otherwise operates with minimum supply current in discharge mode, where the output capacitor supplies charge to the load. This control method is very good to improve efficiency with light loads and has fast response to load variations but produces high output voltage ripple.
Burst Mode[^5] is a control methodology that, when the load current load is less than a prescribed threshold, the clock is turned on and off for a number of clock cycles that depend on the current absorbed by the load. This method allows high efficiency with light loads but produces high output voltage ripple and high tonal spectrum.

The charge pump presented in this work operates with different fractional ratio modes and has two pulse skipping alternative digital control blocks implemented. These alternative control techniques are discussed and compared regarding their associated costs; achieved efficiency and output voltage ripple with different input voltages and output currents. A soft-start circuit that limits the inrush current at the startup phase is also presented. The only external components required for the charge-pump operation are the two flying and one output capacitor.

The structure of this paper is the following: in section 2 a diagram block is presented with the architecture of the complete system, the fractional modes are presented and the power module and the current limit circuit are explained; section 3 presents the two digital control strategies that self adapt the mode of operation to the input voltage and output current; in section 4 the simulation results of the overall system are presented and section 5 presents the conclusions of the work.

### 2. CHARGE PUMP TOPOLOGY

#### 2.1 System Description

The structure of the charge pump is presented in Figure 1. The digital control uses four digital inputs provided by four different comparators: one that compares Vout with a reference voltage and three comparators that compare 2/3, 1/2 and 1/3 of Vin to the reference voltage, providing the information of which mode is theoretically possible. In fact, the lower mode identified by these comparators may not be possible if the load current is high. Therefore, the control methods presented in section 3 are required to constantly adapt the mode of operation to the input voltage and load current.

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Figure 1. Charge pump topology.
The power module and the two external capacitors implementation of the different modes is discussed in section 2.2. The power switches allow different interconnections between the input voltage, the flying capacitors and the output load, implementing different fractional conversion ratios.

2.2 Power Module and fractional modes of operation

Figure 2 presents the power block structure. It is composed by nine switches with fourteen MOS transistors and with two external flying capacitors.

SW1 and SW3, connecting the flying capacitors to the input voltage were implemented with PMOS power transistors, in order to enable full range operation when Vin is also used to supply the charge pump drivers. Switches that connect flying capacitors terminals to ground were implemented with NMOS transistors, allowing lower area implementation for equivalent RDS resistance. The remaining switches were implemented with NMOS and PMOS transistors in parallel, implementing a low equivalent R during startup and normal operation in all modes.

Since the process used is single well, NMOS transistors have their bulk in a common substrate biased to ground. The n-well of all PMOS transistors could be connected to Vin, however, in transistors where the source is at a lower voltage, body effect rises the threshold and resistive losses increase or the area must be increased. Therefore, the bulk of PMOS transistors was tied to Vin only when this node is always the source or when there is no other node at an higher or identical potential then the source. As a consequence of this analysis, the n-well of SW2 and SW9 PMOS transistors are biased to node B, reducing body effect, and without bulk current.

This power module can be configured to implement four conversion ratios: 1/3, 1/2, 2/3 and 1/1. Each conversion ratio consists in one mode of operation that corresponds to a capacitive division between the input and output voltage. In the first three modes listed, conversion ratios are obtained alternating between two clock phases with different switches configuration. The switches turned on in each phase for each mode of operation are identified in Table 1.
Table 1. Power switches configurations.

<table>
<thead>
<tr>
<th>Ratio</th>
<th>Phase 1</th>
<th>Phase 2</th>
<th>Off</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 / 3</td>
<td>1, 4, 7</td>
<td>2, 6, 8, 9</td>
<td>3, 5</td>
</tr>
<tr>
<td>1 / 2</td>
<td>1, 5</td>
<td>2, 6</td>
<td>3, 4, 7, 8, 9</td>
</tr>
<tr>
<td>2 / 3</td>
<td>1, 3, 5, 8</td>
<td>2, 4, 9</td>
<td>6, 7</td>
</tr>
<tr>
<td>1</td>
<td>Always On : 1, 2, 3, 9</td>
<td>4, 5, 6, 7, 8</td>
<td></td>
</tr>
</tbody>
</table>

Table 2 shows the voltages in the flying capacitors for the switches configurations presented in Table 1 when Iout = 0. Transitions between modes 1/3 and 1/2 have no impact in the flying capacitors voltages. However, since mode 2/3 is the only one with lower voltages in the flying capacitors, when leaving this mode the flying capacitors need to be recharged. The procedure implemented to solve this problem is described in section 3.

<table>
<thead>
<tr>
<th>Mode {cm1 cm0}</th>
<th>Ratio</th>
<th>C1</th>
<th>C2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>1 / 3</td>
<td>Vout</td>
<td>Vout</td>
</tr>
<tr>
<td>0 1</td>
<td>1 / 2</td>
<td>Vout</td>
<td>Vout</td>
</tr>
<tr>
<td>1 0</td>
<td>2 / 3</td>
<td>Vout / 2</td>
<td>Vout / 2</td>
</tr>
<tr>
<td>1 1</td>
<td>1</td>
<td>NC</td>
<td>NC</td>
</tr>
</tbody>
</table>

2.3 Current Limit circuit

In order to limit the Joule power losses, power switches are designed to exhibit low equivalent resistance (nearly 3 Ohm). When the charge pump is powered with the flying capacitors and output capacitor discharged, the current would be in the order of magnitude of amps. In order to limit this inrush current during the startup phase a current limiting circuit was implemented in the power transistors connected to the supply source, sw1 and sw3. This circuit is represented in Figure 3.

Figure 3 shows the schematic of the driver and current limiting circuit for SW1, implemented by MP1, controlled by sw input signal.

MP2, MP3, MP4, MN0 and MN6 implement a sensor of the current in transistor MP1. Since MP1 is in the triode region, MP2 can only mirror its current if both source to drain voltages present similar values. MP3 and MP4 have the purpose to bring the drain of MP2 voltage near the voltage of the MP1 drain. This is accomplished by designing MN0 and MN6 with the same ratio as MP4 and MP3. Therefore, MN0 and MN6 force currents that cause the same gate to source voltages in MP3 and MP4 and since their gate is common; their sources will present similar voltages. The saturation current of MN6 is compared with the current mirrored by MP2 and the input of a voltage amplifier, A, is pulled down or pulled up depending on the relative values of these currents. When MP1 current is lower then the limit, the ratio to MP2 is lower then the current in MN6 and the input of A is pulled down, allowing minimum RDS in MP1. If the current in MP1 exceeds the limit, MP2 pulls up the input of amplifier A and limits the current in MP1. In order to ensure stability, an AC open loop analysis was performed and compensation was added. For cleanness, the corresponding RC components were omitted in Figure 3.

MP39 and R3 slow down the turn off of MP1 by introducing two phases. When sw changes from high to low logic level, turning on MP45, the initial reduction on the VSG of MP1 is helped by MP39. However, when MP1 starts to cut-off, so does MP39 and the second phase of VGS reduction is accomplished by R3 alone, limiting di/dt in the Vin bonding wire and therefore the internal supply voltage peak caused by turning off the input current.
MP43, MP44 and MP45 are used to limit MP1 current in the startup phase. MN3 turns off the reference current when sw turns off MP1 and the current limiting cell is disabled in power down mode, with all current mirrors turned off. MN44 and MP6 short, respectively, to ground and to supply voltage the gates of the idle current mirrors.

3. DIGITAL CONTROL

The major challenges in the fractional charge pump control design are: 1) mode optimization; 2) output voltage ripple minimization and 3) area and power consumption minimization.

Mode optimization has high impact in efficiency since a higher mode, than the minimum required, causes unnecessary Joule losses while transferring charges between capacitors with significantly different voltages. Two control algorithms were implemented and are described in the following subsections. Their criteria for changing modes are different and will be preliminarily evaluated in section 4.

Output ripple needs to be minimized in order to fulfill the purpose of the work: to prove that a charge pump can be a replacement for an inductor based DCDC converter, since the output filter of buck DCDC converters can limit the ripple to a minimum, especially if the output capacitor has low ESR. Both controls implemented use equivalent techniques to minimize output ripple based on omitting Phased 1 (of Table 1) until the charge of the flying capacitors becomes insufficient to recharge Cout.
Area and power minimization is a general concern while designing microelectronic circuits. However, in the design of a DCDC converter, the consumption of the control circuitry has a major height in the efficiency at light loads since the control consumption compares to the load useful power. Therefore, the two controls use two radically different logic styles: synchronous and asynchronous, in order to evaluate the relative impact of the control power consumption. Additionally, the power consumption was minimized at system level by disabling the three comparators on the top of Figure 1 as well as turning off a switch in series with the voltage divider of Vin and enabling this circuitry only when the minimum possible mode needs to be sensed. Therefore, only the output voltage comparator is permanently enabled, and this is a switched comparator that sources less then 1μA.

3.1 Control Design I

Figure 4 presents the block diagram with the functionality of the first control implemented. As shown in Figure 4, the criteria for changing to a mode able to provide higher voltage (“change mode up”) is based on the number of clock cycles with the output voltage below the reference value. The criterion to change to a lower mode has two conditions: if the lower mode is possible and if, after Vout < Vref, Vout recovers to Vout > Vref in one or two clock cycles. A synchronous, 1MHz clock, state machine was designed with this functionality, with the referenced constants made programmable via SPI.

The transition between mode 2/3 and mode 1/2 was treated as a special situation since, as explained in section 2.2, flying capacitors in mode 2/3 present a voltage equal to Vout/2 while in mode 1/2 present voltage Vout. Mode 1/1 was implemented according to Table 1, with the flying capacitors off, and therefore, the transition from mode 2/3 to mode 1/1 was not problematic. When changing from mode 1/2 to mode 2/3 there is no impact on Vout ripple since the excess of charge in the flying capacitors will be delivered progressively to the output capacitor as required by the load. On the
contrary, when changing from mode 2/3 to mode 1/2, the lack of charge in the flying capacitors would cause excessive ripple if Phase 2 of mode 1/2 was forced (see Table 1). Therefore, in order to avoid the excessive output ripple, and to allow the flying capacitors to recover the required charge, the initial W cycles in mode 1/2 instead of Phase 2 will have repeated Phase 1.

### 3.2 Control Design II

The second control block diagram is presented in Figure 5. The criteria to optimize the mode of operation consists on trying the minimum, sensed by the resistive divider of Vin, and if it fails to pump Vout to the required value, after “k” clock cycles, the next mode is used until the required Vout value is achieved. The criterion for getting back to the minimum mode is based on “try and error”: the minimum mode is restores after “m” clock cycles and if it proves to be insufficient (due to the load current), after “k” clock cycles of Vout < Vref, the following mode is restored.

Additionally this control was designed as an asynchronous circuit, minimizing power consumption (only seven registers are used).

![Diagram of control II](image)

**Figure 5. Diagram of control II.**

### 4. RESULTS

#### 4.1 Layout

Figure 6 presents the layout of the analog part of the charge pump. The two digital controls, the SPI interface and a digital multiplexer, for debug purposes, were placed in the center of the test chip, filling an L shape free space between cores [6]. Figure 6 shows the placement of the power devices, current limiting cells and comparators. Since a single well technology was used, a major concern was to limit the substrate noise using the only available way to interrupt the channel stop that reduces significantly the substrate surface resistance: an n-well ring was design around the power devices.
Figure 6. Charge Pump layout.

4.2 Line regulation

![Figure 7 – Modes of operation for control I during a Vi sweep with Iout = 60mA.](image)

Figures 7 and 8 show simulation results for Vref=1.2V when Vin changes from 1.6V to 4.8V with a load of 60mA, for control I and II, respectively. Signals cm0 and cm1 identify the mode of operation accordingly to Table 2. For this output...
current, with control I, mode 1/3 is sustainable for \( \text{Vin} > 4 \text{V} \), mode 1/2 was used for \( 4 \text{V} < \text{Vin} < 2.75 \text{V} \), switching between modes 1/2 and 2/3 occurs when \( 2.75 \text{V} < \text{Vin} < 2.5 \text{V} \), mode 2/3 is selected when \( 2.5 \text{V} < \text{Vin} < 2.25 \text{V} \), switching between modes 2/3 and 1/1 occurs when \( 2.25 \text{V} < \text{Vin} < 2 \text{V} \), mode 1/1 is selected when \( \text{Vin} < 2 \text{V} \). Control II causes similar decisions. Vout ripple caused by control II is higher in Figure 8, when switching between modes 2/3 and 1/1, due to the inclusion of the flying capacitors also in mode 11 in this control. However, this is easily solvable in the test chip since the switching configuration active for each mode is programmable via the SPI interface. As the load current increases, the range of \( \text{Vin} \) when mode 2/3 is stable is significantly reduced and at the maximum current of 100mA, the charge pump does not lock in this mode at all.

**Figure 8 – Modes of operation for control II during a Vi sweep with Iout = 60mA.**

### 4.3 Load regulation and load transient

Figure 9 presents the simulation results for a load transient with \( \text{Vin} = 3 \text{V} \) and an Iout sweep from 0 to 100mA. Mode 1/2 is used in almost all the range of Iout.

Vout spikes in each clock cycle are due to the presence of bonding wires, to a realistic ESR for the output capacitor, to the use of the substrate as the reference point for all voltages in the simulation.

The time between the requirement of Phase 1 is progressively reduced as the output current increases.

Figure 10 shows a load transient with \( \text{Vin} = 2.2 \text{V} \) and a Iout changing from 100mA to 1mA and back to 100mA. It can be seen that initial mode of operation is a toggling between modes 2/3 and 1/1 and when the load current drops the mode 11 is not required. The mode 1/2 is not tried because it is theoretically impossible for a 2.2V input voltage and a 1.2V output voltage.

The current limiting cells activity is clearly seen in Figure 10. While operating in mode 2/3, only one current limiting cell is active and, each time a Phase 1 occurs, the input current is limited to 120mA. While in mode 1/1, two current limiting cells are active and, each time a Phase 1 occurs, the input current is limited to 240mA.

The output voltage does not present any significant drop due to the load transient and the output voltage ripple is lower than 20mV.
Figure 9 – Load transient with $V_{in} = 3V$ and an $I_{out}$ sweep from 1mA to 100mA.

Figure 10 - Load transient for worst line conditions.
4.4 Efficiency results

Figures 11 and 12 show the efficiency obtained by simulations of 500us, with different Vin values, for Iout = 1mA, 10mA and 100mA, for both controls implemented. As previously shown in Figures 7 and 8, both charge pump controls adapt to the input voltage and load condition similarly and therefore they present quite similar efficiencies. Moreover, the simulation of 500us is not enough to obtain an accurate value for the efficiency and therefore it is not clear if the differences between the results are real. The simulation is a very time consuming process and only the silicon (now in the lab) will provide clear conclusions about the usefulness of toggling flying capacitors in Phase 1 or/and Phase 2; optimized values for each constant in the control algorithm and major efficiency differences between control modes. However, the major conclusions can be obtained: efficiencies are always much higher than with a Low Drop-Out (LDO) linear regulator and, for low currents, the most frequent situation for most of the circuits, efficiency is in the same order of magnitude as inductor based DCDC converters.

Figure 11. Efficiency results for control I with Iout = 1mA, 10mA and 100mA.

Figure 12. Efficiency results for control II with Iout = 1mA, 10mA and 100mA.
5. CONCLUSION
A fractional, step-down charge pump was designed and evaluated with the purpose to compare it with the most commonly used DCDC solutions: LDOs and buck DCDC converters. The design targeted a maximum output current of 100mA since this was the expected order of magnitude for which a charge-pump could present advantages over a PFM buck DCDC. The power devices topology was presented and the current limiting cells schematic was analyzed. Two control methods were independently designed that led to identical optimized modes of operation for different input voltages and output currents. Line and load regulation and load transient results were presented showing that this charge-pump adapts very quickly to all possible changes of working conditions, presenting output voltage transients equivalent to the ripple observed for operation under constant conditions – below 20mV for the output capacitor used. Efficiencies are always much higher than with a Low Drop-Out (LDO) linear regulator and, for low currents, the most frequent situation for most of the circuits, efficiency is in the same order of magnitude as inductor based DCDC converters.

6. ACKNOWLEDGMENT
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