A VIDEO CHARGE-PUMP PHASE-LOCKED LOOP WITH LEAKAGE COMPENSATION IN 0.13µm CMOS TECHNOLOGY

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Abstract—In deep sub-micrometer CMOS processes the leakage currents have become an issue in the design of analog integrated circuits. This is due to the thin gate oxide and small subthreshold voltages of transistors. PLLs are not exception, since leakage currents are the main causes of jitter in the output signal of these systems. With the goal of reducing the jitter caused by leakage currents, a new compensation system is proposed, that is based on a conventional video CPLL. The proposed solution is composed by the CPLL’s main and feedback loops, as well as a new compensation loop formed by a CP, an integrated capacitor and an OTA. This compensation loop measures the phase error between the input and feedback signals of the PLL, which is proportional to the value of the leakage currents in the main loop. Next, from the phase error it produces a current that equals the leakage currents, then being injected in the loop filter to reestablish its charge. The new system works with external or integrated loop filter CPLL’s topologies, decreasing its output RMS jitter up to 50 times, when compensating the effects of the leakage currents with a value up to 2.5µA. The proposed system occupies a die area of only 20% more than the original system, when using an external loop filter.

Index Terms— Charge-pump, compensated charge-pump phase-locked loop, phase frequency detector, loop filter, jitter; compensation loop.

I. INTRODUCTION

With the progressive replacement of the old CRT televisions by flat-panel displays, the necessity of analog to digital conversion of RGB signals generated by DVD players, VCRs or PCs it’s a reality.

One of the key elements in these receiver systems is the capacity to extract the synchronism information present in the video signal. From it, they produce (with the help of a Phase-locked loop (PLL)) a high quality and high frequency clock, which is used by the analog-to-digital converters (ADCs) during the conversion of the video signal. These systems must be robust enough due to the usually poor quality of the received signal.

The evolution of deep sub-micrometer CMOS processes has brought many advantages to microelectronic circuits, such as the reduction of power consumption, higher operating frequencies and reduction of die area. However, associated with this ongoing evolution, the effects of the non idealities have equally increased. Namely, the level of leakage currents is now comparable to the operation currents of transistors in weak inversion [1]. In today’s process nodes, the leakages are caused by tunneling charges between the gate and the inversion channel and by sub-threshold current leakages.

The mentioned PLL devices are not immune to the effects of the leakage currents. Indeed, the leakage currents are the main causers of the high jitter observed in PLLs output, which leads to a poor quality of the converted images. Namely, in the top-left corner of the displays, due to the loss of PLL’s synchronism during the vertical back-tracing between images.

The typical implementation of a video PLL consists of a phase frequency detector (PFD), a charge-pump (CP), a passive loop filter, a voltage controlled oscillator (VCO), and a divider which is used in feedback, to clock multiplication. The PLL topology is shown in Fig. 1. This type of PLLs that make use of a PFD and a CP are commonly known as Charge-pump Phase-locked loops (CPLLs).

The loop filter can be external (composed by discrete components) or fully integrated within the Analog-Front-End (AFE) die, where the PLL is implemented. Both types of filter suffer from charge losses due to the mentioned leakage currents. Fig. 2 shows an external loop filter and its connection to the AFE through protection diodes. In this case, the CPLL’s main loop leakage currents are due to leakages through the protection diodes, since the diodes are implemented with transistors. When the loop filter is fully integrated, the leakage currents are verified through its capacitors, since normally large capacitors are used.

In this paper, with the objective of reducing jitter in the

Fig. 1. Block diagram of the CPLL with leakage currents in the main loop.
output signal of the CPLL, a leakage compensation circuit is provided. This circuit works with external or fully integrated loop filters. The proposed compensation system is implemented in a 0,13µm CMOS process technology.

This paper is organized as follows. Section II briefly describes the operation of the existing video CPLLs, its continuous-time steady-state model, and shows the effects of the leakage currents through behavioral models simulations of a CPLL. The proposed system is presented in Section III, where its continuous-time analysis, and large-signal behavioral simulations are made, demonstrating the viability of the new solution. In section IV, the schematics of the compensation system’s building blocks, and how they operate is presented. Finally, in Section V an electric simulation of the proposed system is made, showing its correct convergence when using electric transistors models.

II. CPLL WITH LEAKAGE

The functional block diagram of the CPLL is shown in Fig. 1 along with the state diagram of the PFD. The three state PFD generates Up and Down signals depending on the time (phase) difference between the positive edges of the input and the divider output signals. The CP then converts the digital pulses into an analog current which in turn is converted to a voltage via the passive loop filter network. The resulting control voltage drives the VCO. The negative feedback loop forces the phase/frequency error between the CPLL input and the divider output to zero. Like any other feedback system, a CPLL has to be designed with proper consideration for stability.

The CP adds in, subtracts from, or doesn’t change the charge of the loop filter, in accordance with the PFD output. When only the upper switch of the CP is conducting, a current $I_{CP}$ goes into the filter, increasing the control voltage of the VCO. In the same way, when only the lower switch is conducting, a current $I_{CP}$ comes out of the filter, decreasing the control voltage. When both switches are on or off, the charge on the loop filter shouldn’t change and consequently the control voltage is unaffected, being the CPLL in synchronism.

The loop filter consists of a resistor $R_1$ in series with a capacitor $C_1$. The CP current source and the capacitor $C_1$ form an integrator in the loop, and the resistor provides stability (a zero insertion) by improving the phase margin and hence improving the transient response of the CPLL. However, the resistor causes a ripple of value $I_{CP}R_1$ on the control voltage at the beginning of each PFD pulse. At the end of the pulse, a ripple of equal value occurs in the opposite direction [2], [3]. This ripple modulates the VCO frequency and introduces excessive jitter in the output. To suppress the ripple induced jitter a small capacitor $C_2$ is added in parallel with the $R_1$ and $C_1$ network as shown in Fig. 1, increasing the system order to three. Therefore, the phase degradation due to this pole has to be accounted for by a proper choice of the other loop parameters. Normally, the value of $C_2$ is designed to be one-tenth (or lower) of $C_1$, in order to make its effect negligible in the transient response of the CPLL [4].

A. Small Signal Analysis

Due to the sampling nature of the PFD, the continuous-time analysis of the CPLL is an approximation and can involve a considerable amount of error. However, if the loop bandwidth of the CPLL is about one-tenth of the PDF update frequency (or lower), the mentioned approximation is reasonable [2], [3] and [5].

When the CPLL is in near lock condition, it can be represented in a phase-domain block diagram format as shown in Fig. 3. The combined gain of the PFD along with the CP can be shown to be $I_{CP}2\pi$. The transfer function, $Z(s)$, of the loop filter can be derived using linear analysis and is equal to,

$$
Z(s) = \frac{1}{C_2} \frac{s + \frac{1}{R_1C_2}}{s - \frac{C_1 + C_2}{R_1C_2}}
$$

The VCO is an ideal integrator with gain $K_v$. The open loop transfer function of the CPLL is given by,

$$
LG = \frac{I_{CP}K_v}{2\pi N} \frac{s + \frac{1}{R_1C_1}}{s^2 + \frac{C_1 + C_2}{R_1C_2}}
$$

The loop has a zero and three poles. A Bode plot is shown in Fig. 4, for a given set of loop parameters represented in the figure. A careful look at the Fig. 4 reveals a relatively flat portion of the phase plot where the phase lag due to the third pole nearly cancels the phase lead introduced by the zero. An optimal choice of the capacitor
rate $C_1/C_2$ leads to a phase margin that is relatively immune to process variations. The phase margin in this specific case is 55.1º, as indicated in Fig. 4.

Applying the feedback systems theory leads to the closed loop transfer function given by,

$$
\Phi_s(s) = \frac{1}{s + \frac{1}{R_i C_i} + \frac{1}{s + \frac{1}{2n C_2 N} + \frac{1}{s + \frac{1}{2n R_i C_i C_N}}} + \frac{1}{l_{pK_\nu}}}
$$

confirming that CPLL is a third order system. The frequency response of the system is shown in Fig. 5, where we obtain its loop bandwidth which is about 4 kHz. Knowing that the input signal frequency is 31.5 kHz, the continuous-time analysis is valid, since the loop bandwidth of the PLL is about one-tenth of the PFD update frequency.

### B. Behavioral Simulations

The effects of the leakage currents in the main loop of the CPLL are now verified through behavioral simulations. Using Simulink from MATLAB, the most important CPLL’s blocks functionalities are modeled, taken into account its main non idealities. The CP mismatch, CP leakages and loop filter leakages are emphasized. Such behavioral models provide the advantage of short simulation time without compromising the fundamental functionality of the CPLL architecture, as well as the separate observation of the impacts of the several non idealities. The behavioral simulations loop parameters used are represented in Fig. 5, and the frequency of the system’s input signal is 31.5 kHz.

In Fig. 6 is shown the time progress of the CPLL’s output signal frequency in lock condition, considering the three non idealities mentioned. In this behavioral simulation the value of the loop filter's leakage currents was of 2.5µA, the CP leakages were 0.01% of its nominal current, and CP mismatch was of 2%. Due to the leakage currents in the CPLL’s main loop, the charge on the filter goes down over each period of the input signal. At the end of each period there is a phase/frequency error between the input and feedback signals, which is detected by the PFD that throughout the CP restores the lost charge on the filter. This process induces a pattern jitter in the output signal, which is about 202ps RMS as shown in Fig. 6.

In order to simulate the back-tracing time interval between the images, no input signal is set for the CPLL and the PFD is turned off. The system’s output frequency for this situation in shown in Fig. 7. As we can see in this figure, during the back-tracing time, there is a roughly drop of the output frequency that in real situations can lead the CPLL out of lock. This is due to the loop filter’s charge loss. When the PFD is turned on again, the system transient response may affect the quality of the first converted pixels of each image.

### III. PROPOSED COMPENSATION SYSTEM

The proposed system is based on the CPLL presented in the last section. The new system is composed of a conventional CPLL like the one shown in Fig. 1, in which a compensation
loop that includes a second CP, a third capacitor, and an operational transconductance amplifier (OTA), is added. This can be seen Fig. 8.

As stated in the last section, the mentioned phase/frequency error is proportional to the leakage currents in the main loop, when the CPLL is in steady-state. So the basic principle of the compensation loop is to measure the phase error, and from it, to generate a current that equals the leakage currents, supplying it to the control node of the VCO. Ideally, when the compensation loop’s output current equals the leakage currents, the phase error is zero, and the system becomes stabilized.

Since the phase error information is present at the output signals of the PFD, the leakage compensation loop generates the compensation current using the same Up and Down control signals employed to maintain phase lock. The compensation CP adds charge to and subtracts charge from the third capacitor \( C_{CL} \), based on the relative difference between the compensation and leakage currents. Then the charge on the third capacitor affects the control voltage of the OTA, varying its output current in order to decrease the mentioned current difference.

The third capacitor has to be a low leakage capacitor, so it’s mandatory that it is an integrated capacitor, and it’s desirable to be implemented only in metal layers. As we will see later, in this work, the third capacitor has a capacitance of sixty picofarads, and its implementation is made of six metal layers, occupying 10% of the CPLL area.

### A. Small Signal Analysis

The insertion of the compensation loop into the original CPLL topology has caused changes in its stability. So it’s necessary a proper design of the new system taking into account a reasonable maximum value of the leakage currents (2.5\( \mu \)A) [1], and the above mentioned third capacitor restrictions.

When the proposed system is in near lock condition, it can be represented in a phase-domain block diagram format as shown in Fig. 9. Since the nominal current of the compensation CP may not be equal to the current of the main loop CP, their ratio is expressed as \( 1/\alpha \). The transfer function of the loop filter is \( 1/(sC_{CL}) \), and \( G_{CL} \) represents the transconductance of the OTA. The open loop transfer function of the proposed system is given by,

\[
LG = \frac{l_{c}K_{v}}{2\pi C_{N}} \left( \frac{s+G_{CL}}{s+G_{CL}} \right) \left( \frac{s}{s+C_{1}+C_{2}} \right) \left( \frac{s}{s+C_{1}+C_{2}} \right) \]

Comparing the open loop transfer functions of the original and the proposed system, (2) and (4), we see that the compensation loop has added a new pole at the origin and a new zero at \( G_{CL}/(\alpha C_{CL}) \) [rad]. The basic principle of the new system design is to place the new zero at low frequencies in order for its phase lead to cancel the phase lag due to the third origin pole. Affecting the choice of how low one can place the zero is the fact of the OTA’s transconductance cannot be too small, and \( \alpha \) and \( C_{CL} \) cannot be too great.

A Bode plot is shown in Fig. 10, where we can see that approximately the same phase margin was obtained for the proposed system. The Bode plot was obtained with the parameters indicated in Fig. 10, where the loop filter parameters were changed in order to move the pole introduced by the filter for higher frequencies. This itself causes the phase lead (introduced by the two zeros) to be cancelled later, improving the system’s phase margin. The increment on the main loop CP current is associated with the CPLL loop bandwidth, as we will see next. The transconductance of the OTA is 30\( \mu \)S, which allow a compensation leakage current from -3\( \mu \)A to 3\( \mu \)A, when the input voltage of the OTA varies from 500mV to 700mV.

By applying the feedback systems theory to the proposed system, the closed loop transfer function becomes,

\[
\Phi(s) = \frac{l_{c}K_{v}}{2\pi C_{N} \left( s^4 + s^3 \omega_1 + s^2 \omega_2 + s \omega_3 + \omega_4 \right)} \left( s + \omega_{5} \right) \left( s + \omega_{6} \right) \]

where,

\[
\omega_1 = \frac{1}{R_{C} \omega_0}; \quad \omega_2 = \frac{G_{CL}}{\alpha C_{CL}}; \quad \omega_3 = C_{1} + C_{2} \frac{R_{C}}{C_{CL}}
\]

By integrating the compensation loop in the CPLL, the system becomes of fourth order. The frequency response of the new system along with the response of the original CPLL is shown in Fig. 11. The changes made in the values of the loop filter’s parameters and in the main loop CP

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Fig. 8. Block diagram of the CPLL with the leakage compensation circuit.

Fig. 9. Steady-state phase-domain CPLL block diagram with leakage compensation.
current, allowed the frequency response of the new system to be approximately equal to the response of the original CPLL. Hence, the system maintains the same behavior, while decreasing the jitter in its output signal.

### B. Behavioral Simulations

A new created compensation loop model is added to the original system model, to verify its correct behavior. In addition to the building blocks functionalities, the mismatch of the second CP (10%), its leakage currents (0.01% of the nominal current) and the OTA bandwidth (1MHz), were also modeled.

Fig. 12 shows the time progress of the output signals frequency of the both systems, the original CPLL and the proposed system. In these simulations an input signal frequency of 31.5kHz was applied to both systems, and leakage currents in the loop filter with a value of 2.5µA were modeled. This procedure is similar to the one presented in the last section. Comparing the values of RMS jitter indicated in the Fig. 6 and in Fig. 12, we conclude that the proposed system reduces the effects of leakage currents in the main loop about fifty times. The value of 3.59ps RMS jitter in the output signal of the proposed system is due to the CPs mismatches and to the second CP leakages.

Fig. 13 shows the situation where the input signal of the CPLL is missing and the PFD is turned off to simulate the back-tracing time interval between the images. As seen in the last section, the original CPLL cannot hold on the output frequency in the mentioned interval. The proposed system is able to maintain the control voltage of the VCO, due to the continuous re-establishment of the lost charge in the loop filter. Therefore, the output frequency of the system during the absence of the input signal remains unaffected. In this manner the system transient response at the beginning of each image is almost eliminated, as seen in Fig. 13.

### IV. CP AND OTA TOPOLOGIES

In this section the topologies of the CP and the OTA of the compensation loop are presented, and the way they operate is explained.

#### A. Charge-pump

The charge-pump circuit is a key element in a PLL. Its function is to transfer the digital signals Up and Down from the PFD to an analog signal. In this specific case, the output signal of the charge-pump circuit controls the output current of the compensation loop. When the CPLL locks in some frequency, and the compensation loop locks in some output current, the output voltage of the charge-pump circuit must be held on a constant voltage. Therefore, it’s very important to produce a low mismatch output current, and a stable output voltage in the designing of a charge-pump [6].

The topology of the CP used in this work is shown in
Fig. 14. It is composed of a source \( (I_{up}) \) and a sink \( (I_{dw}) \) current, which are simple CMOS current mirrors. Other type of more advanced current mirrors would bring improvements to the system output jitter, however the limited supply voltage of the technology \( (1,2\, \text{V}) \) restrains one of using them. In fact this limited supply voltage would prevent transistors from operating in saturation.

The CP operates in a tri-state mode as shown in Fig. 1. When the transmission gate PG1 is on and PG2 is off, the load capacitor \( C_{CL} \) is charged by \( I_{up} \) and the voltage \( v_{REP} \) rises. When the transmission gate PG1 is off and PG2 is on, then the load \( C_{CL} \) is discharged by \( I_{dw} \) and \( v_{REP} \) falls. When PG1 and PG2 are both off, no current flows into \( C_{CL} \) and \( v_{REP} \) is held, which means that the CPLL is locked and the output current of the compensation loop is equal to the leakage currents in the CPLL’s main loop. In the ideal case, PG1 and PG2 will never be on at the same time. However, to eliminate the dead zone of the PFD/CP [7], there is a series of short periods in which the two transmission gates are on simultaneously.

The inclusion of the amplifier and the transmission gates PG3 and PG4 in the CP circuit shown, in Fig.14, mitigates the phenomena of charge sharing [8]. Fundamentally the charge sharing is mostly caused by the positions of the transmission gates PG1 and PG2. When they are both off, the voltage at the node X, \( V_X \) is pulled up to \( V_{DD} \), the voltage at the node Y, \( V_Y \) is pulled down to ground and \( v_{REP} \) is floating. In the short periods in which PG1 and PG2 are both on, \( V_X \) will decrease and \( V_Y \) increase, which results in a consequent deviation in the output \( v_{REP} \), due to the charge sharing between \( C_{CL} \) and the parasitic capacitances at nodes X and Y. A conventional solution is to use a unity-gain amplifier to keep the \( V_X \) and \( V_Y \) at the same level equal to \( v_{REP} \) in all states of the CP.

In order to decrease the effects of charge injection [8], transmission gates are used instead of single transistors as switches. This way relevant disturbance in \( v_{REP} \), due to the turning off of the MOS switches is prevented.

Another issue in the CP design is the current mismatch between \( I_{up} \) an \( I_{dw} \). For the proposed CP, the current matching is improved, by enlarging the output impedance of the source and sink currents. However, this method cannot produce perfect current matching characteristics because of the sizable output impedance of practical devices used in the circuit. The authors of [9] propose a CP with perfect current matching characteristics, which can be an option for future works.

B. Operational Transconductance Amplifier

The topology of the OTA used in this work is shown in Fig. 15. It consists of two complementary differential input pairs \( (M1, M2\) and \( M3, M4) \) with two complementary current mirrors (\( M5, M6 \) and \( M7, M8 \)) as active loads. The use of two complementary differential input pairs allows one to obtain a symmetrical OTA’s transcondutance characteristic. Therefore, it’s possible supply or subtract current from the CPLL’s main loop, depending on the direction of the leakage currents.

The OTA’s transcondutance is designed to meet the previous section dimensioned value of \( 30\, \mu \text{S} \). The OTA’s transcondutance is given by the sum of the transcondutances of each differential input pair [10], when the differential input voltage is zero. The extreme limits of the output current are \( \pm(2\times I_{T_{AIL}}) \), being \( I_{T_{AIL}} \) defined as \( 2,5\, \mu \text{A} \), in order to compensate the specified maximum leakage currents of \( 2,5\, \mu \text{A} \), taking into account the worst operation corner.

The input offset voltage of the OTA is not a problem in this case, since this non ideality gives rise to a phase/frequency error that is cancelled by the feedback loop and the PFD. Also the OTA bandwidth it is not a restriction, due to the low frequency of the CPLL’s input signal and, since, once the system has locked, the OTA’s input signal variation is slow.

V. SIMULATION RESULTS

The proposed system was designed using a UMC CMOS 0.13μm technology and simulated with HSIM from Synopsys.

Since PLLs are difficult to simulate because they require a long simulation time, a few modifications in the CPLL topology were made. Thus, the divider was removed from
the feedback loop, and the VCO was substituted by a behavioral model. The gain of the VCO behavioral model was divided by N to maintain the system frequency response, and its free running frequency was defined to be equal to the input frequency of the system. This way, the simulation time is improved, considering the equal input and output frequencies of the system.

In Fig. 16 the simulation results of the proposed system are shown. These were obtained using an input frequency of 100kHz. Also, to reduce the simulation time was used an initial condition of nearly 0,6V for the VCO control voltage, making the system start practically from the locked state. Since the transistors models do not consider its leakage currents, a current source was placed in parallel with the loop filter to model the main loop leakage currents with a value of 2,5µA.

The upper graph of Fig. 16 shows the time progress of the VCO control voltage. It can be seen that the CPLL has locked, since the VCO control voltage has stabilized in 0,6V. The time progress of the compensation loop output current is shown in the lower graph of Fig. 16. The validity of the proposed system is verified, since the mentioned output current converges to the modeled value (2,5µA) of leakage currents, mitigating its jitter effects on CPLL’s output signal.

It is clear from this electric simulation results that the proposed system is stable. The proposed method of producing a compensation current equal to the leakage currents, based on the measurement of the steady-state phase error is then validated.

VI. CONCLUSIONS

The output jitter in a video PLL, due to the leakage currents in its main loop, can be drastically reduced, with low complexity changes on the existent schematic. In this paper, an additional compensation loop was proposed that can be fully integrated within a conventional PLL. The compensation loop is only composed by a second CP, an integrated capacitor and an OTA. The integrated capacitor has to be implemented with metal layers only, since the successful of the proposed solution is dependent of leakage currents through it.

Open loop and closed loop s-domain transfer functions of the entire system are presented, making possible the design of the CPLL’s parameters.

Through s-domain design a new system that has practically the same phase margin and frequency response of the original system was obtained. For that an OTA’s transconductance and a ratio between the two CP’s currents were obtained, and a few changes in the loop filter of a video PLL were made. It was shown through behavioral models that the output jitter of the CPLL, from leakage currents, is mitigated with the addition of the proposed compensation loop.

The implemented system was designed using a UMC CMOS 0,13µm technology. The electric simulation results have shown the successful system lock acquisition, and the correct convergence of the compensation loop output current. The leakage currents modeled in the CPLL’s main loop are then compensated. As future work the system’s average power consumption should be obtained. It would be also interesting changing the CP’s topology to another with perfect current matching, decreasing even more the system’s output jitter.

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