Cyclic ADC with Programmable Resolution and Bias Current Adaptation

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Abstract—These Data conversion is fundamental to many electronic devices seen today. With the ever growing demand for portability and autonomy, it becomes essential to find ways to reduce power consumption and area, in order to decrease costs. Autonomy and cost are vital for the consumer electronics market. For this work an analog to digital converter (ADC) architecture, which tries to embrace this issues is presented and implemented. Cyclic/algorithmic ADCs have a relatively small area due to the existence of only one functional stage. The different cycles of operation are characterized by different bias current, since the precision required changes with the bit on analyses. The ADC has a programmable resolution of 8, 10 or 12 bits and is projected for a 90nm technology from TSMC.

Index Terms—cyclic, algorithmic, analog to digital converter, programmable, current adaptation

I. INTRODUCTION

This paper presents an implementation of a Cyclic ADC with current adaptation. Cyclic ADCs are characterized by their small area and small power consumption. Those characteristics have origin in the existence of a single amplification stage. Such traits have a high impact on today’s World of consumer electronics where they translate on lower prices and larger autonomy. Another helpful element of the architecture is the support for redundancy and digital correction.

The existence of a single amplification stage limits the freedom that the designer has to shape the converter in order to optimize it as the conversion progresses, for instance in this kind of ADC architecture all the extracted bits are obtained using exactly the same hardware although the precision required by the most significant bit is higher that the precision needed for the determination of the least significant. One way of mitigating this shortcoming is changing the value of the current as the conversion advances. This solution is implemented in the work described.

Other ability that the described converter possesses is to operate with three different resolutions (8, 10 and 12 bits).

The present paper organization follows. Section II gives a general description of the way in which the converter operates and the blocks that make it function. In section III the state-machine implemented is presented. Details about the chosen current variation in section IV are given. Section V addresses the results obtained. Section VI is the conclusion of the work.

II. GENERAL DESCRIPTION

The general conversion scheme is presented in Fig. 1. When the conversion process begins the input signal is sampled, afterwards the input voltage value is compared to a set of predefined references. For an ADC without redundancy the referred comparison allows the circuitry to obtain directly one bit of the conversion result, in such circumstances only one comparator would be required making the distinction between positive and negative input values. The constructed ADC uses redundancy, two comparators are used to define three levels being that the middle one (“unknown”) represents a situation in which no suppositions are made about the bit to extract. After this first analyses a “residue” must be generated. A “residue” is nothing more that the initial signal without the analog value of the extracted multiplied in order to maintain to maintain the voltage scale throughout the entire conversion. The block responsible by the referred comparisons is a 1.5 bit flash ADC (sub converter).

Following cycles of operation repeat the described succession of events but with successive “residues” instead of the input signal. The final two bits are obtained simultaneous and without redundancy by means of a 2 bit flash ADC. The...
the correct operation of the converter. First it analyses the input signal and every residue, extracting bits fundamental for scrutiny. Fig. 2 shows the structures that compose the block under architecture follows.

A. S&H/MDAC

The only fully analog block present is responsible for the sampling of the input signal and by the generation of the residue. Both sampling (Sampling & Hold) and residue generation (Multiplying Digital Analog Converter) are characterized as part of the same functional unit because they share the same operational amplifier (opamp). The totally of this block consists of three capacitive nets and the opamp. Of the three nets one is a sampling net and two are multiplying nets. The existence of two MDAC nets allows the duplication of the frequency at which residues are produced and bits are extracted.

All three nets have two phases of operation. For the S&H they are the sampling phase and the holding phase, when considering MDAC’s case the phases are of sampling and of multiplication. The reasons for the existence of a S&H net is the ability to adapt the circuitry when different input voltage references are used. This may be accomplished by changing the relation between the capacitances of the S&H.

B. 1.5 bits Flash ADC

The 1.5 bits Flash ADC has two important contributions for the correct operation of the converter. First it analyses the input signal and every residue, extracting bits fundamental for the generation of the final digital word. The second role played by the 1.5 bits flash is sending to the MDAC the information required for the correct residue creation. The comparisons that take place inside the flash determine the region (high, low, unknown) of the analyzed signal which in turn determines the value to be added. Fig.3 is a representation of the 1.5 flash ADC.

The references used for comparison are of $V_{ref}/8$ and $-V_{ref}/8$ ($V_{ref}$ is the full differential scale that corresponds to 1V). The referred values set the limits of the “unknown” stage. Those limits can not exceed under any circumstances $V_{ref}/4$. If such limit is not respected the circuitry can saturate.

C. Digital Correction

The digital correction is the final step of the conversion process. In fact it takes place when the next conversion is already under way. The correction removes the redundancy introduced by the 1.5 bit flash and produces the final conversion result. It requires all the bits originated by the two flash ADCs. This leads to the need for a structure dedicated to the storage of the digital output. Such structure is an aggregate of shift-registers.

The 2 bit flash ADC sends three bits codified in thermometer to the digital correction. Those bits are codified to binary, being that the least significant flows directly to the exit and the most significant gives start to the redundancy elimination.

The 1.5 bit flash ADC supplies the digital correction with two bits from each cycle it operates. The codification with which they arrive is such that the most significant bit is only ‘1’ when a “high” is detected and the least significant is only ‘1’ when an “unknown” occurs. The pairs of bits from the 1.5 bits flash are received by a structure that also receives a “carry” bit from a previous similar structure or from the decoding of the bits received from the 2bit flash.

The most significant bit with origin in any of the 1.5 bit comparisons, if ‘1’, will always result in the structure’s carry bit being activated (‘1’), if this bit is ‘0’ it has no influence to the output.

The least significant bit from the 1.5 bit flash is added with a carry bit, such operation removes the redundancy, if the bit is ‘1’ an ‘1’ carry value leads to the conclusion that the value should have been “high” if no redundancy was present. The circuitry responds by putting the carry bit of the structure with value ‘1’.

The behavior described results from the fact that most significant bit of the conversion result being associated with the value of the output carry generated by the block that
receives the bits from the first analyses conducted by the 1.5 bit flash ADC.

In Fig. 4 a schematic of the digital block is shown.

![Fig. 4 Digital Correction Block [1]](image)

This block also contains registers that safe keep the final result during a full conversion cycle.

### III. STATE-MACHINE

The cyclic nature of the ADC requires the knowledge of the current situation of the conversion. This is particularly relevant due to the existence of two different MDAC nets, of resolution control and the ability to change the bias current supplied as the cycles pass.

Fig. 5 shows the implemented state-machine. Each stage last for a clock cycle, during such cycle two different phases of MDAC operation happen and two conversions are done by the 1.5 bit flash ADC.

![Fig. 5 State-Machine [1]](image)

The functional behavior of the converter is the same for most states. Only the final and the first states present differences. During the last state the 2 bits flash ADC is activated. During the first state the S&H is connected to the amplifier and one of the MDAC nets is brought offline and the exit of the ADC is updated. Also during the first phase of the first cycle the opamp suffers a reset by means of short-circuit of the output nodes.

During the remaining cycles both MDAC are active.

The answer of the state machine to programmable resolution ability is the existence of three separate states that can be associated with the first conversion cycle. When the maximum resolution is selected all states are active and St1 is active when the conversion begins. When lower resolutions are selected the first states are turned off, in effect is like the state machine has less states.

The existence of individual states for each cycle is important for the current scaling.

### IV. CURRENT SCALING

One of the more important aspects the ADC is its ability to adapt the supplied current as the need for precision decreases.

The determination of the correct current adaptation to be made was done by means of several simulations done to the S&H/MDAC with different bias current values. In which simulation the minimum precision obtained was recorded.

Finally, after resorting to a script that receives the precision values and simulates the abilities of the converter, the scaling presented on Fig. 6 was achieved.

![Fig. 6 Current Scaling](image)

The presented scaling doesn’t have data correspondent to the first stage of conversion when 12 bits of resolution is selected. This is due to the inability of the used opamp to reach enough precision to allow the ADC to reliably operate at resolutions of 12 bits. Given this, the state that is only used when maximum resolution is selected provides 100% (120µA) bias current. The indicated percentages relate to the maximum current that the used current source (imirror) is able to supply.

By comparing the medium bias current with the constant current that would be supplied if no scaling was conducted the current gains obtained are of 24% for 10 bit resolution and of 12.5% for a resolution of 8 bits.

### V. RESULTS

In order to demonstrate that the validity of the solutions taken some simulations where conducted. These simulations did not include the digital correction block. In order to accommodate this a program written in C was used. The program follows the hardware morphology present in the correction block.

![Fig. 7 ADC response to a ramp](image)

The graphic presented in Fig.7 is a sobreposition of the results obtained by the program and the values taken during the sampling stage. Eighty-Six samples where taken which means that exist a lapse between samples of about 12mV. The
maximum error obtained was 1 LSB.

VI. CONCLUSION

The ADC was able to operate with a working frequency of 60 MHz. In terms of sample frequency it operates with 15 MS/s, 12 MS/s or 10 MS/s, depending on the frequency selected.

There are several aspects that can be improved namely the use of a more capable amplifier so that the full spectrum of resolutions becomes viable. Other issue is the introduction of multiple aggregates in the S&H net so that the circuit could operate with several input tensions without redesign.

REFERENCES