A CAPACITOR-LESS LOW DROPOUT VOLTAGE REGULATOR FOR SMALL ANALOG CORES

Alexandre Henrique Rodrigues Neves

Dissertação para obtenção do Grau de Mestre em Engenharia Electrotécnica e de Computadores

Júri

Presidente: Prof. José António Beltran Gerald
Orientador: Prof. Marcelino Bicho dos Santos
Co-Orientador: Prof. Maria Beatriz Mendes Batalha Vieira Vieira Borges
Vogal: Prof. Maria João Marques Coelho Carrilho do Rosário

Outubro de 2007
I wish to acknowledge my gratitude to all those who helped and supported me in this journey. Firstly I would like to thank professor Marcelino Santos and professor Maria Beatriz Borges that supervised my work for their thoughtful guidance and advice, for expressing their confidence in my abilities and encouraging me all the way. I also would like to thank professor Júlio Paisana for his concern and availability.

I am specially grateful to the members of Chipidea®, especially to Floriberto Lima who with his vast experience and kindness supported me in every moment, to Gabriel and Daniel who were always available to give me advice and the needed support, and all the others that helped me during this work.

The accomplishment of this work also signify the end of the 5 five years of intense work, for that I would like to thank all the friends and colleagues. With who I have spent lots of hours of great work, sad moments, but also victories and joys.

Finally but not least important, I would to thank my whole family for their education, advice, support and tolerance. Not forgetting anyone, would like to give special thanks to my mom, dad, sister, grandmother Ofélia and cousins Nuno, Rute and Paulo. Without them I would never reach this far.

To everyone my most sincere gratitude,

Alexandre Henrique Rodrigues Neves
Lisbon, Portugal
October, 2007
Abstract

The presented research provides a solution to the present days needs in the integrated low power regulation field, for mobile applications. Several topologies are presented in order to compose a new low current capacitor-less LDO regulator. Less capacitance, lower current ($I_{\text{Load max}} = 1$ mA) and lower output voltage (1.55 V) allows the mobile devices to become smaller and more autonomous. The regulator is designed in SMIC 0.13 $\mu$m CMOS technology, consuming only 96 $\mu$A of ground current with a dropout voltage of 150 mV. Simulated results show that the proposed capacitor-less LDO achieves the expected specifications. The architecture appears to be robust to the process variations and the load conditions. Thus, the presented capacitor-less LDO voltage regulator is designed for system-on-chip (SoC) solutions.

**Index Terms:** LDO Voltage Regulator, Capacitor Less, Mobile Devices, Low Output Voltage and Current, SoC.
Resumo Analítico

A investigação desenvolvida neste trabalho contribui com uma solução, no campo da regulação de baixa tensão, para aplicação a dispositivos móveis. Várias topologias são apresentadas, compondo o regulador de tensão sem condensador de saída. Menos capacidade, menor corrente ($I_{\text{Load max}} = 1$ mA) e menor tensão de saída (1.55 V) permitem reduzir as dimensões dos dispositivos móveis bem aumentar a sua autonomia. O regulador foi desenhado com recurso à tecnologia SMIC 0.13 µm CMOS, apresentando um consumo total de 96 µA com margem de regulação (dropout) de 150 mV. Os resultados de simulação mostram que o regulador cumpre as especificações previstas. A arquitectura aperenta ser robusta às variações de processo de fabrico e a variações de carga. O regulador, sem condensador de saída, desenvolvido insere-se no âmbito dos sistemas integrados analógicos.

**Palavras-chave:** Regulador baixa de tensão, Sem condensador de saída, Dispositivos móveis, Circuitos integrados, Baixa tensão e corrente de saída.
# Table of Contents

Acknowledgements .................................................. i

Abstract ....................................................................... iii

Resumo Analítico ....................................................... v

Table of Contents ........................................................ vii

List of Figures ................................................................ x

List of Tables ................................................................ 1

1 Introduction ................................................................. 3
   1.1 Power Management Unit (PMU) ............................... 3
      1.1.1 DC-DC converter ........................................... 3
   1.2 Low Drop Out (LDO) Regulator ............................... 4
   1.3 Objectives and Specifications .................................. 5
   1.4 Structure of the work ............................................. 5

2 Conventional PMOS LDOs Regulators ....................... 7
   2.1 PMOS LDO Regulator Characterization .................... 9
   2.2 State of the art .................................................... 12

3 The new PMOS LDO topology ..................................... 13
   3.1 The Core circuit .................................................. 13
   3.2 Improving the LDO .............................................. 14
   3.3 Shunt regulation .................................................. 15
   3.4 Faster feedback loop ............................................ 16
   3.5 Amplifying the Reference Voltage ......................... 17

4 LDO Design ............................................................... 21
   4.1 Transistors Parameters .......................................... 21
   4.2 Schematic Design ................................................ 21
      4.2.1 Pass Transistor Design ................................... 22
      4.2.2 Design Criteria ............................................. 24
   4.3 Layout ............................................................... 25
<table>
<thead>
<tr>
<th>Chapter</th>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>Results</td>
<td></td>
</tr>
<tr>
<td>5.1</td>
<td>AC analysis</td>
<td>29</td>
</tr>
<tr>
<td>5.2</td>
<td>Transient Analysis</td>
<td>33</td>
</tr>
<tr>
<td>5.2.1</td>
<td>Power up and down Analysis</td>
<td>34</td>
</tr>
<tr>
<td>5.3</td>
<td>Steady-state Parameters</td>
<td>34</td>
</tr>
<tr>
<td>5.4</td>
<td>PSRR Analysis</td>
<td>34</td>
</tr>
<tr>
<td>5.5</td>
<td>Monte Carlo Simulations</td>
<td>35</td>
</tr>
<tr>
<td>6</td>
<td>Conclusions</td>
<td>47</td>
</tr>
<tr>
<td>6.1</td>
<td>Future Work</td>
<td>48</td>
</tr>
</tbody>
</table>

Bibliography | 49 |

Appendix | |
| A | LDO Schematic | 51 |
| B | Test Benches | 53 |
List of Figures

1.1 Typical Power management Unit............................................ 4
1.2 Topologies of Buck and Boost converters............................... 4
1.3 High efficiency linear regulation........................................ 5

2.1 PMOS voltage regulator topology....................................... 7
2.2 Pole locations of the PMOS voltage regulator.......................... 8
2.3 PMOS voltage regulator topology with output capacitor.............. 8
2.4 Pole locations of the PMOS voltage regulator with output capacitor.. 9
2.5 LDO feedback loop..................................................... 10

3.1 The core of the new PMOS LDO topology............................... 13
3.2 The improved PMOS LDO topology...................................... 15
3.3 Shunt circuit............................................................ 16
3.4 Example of the shunt circuit functionality............................ 17
3.5 Circuit of the fast loop................................................ 18
3.6 The transconductance opamp.......................................... 19
3.7 The non-inverting topology............................................ 20

4.1 Circuit used to extract the transistors parameters.................... 21
4.2 Final LDO circuit....................................................... 22
4.3 Pass transistor design................................................ 23
4.4 LDO layout............................................................ 26
4.5 LDO differential pair design.......................................... 27

5.1 LDO block diagram..................................................... 30
5.2 Parasitic feedbacks...................................................... 31
5.3 AC open loop analysis with full load.................................. 31
5.4 AC open loop analysis without load.................................. 32
5.5 Transient analysis in all 64 corners.................................. 36
5.6 Power up analysis...................................................... 37
5.7 Power down analysis.................................................. 38
5.8 Consumption analysis................................................ 39
5.9 Line regulation with full load........................................ 40
5.10 Load regulation....................................................... 41
5.11 PSRR analysis without load.......................................... 42
5.12 PSRR analysis with load............................................ 43
## List of Tables

1.1 Overall specifications. .......................... 6
4.1 Transistor Parameters. ....................... 22
4.2 Transistor Parameters. ....................... 24
5.1 Simulated Corners. ............................ 29
5.2 Simulated Poles and Zeros Location. .......... 33
6.1 Final Results. ................................. 47
In these times technology develops every day, we can see that in all types of gadgets that surround us. This evolution is especially noticed in mobile devices like cellular phones, PDAs, MP3 players, GPS, and all kind of devices that have a chip inside. Each new model tends to be smaller than the previous version and more complete (with more features). This evolution is due to the miniaturization/integration of the technology and to the increase of complexity in electronic circuits. Consequently this two factors bring a new challenge: the autonomy of the gadget. Therefore, power-management-units (PMU) need to be more efficient than ever and integrated circuits (ICs) to power regulation and management have become one of the fastest growing segments of the electronic industry.

1.1 Power Management Unit (PMU)

Every electronic device needs a power-source to work. In mobile devices this source is the battery. The battery management is very important since it is the good use of the battery energy that allows the devices to become more and more autonomous. Therefore, when designing a circuit, the designer needs to target the maximum efficiency. The power management unit is responsible for a balanced distribution of energy according to the consumption of the further circuits and the state of operation (e.g. the devices need less power when they are in the stand by mode). A PMU is composed by three types of systems: DC-DC converters and two types of LDOs (Low Drop Out Regulators), Analog and Digital, as shown in Figure 1.1.

1.1.1 DC-DC converter

DC-DC converters convert one DC voltage into another DC voltage. Usually, in mobile devices, the main DC input is a Lithium ion battery that supplies 2.75V to 4.25V. Essentially, there are two types of DC-DC converters: Buck, with the output voltage lower than the input voltage and Boost, with the output voltage higher than the input voltage. The topology of this two converters is shown in Figure 1.2.

This type of converters are also called switched converters. Their principle is based on the transfer of the energy stored in a storage element (the inductor). Linear converters, such as LDOs, are based on a dissipative element (pass transistor). That is why switched converters reach much higher levels of efficiency, near 100%.
1.2 Low Drop Out (LDO) Regulator

The purpose of using a voltage regulator is to regulate (as the name suggests) the output voltage, independently of the operation state of the circuits supplied by the LDO. In other words, a LDO is a voltage source which maintains the voltage level of a rail constant during the battery discharge and load variations. The LDO response time to load variations is very important, not only to lower the consumption, but also to ensure the fast response of the device to the user needs. Circuits that are not performing tasks are temporarily turned off, lowering the overall power consumption. When the circuits need to perform tasks they must be powered up quickly. This kind of circuits are ideal for many applications, particularly to mobile devices not only because of the small difference of drop out (Vin-Vout), but also because of their low noise characteristics, small size and complexity. For low power applications, linear regulators are preferred, not only because of their efficiency, but also due to the lower cost and lower quiescent currents.

In modern PMU the LDOs are used as post regulators. The DC-DC converters are used to
1.3. OBJECTIVES AND SPECIFICATIONS

convert one voltage level into a lower one because of their high efficiency. The main problem of not using only the DC-DC converter is the ripple in the output voltage. So, in order to remove this ripple and load variations, a LDO is used after the DC-DC converter. The DC-DC regulator is designed to minimize the voltage drop across the linear regulator during loading conditions, as shown in Figure 1.3.

![Figure 1.3: High efficiency linear regulation.](image)

Figure 1.3 illustrates that the LDO has two inputs, one is $V_{in}$ and the other is $V_{ref}$. The last one is the voltage reference to the regulation of the LDO, which is provided by the bandgap circuit. This reference voltage is very stable, independently of the temperature. The problem is to supply the current that the load needs and also the load variations that occur during the work of the device. Therefore, a regulator is used to regulate the voltage provided by the DC-DC converter (which is connected to the battery).

1.3 Objectives and Specifications

Table 1.1 describes the overall specifications of the PMOS LDO proposed in this thesis. The design variables such as consumption, loop gain and output capacitor are chosen to improve the performance of the LDO versus the implicit trade offs.

1.4 Structure of the work

This thesis is organized as follows: In Chapter 2 the conventional LDO’s topologies and the state of the art are presented. The new architecture of the PMOS LDO is presented in Chapter 3 stage by stage. Chapter 4 describes the designing of the LDO taking into account the specifications and also includes the circuit final layout. In Chapter 5 the simulated results are presented. Finally, in Chapter 6 the conclusions and the future work are presented.
### Table 1.1: Overall specifications.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vin</td>
<td>Supply voltage</td>
<td>1.7</td>
<td>2.65</td>
<td>3.7</td>
<td>V</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>-40</td>
<td>25</td>
<td>125</td>
<td>deg</td>
<td></td>
</tr>
<tr>
<td>Vref</td>
<td>Reference Voltage</td>
<td>-0.775</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Ibias</td>
<td>Bias Current</td>
<td>0.4</td>
<td>0.5</td>
<td>0.6</td>
<td>µA</td>
</tr>
<tr>
<td>Vout</td>
<td>Output Voltage</td>
<td>1.47</td>
<td>1.55</td>
<td>1.63</td>
<td>V</td>
</tr>
<tr>
<td>Iout</td>
<td>Output Current</td>
<td>0.005</td>
<td>-</td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td>Itot</td>
<td>Current Consumption</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>µA</td>
</tr>
<tr>
<td>Area</td>
<td>Total core area</td>
<td>0.03</td>
<td>mm²</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Most of the conventional LDOs are PMOS LDOs. The LDO regulator uses a single transistor in common-source configuration operating in the saturation region. The topology of this kind of LDOs is shown in Figure 2.1.

This topology consists of a PMOS transistor, controlled by an error amplifier which compares the voltage reference with the output voltage sensed through the feedback resistors $R_1$ and $R_2$. The error signal controls the gate of the pass transistor and forms the negative feedback loop. A typical frequency response of this topology is shown in Figure 2.2. Analyzing Figure 2.2 we can see two poles. The first one, $P_1$, is the dominant pole created by the error amplifier. The second, $P_2$, moves with the load at higher frequencies.

The most important challenge for this circuit is to keep the pass transistor always in the saturation region, in order to operate properly. Maintaining the pass transistor in the saturation region becomes hard with the topology presented in Figure 2.1 due to significant variations of the load. These variations move the pole $P_2$ and can lead the LDO to become unstable. In order to minimize this problem a large, internal or external, capacitor in the output node is used. This compensation circuit is shown in Figure 2.3.
The output capacitor, $C_{\text{out}}$, and equivalent series resistance, ESR, pair creates a zero, $Z_1$, and a pole, $P_3$, as we can see in Figure 2.4. The idea of this type of compensation is to insert the zero $Z_1$ very close to pole $P_2$, adding phase to reach stability. In this topology the stability key of the circuit is the value of the ESR. When the ESR is decreased, the location of $Z_1$ moves to the right and has no effect on the phase margin. When the ESR is increased, the pole $P_3$ moves below the gain-bandwith and the circuit becomes unstable.

Face to this, the purpose of this thesis is to present alternative solutions to the use of the large output capacitor. The output capacitor will have the minimum capacitance, so we will explore more than one typical error amplifier feedback loop topology.
2.1 PMOS LDO Regulator Characterization

Ideally LDO voltage regulators have constant output voltage, regardless of their voltage supplier normal discharge or the load variations. There are three categories of specifications for voltage regulators: static-state specifications, dynamic-state specifications, and high-frequency specifications.

- Static-state Specifications

The static-state parameters include the line regulation, the load regulations and the temperature coefficient effects. The line regulation defines the ratio of output voltage deviation to a given input voltage maintaining a constant load. This quantity reflects the relative deviation after the regulator has reached a steady-state. A general line regulation equation is given by equation 2.1.

\[
\frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} \approx \frac{g_{mp} r_{op}}{A \beta} + \frac{1}{\beta} \left( \frac{\Delta V_{\text{ref}}}{\Delta V_{\text{in}}} \right)
\]  

(2.1)

Analyzing equation 2.1, line regulation depends on the pass transistor transconductance, \(g_{mp}\), the LDO output resistance, \(r_{op}\), the LDO loop gain (\(A \beta\)) and the feedback gain, \(\beta\). Figure 2.5 shows the LDO feedback loop and the respective parameters.

A small output voltage deviation for a given DC change in the input voltage, corresponds to a better voltage regulator. To increase the line regulation, the LDO regulator must have a large loop gain.

Load regulation is a measure of output voltage deviation during no-load and full-load current conditions, maintaining a constant input voltage. The load regulation is related to the loop
gain, $A\beta$, and the pass transistor output impedance, $r_{op}$. This relation is given in equation 2.2.

\[
LR_{load} = \frac{\Delta V_O}{\Delta I_O} = \frac{r_{op}}{1 + A\beta} \tag{2.2}
\]

The load regulation improves as the loop-gain increases and the output resistance decreases. The load regulation only applies to the LDO regulator in steady-state conditions and does not include load transient effects.

The temperature coefficient defines the output voltage variation due to temperature drift of the reference and the input offset voltage of the error amplifier. The temperature coefficient is given in equation 2.3.

\[
TC = \frac{1}{V_{out}} \frac{\delta V_{out}}{\delta Temp} \approx \frac{1}{V_{out}} \frac{\Delta V_{TC}}{\Delta Temp} = \frac{[\Delta V_{TCref} + \Delta V_{TCvos}]}{V_{out}^2} \frac{V_{out}}{V_{ref}} \frac{\Delta V_{ref}}{\Delta Temp} \tag{2.3}
\]

The output voltage regulation improves as the error amplifier offset voltage is reduced and the reference voltage temperature dependence is minimized.

The LDO regulator’s dropout voltage determines the maximum allowable current and the minimum supply voltage. The following specifications, such as dropout voltage, maximum load current and minimum supply voltage, all depend on the pass transistor parameters. A particular LDO design typically specifies the maximum load current and the minimum supply voltage to operate properly, i.e. maintaining the pass transistor in the saturation region. Equation 2.4 relates the LDO dropout voltage to the device parameters were $I_{LOAD}$ represents the maximum sustainable output current.
2.1. PMOS LDO REGULATOR CHARACTERIZATION

\[ V_{\text{dropout}} = I_{\text{load}} R_{\text{on}} = V_{DSat,PMOS} \]  

The pass transistor dimensions are designed to obtain the desired \( V_{DSat} \) at the maximum load current, \( I_{\text{load}} \).

- Dynamic-state

The LDO regulator’s dynamic-state specifications determines the LDO regulator’s capability to regulate the output voltage during load and line transient conditions. The LDO regulator must respond quickly to transients in order to reduce variations in output voltage.

- High-frequency

Power-supply-rejection-ratio (PSRR) defines the LDO regulator’s ability to reject high-frequency noise on the input line. PSRR is a function of the pass transistor parasitic capacitances and is proportional to the reciprocal loop gain. The error amplifier plays a major role in improving the PSRR (that is the reason why it is supplied by the output voltage, \( V_{\text{out}} \) instead of the input voltage \( V_{\text{in}} \)). The combined individual error amplifier PSRR and the individual pass transistor PSRR is desired to sum to zero at the output voltage node. The design techniques to minimize the PSRR are studied later on in the text.

- LDO Regulator’s Efficiency

The LDO regulator efficiency is determined by three parameters: ground current, load current, and pass transistor voltage drop. The total no-load quiescent current consumption for the entire LDO regulator circuitry is defined as the ground current. Equation (2.5) relates the LDO regulator power efficiency.

\[
\text{Eff} = \frac{V_{\text{out}} I_{\text{LOAD}}}{V_{\text{in}} (I_{GND} + I_{\text{LOAD}})}
\]  

There are two cases for power efficiency, one for small load currents and one for large load currents. The relation reduces to equation (2.6) for small load currents.

\[
\text{Eff} = \frac{I_{\text{LOAD}}}{(I_{GND} + I_{\text{LOAD}})}
\]  

Thus, ground current affects the LDO regulator efficiency much more at very low load currents. The longevity of battery life for low current applications can be significantly increased by reducing the quiescent ground current. At the other extreme, for very large load currents, the power efficiency is solely dependent on the pass transistor voltage drop, shown in equation (2.7).
\[ \text{Eff} \approx \frac{V_{\text{out}}}{V_{\text{in}}} \]  

(2.7)

The efficiency of the linear regulator approaches 100% as the output voltage approaches the input voltage. This scenario, however, requires a large pass transistor and would result in a large gate capacitance. Clearly, there is a tradeoff between consumption and speed of the LDO regulator.

- Specifications Trade-offs

All the LDO regulator’s specifications are interrelated and lead to important tradeoffs. The largest among all the other specifications is efficiency, stability, and transient response. The optimization, especially with tight constrains, becomes very convoluted. The tradeoffs will be more apparent when designing the LDO regulator.

### 2.2 State of the art

The development of technology leads to a higher integration capability but with lower supply voltages. On the other hand, the autonomy of portable equipment depends on lower consumptions. Those are the reasons why the LDO proposed on this thesis has lower output voltage and a lower output current comparing with earlier LDOs developed in other technologies as the [3]. Additionally, there is another concern that is the fast response of the regulator, due to the fast load variations. This concern leads us to the search for new approaches to improve the transient response as the shunt regulation, presented in reference [2], but never forgetting the stability problems associated to this type of circuits [6] and the PSRR [1]. It is hard to refer a state of the art for this kind of circuits due to the applications’ (technology and output specifications) needs, as they create different goals in permanent evolution. However, the references presented in this section are good markers for global performance of today’s LDOs.
3.1 The Core circuit

The core of the new LDO is presented in this chapter. Figure 3.1 shows the basic topology. In this coarse representation, the circuit was simplified in order to explain the basic functionality. Alike the typical LDO topology there is a passive element: the pass transistor (M87 of Figure 3.1). This transistor operates in the saturation region; the current that flows through this transistor can be approximated by equation \(3.1\).

\[
I_D = \frac{1}{2} \frac{W}{L} \mu C_{ox} (V_t - V_{sg})^2
\]  

(3.1)

The current is distributed between the load (if any load is connected to the LDO) and the transistor MP2, as shown in Figure 3.1. The transistor MP2, like the M87, operates in the saturation region. The gate of MP2 is set to the reference voltage provided by the Band-gap (the voltage value that the LDO regulates). MP2 transistor operates like a comparator because the drain current that flows through this transistor \(I_1\) has dependency with \(v_{sg} = V_{out} - V_{ref} \) (v_{sg} = V_{out} - V_{ref}). The transistor
MP78 acts like current source and an active load, providing the current $I_2$. Current source $IC_2$ has a static value of current $I_t$ which is the result of sum $I_1$ with $I_2$.

After the presentation of each component that composes this circuit, it will be now explained how the LDO regulates the output voltage. Like in the typical LDO, the comparator closes the feedback loop. As referred earlier, MP2 regulates the amount of current, $I_1$ depending on the load variations, that will be summed with $I_2$ is forced by MP2 and $IC_2$ to $I_2 = I_t - I_1$. Theoretically it is easy to show the $V_{out}$ independence of $R_L$. In equation 3.2 $V_{out}$ depends only on constants and on $I_1$.

$$I_1 = k_{\mu p}2(V_{out} - V_{ref1} - V_t)^2$$

However this current is the difference between two constant currents ($I_1 = I_2 - I_t$). Therefore, $V_{out}$ is defined by equation 3.3.

$$I_2 - I_t = k_{\mu p}2(V_{out} - V_{ref1} - V_t)^2$$

For variations of the load $R_L$ MP78 acts like an active load which means that the voltage gate of the pass transistor $v_{gs}$ is controlled by the variations of the current $I_2$. Therefore, the current that flows through the pass transistor is controlled by $I_2$ which in turn is controlled by $I_1$ ($I_t$ has a constant value which allows $I_1$ control $I_2$).

Now taking the example of a load change, from full load to the absence of load. This situation will produce a $V_{out}$ increase, consequently $I_1$ will increase due $v_{SG} = v_{OUT} - v_{REF1}$ of MP2. When $I_1$ increases, $I_2$ will decrease, making the voltage in the gate ($v_g$) of the pass transistor higher (this is because, M78 acts like an active load). If $v_G$ becomes higher, the $v_{SG}$ of the pass transistor becomes lower and the drain current also becomes lower. The current that flows through the pass transistor regulates the current $I_1$ to a lower value and consequently lowers the output voltage as required.

Now the opposite situation: from no load to a situation of full load. This change of load will produce a $V_{out}$ decrease, consequently, $I_1$ will decrease due to the $v_{SG} = v_{OUT} - v_{REF1}$ of MP2. So if $I_1$ decreases, $I_2$ will increase making the voltage in the gate ($v_g$) of the pass transistor lower (once again M78 acts like an active load). If $v_G$ becomes lower the $v_{SG}$ of the pass transistor becomes higher making the current that flows through it higher, regulating the current $I_1$ to a higher value and consequently increases output voltage the required voltage.

### 3.2 Improving the LDO

In the previous section it was presented the concept of the new topology. In this section new components are added to the basic circuit, to improve it and to allow the integrated implementation. In Figure 3.2 the changes are presented, introducing three new elements.
3.3. SHUNT REGULATION

Analyzing Figure 3.2 we can see a cascode transistor M127. This transistor maintains the voltage in the gate of the pass transistor at a level which keeps the pass transistor, always in the saturation region. MP5 is needed so that the $V_{out}$ dependency on $V_{ref}$ becomes independent of the $V_t$ of PMOS transistors. The $C_{out}$ is used to keep $V_{out}$ steady for high frequency load variations. If the load connected to LDO increases, $C_{out}$ discharges to the load in order to keep the $V_{out}$ steady.

![Figure 3.2: The improved PMOS LDO topology.](image)

3.3 Shunt regulation

In order to improve the transient response of the LDO during load variations, a new configuration of shunt regulation is proposed. As shown in Figure 3.3, the shunt transistor, M109, is driven by the sense transistor, M110, if there is a peak of current M108 is the active load of M110. M106 and 107 just act as a voltage divider to bias the gate of M110. The current mirror (M73, M74, M70 and M102, controlled by M99), allow to reduce the sensibility of this shunt regulation for higher load currents. If $v_{gs}$ of M87 and M99 increases due to a larger current consumption in the load, M108 will reduce the $v_{gs}$ of M109 reducing the shunt regulation influence in $V_{out}$. When needed, the source of M110 is pulled up by $V_{out}$, $v_{gs}$ of M109 increases and M109 drains the excess of charge, reaching the voltage and current stability faster. This occurs when the load
that is connected to the LDO is suddenly disconnected, creating a peak of current as illustrated in Figure 3.4. Analyzing this figure we can see on the top of the load variation between 1mA and 5µA, with rise and fall time of 2.5µs. The transient analysis in the middle presents the LDO output voltage without the shunt circuit. The bottom transient analysis shows the LDO output voltage with the shunt circuit active. Comparing the simulations, significant differences can be noticed, such as the peak levels that are lower with the shunt circuit. Additionally, the shunt circuit removes the oscillation that occurs after load variations, which means that the LDO gains phase margin (becomes more stable) with the shunt circuit.

![Figure 3.3: Shunt circuit.](image)

### 3.4 Faster feedback loop

This additional feedback loop makes the response of the LDO faster. The topology of this loop is shown in Figure 3.5. This loop controls the current that flows through the current mirror (M130, M80, M120 and M100) which provides $I_2$ the current in the active load (current mirror composed by M77 and M78). The work of this subcircuit is quite simple. This fast path makes the current $I_2$ lower or higher according to the current peaks due to load variations, controlling the pass transistor, M87, before the response of the main loop.
3.5 Amplifying the Reference Voltage

The voltage provided by the bandgap ($V_{\text{ref}}$) has half the value of the output voltage ($V_{\text{out}}$). Therefore, the reference voltage needs to be amplified. As shown in Figure 3.6, a transconductance amplifier is used for this purpose.

The amplification topology used is the non-inverting, as shown in Figure 3.7.
CHAPTER 3. THE NEW PMOS LDO TOPOLOGY

Figure 3.5: Circuit of the fast loop

The equations of this topology are:

\[
\begin{align*}
V_- &= \frac{R_1}{R_1 + R_2} V_{out} \\
V_+ &= V_{in} \\
V_{in} &= \frac{R_1}{R_1 + R_2} V_{out} \\
V_{out} &= \frac{V_{in}}{1 + \frac{R_2}{R_1}}
\end{align*}
\]

(3.4)

By using two transistors (with the same size) instead of two resistors, we still reach the desirable gain and we have less consumption and more integration capability. The transistors have the drains shunted with the gates (connected like diodes) and they are designed to guarantee that they are always in the saturation region, in order to achieve a good resistive behavior.

\[
\begin{align*}
R_1 &= R_2 \\
\frac{V_{out}}{V_{in}} &= 2
\end{align*}
\]

(3.5)
This amplifier is powered by the LDO $V_{out}$, increasing the PSRR (power supply rejection ratio). PSRR is very important to LDOs because it relates $V_{out}$ with the variation in the supply voltage $V_{in}$. The purpose of this technique is to make the LDO as independent as possible of the supply voltage. In the next chapter, the LDO design is explained.
Figure 3.7: The non-inverting topology
This chapter presents the final circuit and explains the design criteria for the transistors of the LDO.

4.1 Transistors Parameters

The essential parameters for the design of the transistors are the $V_{tn}$, $V_{tp}$, $\mu_n C_{ox}$ (NMOS) and $\mu_p C_{ox}$ (PMOS). These parameters were obtained by simulation of the circuit presented in Figure 4.1 created for this purpose. In order to ensure operation in the saturation region, both transistors (PMOS and NMOS), with $W = 1\mu m$ and $L = 1\mu m$, are polarized with the maximum voltage (3.3 V) and the current sources provide $1\mu A$.

![Figure 4.1: Circuit used to extract the transistors parameters.](image)

Running the simulation, $V_{th}$ (NMOS and PMOS), $V_{GS}$ (NMOS) and $V_{SG}$ (PMOS) are obtained. Using these parameters, $\mu_n C_{ox}$ and $\mu_p C_{ox}$ can be calculated using the equation 3.1. The respective results ($\mu C_{ox}$) are presented in Table 4.1.

4.2 Schematic Design

This section presents the final LDO circuit and a description of the design strategy of each subcircuit that composes the LDO. The design strategy is based on the functionality of each subcircuit face to tradeoffs such as low current consumption, low supply, fast transient response, stability...
CHAPTER 4. LDO DESIGN

Table 4.1: Transistor Parameters.

<table>
<thead>
<tr>
<th></th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{gs}$</td>
<td>706, 4371 mV</td>
<td>878, 0455 mV</td>
</tr>
<tr>
<td>$V_{th}$</td>
<td>619, 3415 mV</td>
<td>647, 4683 mV</td>
</tr>
<tr>
<td>$\mu_nC_{ox}$</td>
<td>264 μA/V$^2$</td>
<td>37 μA/V$^2$</td>
</tr>
</tbody>
</table>

and PSRR. As shown in Figure 4.2 (this figure is represented in Appendix A in landscape format) we can find all the subcircuits that were previously presented.

4.2.1 Pass Transistor Design

There are two key parameters to design the LDO pass transistor: the dropout (difference between the source voltage $V_{in}$ and the drain voltage $V_{out}$) and the maximum drain current. In this case, the dropout voltage of the capacitor-less LDO is 150 mV for a maximum load current of 1 mA. The pass transistor is designed to deliver a maximum drain current of 1 mA, been kept in the saturation region with $V_{DS} \geq V_{GS} - V_T$. The pass transistor stage is shown in Figure 4.3.

First order approximations were used to find the device dimensions. The relation used is shown in equation 4.1

$$V_{DROPOUT} = V_{DSAT} = \sqrt{\frac{2I_{MAX}}{\mu_pC_{OX}W/L}}$$

$I_{MAX}$ defines the maximum output current, forcing the dimensions of the pass transistor,
4.2. SCHEMATIC DESIGN

Figure 4.3: Pass transistor design.

$W/L$, for a desired minimum $V_{DROPOUT}$. The variables $\mu_p$, hole mobility, and $C_{\text{OX}}$, the gate capacitance per unit area, are device technology parameters and are given in table 4.1. Equation 4.1 was rearranged to find the pass transistor device dimensional ratio $(W/L)$, shown in equation 4.2.

$$\left[\frac{W}{L}\right]_{\text{PASS}} = \frac{2I_{\text{MAX}} \mu_p C_{\text{OX}} V^2_{\text{DSAT}}}{2} = 2.40 \times 10^3$$ (4.2)

In order to improve the PSRR analysis and achieve a better performance in corners simulations, the W of the pass transistor was increased up to 1.2 mm. Table 4.2 shows the pass transistor calculated and the parameters obtained by simulation.

Such a large transistor has considerable capacitance, as shown in Table 4.2. Miller effect of $C_{\text{GD}}$, must be considered in the calculation of the gain of the LDO, due to its considerable value. The Miller effect is responsible for the dominant pole. Pass transistor subthreshold operation is another major concern. For large variations in the load current, the PMOS transistor will undergo a transition from operating in the saturation region to operating in the subthreshold region. The
pass transistor exhibits an exponential relation while operating in subthreshold in contrast to the nominal square law relation of $I_D$ with $v_{GS}$. The relation is given by equation 4.3 [3].

$$I_D \approx I_{DO} \left( \frac{W}{L} \right) e^{V_{GS}/nkT} \quad (4.3)$$

### 4.2.2 Design Criteria

The design of the whole circuit always aims for lower consumption. Therefore the design of each subcircuit was based on the current budget available and on the overdrive voltages that were decided based on the number of transistors stored in each branch. Given the budget of the current available, the biasing current in the main branches was defined as $I_1 = I_2 = 2\mu A$.

Attached to these concepts there are goals for each subcircuit:

- **Shunt Circuit**

  The transistors of the shunt regulation are restricted by supply voltage ($V_{\text{out}}$), and therefore they have low overdrive voltages (PMOS around 150 mV and NMOS around 40 mV). The transistor M99 makes the DC bias point to all the current mirrors of the shunt regulation subcircuit, while M110 senses the current peaks (due to load variations) and trigger the shunt regulation transistor, M109. For this reason the $g_m$ of these two transistors is high.

- **Fast loop**

  In this subcircuit, the current mirrors are supplied by $V_{\text{in}}$. However, the currents that flow through these current mirrors are low ($0.5\mu A$ to $2\mu A$). Therefore the overdrive voltages of the transistors are a little lower (PMOS around 90 mV and NMOS around 33 mV). One of the most important things in this subcircuit is that the $r_o$ of the transistor M78, that is connect to the gate of the pass transistor, must be high (around 5.6 MΩ) in order to achieve a current mirror that works like an active load and to improve the LDO open loop DC gain. Besides this requirement, the fast loop controls the voltage in the gate of the pass transistor earlier than the main loop. However, when the main loop adjusts the $v_{sg}$ of the pass transistor, this fast loop remains working ($I_2$ changed).

- **Error Amplifier**

Table 4.2: Transistor Parameters.

<table>
<thead>
<tr>
<th>CALCULATED</th>
<th>SIMULATED</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W = 0.84\text{mm}$</td>
<td>$W = 1.2\text{mm}$</td>
</tr>
<tr>
<td>$L = 350\text{nm}$</td>
<td>$L = 350\text{nm}$</td>
</tr>
</tbody>
</table>
4.3 LAYOUT

Besides the considerations made about current mirrors that are supplied by $V_{out}$, there are other aspects that are relevant. The differential pair is made with low voltage transistors (1.5V instead of 3.3V) due to the lower supply voltage and also to avoid the mismatch between these two transistors. In order to improve the open loop gain, the gm of the differential pair (composed by M62 and M63) should be high (around $15 \, \mu A/V$). The output stage is a low voltage current mirror (M66 and M85) in order to achieve high output impedance. Therefore the gm and $r_o$ of these two transistors should be high (around $10 \, \mu A/V$ and $8.6 \, M\Omega$, respectively).

The two feedback resistors, as previously referred, are implemented with two equal transistors connected as diodes. They are PMOS transistors because they are more resistive than the NMOS. Another consideration in the design of these two transistors is the huge L (around $20 \, \mu m$), to become very resistive.

4.3 Layout

In this section, the final capacitor-less LDO voltage regulator layout is presented. The LDO was laid out in SMIC 0.13 $\mu m$ CMOS technology. Figure 4.4 shows the final capacitor-less LDO voltage regulator layout.

There are several aspects that should be referred such as: The implementation of the capacitors are made with transistors (MOSCAPs) instead of CVPP (capacitors that are made between armors of the same metal layer) in order to spare area. For the same reason, and as previously referred, the two feedback resistors are implemented with two equal transistors connected as diodes.

It is impossible to see in Figure 4.4 how the current mirrors and the differential pair are designed. So, it was made a zoom in Figure 4.5, to show that they are inter-digitally designed (M62 and M63 are the differential pair transistors), in order to minimize the mismatch effect inherent to the fabrication process (for example, if there is a temperature gradient along the wafer).
Figure 4.4: LDO layout.
Figure 4.5: LDO differential pair design.
This chapter presents the simulated results that characterize the LDO. The results presented cover several circumstances that the circuit could be subjected to. The simulation variations are presented in Table 5.1.

Table 5.1: Simulated Corners.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Variations</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOS</td>
<td>ff, fs, sf, ss</td>
</tr>
<tr>
<td>RES</td>
<td>min (-30%) → max (+30%)</td>
</tr>
<tr>
<td>Ibias</td>
<td>min (-20%) → max (+20%)</td>
</tr>
<tr>
<td>Temp</td>
<td>min (-40°C) → max (125°C)</td>
</tr>
</tbody>
</table>

Analyzing Table 5.1 we find several parameters. The first one is MOS. This parameter comprehend some fabrication process variations (such as thin oxide, Vth, transistor capacitances etc...), that make the transistors faster or slower (f stands for fast and s stands for slow). To each pair of letters, the first letter concerns to PMOS and the second one to NMOS. The second parameter concerns about the variations of the resistances. The third one is the variation of the bias current referenced to the nominal value. The last parameter is the temperature range. All these variations are combined and produce a total of 64 corners.

All the test benches used to simulate the capacitor less LDO are shown in Appendix B.

5.1 AC analysis

In this section the AC analysis is performed only for the generic corner, due to the complexity of the circuit. Since the circuit has several feedback loops it is important to decide which loop should be open for the Open loop stability analysis. The loop with higher gain was selected.

The theoretical analysis consists in the calculation of the DC gain and the dominant pole location and make a comparison with the simulated results. In Figure 5.1 the LDO block diagram is presented (this figure gives a good block diagram for the DC gain calculation).

The DC gain (when the LDO has full load), is given by equation 5.1 that as we can see has four terms (separated by ×). The first term corresponds to the error amplifier, the second term to the factors of the current mirrors (of the main core and fast loop) that are used to amplify
the current which compounds the LDO ($F_1 = F_2 = 4$). The third term corresponds to the pass transistor transconductance multiplied by it's gate resistance $R_x$, which is given by equation 5.2. The last of the DC gain is the output resistance which is given by equation 5.3.

$$A_{DC} \approx \frac{1}{4} gm_{\text{differential pair}} \times (F_1 + F_2) \times gm_{\text{pass transistor}} R_x \times R_{out} = 71\, \text{dB} \quad (5.1)$$

$$R_x = r_{o78} / (gm_{127} \times r_{o127} \times r_{o95}) \quad (5.2)$$

$$R_{out} = r_{o87} / ((r_{o49} + r_{o50}) / R_L) \quad (5.3)$$

As referred previously one of the concerns when designing the LDO is the improvement of the PSRR analysis. That is why the subcircuits are supplied by the output voltage $V_{out}$. However, this solution introduces feedback produced by the $r_o$ of the current mirrors that compound the projected feedback loops (the “cut AC” block shown in Figure 5.1 doesn’t cover this feedbacks).
5.1. AC ANALYSIS

This effect is illustrated in Figure 5.2. Figure 5.1 shows the interruption of the AC feedback of the main loop, keeping the DC feedback. The open loop analysis was performed adding this cut AC instance and simulating the $v_{\text{out}}/v_{\text{in}}$ ratio.

![Figure 5.2: Parasitic feedbacks.](image)

The DC gain is not independent of the LDO operation state (full load and no load) because
of the $R_L$ dependency in $R_{\text{out}}$. Analyzing the simulated results shown in figures 5.3 and 5.4, we can conclude that the $R_{\text{out}}$ term is not the dominant term, since the DC gains are very similar. However, it still can be seen that the no load simulation has a DC gain which is a little higher than the full load simulation, since the term $R_{\text{out}}$ is higher in the no load situation. In this two figures we can also see that the phase margin in both cases is around 80 degrees, which means that the circuit is very stable in both situations. This is new in this kind of circuits because of the dependency of the second pole with the load, when compared to the typical LDOs referred in Chapter 2.

Using a tool of the simulator (.PZ) we can extract the location of the poles and zeros. Table 5.2 shows only the poles and the zeros which are comprehended in the frequency range of the phase margin.

- First Pole

  The first pole is also called the dominant pole. This pole is produced by the Miller effect associated to the $C_{\text{GD}}$ of the pass transistor. Equation 5.4 gives the theoretical value for the frequency.
5.2 Transient Analysis

This chapter shows the behavior of the capacitor less LDO voltage regulator, during the load variations. These variations are simulated with a current source in the output of the LDO, between 5\(\mu A\) and 1\(mA\) (no load situation and full load situation respectively), with a rise time and a fall time of 2.5\(\mu s\). This analysis is much more reliable than the Ac analysis, since in this simulation there is no need to interrupt any feedback.

The simulation described in this section was made for all the 64 corners, as it can be seen in Figure 5.5. The result achieved is very good because the overshoot peaks are small and the time response of the circuit is fast, even in the worst corners. It can also be seen that after the transient occurs, the regulator’s offset for all corners, in both situations, is less than 10 mV (\(\approx 0.65\%\)).

### Table 5.2: Simulated Poles and Zeros Location.

<table>
<thead>
<tr>
<th></th>
<th>No Load</th>
<th>Full Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>(f_{p1})</td>
<td>6.3 Hz</td>
<td>7.4 Hz</td>
</tr>
<tr>
<td>(f_{p2})</td>
<td>5.5 kHz</td>
<td>58.8 kHz</td>
</tr>
</tbody>
</table>

\[
f_{p1} = \frac{1}{2\pi R_x A_{pass} C_{gdpass}} \tag{5.4}
\]

Based on equation 5.4, it is easy to see that there is no significant dependency on the load. Only the changed imposed by the gain (\(A_{pass}\)). The terms that compound the pole location are:

- \(R_x\), is the resistance in the gate of the pass transistor, which is given by equation 5.2.
- \(A_{pass}\) represents the gain of the pass transistor, which is given by the equation 5.5.
- \(C_{gdpass}\) is the capacitance of the pass transistor between the gate and the drain.

\[
A_{pass} \approx gm_{87} \times (r_{o87}/R_L) \tag{5.5}
\]

- **Second Pole**

This pole is introduced by the output capacitor and the load resistance. The location of this pole is given by equation 5.6.

\[
f_{p2} = \frac{1}{2\pi C_{out}(r_{opass}/R_{load})} \tag{5.6}
\]
5.2.1 Power up and down Analysis

In this subsection, the power up and power down transient behavior is presented. Figure 4.2 shows several transistors that appear necessary for the voltage regulation. The function of these transistors is to pull down or pull up all the required nodes in order to put the LDO in standby mode. In Figure 5.6 it can be seen the enable signal switching from a lower level to a higher level and the LDO output voltage responding to this variation.

Looking carefully to Figure 5.6, it can be seen that the power up occurs between $10\mu s$ and $15\mu s$ for all the simulated corners. This means that, even in the worst case, the LDO is turned on very quickly. Figure 5.7 illustrates the opposite change. The LDO has a fast shutdown response. Looking at Figure 5.8 we realize that in standby the LDO consumption is near $0\,A$ and when it is turned on its consumption is around $96\mu A$.

5.3 Steady-state Parameters

The steady-state parameters define the capacitor-less LDOs static state conditions. Two important characteristics defined the steady-state LDO parameters, the line regulation and the load regulation. The line regulation was simulated for full load condition, $1mA$ output current (because most of the time the regulator is working in a full load condition). The input voltage was swept from $1.7\,V$ to $3.7\,V$ with a step of $1\,mV$ and the correspondent output voltage was measured. The results are shown in Figure 5.9.

For the load regulation analysis, the input voltage was fixed in $2.65\,V$, and the output current was swept from $0\,mA$ to $1.1\,mA$ with a sept of $0.01\,mA$. Figure 5.10 shows the simulation results. The output voltage deflects from the nominal $1.5\,V$ output. However in both cases the deflection is inferior to $3\,mV$ for the worst corner, which means that the regulator has a good behavior for the steady state conditions.

5.4 PSRR Analysis

This section presents the PSRR analysis. This analysis evaluates how the supply variations impact on the output voltage. One of the concerns on the LDO design is to have a low PSRR. In this case the LDO will be integrated with a DC-DC that operates at $2MHz$. In order to improve the PSRR several filters and pole/zeros were added and some parts of the circuit were supplied with the output voltage. Figures 5.11 and 5.12 show the PSRR analysis without and with load, respectively. Analyzing these two figures, we see that at $2MHz$ we have PSRR less or equal than $-20dB$ for almost all of the simulated corners.
5.5 Monte Carlo Simulations

Monte Carlo analysis was performed to study the capacitor less LDO sensitivity to process variations such as carrier mobility and MOSFET threshold voltage. The Monte Carlo analysis was performed in the DC steady-state output voltage (with sampling of M=100, in order to get reliable results). The simulation was performed in the two extreme conditions: with no load and with full load, in order to observe the offset of the regulator due to the process variations. These results are shown in Figure 5.13 and Figure 5.14 respectively.

The results show that the two simulations are very similar. Looking more carefully to the results it can be seen that the maximum offset is 30 mV and only in few cases (in both figures). A great part of the cases are in the desired voltage or in it's neighborhood. These results mean not only that the DC steady-state of the regulator is not affected by the load, but also shows the robustness of the regulator to the process variations.
Figure 5.5: Transient analysis in all 64 corners.
Figure 5.6: Power up analysis.
Figure 5.7: Power down analysis.
Figure 5.8: Consumption analysis.
Figure 5.9: Line regulation with full load.
5.5. MONTE CARLO SIMULATIONS

Figure 5.10: Load regulation.
Figure 5.11: PSRR analysis without load.
5.5. MONTE CARLO SIMULATIONS

Figure 5.12: PSRR analysis with load.
Figure 5.13: Process variation on DC steady-state output voltage for $I_{out} = 0mA$. 
5.5. MONTE CARLO SIMULATIONS

Figure 5.14: Process variation on DC steady-state output voltage for $I_{out} = 1mA$. 

![Histogram showing process variation on DC steady-state output voltage for $I_{out} = 1mA$.]
Conclusions

A novel LDO topology has been presented that allows to remove the large external capacitor found in typical LDOs. The new capacitor less LDO presents good results in all kinds of analysis. The good results presented are not only result of the combination of fast feedback loops but also due to the regulator’s core. This core combines a transconductance amplifier, acting like an error amplifier, with current amplifiers that drive active load connected to the gate of the pass device. The shunt regulation was also introduced in order to improve the transient response and to minimize the output capacitor. Another very important concern in the regulator design was the PSRR. The architecture also proven to be robust to process variations (by Monte Carlo simulations). The proposed capacitor less LDO voltage regulator was designed in SMIC 0.13 \( \mu \text{m} \), CMOS technology in Chipidea®. The final characteristics of the LDO designed are presented in Table 6.1.

Table 6.1: Final Results.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vout</td>
<td>Output Voltage - Line Regulation</td>
<td>1.547</td>
<td>1.55</td>
<td>1.5495</td>
<td>V</td>
</tr>
<tr>
<td>Vout</td>
<td>Output Voltage - Load Regulation</td>
<td>1.547</td>
<td>1.55</td>
<td>1.551</td>
<td>V</td>
</tr>
<tr>
<td>Vout</td>
<td>Output Voltage - Monte Carlo Simulation</td>
<td>1.53</td>
<td>1.55</td>
<td>1.58</td>
<td>V</td>
</tr>
<tr>
<td>Itot</td>
<td>Current Consumption</td>
<td>-</td>
<td>-</td>
<td>96</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>Itot</td>
<td>Current Consumption - Power down</td>
<td>-</td>
<td>-</td>
<td>168.51</td>
<td>pA</td>
</tr>
<tr>
<td>PM</td>
<td>Phase Margin</td>
<td>83</td>
<td>-</td>
<td>83</td>
<td>deg</td>
</tr>
<tr>
<td>PSRR</td>
<td>PSRR (at 2 Mhz with load)</td>
<td>-29</td>
<td>-25</td>
<td>-18</td>
<td>db</td>
</tr>
<tr>
<td>Cout</td>
<td>Output Capacitor</td>
<td>-</td>
<td>30</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series resistor</td>
<td>-</td>
<td>1.55</td>
<td>-</td>
<td>k( \Omega )</td>
</tr>
<tr>
<td>Area</td>
<td>Total core area</td>
<td></td>
<td></td>
<td>0.025</td>
<td>mm(^2)</td>
</tr>
</tbody>
</table>

As shown in Table 6.1 all the specifications defined in Chapter 1 were achieved. The whole development process provided an excellent view of microelectronic power circuits design and how this design takes place in the industrial world.
6.1 Future Work

Even though this capacitor less LDO design has met the specifications that were defined for the inclusion in a mobile PMU, there is also a scope for improvement. Other feedback loops need to be experimented.

The major concerns in this type of circuits are: fast response, consumption, PSRR and area. These are relevant aspects, that the future work should focus on, in order to achieve better trade-offs with new technologies.
Bibliography


Figure A.1: Final LDO circuit.
Test Benches
Figure B.1: AC open loop test bench.
Figure B.2: Transient test bench.
Figure B.3: Transient power up and down test bench.
Figure B.4: Transient power up and down test bench.
Figure B.5: Line regulation test bench.
Figure B.6: Load regulation test bench.
Figure B.7: PSRR test bench.