Integrated Thermal Monitor for SOC

Nelson Paulo Vitorino Pires

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Júri
Presidente: Prof. José António Beltran Gerald
Orientador: Prof. Marcelino Bicho dos Santos
Co-Orientador: Prof. José Júlio Alves Paisana
Vogais: Prof. Jorge Manuel dos Santos Ribeiro Fernandes

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To my parents for their encouragement, love, and support.
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Abstract

A low-voltage temperature sensor, with an accuracy of ±1ºC in the range of -55ºC to 130ºC, was designed using the SMIC 0.13 µm technology. A PTAT circuit and a sigma-delta ADC are used in order to convert the temperature into a digital word. Since the error introduced by the offset voltage of the sigma-delta op-amp can be important, in order to obtain high accuracy, an auxiliary circuit for the compensation of the offset voltage is proposed. The quiescent current of the temperature sensor is 376 µA and the power supply 1.55V. However, since the temperature sensor is digitally controlled, the average current consumption could be as low as 5 µA. Compared with traditional temperature sensors, the proposed one has a much more lower consumption, making it perfect for portable devices such as mobile phones, i-pods, etc.

Keywords

Temperature sensor
Low-voltage IC
PTAT
Sigma-delta ADC
Offset voltage compensation
Resumo

Foi projectado um sensor de temperatura de baixa tensão, com uma exactidão de ±1ºC na escala de -55ºC a 130ºC, usando a tecnologia SMIC 0.13 µm. Para converter a temperatura numa palavra digital é usado um circuito PTAT e conversor A/D sigma-delta. No entanto, como o erro introduzido pela tensão offset do ampop do conversor sigma-delta é significativo, a fim obter uma exactidão elevada, é proposto um circuito auxiliar para a compensação da tensão offset. A corrente consumida pelo sensor de temperatura é de 376 µA e a alimentação de 1.55V. No entanto, como o sensor de temperatura é controlado digitalmente, o consumo médio pode ser na ordem dos 5 µA. Comparando este sensor com os sensores de temperatura tradicionais, este tem um consumo muito mais baixo, sendo perfeito para dispositivos portáteis tais como telemóveis, i-pods, etc.

Palavras-chave

Sensor de temperatura
CI de baixa tensão
PTAT
Conversor A/D sigma-delta
Compensação da tensão de desvio
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<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>ΣΔ</td>
<td>Sigma-Delta</td>
</tr>
<tr>
<td>A/D Converter</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer-Aided Design</td>
</tr>
<tr>
<td>DRC</td>
<td>Design Rule Check</td>
</tr>
<tr>
<td>ERC</td>
<td>Electrical Rule Check</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>JTM</td>
<td>Junction Thermal Monitor</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>LVS</td>
<td>Layout Versus Schematic</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>NMOS</td>
<td>MOS Transistor Type N</td>
</tr>
<tr>
<td>OP-AMP</td>
<td>Operational Amplifier</td>
</tr>
<tr>
<td>PMOS</td>
<td>MOS Transistor Type P</td>
</tr>
<tr>
<td>PTAT</td>
<td>Proportional-To-Absolute-Temperature</td>
</tr>
<tr>
<td>RTD</td>
<td>Resistance-Temperature-Detectors</td>
</tr>
<tr>
<td>SMIC</td>
<td>Semiconductor Manufacturing International Corporation</td>
</tr>
</tbody>
</table>
List of Programmes

CosmosScope® (Synopsys®)
Calibre® (Mentor®)
HSPICE® (Synopsys®)
Matlab® (The MathWorks®)
Virtuoso® (Cadence®)
Chapter 1

Introduction

This chapter gives a brief overview of the work. Before establishing work targets, the scope and motivations are brought up. The current State-of-the-Art in relation to the scope of the work is also presented. At the end of the chapter, the workflow is provided.
1.1 Overview

In this work a low voltage digital temperature sensor is developed and implemented in the SMIC 0.13 technology with an accuracy of ±1°C in the range of -55°C to 130°C. The sensor uses a PTAT (proportional-to-absolute-temperature) circuit and a first order sigma-delta A/D converter in order to digitize the temperature value. One of the most critical problems in temperature measurement is the offset voltage of the amplifier used in the converter. Since this offset could introduce a significant error, an auxiliary circuit for compensation is included. This temperature sensor is implemented with a low power supply of 1.55V and works with a quiescent current of 376uA.

1.2 Relevance and Motivation

Nowadays temperature sensors exist in almost all kind of electronic based systems. This need for thermal management is due to the fact that changing half-a-degree Celsius in a system can make the difference between a correct work or a failure in the corresponding functionality. There are many devices available for temperature measurement, including RTDs (resistance-temperature-detectors), thermistors, thermocouples and more recently integrated circuits (IC) temperature sensors. Although the range of the IC temperature sensors maybe small when compared to thermocouples and RTDs, they have several advantages such as: size, accuracy, price and interface simplicity.

Table 1.1 shows some typical applications of temperature sensors.

<table>
<thead>
<tr>
<th>Monitoring</th>
<th>Compensation</th>
<th>Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>Portable Equipment</td>
<td>Oscillator Drift in Cellular Phones</td>
<td>Battery Charging</td>
</tr>
<tr>
<td>CPU Temperature</td>
<td>Thermocouple Cold-junction Compensation</td>
<td>Process Control</td>
</tr>
<tr>
<td>Battery Temperature</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 1.1 – Typical applications of temperature sensors.
Thermal monitors can be divided in two main types: analog and digital. Although digital temperature sensors are more often used than the analog ones, they continue being used in many applications and also in every digital temperature sensor.

In today’s electronic industry many applications require the temperature to be digitized so that can be properly interpreted by a microprocessor.

In Figure 1.1 the basic blocks of the digital integrated temperature sensor implemented in this thesis is presented.

![Diagram of the temperature sensor topology](image)

Figure 1.1 - Temperature sensor topology.

Since the implemented temperature monitor has a digital output, it can be easily connected to a microprocessor in order to allow control of the temperature being measured. This leads to a huge number of possible applications, like fan speed control, shutdown mode due to short-circuit, etc.


1.3 State-of-the-Art

Heat is one of the main problems in today’s electronics industries due to the use of high frequencies and to the high level of integration. IC temperature sensors have an important role here because they can monitor the heat and also control it with a fan.

Actual IC temperature sensors have an operating range from about -55 °C to 150 °C and all of them use a bipolar junction to measure the temperature.

In Table 1.2 some analog and digital temperature sensors characteristics are presented.

<table>
<thead>
<tr>
<th>Temperature Sensor</th>
<th>Type</th>
<th>Vdd</th>
<th>Temperature Range</th>
<th>Max. error over temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD592</td>
<td>Current output</td>
<td>4V-30V</td>
<td>-25ºC +105ºC</td>
<td>±1ºC</td>
</tr>
<tr>
<td>TMP17</td>
<td>Current output</td>
<td>4V-30V</td>
<td>-40ºC +105ºC</td>
<td>±1ºC</td>
</tr>
<tr>
<td>TMP35</td>
<td>Voltage output</td>
<td>2.7V-5.5V</td>
<td>+10ºC +125ºC</td>
<td>±2ºC</td>
</tr>
<tr>
<td>TMP36</td>
<td>Voltage output</td>
<td>2.7V-5.5V</td>
<td>-40ºC +125ºC</td>
<td>±2ºC</td>
</tr>
<tr>
<td>TMP37</td>
<td>Voltage output</td>
<td>2.7V-5.5V</td>
<td>+5ºC +100ºC</td>
<td>±2ºC</td>
</tr>
<tr>
<td>TMP03/TMP04</td>
<td>Digital output</td>
<td>5V</td>
<td>-40ºC +100ºC</td>
<td>±1.5ºC</td>
</tr>
</tbody>
</table>

Table 1.2 - Commercial analog and digital temperature sensors.

Digital temperature sensors have a number of advantages over the analog counterparts, especially in remote applications.

The topologies of the TMP03 and TMP04 are similar to the topology of the sensor designed in this thesis. These sensors include a $V_{PTAT}$ generator, sigma-delta ADC, and a clock source. However, in this thesis, a circuit is included for the compensation of the offset voltage in the sigma-delta op-amp (see Figure 1.1). In reference [1] an example of a digital temperature sensor is presented, with an accuracy of 0.1C, and a low-offset second order sigma delta converter. The operating principle of this temperature sensor is presented in Figure 1.2.

![Figure 1.2 - Principle of operation of the Temperature Sensor in reference [1].](image)
As shown in Figure 1.2, it uses two pnp transistors in order to generate two voltages $V_{BE}$ and a $\Delta V_{BE}$. These voltages are combined to produce the PTAT and reference voltages, which are converted into a digital word.

Higher accuracy is achieved by using dynamic element matching, a chopped current gain independent PTAT bias circuit, and a low-offset, second order sigma delta ADC.

### 1.4 Objectives and Specifications

The objective of this work is to implement a low voltage temperature sensor with offset compensation in SMIC 0.13. This thesis was proposed in cooperation with Chipidea. The basic architecture of the sensor was given by the company.

The design of the integrated temperature sensor is developed in three phases. The first phase corresponds to create a Matlab® model for the circuit in order to conclude about the mandatory specifications for each of its components. The design and implementation in SMIC 0.13 is the second step where the blocks are created and sized as well as simulated. The schematic was design with Cadence tools and simulated with Hspice. The different blocks that compose the temperature sensor are simulated separately and also in the complete sensor, with changes in important parameters such as power supply, bias current, properties of the transistors, etc.

Finally, the layout of the circuit is designed in order to allow physical implementation.

The initial specifications of the integrated temperature sensor are presented in the Table 1.3.
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td></td>
<td></td>
<td>SMIC 0.13 µm Metal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tj</td>
<td>Junction Temperature Range (JTM)</td>
<td>-55</td>
<td></td>
<td>130</td>
<td>°C</td>
</tr>
<tr>
<td>Vavdd</td>
<td>Analog supply range</td>
<td>1.5</td>
<td>1.55</td>
<td>1.6</td>
<td>V</td>
</tr>
<tr>
<td>Vdvdd</td>
<td>Digital supply range</td>
<td></td>
<td>1.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Trange</td>
<td>Temperature Range</td>
<td>-55</td>
<td></td>
<td>160</td>
<td>°C</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>Meas. cycle duration</td>
<td>0</td>
<td>5</td>
<td>488</td>
<td>Hz</td>
</tr>
<tr>
<td>jtmclk</td>
<td>clock frequency</td>
<td></td>
<td>32</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Ijtmhigh</td>
<td>High current for Δvbe</td>
<td>310</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Ijtmlow</td>
<td>Low current for Δvbe</td>
<td>10</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Iq</td>
<td>Quiescent current</td>
<td></td>
<td>400</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Ibias</td>
<td>bias current Range</td>
<td>0.8</td>
<td></td>
<td>1.2</td>
<td>µA</td>
</tr>
<tr>
<td>Total area</td>
<td>Analog Core</td>
<td></td>
<td>0.075</td>
<td></td>
<td>mm²</td>
</tr>
</tbody>
</table>

Table 1.3 - Specifications of the temperature sensor.

1.5 Thesis Organization

The structure of this thesis corresponds to the workflow presented in Figure 1.3. In chapter two, integrated temperature sensors theory is discussed and a Matlab® model for the sensor is presented and simulated. In chapter three, the blocks of the temperature sensor are explained and design, and the simulations and layout are presented. In chapter four, simulations and results of the whole thermal monitor are presented and analysed.

The last chapter presents the global conclusions of this thesis and future developments of this work are discussed.
Figure 1.3 - Thesis workflow.
This chapter presents and discusses the methods of measuring temperature in ICs. In the first section a method for converting the temperature into a voltage is presented. It is also explained how to convert this analogue value into a digital word. In section 2.2 the topology adopted in this thesis for the measurement is discussed. Finally, in section 2.3, this topology is simulated using Matlab® in order to conclude about individual blocks requirements.
2.1 Temperature Sensors

In this section the basic principles of operation of the circuits used in the temperature sensor are described. First, a junction is used in order to create a voltage proportional to the temperature. Then, the sigma delta A/D converters are used to convert this voltage into a digital word.

2.1.1 Junction

In order to measure the temperature in integrated circuits, it is commonly used a PTAT circuit. This type of circuit creates a voltage that is proportional to the absolute temperature. To understand how this PTAT voltage can be created let’s see the base-emitter voltage junction of a bipolar transistor. As shown in equation (2.1), this $V_{BE}$ voltage can be written as a function of the collector current and the temperature [10].

$$V_{BE} = V_{G0} \left(1 - \frac{T}{T_0}\right) + V_{BE0} \frac{T}{T_0} + \frac{m k T}{q} \ln \left(\frac{T}{T_0}\right) + \frac{k T}{q} \ln \left(\frac{I_c}{I_{c0}}\right)$$  \hspace{1cm} (2.1)

In equation (2.1) $V_{G0}$ represents the bandgap voltage of silicon, $k$ is the Boltzmann’s constant, $m$ is a temperature constant, $I_{c0}$ is the collector current at a reference temperature $T_0$, $I_c$ is the collector current at true temperature $T$, $V_{BE0}$ is the base-emitter junction voltage at reference temperature $T_0$ and $V_{BE}$ is the base-emitter junction voltage at true temperature $T$. Using equation (2.1), if two different collector currents are applied, $I_{c1}$ and $I_{c2}$, to a base-emitter junction, we will obtain two different junction voltages $V_{BE1}$ and $V_{BE2}$ respectively. The difference between these two voltages is given by equation (2.2).

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{k T}{q} \ln \left(\frac{I_{c1}}{I_{c2}}\right)$$  \hspace{1cm} (2.2)

Equation (2.2) is the fundamental equation that gives the relationship between the voltage, $\Delta V_{BE}$, and the absolute temperature, $T$ (equation (2.3)).

$$\Delta V_{BE} = CT \hspace{1cm} C = \frac{k}{q} \ln \left(\frac{I_{c1}}{I_{c2}}\right)$$  \hspace{1cm} (2.3)

In a PTAT circuit, temperature is quite accurate, even if the currents $I_{c1}$ and $I_{c2}$ change, as long as the ratio $\frac{I_{c1}}{I_{c2}}$ remains constant [10]. A PTAT circuit is presented in Figure 2.1. As it can be seen, the $\Delta V_{BE}$ voltage is created by subtracting two base-emitter voltages of two different junctions, each one of them biased with different collector currents. For more information on PTAT circuits see references [1], [14] and [15].
2.1.2 A/D Converters

As it was referenced in Chapter one there are two types of IC temperature sensors: analog and digital. The IC temperature sensor presented in this thesis is digital, so the output has to be converted into a digital format of 1’s and 0’s. Thus, we need an A/D converter.

There are two main types of A/D converters: Nyquist-Rate Converters that convert samples usually at a frequency corresponding to the double of the input signal, and, oversampling converters that operate at much faster frequencies. Although Nyquist converts have higher bandwidth, oversampling converters have more resolution, being more used in applications that require higher precision [9]. Therefore, in this case, since temperature changes slowly with time, and it is crucial to have a high precision, the A/D converter used is an oversampling sigma-delta (ΣΔ) converter.

Another advantage of oversampling converters is the reduced matching requirements on tolerances and gains of the analog components [4]. However, the temperature measurement error is also dependent on these factors as it will be shown in section 2.3.

2.1.3 A/D Sigma-Delta Converter

Figure 2.2 shows the architecture of a ΔΣ oversampling A/D converter. A continuous-time anti-aliasing filter is used in the first block to limit the input signal $X_{in}(t)$. The filtered signal $X_c(t)$ is then sampled by a sample-and-hold. The next block is a ΔΣ modulator, which converts the analog signal $X_a(t)$ into a digital bit stream. In the last block a decimation filter is used where the signal passes through a low-pass filter followed by a down sampler.
A shaped quantization noise applied to the oversampling signal is commonly referred to as sigma-delta ($\Sigma\Delta$) modulation (reference [4]) and is shown in Figure 2.3.

Although multibit quantizers can be used in the sigma-delta modulator, as shown in Figure 2.3, most of the oversampling converters use only 1-bit quantizer. With a high sampling rate, the output of the converter can be filtered to obtain the desired number of bits.

In the sigma-delta topology, the effect of the noise in the output is reduced by the feedback and by the transfer function $H(z)$. However, we will see shortly that this noise reduction changes with frequency.

Assuming $e(n)$ to be the noise introduced by the quantizer, the $\Sigma\Delta$ modulator can be described by the linear model presented in Figure 2.4.

As it can be seen in Figure 2.4, the linear model of the $\Delta\Sigma$ has two independent inputs, so we can derive a signal transfer function, $S_{TP}(z)$, and a noise transfer function, $N_{TP}(z)$.

\[
S_{TP}(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)} \quad (2.4)
\]

\[
N_{TP}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \quad (2.5)
\]

Equations (2.4) and (2.5) show that if $H(z)$ goes to infinite then $N_{TP}(z)$ will go to zero and $S_{TP}(z)$ will
be approximately one.

**First-order noise Shaping**

A first-order $\Delta \Sigma$ modulator can be implemented by high-pass filtering the quantization noise. Therefore, the noise transfer function, $N_{TF}(z)$, should have a zero at dc ($z=1$). One way of doing this is letting $H(z)$ be a discrete time integrator (pole $z=1$).

$$H(z) = \frac{1}{z^{-1}}$$

(2.6)

Using equation (2.6), the signal transfer function, $S_{TF}(z)$, is given by equation (2.7) and the noise transfer function $N_{TF}(z)$ is given by equation (2.8).

$$S_{TF}(z) = \frac{y(z)}{u(z)} = \frac{1/(z-1)}{1+1/(z-1)} = z^{-1}$$

(2.7)

$$N_{TF}(z) = \frac{y(z)}{e(z)} = \frac{1}{1+1/(z-1)} = 1 - z^{-1}$$

(2.8)

Since equation (2.8) represents a high-pass filter, the quantization noise can be reduced or eliminated in the band of interest but not for high-frequencies. However, at the modulator’s output, the signal is then low-pass filtered to reduce this high-frequency noise.

Assuming the feedback is operating correctly and the system is stable, from a time domain point of view, the signal $X(n)$ is bounded, and as well as the integrator has an infinite dc gain, the average value of his input must be zero. Therefore, in a first-order $\Sigma \Delta$ modulator, the average value of the output signal must equal the average of the input signal. For more information on the subject see reference [4] and [9].

**First-order $\Delta \Sigma$ Modulator**

One way of implementing a first-order $\Delta \Sigma$ modulator is using switched-capacitor circuits. An example of a modulator is presented in Figure 2.5. The modulator consists on an integrator and a comparator working as a 1-bit quantizer. This type of implementation has the advantage of including the sample-and-hold functionality inherently in the switched-capacitor input circuit of the integrator.

![Figure 2.5 - Typical Sigma delta modulator.](image_url)
2.2 Used Topology

As referred in section 2.1, in integrated temperature sensors, a junction is used for obtaining a voltage proportional to the temperature, and an A/D converter translates it into a digital word. The topology of the analog part used in this thesis is presented in Figure 2.6. The analog part consists of a PTAT circuit and of a sigma delta modulator. The PTAT circuit uses two biasing currents, $I_{c1}$ and $I_{c2}$, and the bipolar junction transistor.

\[ Q_3 = (V_{BE1} - V_{ref}) \times C_3 \]  
(2.9)

In order to explain how this PTAT voltage is obtained the circuit is analysed without feedback. In phase one ($\Phi_1$ closed and $\Phi_2$ open), the bipolar junction biased with $I_{c1}$ current creates a $V_{BE1}$ voltage. Thus, the charge at the capacitor $C_3$ is given by equation (2.9).

\[ Q_3 = (V_{BE1} - V_{ref}) \times C_3 \]

In phase two ($\Phi_1$ open and $\Phi_2$ closed), because the current changes to $I_{c2}$, the voltage at the left side of the $C_3$ changes to $V_{BE2}$. Thus, giving a charge difference of:

\[ Q_3 = (V_{BE1} - V_{ref} - V_{BE2} + V_{ref}) \times C_3 \]

\[ Q_3 = \Delta V_{BE} \times C_3 \]  
(2.11)

Therefore, the voltage between the two terminals of $C_3$, is a PTAT voltage (see section 2.1).

Consider now the circuit with feedback. If the DAC output is equal to $V_{ref}$, then the charge in $C_1$ will be null, as justified by equation (2.12).

\[ Q_{11} = (V_{ref} - V_{ref}) \times C_1 = 0 \]  
(2.12)

Moreover, if the DAC output is equal to gnd, the charge in $C_1$ is given by equation (2.13).

\[ Q_{12} = (0 - V_{ref}) \times C_1 \]  
(2.13)

Using equations (2.12) and (2.13), we have two types of increments at the output of the op-amp.
(equations (2.14) and (2.15)).

\[
\Delta V_{i01} = \Delta V_{BE} \frac{C_3}{C_2}
\]

\[
\Delta V_{i02} = \Delta V_{BE} \frac{C_3}{C_2} - V_{Ref} \frac{C_1}{C_2}
\]

Analysing the comparator it can be seen that the signal \(V_{out}\) becomes positively saturated when the output of the integrator is greater than \(V_{ref}\). Therefore, in order to make the system stable, in the next phase, the output of the integrator must go down. In order to do this the output of the D/A converter must be \(\text{agnd}\), and \(\Delta V_{i02}\) must be negative.

\[
\Delta V_{i02} \leq 0
\]

From equations (2.15) and (2.16) we can obtain equations (2.17) and (2.18).

\[
\Delta V_{BE\max} \frac{C_3}{C_2} - V_{Ref} \frac{C_1}{C_2} \leq 0
\]

\[
V_{Ref} \geq \Delta V_{BE\max} \frac{C_1}{C_1}
\]

Another constrain is due to the fact that the reference voltage is limited to the power supply, and we don’t want the output of the integrator to be saturated. This restriction leads to equation (2.19).

\[
\Delta V_{BE\max} \frac{C_3}{C_2} + V_{Ref} \frac{C_1}{C_2} < avdd
\]

Therefore, the output of the integrator will be reduced according to (2.15) when \(V_{out} = 1\) and will be increased according to (2.14) for \(V_{out} = 0\), within safety limits, contributing for the stability of the system.

\[\text{Digital part}\]

In order to convert the bit stream from the modulator output into a digital word, a digital block is needed. This block, as described in section 2.1.3, is a decimation filter, and can be as simple as a counter.

Therefore, the digital part of the sigma delta converter simply counts the number of ‘1’s at the output of the modulator in \(2^n\) periods (n is the number of bits) of the sampling frequency.

Table 2.1 presents the time required to make the conversion of a temperature sample in the range from 10 bits to 19 bits.
<table>
<thead>
<tr>
<th></th>
<th>2u (fs=500kHz)</th>
<th>1u (fs=1MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>19 bits</td>
<td>1.049s</td>
<td>0.524s</td>
</tr>
<tr>
<td>18 bits</td>
<td>0.524s</td>
<td>0.262s</td>
</tr>
<tr>
<td>16 bits</td>
<td>0.131s</td>
<td>0.066s</td>
</tr>
<tr>
<td>12 bits</td>
<td>8.2ms</td>
<td>4.1ms</td>
</tr>
<tr>
<td>10 bits</td>
<td>2.05ms</td>
<td>1.02ms</td>
</tr>
</tbody>
</table>

Table 2.1 - Time required for the conversion with different number of bits.

As it can be seen, the resolution of the converter could be as high as 19 bits, due to the fact that temperature changes slowly. Although the conversion with fewer bits is faster, we will see in the next section that it leads to larger errors.

Assuming that the reference voltage is fixed and using equation (2.17), the maximum input voltage is given by equation (2.20).

\[ \Delta V_{BE_{\text{max}}} = V_{\text{Ref}} \frac{c_1}{c_3} \]  

(2.20)

Thus, the \( \Delta V_{BE} \) can be divided in digital words as shown in equation (2.21).

\[ \Delta V_{BE} = \frac{m}{2^n} V_{\text{Ref}} \frac{c_1}{c_3} \]  

(2.21)

In equation (2.21) \( m \) represents the decimal value of the digital word, and \( n \) represents the number of bits.

Therefore, using (2.20) and (2.3), we can relate the temperature and the digital word in equation (2.22).

\[ T = \frac{m}{2^n} V_{\text{Ref}} \frac{c_1}{c_3} \frac{1}{C_3} \]  

(2.22)

In the next section it will be discussed how the components of the sigma-delta modulator, can affect the measure of the temperature.
2.3 Matlab Implementation

In this section the topology presented in chapter 2.2 is modelled and simulated. The objective is to create a model of the circuit presented in Figure 2.6, in order to analyse the requirements for each block. The modelling and simulation was carried out using Matlab®.

2.3.1 Analog Part

**Junction**

The junction, as well as the whole PTAT circuit, was replaced in the Matlab® by two fixed voltages. As shown in Figure 2.7, these voltages represent here $V_{BE1}$ and $V_{BE2}$.

**Sigma delta modulator**

The model created in Matlab® for the sigma delta modulator is presented in Figure 2.7.

![Figure 2.7 - Matlab model of the PTAT circuit and the sigma delta modulator.](image)

Figure 2.7 includes some new components that were added in Matlab® for modelling purposes. The switches have an on resistance of 100 ohms and an off resistance of 12T ohms, making them almost ideal. A flip-flop is introduced because the comparator needs to maintain the state during phase one. Using (2.18) and (2.19), and taking into account equation (2.23), for an avdd of 2.55V we obtain: $C_1 = 1\, pf$, $C_2 = 1\, pf$, $C_3 = 6\, pf$ and $V_{REF} = 1.1\, V$. 

\[ \Delta V_{BE_{max}} = \Delta V_{BE_{160^\circ C}} \] (2.23)

Replacing these values in (2.21) and (2.22), we get equations (2.24) and (2.25).

\[ \Delta V_{BE} = \frac{m}{2^n} \times 1.1 \times \frac{1}{6} \] (2.24)

\[ T = \frac{m}{2^n} \times 1.1 \times \frac{1}{6} \times \frac{1}{296.18 \times 10^{-6}} \] (2.25)

A simulation of the sigma delta modulator model of the Figure 2.7 is presented in Figure 2.8. In this simulation, a frequency of 1MHz was used, a \( \Delta V_{BE} \) of 0.02V and an ideal op-amp (infinite gain and bandwidth) were considered.

![Figure 2.8 - Simulation of the ΔΣ modulator.](image)

Analyzing the graphic of Figure 2.8, it can be seen that the voltage at the output of the integrator rises \( \Delta V_{BE} \times 6 = 0.12 \ V \) each period, according to (2.14). When this voltage reaches \( V_{ref} \), the modulator output changes to one and, in the next phase 2, the integrator output falls \( \Delta V_{BE} \times 6 - V_{ref} = -0.96 \ V \), according to (2.15).

Another simulation is presented in Figure 2.9, however now a non-ideal op-amp was considered (finite gain and bandwidth).
Although the output of the integrator takes more time to reach $V_{Ref}$, the output of modulator remains the same. This suggests that it is important to make a precise analysis in order to translate the sensor specifications into op-amp requirements.

In order to reach the exact minimum specifications, a model for the op-amp was created. This model is presented in Figure 2.10.

\[ R_{in} = 10 \, M\Omega, \, R_{p1} = 1 \, k\Omega, \, C_1 = \text{variable}, \, R_{out} = 100 \, \Omega, \, \text{Gain} = \text{variable}. \]

The resistance $R_{p1}$ and the capacitor $C_1$ introduce a pole that defines the bandwidth. The frequency of the pole is given by equation (2.26).

\[ f_{p1} = \frac{1}{2\pi \times R_{p1} \times C_1} \]  

(2.26)

Therefore, changing $f_{p1}$ and the gain, it is possible to identify the required specifications.
2.3.2 Digital

The digital part of the A/D sigma delta converter is presented in Figure 2.11. It consists of two counters. The upper counter is responsible for counting the number of ‘1’s at the output of the modulator. This upper counter is stopped by the lower counter according to the number of bits chosen for the converter.

![Digital Model Diagram](image)

Figure 2.11 - Digital model for the digital part of the ∆Σ converter.

As referred in Chapter 1, a resolution of 1ºC is needed. Therefore, according to equation (2.22), the minimum number of bits of the converter is 10 due to the fact that we have a quantification step of 0.605 ºC.

The number of bits chosen for this model of the sigma delta A/D converter is 12 bits because it counts 4096 periods of the sampling frequency and it gives the accuracy needed in error evaluation.

2.3.3 Results

To achieve the accuracy presented in Chapter 1 for the temperature sensor there are specifications for the op-amp, as the gain, the gain-bandwidth product and the offset voltage that must be respected. All analysis were done at the sampling frequency of 1MHz and for a $\Delta V_{BE}$ corresponding to a temperature of 160.27ºC, so that, according to equation (2.22), the integer digital word 717 (in decimal) should be obtained in the absence of measurement error.
As shown in Figure 2.12, the temperature error diminishes as the op-amp gain rises. When rising the number of bits, we are reducing the quantification step, that is 0.605°C for 10 bits and 0.1511°C for 12 bits. Thus, the error is also reduced as the number of bits increases.

Therefore, by the analysis of the graph in Figure 2.12, it is possible to conclude that the gain of the op-amp is extremely important for the correct measurement of the temperature, and if we want to limit the error to a maximum of 1°C, the gain must be at least 6000 (or 75.5 dB).

The gain-bandwidth product is a very important factor too due to the fact that this op-amp is included in a switched capacitor circuit. Thus, maintaining the gain of the op-amp fixed to 80dB, an analysis of the gain-bandwidth product was done according to equation (2.27). The result of this analysis is presented in Figure 2.13.
Analysing Figure 2.13, it can be seen that, for the range of the gain-bandwidth product presented, that the error introduced is not very relevant. A gain-bandwidth product between 5MHz and 10MHz is acceptable since the resulting temperature error is limited between 0.21ºC and 0.1ºC.

Another analysis was done to evaluate the impact of the op-amp dc gain maintaining the gain-bandwidth product constant. Therefore, the gain is increased as the bandwidth (fp1) decreases.
Analysing the graph of the Figure 2.14, as it was expected, the error in the temperature diminishes as the gain rises. However, for high gain, the error starts to stabilize. Comparing the two graphs, it can be seen that the error with 5MHz gain-bandwidth is greater than the error with 10MHz. Therefore a gain bigger than 90 dB, and a gain-bandwidth of at least of 5MHz are the ideal specifications of the op-amp for the modulator’s best performance.

The last analysis was done in order to evaluate the impact of the offset voltage of the op-amp in the temperature measurement error. A $V_{os}$ voltage was placed in series with the $V_{Ref}$ at the positive input of the op-amp. We change $V_{os}$ and we measure the temperature error. In Figure 2.15 the error is represented as a function of the $V_{os}$ voltage, for a fixed gain of 80dB.

![Graph: Error in temperature as a function of the op-amp offset voltage.](image)

Analyzing the graph of Figure 2.15, for small increases of $V_{os}$, the error in temperature rises significantly. Notice that the offset voltage scale is µV and the error scale is m°C. Thus, for 200µV of offset voltage we already have an error approximately of 0.8°C.

In a standard op-amp topology the typical offset voltage is around 4mV [9]. With a standard op-amp the temperature error, according to the graph, would be huge and intolerable. Therefore, it is necessary to create an auxiliary circuit for compensation of the offset voltage.
From these analyses it can be concluded that the op-amp is a critical component of the modulator.

All the tests were done at a sampling frequency of 1MHz. However, due to the fact that this frequency is very high for temperature measurement it is possible to use a lower frequency. Reducing the frequency will make the system more accurate, with less error and giving more margin for the gain-bandwidth product of the op-amp.

The final specification of the op-amp and the A/D converter is presented in Table 2.2.

<table>
<thead>
<tr>
<th>DC Gain (op-amp)</th>
<th>&gt;90 dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain-Bandwidth Product (op-amp)</td>
<td>&gt;5MHz</td>
</tr>
<tr>
<td>Offset Voltage (op-amp)</td>
<td>&lt;40uV (with auxiliary circuit)</td>
</tr>
<tr>
<td>Number of Bits</td>
<td>10-19 bits</td>
</tr>
<tr>
<td>Sampling Frequency</td>
<td>&lt;1MHz</td>
</tr>
</tbody>
</table>

Table 2.2 - Op-amp and A/D converter specifications.

The most critical parameter of the whole circuit is the offset voltage of the op-amp. We will see in Chapter 3 how is possible too reach such a low offset voltage.
Chapter 3
Implementation in SMIC

In this chapter the blocks of the temperature sensor are explained, designed and simulated. Moreover, a first typical analysis of the analog part of the sensor is performed. In the first section, the technology parameters are obtained. In sections 3.2, 3.3, 3.4 and 3.5 the op-amp, the phase generator, the switches and the bias generator, respectively, are designed, implemented and simulated. The analog part of the temperature sensor is presented in section 3.6. The offset control circuit is implemented and simulated in section 3.7. In section 3.8 a CCO (current controlled oscillator) is presented and simulated. Finally, section 3.9 includes some layout considerations.


3.1 Technology Parameters

Before we can start to design the JTM (junction thermal monitor), we need to know the technology parameters of the target technology, such as, $K_p$ and $V_{TH}$. These parameters were not known and consequently they were extracted by simulation.

Figure 3.1 shows the circuit used to extract these parameters for a high voltage PMOS transistor. As it can be seen, the drain is connected to the gate, to put the transistor always in the saturation region. A current of $1\mu A$ is used to bias the transistor because it is the default bias current of the temperature sensor.

![Figure 3.1 - Circuit for extraction of $K_p$ and $V_{TH}$](image)

Assuming an overdrive voltage ($V_{OO}$) of 200mV, by simulation, we obtain the values for the width and length of the PMOS transistor:

$$W(\text{width})=4\mu$$

and

$$L(\text{length})=3.14\mu.$$
These values of W and L can be replaced in the equation of the saturation current (3.1) in order to obtain $K_p$[9].

$$I_D = \frac{1}{2}K_p \frac{W}{L}(V_{OD})^2 \quad (3.1)$$

$$V_{OD} = V_{GS} - V_{TH} \quad (3.2)$$

For this technology, the $K_p$ for the PMOS transistor obtained is $39.25 \mu A/V^2$.

The threshold voltage ($V_{TH}$) for the PMOS transistor was taken experimentally too and it is $0.655 \, V$.

The same type of simulation was done with a NMOS transistor (Annex B). The parameters, $V_{TH}$ and $K_p$, for the PMOS and the NMOS transistors are listed in the Table 3.1.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$K_p(\mu A/V^2)$</th>
<th>$V_{TH}(V)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS</td>
<td>39.25</td>
<td>-0.655</td>
</tr>
<tr>
<td>NMOS</td>
<td>153.25</td>
<td>0.594</td>
</tr>
</tbody>
</table>

Table 3.1 - PMOS and NMOS transistors parameters.

For this technology, the relation between the NMOS $K_p$ and the PMOS $K_p$ is almost four times. This means that the NMOS transistors have approximately four times more transconductance than the PMOS transistors.

### 3.2 Op-Amp

The amplifier in the sigma delta modulator is a critical component (Chapter 2). Thus, it is important to carefully design this module. Table 4.2 presents the specifications of the op-amp obtained by the Matlab® simulations presented in Chapter 2.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>&gt;90 dB</td>
</tr>
<tr>
<td>Gain-Bandwidth Product</td>
<td>&gt;5 MHz</td>
</tr>
<tr>
<td>Offset Voltage</td>
<td>&lt;40uV (with auxiliary circuit)</td>
</tr>
</tbody>
</table>

Table 3.2 - Specifications of the op-amp.

Although the op-amp needs a relatively high dc gain, only a small gain-bandwidth product is required.
Since a single stage topology could never achieve this high dc gain, a two-stage or a Gain-Boosted topology [5] must be used.

Analysing this two topologies, according to reference [5], we see that the Gain-Boosted has a high dc gain but consumes a lot of power. However, a two stage topology has less power consumption and even higher gain, at the cost of a low GBW.

Thus, the op-amp chosen for the modulator is the two-stage op-amp presented in Figure 3.2. As the figure shows, the first stage is a folded-cascode topology and the second stage a class AB amplifier.

\[ |A_{VFc}| = g_{m,2b} \left\{ \frac{g_{m,mc4b}r_{o,mc4b}}{r_{o,m4b}r_{o,m2b}} \right\} \left\{ \frac{g_{m,mc3b}r_{o,mc3b}}{r_{o,m3b}} \right\} \]  

(3.3)

Although this topology has a high dc gain, unfortunately this gain is not enough for the JTM circuit.
Analysing the output of the folded-cascode we see that its output swing is limited to a maximum and a minimum given by equations (3.4) and (3.5) respectively.

\[ V_{\text{OUT, max}} = avdd - |V_{ODm3b}| - |V_{ODm3b}| \]  
\[ V_{\text{OUT, min}} = V_{ODm4b} + V_{ODm4b} \]  

Since neither the gain nor the output swing are in the limits of the specifications, a second stage is introduced, and it is represented in Figure 3.3.

The class AB topology not only will increase the gain, but will increase the output swing too. The small signal analysis of the class AB stage is presented in Figure 3.4.
Figure 3.4 - Small signal analyse of the class AB stage.

Considering the inputs signals $V_x$ and $V_{in}$, and analysing Figure 3.4, equations (3.7) and (3.8) are obtained.

\[
V_x = V_{in} + \left( \frac{r_{ds(m6b downt)}}{r_{ds(m5b)}} \right) \left( g_{m(m6b downt)} V_{in} - g_{m(m5b)} V_x \right) \tag{3.6}
\]

\[
V_x = V_{in} \left( \frac{\frac{1}{1+g_{m(m5b)}} \left( \frac{r_{ds(m5b)} V_{in}}{r_{ds(m5b)}} \right)} {\frac{1}{1+g_{m(m6b downt)}} \left( \frac{r_{ds(m6b downt)}}{r_{ds(m5b)}} \right)} \right) \tag{3.7}
\]

\[
V_{out} = -\left( \frac{r_{ds(m7b)}}{r_{ds(m6b downt)}} \right) \left( g_{m(m6b downt)} V_{in} + g_{m(m7b)} V_x \right) \tag{3.8}
\]

Replacing equation (3.7) in equation (3.8), depending on the input, $V_{in}$ or $V_x$, the gain of the class AB is given respectively by equations (3.9) and (3.10).

\[
A_{V_{out}/V_{in}} = -\left( \frac{r_{ds(m7b)}}{r_{ds(m6b downt)}} \right) \left( g_{m(m6b downt)} + g_{m(m7b)} \left( \frac{1}{1+g_{m(m5b)}} \left( \frac{r_{ds(m5b)}}{r_{ds(m6b downt)}} \right) \right) \right) \tag{3.9}
\]

\[
A_{V_{out}/V_x} = -\left( \frac{r_{ds(m7b)}}{r_{ds(m6b downt)}} \right) \left( g_{m(m6b downt)} \left( \frac{1}{1+g_{m(m5b)}} \left( \frac{r_{ds(m5b)}}{r_{ds(m6b downt)}} \right) \right) \right) + g_{m(m7b)} \tag{3.10}
\]

In order to achieve a good PSRR (see reference [10]), equations (3.9) and (3.10) must be equal, resulting in equation (3.11).
Using equation (3.11), the gain of the class AB is given by equation (3.12).

\[ A_{V_{AB}} = -\left( \frac{r_{ds(m\gamma b)}}{r_{ds(m\gamma b)}} \right) \left( g_{m(m\beta b)} + g_{m(m\gamma b)} \right) \]  

(3.12)

Thus, the overall gain of the whole topology is given by equation (3.13).

\[ A_V = A_{V_FC} \times A_{V_{AB}} \]

(3.13)

Analysing the output swing of the class AB in relation to the folded-cascode, there is an increase by one overdrive voltage. The maximum and the minimum possible outputs of the class AB are given by equations (3.14) and (3.15) respectively.

\[ V_{OUT,max} = avdd - |V_{OD,1}| \]  

(3.14)

\[ V_{OUT,min} = V_{OD,5} \]  

(3.15)

Therefore, it is possible to conclude that, with this topology, we can achieve a high gain and a high output swing.

**Sizing**

In this section the considerations for the design of the op-amp with class AB output are discussed. Starting with the folded-cascode and ending with the class AB stage. We will see shortly that the main problem is the low power supply.

For the design of the op-amp, the specifications listed in Chapter 2 were used. The first considerations for the design of the op-amp were the currents (see Figure 3.2) and the overdrive voltages.

In Figure 3.2 the bias current applied to the differential pair is 4µA. Consequently each branch of the pair will have 2µA. From equation (3.3), we see that the gain increases with the increase of the transconductance of m2b (or m2a).

In order to have a high transconductance, we need a low overdrive voltage at the transistor (see reference [10]). Thus an overdrive voltage of 20mv is used for sizing the differential pair.

The biasing circuit for the NMOS cascode transistor, mc4b, is presented in Figure 3.5.
Figure 3.5 - Biasing circuit for the cascode transistor.

Transistors mb15 and mc4b were designed to be matched. Therefore, vxb14 and vx2b are virtually the same net. The main objective of this topology is to force the transistor m4b to have a fixed $V_{ds}$ voltage.

The transistor mb14 is designed for an overdrive voltage of 100mV, and it must be in the saturation region. Therefore, the $V_{ds}$ voltage applied to mb14 must be at least 100mV greater than the overdrive voltage. Analyzing the circuit we obtain equations from (3.16) to (3.19):

\[ V_{DS,mb14} \geq V_{0,mb14} + V_{edge} \]  

(3.16)

\[ V_{DS,mb14} \geq V_{IB} - V_{TH} + V_{edge} \]  

(3.17)

\[ V_{GS,mb15, dnw} = V_{IB} - V_{DS,mb14} \]  

(3.18)

\[ V_{GS,mb15, dnw} \leq V_{TH} - V_{edge} \]  

(3.19)

Therefore, by equation (3.19), the transistor mb15_dnw must be in the subthreshold region. In order to do this, the transistor has to be biased with low current.

Knowing that $V_{0,mb14} = 0.1V$, $V_{TH} = 0.6V$, $V_{edge} = 0.1V$ and replacing these values in equations from (3.16) to (3.19), equation (3.20) is obtained.

\[ V_{GS,mb15, dnw} \leq 0.5V \]  

(3.20)

However, mb15_dnw is affected by body effect, and the $V_{TH}$ voltage will not be constant. Therefore,
the transistor is made in a deep n-well in order to allow the free polarization of the transistor substrate and insure the absence of body effect.

Class AB

Considering now the class AB output stage, we see that the PMOS and the NMOS transistors are symmetric. Thus the analysis will be simplified to the NMOS case. The NMOS side of the class AB is represented in Figure 3.6.

As it is shown in Figure 3.6, two low-voltage NMOS transistors, m8b and mb10, are introduced. This is done due to the low power supply. Suppose that instead of low-voltage we were using high-voltage transistors. Knowing that mb10 and m8b are matched, and m8b is in the output stage, an overdrive voltage of 200mV is needed in order to reduce the output noise. Thus considering equations (3.21) and (3.22), in the biasing branch (mb10, mb9_dnw, and mb8), we have a minimum voltage giving by equation (3.23).

\[
V_{OD,m8b} = 200mV = V_{OD,mb10}
\]

\[
V_{OD,mb9} = 50mV
\]  

\[
V_{min} = V_{DS,m8b} + V_{TH,mb9_dnw} + V_{OD,mb9_dnw} + V_{TH,mb10} + V_{OD,mb10}
\]  

Replacing equations (3.21) and (3.22) in equation (3.23) we get equation (3.24).

\[
V_{min} = 50mV + 600mV + 50mV + 600mV + 200mV \quad V_{min} = 1.5V \approx avdd
\]

A difference of 50mV between the \(V_{min}\) and the avdd would not be tolerable due to changes of the \(V_{TH}\) and power supply. Thus, a low voltage transistor is used due to its lower \(V_{TH}\) that is typically 300mV.
Using equation (3.23) with a low voltage transistor we get equation (3.25).

\[ V_{\text{min}} = 1.2V < \text{avdd} \]  

(3.25)

From the result in equation (3.25), we conclude that with a low voltage transistor we get more margin for possible changes in the transistor’s \( V_{TH} \) and in the power supply. Nevertheless, we need to make mb9 in a deep n-well in order to reduce its \( V_{TH} \), since this transistor would suffer from body effect.

A problem arises with the low voltage transistor in the output stage, due to the fact that its \( V_{ds} \) voltage must be less than 1.2V. Thus, to prevent the disruption of the transistor, another transistor functioning as a switch (mc8b_dnw) is placed in series. With the gate of mc8b_dnw connected to avdd, the maximum \( V_{ds} \) voltage at m8b is given by equation (3.26).

\[ V_{\text{ds,mc8b}_\text{max}} = \text{avdd} - V_T \approx 1V \]  

(3.26)

Thus protection the transistor from damage and maintain the correct functionality of the circuit.

**Simulations**

Different simulations were made with the op-amp in order to extract the relevant parameters. In this section, the results of the AC open loop and Monte Carlo simulations are presented since they are the most important ones.

A test bench for the AC open loop analysis is presented in Annex C. The parameters presented in Table 3.3 are extracted from the typical simulation and in Figure 3.7 a simulation of the op-amp with corners is presented.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>126.07 dB</td>
</tr>
<tr>
<td>GBW</td>
<td>3.42 MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>88.74º</td>
</tr>
<tr>
<td>Gain Margin</td>
<td>29.98dB</td>
</tr>
</tbody>
</table>

Table 3.3 - Results from the typical simulation.
Figure 3.7 - AC simulation with corners for Vout equal to Vref.

As it is shown in Figure 3.7, the op-amp has a typical behaviour. According to references [5] and [10], the phase margin and the gain margin present excellent values. Comparing the results in Table 3.3 with the specifications for this block (section 2.3.3), the gain is achieved, however the GBW product is bellow the requirements. Therefore, since the sampling frequency when acquiring the temperature is not a critical parameter, it is changed from 1MHz to 500kHz, in order to maintain this GBW in the op-amp.

<table>
<thead>
<tr>
<th></th>
<th>Output = 207mV (-40°C)</th>
<th>Output =935mV (160°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gain</strong></td>
<td>89.15dB</td>
<td>126.51 dB</td>
</tr>
<tr>
<td><strong>GBW</strong></td>
<td>2.2 MHz</td>
<td>2.79MHz</td>
</tr>
<tr>
<td><strong>Phase Margin</strong></td>
<td>78.9°</td>
<td>80.89°</td>
</tr>
<tr>
<td><strong>Gain Margin</strong></td>
<td>31.5dB</td>
<td>33.97dB</td>
</tr>
</tbody>
</table>

Table 3.4 - Average results from simulations with corners.

Table 3.4 presents the results of the simulations with corners for the maximum (160°C) and the minimum (-40°C) possible outputs. When the output of the op-amp diminishes, the lowest gain is obtained. However, always according with the specifications.
In order to extract the offset voltage of the op-amp, a Monte Carlo simulation was done. The results of the simulation are presented in Figure 3.8, and its test bench is presented in Annex C.

![Figure 3.8 - Monte Carlo simulation of the op-amp.](image)

Analysing Figure 3.8, and knowing that $V_{\text{Ref}}$ is 0.55V, the offset voltage is given by equation (3.29).

\[ V_{\text{offset}_1} = 0.55 - 0.54505 \]  \hspace{1cm} (3.27)

\[ V_{\text{offset}_h} = 0.55482 - 0.55 \]  \hspace{1cm} (3.28)

\[ V_{\text{offset}_{\text{max}}} = 4.95 \text{mV} \]  \hspace{1cm} (3.29)

As it is shown in Figure 3.8, the histogram has a concentration of the offset voltage around $V_{\text{Ref}}$, meaning that the extremes have less probability of happen. However, the maximum should be taken into account. Therefore, for this op-amp it will be assumed an offset voltage of 5mV. This offset does not match the requirements and therefore an auxiliary circuit for compensation is needed. This circuit is described in section 3.7.
3.3 Phase Generator

The operation of the ΔΣ modulator is controlled by a nonoverlapping two-phase clock. During phase 1 (Φ₁ₓ closed and Φ₂ₓ open) the input voltage $V_{BE}$ is sampled in $C_3$, and in phase 2 (Φ₁ₓ open and Φ₂ₓ closed) the charge stored on $C_3$ is transferred to $C_2$ (see Chapter 2).

With this clocking arrangement, the time available for the integration and for the comparison are both one-half of a clock cycle. Since $Φ_{1₁}$ and $Φ_{2₁}$ suffer from charge injection, with the opening of the switches $Φ_{1₂}$ and $Φ_{2₂}$ slightly before $Φ_{1₁}$ and $Φ_{2₁}$, respectively, we can suppress the signal-dependent charge injection.

The circuit created for this purpose is presented in Figure 3.10.

Figure 3.9 - Analog part of the temperature sensor.

Figure 3.10 - Schematic of the phase generator.
The delayed phases are created with the delay introduced by the inverters. In order to achieve an appropriate delay in the inverters, the length of its transistors has to be large.

**Simulations**

In Figure 3.11 a typical simulation of the phase generator implemented is presented.

![Figure 3.11 - Typical simulation of the phase generator.](image)

As Figure 3.11 shows, phase 1 occurs 4ns before phase1d. This difference is enough for the correct function of the sigma delta as shown in section 3.6. Therefore, to suppress the signal-dependent charge injection, phase1 and phase1d will be applied to $\Phi_{12}$ and $\Phi_{13}$, respectively.
3.4 Switches

The topology of the switches implemented in the circuit of the sigma delta modulator is presented in Figure 3.12.

These switches use only a NMOS transistor in order to save area and due to the fact that the voltages at their terminals in the sigma delta modulator is always \( V_{\text{Ref}} \) or gnd. Considering the power supply and \( V_{\text{Ref}} \), 1.55V and 0.55V respectively, since the \( V_{GS} \) of the NMOS transistor M0 is given by equation (3.30), the overdrive voltage is obtained by equation (3.31).

\[
V_{GS} = v_{\text{dd}} - V_{\text{Ref}} = 1V
\]  \hspace{1cm} (3.30)

\[
V_{OD} = V_{GS} - V_{TH} = 405mV
\]  \hspace{1cm} (3.31)

Therefore, the transistor M0 has enough margins for variations in the \( V_{TH} \) or other parameters.

Consider the model present in Figure 3.13, where the two capacitances Cgd and Cgs are introduced. With these capacitances, when a transition at the gate of the NMOS transistor (M0) occurs, charge will be injected from the gate into the two terminals of the switch. To suppress this charge injection, two NMOS transistors are introduced (M4 and M5).
Consider the injection in the right side of the NMOS switch presented in Figure 3.13. As shown, when a positive edge occurs at the gate of M0, charge will be injected to node b. However, when the negative edge occurs at the gate of M4, the node b will be discharge. In order to guarantee that the charge injected in node b equals the discharged, equation (3.32) must be respected.

\[
C_{gd,M0} = C_{gs,M4} + C_{gd,M4}
\]  

(3.32)

Equation (3.32) implies that the dimensions of M0 must equal to the double of M4 or M5 (3.33).

\[
\frac{W}{L}_{M0} = 2 \times \left( \frac{W}{L}_{M4 \text{ or } M5} \right)
\]  

(3.33)

In Figure 3.14 a simulation of the switch working in the sigma delta modulator is presented.

As Figures 3.14 shows, the compensation of the charge injection is working properly for a sampling frequency of 500kHz. For more information on switches see reference [3].
3.5 Bias JTM generator

This block generates the two collector currents $I_{C1}$ and $I_{C2}$ of the bipolar transistor according to the respective phases $\Phi_{11}$ and $\Phi_{21}$. The circuit is presented in Figure 3.15 and it consists mainly on cascode current mirrors.

This block is one of the most important blocks in the temperature sensor because the $\Delta V_{BE}$ at the terminals of the transistor is obtained with these two currents [15]. Therefore, to guaranty a good precision in the currents, and that the relationship $I_{C1}/I_{C2}$ is maintained, cascode current mirrors are used. With this cascode topology the current is more accurate than with the simple mirrors due to the fact that a fixed $V_{ds}$ voltage is imposed at the mirroring transistors.

The $I_{C1}$ and $I_{C2}$ currents are respectively 310µA and 10µA, making the relation between them to be 31. Due to the low power supply the transistors must have a low overdrive voltage, however this voltage could not be very low because the precise of the current that passes in the transistors depends on how big this voltage is. Therefore in order to maintain the transistors in the saturated region and to have a good precision for the output current, equations from (3.34) to (3.36) are considered.

\[
V_{casc} = 0.3V \quad (3.34)
\]
\[
V_{DD,pmos} = 120mV \quad (3.35)
\]
\[
V_{DD,nmos} = 100mV \quad (3.36)
\]
According to (3.34), (3.35), (3.36) and the currents identified in Figure 3.15, the transistors are sized. Analysing Figure 3.15, it is possible to conclude that only one switched is required because the current of 10µA can be always present.

**Simulations**

A test bench is created to simulate this block and it is presented in Annex E. In order to have a realistic analysis, different simulations are done with the change of some parameters (corners). In Figure 3.16, simulations changing the bias current, power supply, temperature and parameters of the MOS transistors are presented.

Analyzing Figure 3.16, there is a significantly variation of the collector currents. However according to section 2.1.1, what is most important in this block is to maintain the relation between $I_{c1}$ and $I_{c2}$ even if the currents change. Therefore, in Table 3.5 the measures of the currents extracted from the simulations are presented in order to conclude about their relationship.
<table>
<thead>
<tr>
<th></th>
<th>$I_{C1}$ (µA)</th>
<th>$I_{C2}$ (µA)</th>
<th>$I_{C1}/I_{C2}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ideal values</td>
<td>310</td>
<td>10</td>
<td>31</td>
</tr>
<tr>
<td>Typical simulation</td>
<td>309.97</td>
<td>10.02</td>
<td>30.94</td>
</tr>
<tr>
<td>Corners With $I_{BIAS} = 1.2$ µA</td>
<td>370 (mean value)</td>
<td>12 (mean value)</td>
<td>30.74</td>
</tr>
<tr>
<td>Corners With $I_{BIAS} = 0.8$ µA</td>
<td>249 (mean value)</td>
<td>8.04 (mean value)</td>
<td>30.93</td>
</tr>
</tbody>
</table>

Table 3.5 - Average values of the currents $I_{C1}$ and $I_{C2}$ for different corners.

From the analysis of Table 3.5, it is possible to conclude that even with the variation of the currents, $I_{C1}$ and $I_{C2}$, the relationship $I_{C1}/I_{C2}$ stays approximately constant and around 31, meaning that the circuit is working properly.
3.6 Implementation of the Analog Module

With the blocks already presented and according to Figure 3.9, the analog module of the temperature sensor is implemented. In Figure 3.17 the schematic of the analog part of the temperature sensor (already with offset compensation) is presented.

![Figure 3.17 - Schematic of the analog part of the temperature sensor.](image)

A 1-bit digital to analog converter is implemented for the feedback of the sigma delta modulator. This DAC is presented in Figure 3.18 and it is as simple as one inverter and two switches (Chapter 2).

![Figure 3.18 - 1-bit DAC for the feedback in the sigma delta modulator.](image)

1this schematic is repeated in Annex F in landscape view.
A latch was provided by the Chipidea, and it was tested in order to see if any changes were needed. The relevant simulation is presented in Annex D and no modifications were required.

Finally a biasing block with typical current mirrors was implemented.

**Simulations**

A test bench is created in order to simulate this block and is presented in Annex F. Since the digital part was not implemented, the digital word cannot be obtained directly by simulation. Therefore a technique for measuring the digital word that is generated at the output of sigma-delta converter is used.

![Figure 3.19 - Technique for measuring the digital word.](image)

In Figure 3.19 the output of the integrator and the output of the modulator are presented. For a given input, when the integrator is in a steady state, its output is periodic as well as the output of the modulator. Therefore, considering $\Delta V_{UP}$ the positive variation and $\Delta V_{DOWN}$ the negative variation at the output of the integrator (Section 2.2) and $D$ the fraction of time that the output of the modulator is at a positive value, equation (3.37) is obtained.

\[
(1 - D)\Delta V_{UP} = |D\Delta V_{DOWN}| \iff D = \frac{\Delta V_{UP}}{\Delta V_{UP} + |\Delta V_{DOWN}|} \tag{3.37}
\]
The digital word at the output of the converter (counter) is given by equation (3.38).

\[ \text{Count} = D \times 2^n \quad \text{Where } n \text{ is the number of bits.} \quad (3.38) \]

This technique for measuring the digital word is only possible because the precision of the simulator in the values of \( \Delta V_{UP} \) and \( \Delta V_{DOWN} \) is very high.

For the simulations, the model of the bipolar transistor 2N3904 (see Annex F) was requested to Fairchild since it is commonly used as a temperature sensor.

A first typical analyse was done at 27ºC without the introduction of any offset voltage. The values of \( \Delta V_{UP} \) and \( \Delta V_{DOWN} \) were then taken from the simulation. Using (3.37) and (3.38), for a number of bits equal to ten, we obtain:

\[ \text{Count} = 497,5135. \]

Since this digital word has to be rounded, we can have two possible digital words:

\[ \text{Count}_{min} = 497 \]

and

\[ \text{Count}_{max} = 498 \]

Then using (2.24), the two possible temperatures readings from the digital are:

\[ T_{min} = 27.279^\circ C \quad \text{and} \quad T_{max} = 27.884^\circ C. \]

The difference between \( T_{min} \) and \( T_{max} \) is due to the quantification step. As the number of bits increase this error is reduced. This error is not taken into account in the next simulations because, for a number of bits greater than 12, the quantification step is too small. Thus, for a higher number of bits the temperature measured by the whole sensor at 27ºC is:

\[ T = 27.59^\circ C \]

giving an absolute error of 0.59ºC.

This error comes mostly from the \( \Delta V_{BE} \) created by the transistor 2N3904. Measuring this \( \Delta V_{BE} \) and using (2.3) we get:

\[ T = 27.64^\circ C. \]

This result means that the error in the sigma delta converter is 0.05ºC.

Another simulation is done forcing an offset voltage at the negative terminal of the amplifier. Introducing the offset voltage obtained for the op-amp in section 3.2 (5mV) we get, at 27ºC, a temperature reading of 51.41ºC. Since this error is not tolerable, an auxiliary circuit for the compensation of the offset voltage was implemented and it is presented in the next section.
3.7 Offset voltage compensation

A digital technique for the compensation of the offset voltage was implemented and the corresponding block diagram is presented in Figure 3.20. This offset voltage occurs due to the fact that transistors aren’t perfectly matched and the currents that pass in the differential pair or in the class AB stage are not equally distributed. However, the offset can be reduced just by injecting the right amount of current in the class AB stage (reference [12]). To know how much current is required, an auxiliary circuit using a current mirror DAC, switches, the latch and a digital control is implemented.

![Digital Control](image)

Connecting the two inputs of the op-amp to $V_{ref}$ it will saturate at the positive or negative power supply depending on its offset voltage.

Supposing the output of the op-amp is at $avdd$ as well as the output of the latch. The digital control will start to sweep the bits from “00000000” until the output of the latch reaches “0”. When this happens, we have the digital word corresponding to the minimum offset voltage possible and the digital control stops sweeping.

Considering the maximum offset measured in section 3.2 and knowing that it must be smaller than 40uV, some experimental analysis were done. In Table 3.6 the offset voltage obtained at the output of the op-amp for different injected currents is presented.
### Offset voltage vs Injected current

<table>
<thead>
<tr>
<th>Offset voltage</th>
<th>Injected current</th>
</tr>
</thead>
<tbody>
<tr>
<td>5mV</td>
<td>330nA</td>
</tr>
<tr>
<td>30µV</td>
<td>2nA</td>
</tr>
<tr>
<td>10µV</td>
<td>1nA</td>
</tr>
</tbody>
</table>

Table 3.6 - Offset voltage obtained in the op-amp for different injected currents.

As Table 3.6 shows, the injection of 2nA gives a 30µV variation in the offset voltage and a current of 330nA is needed to compensate 5mV of offset voltage. Therefore, since a minimum of 2nA is needed in order to get an error smaller than 40µV and a minimum output of 330nA to compensate 5mV of offset voltage, an 8-bit DAC must be implemented.

### Current DAC

The current mirror DAC implemented is presented in Figure 3.20. Since the current at the output of the DAC needs to be precise, cascode current mirrors are used (Section 3.3).

As Figure 3.21 shows, the DAC is divided in different stages. The first stage has the purpose of reducing in successive times the 500nA bias current to 2nA (LSB). In the other stages the current is successive mirrored from the LSB (Least Significant Bit) to the MSB (Most Significant Bit). The output current is controlled by a digital word applied to the switches, respectively, from the LSB to the MSB.

In the other stages, the block with the four most significant bits is separated from the block with the four last significant bits in order to save area in the mirroring transistors. For more information see reference [18].
Simulations

Simulations of the DAC are presented in Figure 3.22.

As Figure 3.22a) shows, the value of the least significant bit is very close to the expected. In Figure 3.22b) a sweep of the bits is performed and, as it shows, the current rises from 0nA to 518.39nA as expected.

Simulation with offset compensation

The circuit for the offset compensation was implemented in the sigma delta modulator as it is shown in Figure 3.17. The temperature sensor has two modes: the normal mode where the temperature is measured (en_ctr=0) and the control mode where the offset is compensated (en_ctr=1).

Introducing a 5mV offset voltage and going to compensation mode the digital word obtained is “10100010”. In Figure 3.23 the simulation in the compensation mode is presented.
Figure 3.23 - Current obtained in compensation mode.

Figure 3.23 shows that, when the modulator turns to “0”, the output of the DAC drives 329.67nA (“10100010”). Comparing this result with Table 3.6, the error in the compensation current is very low.

To obtain the digital word “10100010” the digital control must have a frequency of 15.625 kHz in the sweep of the least significant bit meaning that the total time for sweeping all bits is 8.192mS. Therefore because there are two DACs and the digital control could choose first the wrong one, the maximum time for the compensation of 5mV offset voltage is given by equation (3.39).

\[
T_{\text{max,comp}} = 8.192\text{m}s + 5.2064\text{m}s \approx 13.4\text{m}s
\] (3.39)

Applying the digital word “10100010” on the normal functioning of the sensor the new reading of temperature is 27.56ºC instead of 51.41ºC meaning that the compensation of the offset is working as expected.
3.8 CCO

The CCO (current controlled oscillator) was already implemented in TSMC 90nm technology. Therefore a porting was done from TSMC to the technology of the temperature sensor (SMIC).

This block also was also included in a project that was occurring at Chipidea.

The CCO circuit consists on a ring oscillator limited by the current that is injected in the inverters. This amount of current can be digitally selected in order to adjust the frequency (trimming). For more information see reference [16].

Some changes in the schematic had to be done from the original circuit in order to reach the specifications imposed by the company. Since parameters and design rules change from technology to technology the layout had to be changed also.

This CCO works at a nominal frequency of 32MHz and Table 3.7 presents the frequency from the normal simulation and the pos-layout simulation.

<table>
<thead>
<tr>
<th></th>
<th>Frequency from CCO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Simulation</td>
<td>33.66MHz</td>
</tr>
<tr>
<td>Pos-Layout Simulation</td>
<td>31.47MHz</td>
</tr>
</tbody>
</table>

Table 3.7 - Average Results of normal simulation and pos-layout simulation.

Analysing Table 3.7 this reduction in the frequency is normal since the layout introduces parasitic capacitances. Because the temperature sensor works at a frequency of 500kHz a digital divider is needed to lower the 32MHz of the CCO.
3.9 Layout

The layout consists in the design of the geometry of the various masks that are required during the fabrication process. For the layout implementation some considerations are taking into account:

- The wide transistors are composed by smaller transistors in parallel called fingers.
- Many contacts and vias at poly and metals are used in order to reduce voltage drop and resistance.
- The analog transistors are much wider than the digital ones, therefore in the analog parts it is common the use of many fingers in the transistors.
- When a precision matching is required between transistors, like in the differential pair, the fingers of one transistor should be interdigitated with the fingers of the other transistor. If the geometric center of both transistors is the same, this technique is called Common-Centroid [10].

The design rules of the technology used in the temperature sensor SMIC 0.13 were given by Chipidea. These rules were taken into account in the design of the layout and they specify the minimum or the maximum distances and dimensions between the masks. The program used for layout design was Virtuoso® from Cadence tools.

The layout of the op-amp, cco, phase generator, switch and the 1-bit DAC are presented in Figures 3.25, 3.26, 3.27a), 3.27b) and 3.27c) respectively. For all blocks the layout is verified by verification tools, according to Figure 3.24.
As Figure 3.24 shows, only when the block passes the three verification steps is ready for physical implementation. DRC stands for design rules check and the rules for SMIC 0.13 have to be respected in order to pass with no errors. ERC stands for electrical rules check and LVS stands for layout versus schematic. In the last one the layout is compared with the schematic of the block.

Figure 3.24 - Layout verification process.

Figure 3.25 - Layout of the op-amp.
From this chapter it is possible to conclude that when designing circuits with low voltage it is difficult to maintain the currents precise and constant. Simulations with corners are very important since they can simulate a more realistic situation and give accurate results. Also the compensation of the offset voltage in the temperature sensor is extremely important in order to reduce the measurement error. Therefore in a typical case, at 27°C, the temperature sensor with the transistor 2N3904 and 5mV offset voltage, will measure 27.56°C after offset calibration.
Chapter 4

Simulations and Results

In this chapter, simulations with corners of the temperature sensor are presented and analysed. In the first section the simulations without the offset voltage are presented. In section 4.2 the error introduced by the offset compensation is considered. The consumption of the temperature sensor is presented in section 4.3 as well as the final specifications of the temperature sensor.
4.1 Simulations of the temperature sensor without offset

Using the bipolar transistor 2N3904 functioning as the junction sensor, simulations were done with corners for different temperatures in order to conclude about the error in the temperature sensor, however, without the introduction of any offset voltage. In Figure 4.1 the simulation results with the variation of some parameters such as bias current, power supply, capacitances, resistances and parameters of the MOS transistors are presented. Each corner is a combination of these parameters.

![Error In the Temperature Sensor at 27°C](image)

Figure 4.1 - Error in the temperature sensor at 27°C for different corners.

Figure 4.1 shows the total error in temperature introduced by the whole circuit, at a temperature of 27°C, in the conditions of each corner. Analysing the figure, we conclude that for some corners this error could be as high as 0.9°C, however, all corners have errors below 1°C, therefore fulfilling the specifications. Since the change in corner parameters depends on the process of fabrication, on the circuit temperature and on other occasional factors, the average value is considered as the error of the temperature sensor and is presented in equation (4.1).

\[
\text{Error}_{\text{avg}, 27^\circ C} = 0.51^\circ C \tag{4.1}
\]

In order to find where the principal source of error is, the error introduced by the sigma delta modulator was extracted by simulation and it is presented in Figure 4.2.
As Figure 4.2 shows, for some corners, the error introduced by the sigma delta is approximately zero (6, 16, 25, 33) although for corners 3, 18 and 27 the error is around 0.3°C.

Therefore comparing the graphs of Figures 4.1 and 4.2, it is possible to conclude that the error comes mostly from the bias JTM circuit as it is refereed in Chapter 3. Since this error is within the specifications no changes were done in the circuits.

In Figure 4.3 the average error for each temperature is presented.
Notice that in these simulations all components of the temperature sensor are at the given temperature. Analysing Figure 4.3, the error is almost constant between -55°C and 130°C. However from 140°C the error starts rising. This increase in the error could be compensated by correcting this temperature gain. However this feature was not implemented in this thesis.

It is possible to conclude that the temperature sensor exhibits a correct functionality within the requirements, between -55°C and 130°C, with an error smaller than 1°C.

### 4.2 Simulations with offset Compensation

Since an offset voltage is always present in a real situation, the compensation is needed and the error introduced should be measured. In Table 4.1 is presented the average error in temperature introduced by the sigma delta modulator for three different simulations with corners at 27°C. The simulation with corners in this case is not very accurate since the corners will make the current change and with another calibration another digital word (current) can be obtained. Therefore, only the average error introduced by the sigma delta at 27°C is measured.

<table>
<thead>
<tr>
<th>Digital word</th>
<th>Average Error at 27°C [°C]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without offset</td>
<td>0.1125</td>
</tr>
<tr>
<td>With offset but without compensation</td>
<td>24.4</td>
</tr>
<tr>
<td>10100001 (compensated)</td>
<td>0.30857</td>
</tr>
<tr>
<td>10100010 (compensated)</td>
<td>0.27615</td>
</tr>
<tr>
<td>10100011 (compensated)</td>
<td>0.32912</td>
</tr>
</tbody>
</table>

Table 4.1 - Average error at 27°C introduced by the offset voltage.

As shown in Table 4.1 this offset compensation is extremely important and the average error introduced by the offset voltage with a 2nA resolution DAC is 0.164°C. Although the variation of the least significant bit introduces more error, this error is tolerable. Therefore, even with the introduction of the offset voltage, the temperature sensor error is within the specifications, below 1°C between -55°C and 130°C.
4.3 Power down simulations

From the test bench created, simulations are done in order to measure the current consumption when the circuit is functioning normally and when it is in power down mode (see Annex A). Figure 4.4 shows the current consumption of the whole circuit, starting in power down mode.

![Figure 4.4 - Current consumption in power down and in power up modes.](image)

As presented in Table 4.2, in power down mode a current of 1µA is consumed and when the circuit starts an average consumption of 375.8µA is obtained.

<table>
<thead>
<tr>
<th>Current Consumption (µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Up</td>
</tr>
<tr>
<td>Power Down</td>
</tr>
</tbody>
</table>

Table 4.2 - Average current consumption.

Since temperature changes slowly with time we can shutdown the temperature sensor when the temperature is not being measured in order to save energy and diminish the consumption. Supposing that one sample of the temperature must be measured by second, considering 10 bits and using (4.2) and (4.3) the average current consumption is given by equation (4.6).
\[
T = \frac{t_{\text{measure}}}{D_{\text{on}}} \tag{4.2}
\]
\[
I_{\text{avg}} = D_{\text{on}} \times I_{\text{power\_up}} + D_{\text{off}} \times I_{\text{power\_down}} \tag{4.3}
\]
\[
D_{\text{on}} = \frac{2.048\text{ms}}{15} \tag{4.4}
\]
\[
I_{\text{avg}} = 2.048 \times 10^{-3} \times 375.8\mu\text{A} + (1 - 2.048 \times 10^{-3}) \times 1.0086\mu\text{A} \tag{4.5}
\]
\[
I_{\text{avg}} = 1.776\mu\text{A} \tag{4.6}
\]

However if an offset calibration is needed using (3.39) the average current consumption is given by (4.8).

\[
D_{\text{on}} = \frac{2.048\text{ms} + 13.4\text{ms}}{15} \tag{4.7}
\]
\[
I_{\text{avg}} = 6.8\mu\text{A} \tag{4.8}
\]

With 6.8µA average current and a 1.55V power supply, consumption is very low and it is perfect for portable devices that need power saving.

Since we can perform one calibration per second, for the next analysis the time calibration will be discarded. For 5 samples per second the current is 4.85µA. However if we want more precision from the temperature sensor the consumption will rise as presented in Table 4.3.

<table>
<thead>
<tr>
<th>Number of bits</th>
<th>Time on (ms)</th>
<th>Consumption (µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 bits</td>
<td>2.048</td>
<td>4.85</td>
</tr>
<tr>
<td>11 bits</td>
<td>4.096</td>
<td>8.68</td>
</tr>
<tr>
<td>12 bits</td>
<td>8.192</td>
<td>14.89</td>
</tr>
<tr>
<td>13 bits</td>
<td>16.384</td>
<td>31.71</td>
</tr>
<tr>
<td>14 bits</td>
<td>32.768</td>
<td>62.41</td>
</tr>
<tr>
<td>15 bits</td>
<td>65.536</td>
<td>122.81</td>
</tr>
<tr>
<td>16 bits</td>
<td>131.072</td>
<td>246.63</td>
</tr>
</tbody>
</table>

Table 4.3 - Consumption for 5 samples per second without calibration.

Analysing Table 4.3, with the increase of the number of bits maintaining the five samples per second, the consumption will rise. There is a commitment here, if we want to have more precision the circuit will have more consumption.
Raising the number of samples per second, in order to make a good consumption the number of bits has to diminish too. Analysing Table 4.3 it is possible to conclude that with 5 samples per second more than 16 bits are not possible. The maximum number of samples per second is limited to the time that it takes to get one sample with the specific number minimum of bits. Therefore, for 10 bits, the maximum number of samples is 488 per second. In Table 4.4 the final specifications of the temperature sensor obtained by simulation are presented.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td></td>
<td>SMIC 0.13 5-Metal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature measurement</td>
<td>-55</td>
<td>27</td>
<td>130</td>
<td>°C</td>
</tr>
<tr>
<td>(maximum error of ±1°C)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td>-55</td>
<td>27</td>
<td>160</td>
<td>°C</td>
</tr>
<tr>
<td>Vdd</td>
<td>1.5</td>
<td>1.55</td>
<td>1.6</td>
<td>V</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>0</td>
<td>5</td>
<td>488</td>
<td>Hz</td>
</tr>
<tr>
<td>Digital Clock</td>
<td>-</td>
<td>32</td>
<td>-</td>
<td>MHz</td>
</tr>
<tr>
<td>Analog Clock</td>
<td>-</td>
<td>500</td>
<td>-</td>
<td>kHz</td>
</tr>
<tr>
<td>Power down consumption</td>
<td>-</td>
<td>1</td>
<td>-</td>
<td>µA</td>
</tr>
<tr>
<td>Power on</td>
<td>4.85</td>
<td>-</td>
<td>375.8</td>
<td>µA</td>
</tr>
<tr>
<td>Ibias</td>
<td>0.8</td>
<td>1</td>
<td>1.2</td>
<td>µA</td>
</tr>
</tbody>
</table>

Table 4.4 - Final specifications of the temperature sensor circuit.
Chapter 5

Conclusion

In this chapter the global conclusions of this work are presented and future developments are discussed.
The temperature sensor presented in this thesis was developed at Chipidea, where a good familiarization with the CAD (computer aided design) tools for the design of microelectronic circuits was acquired. The Cadence tools that were used proved to be user friendly and very important in the design of schematic and layout. Since this work was developed in a company environment, the capacity to work and interact with a team was also acquired.

The purpose of this work was to develop an integrated low voltage temperature sensor with an accuracy of 1°C with offset compensation. The design of microelectronic circuits with low voltages is difficult in order to maintain the transistors in the saturation region and to obtain precise currents. However, the specifications were achieved and the temperature sensor has a good performance in the simulations, with an error as low as half a degree at ambient temperature (see Table 4.4).

In order to achieve more accuracy, like in reference [1], the PTAT or bias JTM generator block needs to be changed, since it is the principal source of error. A possible away of improving it is to trim the bias PTAT currents, so that they can be adjusted in order to obtain more accurate digital words.

The temperature sensor has an error bellow 1°C between -55°C and 130°C.

The technique introduced for the offset voltage compensation proved to be very efficient in reducing the error in the temperature measurement. Since this technique is digitally controlled it can be further explored and expanded in order to improve even more the temperature sensor. With 8 bits offset control it was possible to reduce the op-amp offset to 30uV.

Another important factor is the average current consumption that can be different according to the number of bits chosen for the A/D converter or the number of samples per second chosen for the temperature sensor. The sensor can have a current consumption as low as 5µA with 10 bits and 5 samples/second.

Therefore, it is possible to conclude that an important commitment exists between accuracy, and area or consumption. Depending on the application, this trade off must be evaluated. In the case of the designed temperature sensor, it is perfect for the use in portable equipment since it works with a power supply of 1.55 V and exhibits very low current consumption.
Annexes

In Annex A a power down example is presented and discussed. In the other annexes auxiliary test benches, schematics and simulations are presented.
A. Annex - Power down

In every block a power down mode is implemented in order to allow the circuit to be turned off and reduce consumption. Because the method used for power down is the same in all blocks, only one example is presented. In Figure A.1 a typical current mirror with power down is presented.

As Figure A.1 shows, the transistors M13 and M19 are introduced in order to connect the gates of M2 (or M0) and M1 (or M4) to gnd and avdd, respectively. Therefore, when M13 and M19 are “on” (ond = "0" and onz = "1"), the transistors of the current mirror are cut-off and the circuit is in power down mode. When the circuit is turned on (ond = "1" and onz = "0") M13 and M19 are “off” and the current mirror maintains the normal function. With this technique it is possible to shutdown the circuit and diminish almost to zero the current consumption.
B. Annex - Test bench for parameter extraction

Figure B.1 - Test bench for parameter extraction.
C. Annex - Test bench of the op-amp and AC simulations

Figure C.1 - Test bench of the op-amp for AC simulations.
Figure C.2 - Test bench of the op-amp Monte Carlo simulations.
Figure C.3 - Op-amp schematic.
Figure C.4 - Op-amp AC simulations.
D. Annex - Latch simulations

Figure D.1 - Latch test bench.
Figure D.2 - Latch transitory simulation.
E. Annex - JTM bias (PTAT) test bench

Figure E.1 - Test bench for JTM bias.
F. Annex - Temperature sensor

Model Q2N3904NPN

.model Q2N3904NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259
+Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1
+Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75
+Tr=239.5n Tt=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
Figure F.1 - Temperature sensor schematic.
Figure F.2 - Test bench of the temperature sensor.
References


