Ultra Low Dropout Driver for Multicolor LEDs

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Abstract—Electronic applications with a display, like for example a cell phone or a PDA, must have all LEDs from the display shining with the same intensity. Meaning that the current that flows through a LED must be the same that flows through all the others.

To fulfill this requirement it was developed a current regulator to be able to drive a LED with a constant current between 0 and 50 mA, proportional to a digital eight bit word, with ultra low dropout voltage was developed. The lower the dropout voltage, the longer the battery life time is.

The regulator must work for multicolor LEDs, meaning LEDs with different voltage drops.

The proposed solution is able to drive a LED with a 50 mA current, with only 25 mV dropout voltage at 2% (meaning a 2% maximum current variation).

I. INTRODUCTION

A. Overview

The display is a fundamental part of a Cell phone, a PDA or a MP3 player, among others. Like any other part in this kind of applications, it must to be as good as possible in what concerns to three aspects, functionality, size and power consumption. Nowadays, the technology is so much developed, allowing such a small channel length transistors, that size is no longer the main concern. Beside the functionality, what matters the most now is how much the battery lasts.

B. Motivation and Contents

It usually takes more then one LED to light up the display of a cell phone or other portable equipment. It is crucial to have all the LEDs shining with the same intensity. How much a LED shines is determined by the current that flows through it. Meaning that in order to keep an uniform display, this current has to be the same for all the LEDs.

When a voltage is applied to a LED, with a value that is enough to turn the LED on, the current that flows through it is not necessarily the same that flows through a similar LED under the same circumstances. This happens because the $i(v)$ characteristic changes a little from LED to LED. Thus, the current that flows through each LED must be regulated.

The goal for this work is to make a circuit able to control the current that flows through a LED, as shown in figure 1. The anode of the LED is connected to a Charge Pump (see [6]), available from a different module. The voltage that drops across the regulator is called dropout voltage. There is a minimum voltage that the regulator needs in order to be able to regulate the output current. Dropout voltage is a necessary cost for the regulation. Power dissipation increases as the regulator dropout increases according to biasing circuit conditions. The point is to make the regulator work with as low dropout as possible, because the higher the dropout voltage, the less the battery lasts.

In order to control the LEDs brightness, an eight bit number is given as input. This way there are two hundred and fifty six levels of brightness, in other words, two hundred and fifty six levels of output current (LED current). This allows a very thin brightness adjustment. A digital to analog converter (DAC) translates this digital word into a current that is the input current for the regulator. This can also be seen in figure 1.

The circuit composed by the regulator and the DAC known as a LEDs driver.

Subsection 2.5 shows the overall specifications in detail.

The LED current is fifty times greater than the current that leaves the DAC. If all the input bits in the DAC are high, the DAC output current must be 1 mA, corresponding to a maximum LED current of 50 mA. The LED driver circuit can use a 1 µA bias current, available from a different module. Both analog and digital supply voltages are 2.5 V. The voltage applied to the anode of the LED comes from a Charge Pump, connected directly to the battery. It is mandatory that the voltage given by the Charge Pump reaches at least the LED threshold voltage plus the minimum dropout voltage.

A very important aspect to consider is the fact that this regulator has to work for multicolor LEDs. The voltage drop in a LED changes with the color of the LED. For example, a white LED drops around 3.6 V. If the Charge Pump is providing a voltage of 3.7 V for this white LED, it corresponds to a 100 mV dropout voltage. Now if this white LED is replaced by a red one, that drops around 1.8 V, the dropout will become 1.9 V. However, the regulator must work for this
value as it works for lower dropouts. To note that in a real situation the issue is due to the fact that there is only one ChargePump, so the same voltage is at all LEDs anodes and different regulators are connected to different LEDs (to the cathodes of the LEDs). Thus, not all dropouts are equal and a variation as the one described in the example above may happen.

The state of the art of LED drivers is presented in section II.

II. STATE OF THE ART

The presented current regulator is based on the circuit proposed in [2]. As it is shown in section VIII the solution proposed in [2] cannot work for high dropout values, meaning it cannot be used for multicolor LEDs. Another aspect to consider is that the solution proposed here is able to amplify the input current fifty times. The solution in [2] has unitary current gain, which increases the output impedance (as can be seen in [2]). On the other hand, as in the solution proposed here the output transistor is fifty times bigger than the input one, its \( r_{DS,ON} \) is much lower, which allows a much lower dropout (\( v_{DROP}/i_{LED} = r_{DS,ON} \)).

In [1] a few topologies of current mirrors are presented in figure 2. The topology proposed in this work is based on figure 2.c. Figures 2.a, 2.b and 2.d correspond to solutions having two NMOS transistors in series in the output side, which cause the problem a 2\( v_{DS} \) dropout voltage. The solution proposed here has only one \( v_{DS} \) dropout voltage and this can be a triode \( v_{DS} \) (because both \( v_{DS} \) and \( v_{GS} \) of both mirror transistors are the same), which is lower than the saturation one. The solution proposed in [1] (figure 3.a) also needs 2\( v_{DS} \) dropout voltage to work.

A research has been made in order to realize what the market has to offer in this field. The best solution found is offered by MAXIM. In this solution they claim to achieve 60\( mA \) output current with 80\( mV \) dropout voltage, at 5\% (meaning 5\% maximum LED current variation). This work aims at 2\% output current maximum variation. With a 5\% current variation, the worst case scenario for a display with four LEDs corresponds to have some of them 5\% bellow the reference current and the rest of them 5\% above. For a 50\( mA \) current this means dispersion between 47.5\( mA \) and 52.5\( mA \) while a 2\% variation corresponds to dispersion between 49\( mA \) and 51\( mA \).

III. OVERALL SPECIFICATIONS

Table I shows the overall specifications. The minimum, typical and maximum acceptable values are shown.

IV. MINIMUM OUTPUT IMPEDANCE

From the overall specifications, the minimum output impedance of the regulator can be calculated in the following way:

\[
\Delta z_{OUT} = \frac{\Delta v_{DROP}}{\Delta i_{LED}}
\]

\[
z_{OUT} = \frac{v_{DROP,MAX} - v_{DROP,MIN}}{2\%50mA}
\]

\[
z_{OUT} = \frac{3.3V - 0.03V}{1mA} = 3.27K\Omega
\]

V. DIGITAL TO ANALOG CONVERTER - DAC

VI. PRINCIPLE OF OPERATION

As mentioned in the chapter above, the LED brightness is proportional to the current that flows through it. This current must be 0 if the LED is off and 50\( mA \) if the LED is intended to shine with maximum intensity. The regulator input current goes from 0 to 1\( mA \) and is mirrored to the output with a gain of 50. This is the current that has to be proportional to the digital input, which is an eight bit number. In order to make this conversion, a current mirror based digital to analog converter was designed. This circuit is shown in figure 15 (in the end of this paper).

As one can see in figure 15 there is a reference current of 1\( \mu A \) that flows trough transistor M24, which must be working in the saturation region. Transistors M33 to M26, if working in the saturation region, mirror the reference current, multiplying it by a certain gain. Table II shows the gain of every stage, the dimensions of the transistors and the current that flows through each one. The notation \( Mx[1: a] \) means that transistor \( Mx \) is formed by an array of \( a \) shunted transistors.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L</th>
<th>Fingers</th>
<th>Gain</th>
<th>( i_D ) (if on)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M24</td>
<td>0.5( \mu m / 4\mu m )</td>
<td>2</td>
<td>-</td>
<td>1( \mu A )</td>
</tr>
<tr>
<td>M33</td>
<td>0.5( \mu m / 4\mu m )</td>
<td>8</td>
<td>1</td>
<td>4( \mu A )</td>
</tr>
<tr>
<td>M32[1:2]</td>
<td>0.5( \mu m / 4\mu m )</td>
<td>8</td>
<td>8</td>
<td>8( \mu A )</td>
</tr>
<tr>
<td>M31[1:4]</td>
<td>0.5( \mu m / 4\mu m )</td>
<td>8</td>
<td>16</td>
<td>16( \mu A )</td>
</tr>
<tr>
<td>M30[1:8]</td>
<td>0.5( \mu m / 4\mu m )</td>
<td>8</td>
<td>32</td>
<td>32( \mu A )</td>
</tr>
<tr>
<td>M29[1:16]</td>
<td>0.5( \mu m / 4\mu m )</td>
<td>8</td>
<td>64</td>
<td>64( \mu A )</td>
</tr>
<tr>
<td>M28[1:32]</td>
<td>0.5( \mu m / 4\mu m )</td>
<td>8</td>
<td>128</td>
<td>128( \mu A )</td>
</tr>
<tr>
<td>M27[1:64]</td>
<td>0.5( \mu m / 4\mu m )</td>
<td>8</td>
<td>256</td>
<td>256( \mu A )</td>
</tr>
<tr>
<td>M26[1:128]</td>
<td>0.5( \mu m / 4\mu m )</td>
<td>8</td>
<td>512</td>
<td>512( \mu A )</td>
</tr>
</tbody>
</table>

TABLE I
OVERALL SPECIFICATIONS

TABLE II
SIZE, CURRENT GAIN AND OUTPUT CURRENT OF EVERY STAGE OF THE DAC.
One can see from this table that the maximum output current of the DAC is 1.021mA (in order to compensate for this 0.021mA offset the gain of the regulator may be adjusted in order to provide the maximum of 50mA output current). The gain of 2, when passing from the first stage to the second one does not appear as it usually does in this type of design. This implies that one cannot obtain all integer numbers between 0 and 1023, but once there’s only 8 bits available this would be impossible anyway, which is why this seems like a perfectly acceptable option.

In what concerns to the switches, there’s very good reason for this type of implementation instead of the more typical type with only the PMOS switches bellow M33 to M26. This way, none of the current to be added in the output node has to flow through the switches, implying less area required for the switches. Even though it takes two transistors for each stage flow trough the switches, implying less area required for the same thing happens for all the other stages.

Concerning the principle of operation, if the bit B0 (the less significant one) is high, the switch M6 is open and M48 is closed, placing M33 in the saturation region while connecting its gate to the reference gate of M24, therefore mirroring the reference current times the current gain of the first stage. If instead of this B0 is low, the switches will cutoff M4. The same thing happens for all the other stages.

Transistors M25 and M53 to M57 implement a cascode stage, in order to increase the output impedance of this current source. This cascode transistors are designed to make $v_{SD}$ of the mirror transistors (M26 to M33) approximately equal to the one of the reference transistor M24. So, the influence of the term $1 + \lambda v_{SD}$ in the saturation equation for $i_D$ ($i_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (v_{SG} - v_{Th})^2 (1 + \lambda v_{SD})$) decreases. This makes the current even less dependent on $v_{SD}$, meaning the increasing of the output impedance of the DAC.

The cascode stage works in the following way: there’s a reference voltage applied to the gates of all cascode transistors. These transistors must be saturated so their drain currents are mostly dependent of $v_{SG}$. This way the source voltage is strongly dependent of the drain current. Once the sizes of this cascode transistors keep the relations of the mirror ones, the source voltage of every cascode transistor is approximately equal.

For the reference stage there’s:

$$i_{D_{25}} = 1\mu A = K_{P_{25}} v_{OD_{25}}^2 \tag{4}$$

For the second stage:

$$i_{D_{57}} = 4\mu A = K_{P_{57}} v_{OD_{57}}^2 = 4K_{P_{25}} v_{OD_{25}}^2 \tag{5}$$

The same $K_P$ VS $i_D$ relation is kept for all stages, meaning that all $v_{OD}$’s are the same. The threshold voltage isn’t exactly the same for all cascode transistors due to the body effect and the fact that have not all the same dimensions. However, the effect of the variation is considered neglected. This and the fact that all gates are connected to the same reference voltage make the source voltage be approximately equal for all cascode transistors, meaning all $v_{SD}$’s off the mirror transistors are approximately equal too.

VII. NOVEL CURRENT REGULATOR

A. Principle of Operation

Figure 2 shows the basis of the novel current regulator. As one can see in this figure, the dropout voltage will be $v_{DS}$ of the M2 transistor. The complete LED driver schematic is shown in figure 14 (in the end of this paper).

In a traditional current source, only the gate to source voltage ($v_{GS}$) of both mirror transistors is the same. The drain to source voltage ($v_{DS}$) doesn’t have to be the same because the drain current, $i_D$, is approximately proportional to $v_{GS}$ if both transistors are saturated. But, there’s a small influence of $v_{DS}$, once a NMOS transistor drain current (in the saturation region) is given by

$$i_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (v_{GS} - v_{Th})^2 (1 + \lambda v_{DS}). \tag{6}$$

Once $\lambda$ is much less than one, this influence is not very high but still decreases the output impedance. In the proposed solution, both $v_{DS}$ and $v_{GS}$ of both mirror transistors are the same (as one can see in figure 2) which increases the output impedance. Of course $v_{DS}$ is not exactly the same due to the offset of the opamp. This will be taken into account later but for now it is considered a good approach.

Another advantage of having the same value of $v_{DS}$ and $v_{GS}$ on both transistors of the current mirror is that they can operate in any region, instead of the traditional mirror where they have to be saturated. In fact, the triode region is better because $v_{DS}$ is lower in this region than in the saturation one, meaning less dropout.

For low dropouts the regulator must be working in the triode region because for these situations $v_{DS}$ obeys to the condition:

$$v_{DS} = v_{DROP} < v_{GS} - V_t. \tag{7}$$

As it will be seen later $v_{GS}$ will not be lower than 0.9V. The threshold voltage, $V_th$, for the used high voltage transistors,
is around 0.7V (disregarding the body effect). Meaning that until the dropout reaches around 200mV, the regulator is in the triode region. For this situation the drain currents of the input and output sides are given (respectively) by:

\[ i_{DIN} = \mu C_{ox} \left( \frac{W}{L} \right)_{IN} \left( v_{GS} - v_{Th} \right) v_{DS} - \frac{v_{DS}^2}{2} \] (8)

\[ i_{DOUT} = \mu C_{ox} \left( \frac{W}{L} \right)_{OUT} \left( v_{GS} - v_{Th} \right) v_{DS} - \frac{v_{DS}^2}{2} \] (9)

The current gain is given by:

\[ \left( \frac{W}{L} \right)_{OUT} \left( \frac{W}{L} \right)_{IN} = 50 \] (10)

Meaning that to achieve a gain of 50mA the following condition must be verified:

\[ \left( \frac{W}{L} \right)_{OUT} = 50 \left( \frac{W}{L} \right)_{IN} \] (11)

For dropouts higher than 200mV, the input and output transistors are saturated. For this situation:

\[ i_{DIN} = \frac{1}{2} \mu C_{ox} \left( \frac{W}{L} \right)_{IN} \left( v_{GS} - v_{Th} \right)^2 (1 + \lambda v_{DS}) \] (12)

\[ i_{DOUT} = \frac{1}{2} \mu C_{ox} \left( \frac{W}{L} \right)_{OUT} \left( v_{GS} - v_{Th} \right)^2 (1 + \lambda v_{DS}) \] (13)

The current gain is also given by equation 10 because, as mentioned before, both \( v_{DS} \) and \( v_{GS} \) of both mirror transistors are the same.

Considering now the differential input voltage of the Operational Amplifier, the gate to source voltage for both regulator mirror transistors is given by:

\[ v_{GS} = A_v (v_{plus} - v_{minus}) \] (14)

In this situation the drain to source voltages of both mirror transistors are not exactly the same. This transistors are M22 and M25 in figure 14, but to simplify this analysis lets consider the input side NMOS as M1 and the output one as M2.

This way there’s:

\[ v_{GS1} = v_{GS2} = v_{GS} = A_v (v_{DS1} - v_{DS2}) \] (15)

\[ v_{DS1} = v_{DS2} + \frac{v_{GS}}{A_v} \] (16)

Assuming the regulator is working for low dropouts and therefore is in the linear region, so equations 8 and 9 are valid, there’s:

\[ i_{OUT} = \frac{W_2^2}{W_1^2} Ref \frac{v_{GS}}{A_v - v_{DS2}} \] (17)

From this equation one can see that the higher the gain of the Operational Amplifier, the more accurate the regulator is. This is one way to obtain the minimum Opamp gain that respects the maximum LED current variation of 2%.

VIII. NON DESIRABLE STABLE STATES

The regulator must work for different types of LEDs, meaning LEDs with different voltage drops. For example, a white LED drops about 2.6V while a red one drops about 1.8V. An application with four LEDs must have the regulator instantiated four times, meaning four equal regulators. All the LEDs will be connected to the same charge pump. So, if the application is using LEDs of different colors, different regulators will be working with different dropouts. This results in a serious limitation that was encountered in [2].

For example, if the Charge Pump is providing 3.7V for a white LED connected to a regulator, the dropout is 100mV. If there is a second regulator driving a red LED, connected to the same Charge Pump, the dropout is 1.9V. The problem is that with a 2.5V supply voltage there is certainly less than 2.5V in the plus side of the opamp. If this value is less than 1.9V the opamp is surely saturated, resulting in a agnd output that cuts off both mirror transistors. Even if the plus side voltage is lightly above 1.9V the differential pair may cutoff, once it is a PMOS differential pair to work for low dropouts. To solve this problem a special opamp was designed. It is presented in section IX.

IX. OPERATIONAL AMPLIFIER (OPAMP)

The opamp gain must be very high because it influences directly the output impedance of the regulator. For this application the opamp doesn’t have to be very fast nor have a wide output swing, once its output is to be quite steady. A folded cascode opamp was chosen. Table II at [4] and the fact that a very high input swing is necessary (so the opamp works not only for low but also for high dropout voltages) justify the choice of this type of implementation. This second aspect is the main reason once it’s having this kind of implementation that allows having two differential pairs (which is the case as it is explained bellow) to increase the input swing. Section 9.7 at [5] gives more detailed information about this subject.

The designed Opamp is shown in figure 16 (in the end of this paper). It has two differential pairs. The PMOS differential pair works for low dropouts. When the dropout voltage is so high that the PMOS differential pair transistors can no longer stay saturated (they cutoff), the NMOS differential pair must already be working. This situation can be seen in figure 3.

The NMOS differential pair works normally until the dropout voltage is so high that the plus side can no longer follows the minus side (which has the dropout voltage), once it is limited by a value that’s smaller then the analog voltage supply. To solve this problem a terminal was added to the Opamp. It is the \( V_{n2} \) terminal in figure 16. The result is shown in figure 5. The plus side follows the minus side until the dropout voltage reaches around 2.1V, which is the \( V_{n2} \) terminal voltage (a reference voltage created with this value on
propose). At this point, the plus side can no longer follows the minus side and starts following the $V_{n2}$ terminal. The value 2.1V was chosen for the reference voltage because it is very close to the maximum value that the plus side can assume. Mathematically speaking, what’s done here is the minimum function:

$$v_P = \text{MIN}\{V_N, V_{N2}\}$$  \hspace{1cm} (18)

For dropouts above 2.1V the output current starts to increase a little due to the $(1+\lambda v_{DS})$ term in equation 6. This happens because in this situation $v_{DS}$ is different for both mirror transistors. $v_{DS}$ of the input NMOS is (for this situation), as mentioned before, 2.1V and $v_{DS}$ of the output NMOS is increasing with the dropout voltage, as can be seen in figure 5.

The opamp output ("out" in figure 16) voltage as a function of the dropout voltage is presented in figure 4. This voltage adjusts to compensate for the drain to source voltage variations of the mirror transistors (M1 and M2 in figure 2). It is important to notice that this voltage changes more for low dropouts, because in the beginning (zero dropout) of the characteristic in figure 4, the opamp is saturated (output voltage equal to the analog voltage supply), implying very different drain to source voltages in the mirror transistors. As the dropout increases and the opamp begins to work, the drain to source voltage of the input NMOS starts to approach to that of the output NMOS and the opamp output voltage variation starts to decrease, becoming very close to zero (almost no variation) when the dropout voltage reaches around 0.5V, as can be seen in figure 4.
X. RESULTS

A. DC dropout voltage sweep

In order to realize the minimum dropout voltage value, a DC sweep simulation result is shown in figure 6. This simulation presents the LED current as a function of the dropout voltage.

![Figure 6](image)

Fig. 6. LED current as a function of the Dropout Voltage, Typical Corner

It can be seen that the minimum dropout voltage value, considering a 2% precision, is 25mV. When the dropout voltage reaches about 2.1V, the situation described in section IX happens and, as described there, the output current starts to increase a little due to the \((1 + \lambda v_{SD})\) term in the saturation equation for \(i_D\) \((i_D = kV_{OD}[1 + \lambda v_{SD}])\).

Figure 7 shows the same simulation as in figure 6 but this time in corners. The 64 corners presented are for MOS, resistance, analog voltage supply, bias current and temperature combinations.

![Figure 7](image)

Fig. 7. LED current as a function of the Dropout Voltage, 64 corners
XI. Transient Power Up

Figure 8 shows the same 64 corners as before but for the transient power up simulation. The dropout chosen for this simulations is 40mV. This value was chosen because figure ?? shows that in the worst corner the dropout voltage is still bellow 40mV. But for the typical corner (along with many others) 25mV dropout voltage would be enough. Not all binary inputs are shown here, only 00000000, 00000001, 00000011, ..., 11111111.

![Figure 8](image1.png)

Fig. 8. Transient Powerup simulation results: 64 corners, Dropout Voltage = 40mV

The LED current goes from about 46.3mA to 53.3mA. This values can be trimmed.

Figure 9 shows the output current for all the binary input words (from 00000000 to 11111111).

![Figure 9](image2.png)

Fig. 9. Transient Powerup simulation results: LED current for all binary input words, Dropout Voltage = 25mV, typical corner
XII. AC OPEN LOOP

Figure 10 shows the results of the AC open loop simulation typical corner. As one can see in this figure, the phase margin for the typical corner is about fifty degrees. The static gain is around $140\,dB$.

Fig. 10. AC Open Loop simulation results: Typical corner

Fig. 11. AC Open Loop simulation results: 64 corners, Dropout Voltage = 2V, Regulator Input Current = 100uA
XIII. MONTÉ CARLO SIMULATIONS

Figures 12 and 13 show the result of the Monte Carlo Simulations.

Appendix ?? gives a general introduction to the Monte Carlo method and explains what’s done in this specific case, showing the used parameter variations.

![Monte Carlo Simulation Results for 50 parameter variations: LED current as a function of the Dropout Voltage](image1)

Fig. 12. Monte Carlo Simulation Results for 50 parameter variations: LED current as a function of the Dropout Voltage

![Monte Carlo simulation results for 50 parameter variations: histogram](image2)

Fig. 13. Monte Carlo simulation results for 50 parameter variations: histogram

The peak that can be observed in some of the curves in figure 12 is due to the offset of the operational amplifier. In order to reduce this peaks, offset compensation could be performed. This consists in adding or reducing the current that flows through one of the sides of the differential amplifier or through one of the sides of the output stage of the amplifier.

Figure 13 is a histogram that shows how many samples are in a certain interval of current.

XIV. CONCLUSION

The main objective was to design a current regulator with no more than 100mV dropout voltage, able to drive a LED with a current that can go from 0 to 50mA. This objective was reached and improved. The dropout reached is only 25mV at 2%, which is a five times improvement.
Fig. 14. Novel current regulator complete schematic
Fig. 15. Digital to Analog Converter
Fig. 16. Opamp for the novel current regulator