Ultra Low Dropout Driver for Multicolor LEDs

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Abstract

Electronic applications with a display, like for example a cell phone or a PDA, must have all LEDs from the display shining with the same intensity. Meaning that the current that flows through a LED must be the same that flows through all the others.

To fulfill this requirement it was developed a current regulator to be able to drive a LED with a constant current between 0 and 50mA, proportional to a digital eight bit word, with ultra low dropout voltage was developed. The lower the dropout voltage, the longer the battery life time is.

The regulator must work for multicolor LEDs, meaning LEDs with different voltage drops.

The proposed solution is able to drive a LED with a 50mA current, with only 25mV dropout voltage at 2% (meaning a 2% maximum current variation).

Keywords

Transistor, LED, Dropout, Regulator, DAC, Corners
Resumo

Aplicações electrónicas com écran que contenha LEDs, como por exemplo um telefone celular ou um PDA, têm que ter todos os LEDs a brilhar com a mesma intensidade. Isto implica que a corrente que flui através de um LED deve ter o mesmo valor que a que flui através dos restantes.

Para resolver este problema foi desenvolvido um regulador que impõe num LED uma corrente constante cujo valor pode ir de 0 a 50mA. Esta corrente é proporcional a uma palavra digital de oito bits e é assegurada com um valor mínimo de dropout extremamente baixo. Quanto mais baixo este valor mais a bateria da aplicação em questão dura.

O regulador deve funcionar para LEDs de cores diferentes, ou seja, LEDs com valores diferentes de tensão de limiar.

A solução apresentada consegue regular para 50mA com apenas 25mV de dropout. A dispersão máxima da corrente em relação ao valor pretendido é de apenas 2%.

Palavras Chave

Transistor, LED, Dropout, Regulador, DAC, Corners
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<table>
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<th>Abbreviation</th>
</tr>
</thead>
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<tr>
<td>Light Emitting Diode</td>
<td>LED</td>
</tr>
<tr>
<td>Metal-Oxide-Semiconductor</td>
<td>MOS</td>
</tr>
<tr>
<td>P-Channel Metal-Oxide-Semiconductor</td>
<td>PMOS</td>
</tr>
<tr>
<td>N-Channel Metal-Oxide-Semiconductor</td>
<td>PMOS</td>
</tr>
<tr>
<td>Complementary Metal-Oxide-Semiconductor</td>
<td>CMOS</td>
</tr>
<tr>
<td>Analog Supply Voltage</td>
<td>$dv_{dd}$</td>
</tr>
<tr>
<td>Digital Supply Voltage</td>
<td>$dv_{dd}$</td>
</tr>
<tr>
<td>Reference Current</td>
<td>$i_{BIAS}$</td>
</tr>
<tr>
<td>Current flowing through X</td>
<td>$i_X$</td>
</tr>
<tr>
<td>Voltage at node X</td>
<td>$v_X$</td>
</tr>
<tr>
<td>Small Signal part of the Voltage/Current at X</td>
<td>$v_x/i_x$</td>
</tr>
<tr>
<td>Constant part of the Voltage/Current at X</td>
<td>$V_X/I_X$</td>
</tr>
<tr>
<td>Threshold Voltage</td>
<td>$v_{th}$</td>
</tr>
<tr>
<td>LED Current</td>
<td>$i_{LED}$</td>
</tr>
<tr>
<td>Drain/Source/Gate Voltage</td>
<td>$v_{D/S/G}$</td>
</tr>
<tr>
<td>Drain/Source/Gate Current</td>
<td>$i_{D/S/G}$</td>
</tr>
<tr>
<td>Overdrive Voltage</td>
<td>$v_{OD}$</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$v_{Drop}$</td>
</tr>
<tr>
<td>LED Current</td>
<td>$i_{LED}$</td>
</tr>
<tr>
<td>Operational Amplifier</td>
<td>$Opamp$</td>
</tr>
<tr>
<td>$K_p$</td>
<td>$\mu C_{ox}$</td>
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1.1 Overview

The display is a fundamental part of a Cell phone, a PDA or a MP3 player, among others. Like any other part in this kind of applications, it must to be as good as possible in what concerns to three aspects, functionality, size and power consumption. Nowadays, the technology is so much developed, allowing such a small channel length transistors, that size is no longer the main concern. Beside the functionality, what matters the most now is how much the battery lasts.

The work was done in Collaboration with the company Chipidea and was developed at this company. The overall specifications were given by Chipidea. The technology used was SMIC013, which is a 130nm CMOS technology (meaning that the minimum channel length for the MOS transistors is 130nm). The work was done under the Cadence platform and the simulator used was HSPICE.

1.2 Motivation and Contents

It usually takes more then one LED to light up the display of a cell phone or other portable equipment. It is crucial to have all the LEDs shining with the same intensity. How much a LED shines is determined by the current that flows through it. Meaning that in order to keep an uniform display, this current has to be the same for all the LEDs.

When a voltage is applied to a LED, with a value that is enough to turn the LED on, the current that flows through it is not necessarily the same that flows through a similar LED under the same circumstances. This happens because the \( i(v) \) characteristic changes a little from LED to LED. Thus, the current that flows through each LED must be regulated.

The goal for this work is to make a circuit able to control the current that flows through a LED, as shown in figure 1.1. The anode of the LED is connected to a Charge Pump (see 6), available from a different module. The voltage that drops across the regulator is called dropout voltage. There is a minimum voltage that the regulator needs in order to be able to regulate the output current. Dropout voltage is a necessary cost for the regulation. Power dissipation increases as the regulator dropout increases according to biasing circuit conditions. The point is to make the regulator work with as low dropout as possible, because the higher the dropout voltage, the less the battery lasts.

In order to control the LEDs brightness, an eight bit number is given as input. This way there are two hundred and fifty six levels of brightness, in other words, two hundred and fifty six levels of output current (LED current). This allows a very thin brightness adjustment. A digital to analog converter (DAC) translates this digital word into a current that is the input current for the regulator. This can also be seen in figure 1.1.
Figure 1.1: Basis of the LED driver circuit.

The circuit composed by the regulator and the DAC known as a LEDs driver.

Subsection 2.5 shows the overall specifications in detail.

The LED current is fifty times greater than the current that leaves the DAC. If all the input bits in the DAC are high, the DAC output current must be 1mA, corresponding to a maximum LED current of 50mA. The LED driver circuit can use a 1µA bias current, available from a different module. Both analog and digital supply voltages are 2.5V. The voltage applied to the anode of the LED comes from a ChargePump, connected directly to the battery. It is mandatory that the voltage given by the ChargePump reaches at least the LED threshold voltage plus the minimum dropout voltage.

A very important aspect to consider is the fact that this regulator has to work for multicolor LEDs. The voltage drop in a LED changes with the color of the LED. For example, a white LED drops about 3.6V. If the ChargePump is providing a voltage of 3.7V for this white LED, it corresponds to a 100mV dropout voltage. Now if this white LED is replaced by a red one, that drops around 1.8V, the dropout will become 1.9V. However, the regulator must work for this value as it works for lower dropouts. To note that in a real situation the issue is due to the fact that there is only one ChargePump, so the same voltage is at all LEDs anodes and different regulators are connected to different LEDs (to the cathodes of the LEDs). Thus, not all dropouts are equal and a variation as the one described in the example above may happen.

The state of the art of LED drivers is presented in section 1.3.
1.3 State of the art

The presented current regulator is based on the circuit proposed in [2]. As it is shown in section 3.2 the solution proposed in [2] cannot work for high dropout values, meaning it cannot be used for multicolor LEDs. Another aspect to consider is that the solution proposed here is able to amplify the input current fifty times. The solution in [2] has unitary current gain, which increases the output impedance (as can be seen in [2]). On the other hand, as in the solution proposed here the output transistor is fifty times bigger than the input one, its $r_{DS(on)}$ is much lower, which allows a much lower dropout ($v_{DROP}/i_{LED} = r_{DS(on)}$).

In [1] a few topologies of current mirrors are presented in figure 2. The topology proposed in this work is based on figure 2.c. Figures 2.a, 2.b and 2.d correspond to solutions having two NMOS transistors in series in the output side, which cause the problem a $2v_{DS}$ dropout voltage. The solution proposed here has only one $v_{DS}$ dropout voltage and this can be a triode $v_{DS}$ (because both $v_{DS}$ and $v_{GS}$ of both mirror transistors are the same), which is lower than the saturation one. The solution proposed in [1] (figure 3.a) also needs $2v_{DS}$ dropout voltage to work.

A research has been made in order to realize what the market has to offer in this field. The best solution found is offered by MAXIM. In this solution they claim to achieve $60\,mA$ output current with $80\,mV$ dropout voltage, at $5\%$ (meaning $5\%$ maximum LED current variation). This work aims at $2\%$ output current maximum variation. With a $5\%$ current variation, the worst case scenario for a display with four LEDs corresponds to have some of them $5\%$ bellow the reference current and the rest of them $5\%$ above. For a $50\,mA$ current this means dispersion between $47.5\,mA$ and $52.5\,mA$ while a $2\%$ variation corresponds to dispersion between $49\,mA$ and $51\,mA$.

1.4 Overall Specifications

Table 1.1 shows the overall specifications. The minimum, typical and maximum acceptable values are shown.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Supply Voltage</td>
<td>2.25V</td>
<td>2.5V</td>
<td>2.75V</td>
</tr>
<tr>
<td>Digital Supply Voltage</td>
<td>2.25V</td>
<td>2.5V</td>
<td>2.75V</td>
</tr>
<tr>
<td>Reference Current</td>
<td>0.98\mu A</td>
<td>1\mu A</td>
<td>1.02\mu A</td>
</tr>
<tr>
<td>DAC output current</td>
<td>0mA</td>
<td>-</td>
<td>1mA ± 2%</td>
</tr>
<tr>
<td>Current Regulator input current</td>
<td>0</td>
<td>-</td>
<td>1mA ± 2%</td>
</tr>
<tr>
<td>Current Regulator output current</td>
<td>0</td>
<td>-</td>
<td>50mA ± 2%</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>30mV</td>
<td>-</td>
<td>3.3V</td>
</tr>
</tbody>
</table>

Table 1.1: Overall Specifications
1.5 Minimum Output Impedance

From the overall specifications, the minimum output impedance of the regulator can be calculated in the following way:

\[ z_{OUT} = \frac{\Delta v_{DROP}}{\Delta i_{LED}} \]  \hspace{1cm} (1.1)

\[ z_{OUT} = \frac{v_{DROP_{MAX}} - v_{DROP_{MIN}}}{2\% 50mA} \]  \hspace{1cm} (1.2)

\[ z_{OUT} = \frac{3.3V - 0.03V}{1mA} = 3.27K\Omega \]  \hspace{1cm} (1.3)

In section 3.5, the expression for the output impedance of the proposed solution is calculated. The actual numeric value depends on the technology and is only presented in section 4.3.
Digital to Analog Converter (DAC)

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2.1 Principle of Operation

As mentioned in the chapter above, the LED brightness is proportional to the current that flows through it. This current must be 0 if the LED is off and 50mA if the LED is intended to shine with maximum intensity. The regulator input current goes from 0 to 1mA and is mirrored to the output with a gain of 50. This is the current that has to be proportional to the digital input, which is an eight bit number. In order to make this conversion, a current mirror based digital to analog converter was designed. This circuit is shown in figure 2.1. A larger version of this schematic can be seen in appendix C.

As one can see in figure 2.1 there is a reference current of 1µA that flows through transistor M24, which must be working in the saturation region. Transistors M33 to M26, if working in the saturation region, mirror the reference current, multiplying it by a certain gain. Table 2.1 shows the gain of every stage, the dimensions of the transistors and the current that flows through each one. The notation Mx[1 : a] means that transistor Mx is formed by an array of a shunted transistors.

One can see from this table that the maximum output current of the DAC is 1.021mA (in order to compensate for this 0.021mA offset the gain of the regulator may be adjusted in order to provide...
The maximum of 50mA output current). The gain of 2, when passing from the first stage to the second one does not appear as it usually does in this type of design. This implies that one cannot obtain all integer numbers between 0 and 1023, but once there’re only 8 bits available this would be impossible anyway, which is why this seems like a perfectly acceptable option.

In what concerns to the switches, there’s a very good reason for this type of implementation instead of the more typical type with only the PMOS switches bellow M33 to M26. This way, none of the current to be added in the output node has to flow through the switches, implying less area required for the switches. Even though it takes two transistors for each stage the saved area is huge.

Concerning the principle of operation, if the bit B0 (the less significant one) is high, the switch M6 is open and M48 is closed, placing M33 in the saturation region while connecting its gate to the reference gate of M24, therefore mirroring the reference current times the current gain of the first stage. If instead of this B0 is low, the switches will cutoff M4. The same thing happens for all the other stages.

Transistors M25 and M53 to M57 implement a cascode stage, in order to increase the output impedance of this current source. This cascode transistors are designed to make $v_{SD}$ of the mirror transistors (M26 to M33) approximately equal to the one of the reference transistor M24. So, the influence of the term $1 + \lambda v_{SD}$ in the saturation equation for $i_D$ ($i_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (v_{SG} - v_{Th})^2 (1 + \lambda v_{SD})$) decreases. This makes the current even less dependent on $v_{SD}$, meaning the increasing of the output impedance of the DAC.

The cascode stage works in the following way: there’s a reference voltage (see 2.1.2) applied to the gates of all cascode transistors. These transistors must be saturated so their drain currents are mostly dependent of $v_{SG}$. This way the source voltage is strongly dependent of the drain current. Once the sizes of this cascode transistors keep the relations of the mirror ones, the source voltage of every cascode transistor is approximately equal.

For the reference stage there’s:

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L</th>
<th>Nr of Fingers</th>
<th>Current Gain</th>
<th>$i_D$ (If on)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M24</td>
<td>0.5µm/4µm</td>
<td>2</td>
<td>-</td>
<td>1µA</td>
</tr>
<tr>
<td>M33</td>
<td>0.5µm/4µm</td>
<td>8</td>
<td>1</td>
<td>4µA</td>
</tr>
<tr>
<td>M32[1:2]</td>
<td>0.5µm/4µm</td>
<td>8</td>
<td>8</td>
<td>8µA</td>
</tr>
<tr>
<td>M31[1:4]</td>
<td>0.5µm/4µm</td>
<td>8</td>
<td>16</td>
<td>16µA</td>
</tr>
<tr>
<td>M30[1:8]</td>
<td>0.5µm/4µm</td>
<td>8</td>
<td>32</td>
<td>32µA</td>
</tr>
<tr>
<td>M29[1:16]</td>
<td>0.5µm/4µm</td>
<td>8</td>
<td>64</td>
<td>64µA</td>
</tr>
<tr>
<td>M28[1:32]</td>
<td>0.5µm/4µm</td>
<td>8</td>
<td>128</td>
<td>128µA</td>
</tr>
<tr>
<td>M27[1:64]</td>
<td>0.5µm/4µm</td>
<td>8</td>
<td>256</td>
<td>256µA</td>
</tr>
<tr>
<td>M26[1:128]</td>
<td>0.5µm/4µm</td>
<td>8</td>
<td>512</td>
<td>512µA</td>
</tr>
</tbody>
</table>

Table 2.1: Size, current gain and output current of every stage of the DAC.
\[ i_{D_{M25}} = 1 \mu A = K_{P_{M25}} v_{OD_{M25}}^2 \]  

For the second stage:

\[ i_{D_{M57}} = 4 \mu A = K_{P_{M57}} v_{OD_{M57}}^2 = 4K_{P_{M25}} v_{OD_{M25}}^2 \]  

The same \( K_P \) VS \( i_D \) relation is kept for all stages, meaning that all \( v_{OD} \)'s are the same. The threshold voltage isn't exactly the same for all cascode transistors due to the body effect and the fact that have not all the same dimensions. However, the effect of the variation is considered neglected. This and the fact that all gates are connected to the same reference voltage make the source voltage be approximately equal for all cascode transistors, meaning all \( v_{SD} \)'s off the mirror transistors are approximately equal too.

### 2.1.1 DAC bias current

The DAC reference current is obtained by mirroring the reference current of 1\( \mu \)A available from another module at the top level, which is the level where the DAC and the Regulator are instantiated and connected. A simple current mirror was used for this.

### 2.1.2 DAC cascode voltage

As it is explained above, this reference voltage has the purpose of making similar source to drain voltages for the DAC mirror transistors. But, its value has to be such that the mirror transistors stay saturated, because even with the source to drain voltages similar for each mirror transistor, it is the gate to source voltage that’s really equal. Meaning that the functionality is much better if the mirror transistors are well saturated. The obtention of the cascode voltage has these aspects into account. The value of the drain voltage of the mirror transistors is close to the cascode voltage plus one threshold voltage. For each mirror transistor, the difference between the analog supply voltage and this voltage must be above the overdrive voltage, so it stays saturated. Beside this, the cascode voltage must remain constant. It must not change much with temperature or commutations of the DAC switches. In order to achieve this, this voltage is obtained from the gate of a PMOS transistor which is saturated and has a fixed value of current flowing through it. This situation can be seen in the complete LED driver schematic, shown in the next chapter. The current that flows through transistor M1 is constant and determined by the NMOS transistor M11, which is mirroring the reference current (obtained from a different module). M2 is working in the linear region and thus acting like a resistor, determining the source voltage of M1. M1 is well saturated and so its gate voltage is mostly dependent of its drain current and its source voltage. This drain current and source voltage were determined in order to obtain the desired value for the cascode voltage.
2.2 Low Level Design Considerations

Listed below are some of the considerations that were taken into account when designing the DAC.

- All the mirror transistors have to be well saturated in order to have their drain currents almost exclusively dependent on their source to drain voltages. The same goes to the cascode ones, for the reasons explained above. Thus, the transistors were designed to have $v_{SD} > v_{SG} - v_{th}$.

- The values of $W$ and $L$ for the mirror transistors were chosen to be wide in order to reduce the mismatches (see appendix B). Equation 2.3 gives the voltage offset between the overdrive voltage of the reference transistor ($M_{24}$) and the one of the mirror transistor $M_X$ (where $M_X$ can be any of the transistors $M_{26}$ to $M_{33}$, according to the mismatch one wants to obtain). This overdrive mismatch is due to threshold voltage variations from transistor to transistor during the fabrication process. Multiplying this equation by $g_{mX}$ (equation 2.4) gives the current offset in stage $X$ (difference between the reference current times the gain of stage $X$ and the current actually flowing through stage $X$).

\[
v_{OS1} = \frac{A v_{th}}{\sqrt{W_{MX} \times L_{MX}}} \tag{2.3}
\]

\[
i_{OS1} = \frac{A v_{th}}{\sqrt{W_{MX} \times L_{MX}}} \times g_{mMX} \tag{2.4}
\]

For this reason all mirror transistors are designed to have overdrive voltages above $250 mV$. Because the higher the overdrive voltage the lower the value of $g_{m}$ (according to equation 2.5).

\[
g_{m} = \frac{\partial i_D}{\partial v_{SG}} = \frac{2i_D}{v_{OD}} \tag{2.5}
\]

Another way to look at this is thinking that as the overdrive voltage increases ($v_{SG} - v_{th}$ increases) it becomes less dependent of the threshold voltage (the same variation of $v_{th}$ results in a smaller variation of the overdrive voltage), meaning that the drain current doesn’t suffer such large variations as it would occur if the overdrive voltage was smaller (according the saturation equation for the drain current: $i_D = K v_{od}^2$).

\footnote{Technologies provide the $A_v$ parameter to be used in this equation. The better (and probably more expensive) the technology, the lower this value is, meaning the lower are the mismatches for the same values of $W$ and $L$. This means that for a better technology area can be saved in an application like this where it is very important to have good mismatch. The formula can be found in section 13.2 at [5].}
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3.1 Principle of Operation

Figure 3.1 shows the basis of the novel current regulator. As one can see in this figure, the dropout voltage will be $v_{DS}$ of the M2 transistor. The complete LED driver schematic is shown in figure 3.2. A larger version of this schematic can be seen in appendix C.

In a traditional current source, only the gate to source voltage ($v_{GS}$) of both mirror transistors is the same. The drain to source voltage ($v_{DS}$) doesn’t have to be the same because the drain current, $i_D$, is approximately proportional to $v_{GS}$ if both transistors are saturated. But, there’s a small influence of $v_{DS}$, once a NMOS transistor drain current (in the saturation region) is given by

$$i_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (v_{GS} - v_{Th})^2 (1 + \lambda v_{DS}). \quad (3.1)$$

Once $\lambda$ is much less than one, this influence is not very high but still decreases the output impedance. In the proposed solution, both $v_{DS}$ and $v_{GS}$ of both mirror transistors are the same (as one can see in figure 3.1) which increases the output impedance, as can be seen in section 3.5. Of course $v_{DS}$ is not exactly the same due to the offset of the opamp. This will be taken into account later but for now it is considered a good approach.

Another advantage of having the same value of $v_{DS}$ and $v_{GS}$ on both transistors of the current mirror is that they can operate in any region, instead of the traditional mirror where they have to
be saturated. In fact, the triode region is better because $v_{DS}$ is lower in this region than in the saturation one, meaning less dropout.

For low dropouts the regulator must be working in the triode region because for these situations $v_{DS}$ obeys to the condition:

$$v_{DS} = v_{DROP} < v_{GS} - V_t.$$ \hfill (3.2)

As it will be seen later $v_{GS}$ will not be lower than 0.9V. The threshold voltage, $V_t$, for the used high voltage transistors, is around 0.7V (disregarding the body effect). Meaning that until the dropout reaches around 200mV, the regulator is in the triode region. For this situation the drain currents of the input and output sides are given (respectively) by:

$$i_{D_{IN}} = \mu C_{ox} \left( \frac{W}{L} \right)_{IN} \left( (v_{GS} - v_{TH})v_{DS} - \frac{v_{DS}^2}{2} \right)$$ \hfill (3.3)

$$i_{D_{OUT}} = \mu C_{ox} \left( \frac{W}{L} \right)_{OUT} \left( (v_{GS} - v_{TH})v_{DS} - \frac{v_{DS}^2}{2} \right)$$ \hfill (3.4)

The current gain is given by:
Meaning that to achieve a gain of 50mA the following condition must be verified:

\[
\left(\frac{W}{L}\right)_{\text{OUT}} = 50 \left(\frac{W}{L}\right)_{\text{IN}}
\]  

For dropouts higher than 200mV, the input and output transistors are saturated. For this situation:

\[
i_{\text{DIN}} = \frac{1}{2} \mu C_{\text{ox}} \left(\frac{W}{L}\right)_{\text{IN}} (v_{\text{GS}} - v_{\text{Th}})^2 (1 + \lambda v_{DS})
\]  

\[
i_{\text{DOUT}} = \frac{1}{2} \mu C_{\text{ox}} \left(\frac{W}{L}\right)_{\text{OUT}} (v_{\text{GS}} - v_{\text{Th}})^2 (1 + \lambda v_{DS})
\]

The current gain is also given by equation 3.5 because, as mentioned before, both \(v_{DS}\) and \(v_{GS}\) of both mirror transistors are the same.

Considering now the differential input voltage of the Operational Amplifier, the gate to source voltage for both regulator mirror transistors is given by:

\[
v_{\text{GS}} = A_v (v_{\text{plus}} - v_{\text{minus}})
\]

In this situation the drain to source voltages of both mirror transistors are not exactly the same. This transistors are M22 and M25 in figure 3.2 but to simplify this analysis lets consider the input side NMOS as M1 and the output one as M2.

This way there’s:

\[
v_{\text{GS1}} = v_{\text{GS2}} = v_{\text{GS}} = A_v (v_{DS1} - v_{DS2})
\]

\[
v_{DS1} = v_{DS2} + \frac{v_{GS}}{A_v}
\]

Assuming the regulator is working for low dropouts and therefore is in the linear region, so equations 3.3 and 3.4 are valid, there’s:

\[
i_{\text{OUT}} = \frac{W_2}{W_1} \frac{i_{\text{Ref}}}{1 + \frac{v_{GS}}{A_v v_{DS2}}}
\]

From this equation one can see that the higher the gain of the Operational Amplifier, the more accurate the regulator is. This is one way to obtain the minimum Opamp gain that respects the maximum LED current variation of 2%. In section 3.5 the same result (qualitatively speaking) is achieved recurring to the small signal analysis.
3.2 Non desirable stable states

The regulator must work for different types of LEDs, meaning LEDs with different voltage drops. For example, a white LED drops about 2.6V while a red one drops about 1.8V. An application with four LEDs must have the regulator instantiated four times, meaning four equal regulators. All the LEDs will be connected to the same charge pump. So, if the application is using LEDs of different colors, different regulators will be working with different dropouts. This results in a serious limitation that was encountered in [2].

For example, if the Charge Pump is providing 3.7V for a white LED connected to a regulator, the dropout is 100mV. If there is a second regulator driving a red LED, connected to the same Charge Pump, the dropout is 1.9V. The problem is that with a 2.5V supply voltage there is certainly less than 2.5V in the plus side of the opamp. If this value is less than 1.9V the opamp is surely saturated, resulting in a agnd output that cuts off both mirror transistors. Even if the plus side voltage is lightly above 1.9V the differential pair may cutoff, once it is a PMOS differential pair to work for low dropouts. To solve this problem a special opamp was designed. It is presented in section 3.3.

3.3 Operational Amplifier (OPAMP)

As it is shown in section 3.5 the opamp gain must be very high because it influences directly the output impedance of the regulator. For this application the opamp doesn’t have to be very fast nor have a wide output swing, once its output is to be quite steady. A folded cascode opamp was chosen. Table II at [4] and the fact that a very high input swing is necessary (so the opamp works not only for low but also for high dropout voltages) justify the choice of this type of implementation. This second aspect is the main reason once it’s having this kind of implementation that allows having two differential pairs (which is the case as it is explained below) to increase the input swing. Section 9.7 at [5] gives more detailed information about this subject.

The designed Opamp is shown in figure 3.3. A larger version of this schematic can be seen in appendix C. It has two differential pairs. The PMOS differential pair works for low dropouts. When the dropout voltage is so high that the PMOS differential pair transistors can no longer stay saturated (they cutoff), the NMOS differential pair must already be working. This situation can be seen in figure 3.4.

The NMOS differential pair works normally until the dropout voltage is so high that the plus side can no longer follows the minus side (which has the dropout voltage), once it is limited by a value that’s smaller then the analog voltage supply. To solve this problem a terminal was added to the Opamp. It is the $V_{n2}$ terminal in figure 3.3. The result is shown in figure 3.6. The plus side follows the minus side until the dropout voltage reaches around 2.1V, which is the $V_{n2}$ terminal voltage (a reference voltage created with this value on propose). At this point, the plus side can no
longer follows the minus side and starts following the $V_{n2}$ terminal. The value $2.1V$ was chosen for the reference voltage because it is very close to the maximum value that the plus side can assume. Mathematically speaking, what's done here is the minimum function:

$$v_P = \text{MIN}\{V_N, V_{N2}\} \quad (3.13)$$

For dropouts above $2.1V$ the output current starts to increase a little due to the $(1 + \lambda v_{DS})$ term in equation [3.1]. This happens because in this situation $v_{DS}$ is different for both mirror transistors. $v_{DS}$ of the input NMOS is (for this situation), as mentioned before, $2.1V$ and $v_{DS}$ of the output NMOS is increasing with the dropout voltage, as can be seen in figure [3.6].

The opamp output ("out" in figure [3.3]) voltage as a function of the dropout voltage is presented in figure [3.5]. This voltage adjusts to compensate for the drain to source voltage variations of the mirror transistors (M1 and M2 in figure [3.1]). It is important to notice that this voltage changes more for low dropouts, because in the beginning (zero dropout) of the characteristic in figure [3.5] the opamp is saturated (output voltage equal to the analog voltage supply), implying very different drain to source voltages in the mirror transistors. As the dropout increases and the opamp begins to work, the drain to source voltage of the input NMOS starts to approach to that of the output.
NMOS and the opamp output voltage variation starts to decrease, becoming very close to zero (almost no variation) when the dropout voltage reaches around $0.5V$, as can be seen in figure 3.5.

Figure 3.4: Opamp terminal Voltages and differential pairs currents as a function of the Dropout Voltage

Figure 3.5: Opamp output voltage as a function of the Dropout Voltage
3.4 Low Level Design Considerations

Listed below are some of the considerations that were taken into account when designing the Driver circuit.

- **Regulator mirror:**

  The regulator output transistor is very wide \((W/L = 10\mu m/1\mu m \times 20\) fingers \(\times 45\) shunted transistors) in order to have very low \(r_{DSon}\) \((0.5\Omega\) corresponds to \(25mV\) dropout voltage for \(50mA\) output current) and also to avoid current density problems. If it wasn’t for the first condition the transistors didn’t have to be so large. This is one of the main aspects responsible for the obtention of ultra low dropout voltage.

  The regulator mirror was designed with high values of \(W\) and \(L\) \((L = 1\mu A)\) to reduce mismatches (see appendix B).
• Opamp differential pairs:

The transistors of the differential pairs have large values of $W/L$ ($W/L = 10\mu m/2\mu m \times 8$ fingers) for the PMOS differential pair and the same $W/L$ but half of the fingers for the NMOS one, to compensate the difference between the $\mu C_{ox}$ of the NMOS and PMOS transistors) because, as shown in section 9.2 - equation (9.12), at [5], the gain of the Opamp increases with $g_m$ of the differential pair transistors, and once $g_m$ increases with $W/L$, the larger this value the larger the gain.

The overdrive voltage of the differential pairs transistors is around 40mV. This value must not be much higher. As it increases, the offset at the input of the Opamp increases (see appendix B). This can be explained looking at equations 3.14, 3.15, and 3.16.

\[
v_{OS1} = \frac{A_{vth}}{\sqrt{W_{M52} \times L_{M52}}} \times \frac{g_{m_{M52}}}{g_{m_{M13}}} \quad (3.14)
\]

\[
v_{OS2} = \frac{A_{vth}}{\sqrt{W_{M19} \times L_{M19}}} \times \frac{g_{m_{M19}}}{g_{m_{M13}}} \quad (3.15)
\]

\[
v_{OS3} = \frac{A_{vth}}{\sqrt{W_{M13} \times L_{M13}}} \quad (3.16)
\]

The first term of equation 3.14 gives the voltage offset of the active load ($M52$ and $M53$) (difference between the overdrive voltages due to $v_{th}$ variations). By multiplying this term by $g_{m_{M52}}$ there’s the offset in current (difference between the drain currents of $M52$ and $M53$). Assuming now that all this offset flows to the drain currents of the differential pair, there’s the offset in current at the differential pair due to the active load, which when divided by $g_{m_{M13}}$ translates to the input voltage offset value due to the active low. This is only a part of the input offset. Now by looking at this equation one can see that $g_m$ of the differential pair transistors must be very wide and $g_m$ of the active load transistors must be very small, meaning that the overdrive voltages of the mirror transistors must be very high (around 200mV to 300mV) and the overdrive voltages of the differential pairs transistors must be very low (around 10mV to 40mV). The values of $W$ and $L$ must be very high too.

Another part of the input offset is due to the differential pair itself. Equation 3.16 gives this offset.

Equation 3.15 gives the final part of the input offset and results from an analysis similar to the one made for the offset due to the active load. The overdrive voltage offset multiplied by the $g_m$ gives the offset in current, which flows to the differential pair and when divided by $g_m$ of the differential pair gives the input voltage offset due to the bias mirrors.

Equations 3.14, 3.15, and 3.16 are non-correlated because all mismatches are orthogonal statistical variables (independent). This way the total input offset is given by equation 3.17.
Another fact to consider is that as the overdrive voltage increases the input swing of the opamp decreases. Considering the PMOS differential pair is working (low dropouts zone), one can see from figure 3.3 that, as the $V_{n1}$ terminal voltage increases, the voltage in node $V_x$ also increases (because the drain current is constant). But as this $V_x$ voltage cannot increase above $v_{ODM21} + v_{ODM18}$ (so the mirror and cascode transistors $M21$ and $M18$ stay saturated) the lower the overdrive, the higher the gate voltage of $M13$ can be and still the PMOS differential pair stay working. Of course that as explained above when the dropout voltage is so high that the $M13$ transistor can no longer work, the NMOS differential pair must already be working. For this differential pair the minimum gate voltage is not an issue because it works only for high dropouts (anyway the limit is $v_{ODM48} + v_{GSM51} = v_{ODM48} + v_{ODM51} + v_{thM51}$). The maximum plus side voltage ($v_{GM40}$) is the issue. This voltage can not go above $avdd - v_{ODM26} - v_{ODM53}$ (referring to DAC transistors in figure 2.1). When this situation happens the third terminal starts doing its job as explained in section 3.3.

The overdrive of the mirror transistors can not be very low due to the reasons explained above for other current mirrors, it is around 200mV.

### 3.5 Small Signal Analysis

The small signal schematic for the regulator is presented in figure 3.7. It’s considered here that the opamp gain is $A_V$ and the DAC output impedance is very high when compared with $r_{DS1}$. The output impedance is given by the auxiliar voltage source $v_x$ divided by the current that flows through it, $i_x$. Analyzing the circuit there is:

\[
v_o = A_V(v_y - v_x)
\]

\[
v_y = -gmvo r_1
\]

\[
v_o = -A_V gm_1 v_o r_1 - A_V v_x
\]

\[
v_o = \frac{-A_V v_x}{1 + A_V gm_1 v_o r_1}
\]

\[
i_x = \frac{v_x}{r_2} + gm_2 v_o
\]

from equations 3.19 and 3.20 comes:

\[
R_{out} = \frac{v_x}{i_x} = \frac{r_2(1 + A_V gm_1 r_1)}{1 + A_V gm_1 r_1 - A_V gm_2 r_2}
\]

\[
\frac{1}{R_{out}} = \frac{1}{r_2} \left(1 - \frac{A_V gm_2 r_2}{1 + A_V gm_1 r_1}\right)
\]
This equation shows the same result that was obtained in section 3.1 - equation 3.12. The higher the operation amplifier static gain the more accurate the regulator is.

If $A_V \to \infty$ then

$$R_{out} = \frac{gm_1 r_1 r_2}{gm_1 r_1 - gm_2 r_2}$$

(3.23)

If $gm_1 r_1 = gm_2 r_2$ then $R_{out} \to \infty$.

This is the case in [2] but is not the case here, once the regulator is has to amplify the input current fifty times. Even so, the output impedance is very high.

From equation 3.21 one can see that the opamp gain is very important once the output impedance increases with it. Another important aspect is the DAC output impedance, that was considered to be very high when compared with $r_{DS1}$. To increase this value, cascode transistors were placed at the DAC output, as mentioned and explained in chapter 2.

In the linear region (low dropouts) there is:
\[ i_D = 2A[v_{GS} - v_{th}]v_{DS} \]  

(3.24)

Where \( A = K_p \frac{W}{L} \).

\[ g_m = \frac{\partial i_D}{\partial v_{GS}} = 2A v_{DS} \]  

(3.25)

\[ g_{ds} = \frac{1}{r_{ds}} = \frac{\partial i_D}{\partial v_{DS}} = 2A[v_{GS} - v_{th}] \]  

(3.26)

From equations 3.22 and 3.26:

\[ R_{out} = r_{DSON} \frac{A v_{DSM2}}{2v_{GS} - v_{th}} = \frac{v_{DSM2}}{i_{out}} \frac{A v_{DSM2}}{2v_{GS} - v_{th}} \]  

(3.27)

This means that for an estimation of 0.9V at the output of the amplifier, a 0.7V threshold voltage, 50mA output current, 25mV dropout voltage (drain to source voltage) and 3.27KΩ (see section 1.5), the gain of the differential amplifier must be around 120dB. But, it is important to understand that the calculation in section 1.5 refers to a delta of the dropout voltage counting after the minimum dropout voltage value is reached. At 25mV the output impedance is given by \( \frac{\partial v_{DROP}}{\partial i_{LED}} \) and this value is much lower than 3.27KΩ, as can be seen by the slope of the curve at figure 4.1 at 25mV. This means that the gain of the amplifier does not have to be so wide.

### 3.6 Trimming

As mentioned before, the current mirror has a gain of fifty. But, due to mismatches that may occur during the fabrication process (values of \( W \) or \( L \) slightly different than the specified ones), the gain may not be exactly fifty. One must consider the fact that the mirror transistors are not equal, so the mismatch in one doesn’t have to be the same in the other, which may cause a slightly change in the gain.

Other aspect that influences the output current is the corner in which the regulator is working. In fact, this influences the output current not only due to the regulator but mostly because it changes the DAC output current (regulator input current).

To deal with the fact that the output current may not correspond exactly to the expected, the circuit has trimming. In general, trimming consists in having a few bits that can increase or decrease a variable value, that may be for example a resistance, a capacity, or like in this case, a transistor \( W \).

As it was shown before, the gain of fifty comes from having the output side NMOS \( W/L \) fifty times higher than the one of the NMOS at the input side. The implemented trimming consists in having this gain of fifty by default, but with the possibility of tuning it. This can be used after the

\(^1\)See appendix A
chip is made in order to compensate the previously mentioned aspects that can make the output current be slightly different than the expected.

In practice, when a chip is build it has some inputs that are just for trimmings like this one. After testing the chip, a memory (at the chip) is programmed in order to contain the combinations of bits that compensate little errors caused by the problems mentioned above (mismatches and corners).

The regulator with trimming is presented in figure 3.8 and table 3.1 presents the possible combinations and the corresponding output current offsets. The default current gain value is fifty.

<table>
<thead>
<tr>
<th>Trimming Bits</th>
<th>Output Current Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>0</td>
</tr>
<tr>
<td>0001</td>
<td>-4mA</td>
</tr>
<tr>
<td>0010</td>
<td>+2mA</td>
</tr>
<tr>
<td>0011</td>
<td>-2mA</td>
</tr>
<tr>
<td>0100</td>
<td>+1mA</td>
</tr>
<tr>
<td>0101</td>
<td>-3mA</td>
</tr>
<tr>
<td>0110</td>
<td>+3mA</td>
</tr>
<tr>
<td>0111</td>
<td>-1mA</td>
</tr>
<tr>
<td>1000</td>
<td>+0.5mA</td>
</tr>
<tr>
<td>1001</td>
<td>-3.5mA</td>
</tr>
<tr>
<td>1010</td>
<td>+2.5mA</td>
</tr>
<tr>
<td>1011</td>
<td>-1.5mA</td>
</tr>
<tr>
<td>1100</td>
<td>+1.5mA</td>
</tr>
<tr>
<td>1101</td>
<td>-2.5mA</td>
</tr>
<tr>
<td>1110</td>
<td>+3.5mA</td>
</tr>
<tr>
<td>1111</td>
<td>-0.5mA</td>
</tr>
</tbody>
</table>

Table 3.1: Possible trimming combinations and corresponding output current offsets.

As one can see in figure 3.8 M2 is always mirroring the input current times 46. When the trimming code is 0000 (the default code) M3, M4 and M5 are off but M6 is on due to the inverter connected to the NMOS switch, MS4. Thus, the default current gains is fifty. As the trimming code changes, multiple combinations can occur. This combinations are all shown in table 3.1.

3.7 Power Down

In order to save battery life the circuit has one main input, the enable. This is a digital input that when is high the regulator is working, translating the bits at the DAC input into the analog current that’s mirrored at the regulator with a gain of fifty. But if the enable is low, the circuit is in the so-called power down mode. Meaning the regulator is off no matter what binary word the DAC input has. In this mode the total current consumption must be as low as possible, ideally it should be zero. To turn the circuit off and make this consumption very close to zero, a few transistors were added to the circuit. These are called power down transistors. These transistors can be
The power down transistor $M_3$ in figure 3.2 if ON, pulls the node $G_{N1}$ (in the same figure) to ground. This makes $v_{GS} = 0$ for the mirror transistors $M_{12, 35, 11, 2}$ and $M_{24}$. The power down transistors $M_8, M_5$ and $M_{14}$, if ON, pull the gates of the PMOS mirrors of the bias stages ($M_{36, 0}$ and $M_{9}$) to the analog voltage supply. This makes this transistor’s $v_{SG}$ become zero, cutting them off. But, this also makes a connection between the analog voltage supply and the drains of the NMOS mirror transistors of the bias stages ($M_{12, 35, 11, 2}$ and $M_{24}$). In order to assure that these transistors really cutoff the power down switches $M_{15, 6}$, $M_7$ and $M_{13}$ were placed. If $M_{15}$ cuts off, which appends in the power down mode, it will be assured that the shunting between the analog voltage supply and the ground will be avoided. Power down transistor $M_{10}$, if ON, pulls the gates of $M_{22}$ and $M_{25}$ (as the ones of the trimming transistors $M_{18, 19, 20}$ and $M_{21}$) to ground, cutting them off.

The digital part of the chip, not implemented in the scope of this work, would be responsible to connect all input bits of the DAC to ground (the low digital level) when in power down mode. This would easily power down the DAC due to its implementation (see chapter 2), which is another good advantage of this implementation for the DAC, one that was not mentioned in chapter 2.
3.8 Basic Architecture Considerations

It is to notice that there were other ways to obtain the $50mA$ at the output of the regulator. In this solution the DAC reference current is $1\mu A$ and then it's multiplied by gains in order to reach a maximum of $1mA$ to be amplified fifty times. In other solutions this could be done differently, for example by increasing the reference current and reducing the gains of the DAC. This would be adequate in what concerns to the size of the regulator but would not allow the minimum output current to be as small as in the proposed solution. Another option would be to increase the reference current but reducing the gain of the regulator instead of the DAC gains. This would mean one of two things, to reduce the $W/L$ of the output transistor of the regulator, saving space but increasing its $r_{DS,ON}$ and therefore increasing the Dropout, or increasing the input side transistor $W/L$, which would make the circuit larger but would not affect the dropout. It's important to notice that by increasing or decreasing the $W/L$ of one of the regulator transistors is to increase or decrease its $W$. The length of this transistors is equal for both and chosen considering mismatch issues, as it's explained later in this section. This is way it was said above that the size of the circuit increases or decreases with the $W/L$ of the regulator transistors.

So, the basis of the architecture solution proposed in this work is not necessarily the best but it seems like a very well balanced solution.
4.1 DC dropout voltage sweep

In order to realize the minimum dropout voltage value, a DC sweep simulation result is shown in figure 4.1. This simulation presents the LED current as a function of the dropout voltage.

Figure 4.1: LED current as a function of the Dropout Voltage, Typical Corner

It can be seen that the minimum dropout voltage value, considering a 2% precision, is 25mV. When the dropout voltage reaches about 2.1V, the situation described in section 3.3 happens and, as described there, the output current starts to increase a little due to the \((1 + \lambda v_{SD})\) term in the saturation equation for \(i_D\) \(i_D = k v_{OD}^2 \{1 + \lambda v_{SD}\}\).

Figure 4.2 shows the same simulation as in figure 4.1 but this time in corners. The 64 corners presented are for MOS, resistance, analog voltage supply, bias current and temperature combinations. Appendix A gives a detailed explanation about the used alter files and why these combinations are the chosen ones.

Figures 4.3 and 4.4 are zooms of figure 4.2. From figure 4.3 one can see that in the worst corner the dropout voltage is still below 40mV. The two groups of corners (below and above the typical one) are due to the bias current, as it assumes the minimum (corners below the typical one) or the maximum value (corners above the typical one).
Figure 4.2: LED current as a function of the Dropout Voltage, 64 corners

Figure 4.3: LED current as a function of the Dropout Voltage, 64 corners, zoom 1
Figure 4.4: LED current as a function of the Dropout Voltage, 64 corners, zoom 2
4.2 Transient power up

Figure 4.5 shows the same 64 corners as before but for the transient power up simulation. The dropout chosen for this simulations is 40 mV. This value was chosen because figure 4.3 shows that in the worst corner the dropout voltage is still below 40 mV. But for the typical corner (a long with many others) 25 mV dropout voltage would be enough. Not all binary inputs are shown here, only 00000000, 00000001, 00000011, 000000111, ..., 11111111.

![Figure 4.5: Transient Powerup simulation results: 64 corners, Dropout Voltage = 40mV](image)

Figure 4.6 is a zoom of the first stage on figure 4.5, the one corresponding to the word 1111111 on the input of the DAC. The LED current goes from about 46.3 mA to 53.3 mA. This values can be trimmed once they’re inside the range of the implemented trimming (see section 3.6).

Figure 4.7 shows the second stage (corresponding to 01111111) and figure 4.8 shows the last four stages (00001111, 00000111, ..., 00000000).

Figure 4.9 shows the power down state. The maximum power down current is about 330 nA, which only happens in one corner. There’s another corner slightly above 100 nA but the rest of them are below 10 nA.

Figure 4.10 shows the power up, the start of the regulator. It passes here from the power down state to the first stage where all the input bits are high.

Figure 4.11 shows the output current for all the binary input words (from 00000000 to 11111111). Figure 4.12 is a zoom of the previous mentioned figure, showing the values of the upper levels in more detail.
Figure 4.6: Transient Powerup simulation results: 64 corners, Dropout Voltage = 40mV, Zoom 1

Figure 4.7: Transient Powerup simulation results: 64 corners, Dropout Voltage = 40mV, Zoom 2
Figure 4.8: Transient Powerup simulation results: 64 corners, Dropout Voltage = 40mV, Zoom 3

Figure 4.9: Transient Powerup simulation results: 64 corners, Dropout Voltage = 40mV, Zoom: Power Down
Figure 4.10: Transient Powerup simulation results: 64 corners, Dropout Voltage = 40mV, Zoom: Power Up

Figure 4.11: Transient Powerup simulation results: LED current for all binary input words, Dropout Voltage = 25mV, typical corner
Figure 4.12: Transient Powerup simulation results: LED current for all binary input words, Dropout Voltage = 25mV, typical corner - Zoom
4.3 AC open loop

Figure 4.13 shows the results of the AC open loop simulation typical corner. As one can see in this figure, the phase margin for the typical corner is about fifty degrees.

The static gain is around $140\text{dB}$. As shown in section 3.3, this gain must be very high (see equation 3.27 and the comments below it).

Figure 4.13: AC Open Loop simulation results: Typical corner
Figure 4.14: AC Open Loop simulation results: 64 corners, Dropout Voltage = 2V, Regulator Input Current = 100uA

Figure 4.15: AC Open Loop simulation results: 64 corners, Dropout Voltage = 2V, Regulator Input Current = 100uA - Zoom
4.4 Monte Carlo Simulations

Figures 4.16 and 4.17 show the result of the Monte Carlo Simulations. Appendix B gives a general introduction to the Monte Carlo method and explains what’s done in this specific case, showing the used parameter variations.

Figure 4.16: Monte Carlo Simulation Results for 50 parameter variations: LED current as a function of the Dropout Voltage

Figure 4.17: Monte Carlo simulation results for 50 parameter variations: histogram

The peak that can be observed in some of the curves in figure 4.16 is due to the offset of the operational amplifier. In order to reduce this peaks, offset compensation could be performed. This consists in adding or reducing the current that flows through one of the sides of the differential amplifier or through one of the sides of the output stage of the amplifier.

Figure 4.17 is a histogram that shows how many samples are in a certain interval of current.
Conclusion
The main objective was to design a current regulator with no more than 100\text{mV} dropout voltage, able to drive a LED with a current that can go from 0 to 50 mA. This objective was reached and improved. The dropout reached is only 25\text{mV} at 2\%, which is a five times improvement.

All the overall specifications were fulfilled except the size one. The size specification was for 0.05\text{mm}^2. The used area was around 0.07\text{mm}^2.

It was very possible to fulfill this specification and still achieve less than 100\text{mV} dropout voltage. By decreasing the width of the output transistor its $r_{ds,ON}$ increases and therefore the dropout also increases. However, the size reduction can be performed until the dropout reaches the maximum one wants to obtain. Alternatively, the $W/L$ relation of this output transistor could be kept by reducing both $W$ and $L$ values but this would increase the offset as it was shown in section 3.4.

It was chosen not to reduce the size, although it would certainly allow the fulfilling of the size specification while keeping the dropout bellow 100\text{mV}, because this way a state of the art driver was design and presenter here.

The future work section describes a way to save space and still keep the dropout value and improve the offset. Just by reducing the $W/L$ relations of the main mirror transistors and the DAC transistors and increasing the trimming range, adding more trimming bits, to compensate the consequent offset increasing.
Future Work
The solution presented in this work demonstrated to achieve great results in simulations. Unfortunately this solution could not yet be passed to silicon. This is one very important aspect still to be achieved, the laboratory results.

Some changes could easily be made in this solution in order to save space. Some of this solutions are referred to in section 3.8 such as increase the DAC reference current and reduce the width of the regulator output transistor or the gains of the DAC.

The dropout can still be reduced a little by increasing the width of the regulator output transistor. Only $20\,mV$ dropout voltage (in the typical corner) was actually reached during simulations. In order not to exceed much the space limit it was chosen not to increase so much this width.

Other option, also referred to in section 3.8 would be to increase the size of the regulator output transistor, obtaining the $20\,mV$ dropout Voltage referred above but increasing the DAC reference current and reducing its gains to save area.

Another option would be to add more trimming bits, increasing the range of the adjustment for the output current. This way some space could be save by reducing the size of some transistors like the regulator mirror transistors and the DAC mirror transistors, which would increase the output offset. This size reduction and consequent offset increase could happen as long as the trimming range isn’t exceeded.

Just reducing the $W/L$ relation of the main mirror transistors and the DAC mirror transistors would save space and increase the offset. The increase of the trimming range could compensate for this.

All this solutions have their advantages and their costs. It’s a matter of priorities. Anyway, the customized changes would not be hard to make, except if one wants to improve every single aspect, size, functionality and power consumption, in the same way. Like it was said in chapter two, where the mismatch analysis was introduced, a better technology could save space because it could archive the same mismatches with lower transistor widths and lengths.
Bibliography


Corners Analysis Considerations

The parameters which are available from different modules, like the analog voltage supply and the bias current, all have their variations around their nominal values. From the overall specifications, table 1.1 one can see that the analog supply voltage, \(avdd\), can go from 2.25\(V\) to 2.75\(V\) and the bias current can go from 0.98\(\mu A\) to 1.02\(\mu A\). For the present case, the same voltage supply was used for both analog (current regulator and bias circuits) and digital (DAC) modules. The analog supply voltage was the supply voltage used for all modules.

To note that in the used test benches, the bias current was not provided to the driver circuit directly. It was mirrored with a cascode current mirror, because in the real case there are no ideal current sources with infinite impedance. If such a source was applied directly to the driver module, the results would be much better because the mismatches would reduce (once the first mismatch occur at this mirror at the test bench) and the output impedance would increase.

Beside this there’s the temperature effects. The threshold voltage of a transistor depends on the temperature it is subjected to. This means the temperature under which the circuit is working may be able to affect it a lot.

Other variation affects the transistors by changing some of their parameters in order to make them work faster or slower. The affected parameters are the threshold voltage and the mobilities.

The values of the used resistors (used for the compensation) also varies and its minimum and maximum values are also taken into account for the corners analysis.

The voltage available from the ChargePump circuit was simulated by an ideal source. Variations were not applied to this source except in the case where it’s being swept. In the real situation the Charge Pump only has to guarantee that the LED threshold voltage plus the minimum dropout
voltage of each transistor is reached.

The corners analysis consists in making a simulation that takes all this parameter variations into account. What's done is a set of combinations between the minimum and maximum values of each parameter with the minimum and maximum values of all other parameters. For example, one of the simulations performed combines: minimum analog voltage supply, minimum bias current, maximum temperature, maximum resistance and minimum fast MOS transistors. Each combination corresponds to a different simulation and therefore one of the lines in the correspondent graphic of the corner analysis results in chapter 4. It's possible for the designer to know which line corresponds to which corner. This can be used to debug a circuit and improve certain corners that are not fulfilling all specifications. By comparing the corners one can know in under what circumstances the circuit behaves more poorly, for example by identifying that in some simulation all corners that have high temperature as a common factor present worst results that others.
Monte Carlo Analysis
Considerations

A detailed explanation of the Monte Carlo Method can be found at [7]. For the present case, this method consists in making a gaussian variation of the transistor dimension parameters, \( W \) and \( L \), centered in the respective transistor nominal values, which are the ones specified by the designer. By doing this, the mismatches on the values of the transistor parameters \( W \) and \( L \) that can occur during the fabrication process are simulated.

The differences that can occur between the nominal values and the pos fabrication values can cause undesirable offset to an operational amplifier or a current mirror. Thus, this simulation allows to take this aspects into account. For the operational amplifier case it's easy to understand that this offset comes from the fact that if both transistors of a differential pair are not really equal, then the current that flows through one drain is slightly different from the current in the other drain. This cause the Opamp to have slightly different voltages in both terminals (the plus and the minus ones).
Schematics
Figure C.1: DAC Schematic
Figure C.2: Driver Circuit complete Schematic
Figure C.3: Operational Amplifier Schematic
Layout Considerations

Figure D.1 shows a complete floor plan of the driver circuit layout. The DAC (on the top at left), the regulator main mirror (on the bottom at left) and the compensation capacitors (yellow part at the right) occupy most of the space. The total area is around 0.07 mm$^2$. The driving was taken into account for the design of the floor plan. The fact that the tracks through which 50 mA might be flowing have to be very large was taken in account. For this technology, a track with 1 $\mu$A width can drive around 1 mA current. One way to reduce size is to drive the current through different levels of metal. To note that 5 levels of metal are available.

Most of the DAC connections were actually designed. The driving is done by the tracks that can be seen around the DAC. Not all the tracks have the same width. The ones through which more current passes are larger.
Figure D.1: Layout Floor Plan