Analog Layout - Resistors

- *dummy* resistor should be added in order to minimize the faster *etching* in large areas.

- Contact resistance must be taken into account for small resistance values.

- In order to minimize the noise, the resistor can be designed with a guard ring inside a well to reduce the coupling to the substrate.

- *Matching* between resistors requires that the resistors are designed in the layout:
  - with the same orientation
  - distributed in a interdigitized or common centroid style.
Analog Layout - Resistors

Guard band

dummy
• *dummy* capacitors should be added in order to minimize the faster *etching* in large areas

• In order to minimize the noise, the capacitor can be designed
  • with a guard ring
  • inside a well to reduce the coupling to the substrate

• *matching* between capacitors requires that the capacitors are designed in the layout using a common centroid style
Analog Layout - Transistors

- The gate resistance is reduced by dividing the gate in several sections (each section with a width < 40um). \( N \) transistors can be instantiated in parallel if the instance name is \text{INST\_NAME}\<1:N>\.

- The gate resistance is reduced also by adding contacts in both sides of the \text{poly} stripes that implement the gate.

- \text{dummy} gates can be added in order to minimize the faster etching in large areas.

- Guard rings are useful to obtain noise immunity and good substrate biasing, preventing latch-up.

- Matching between transistors requires that the layout is designed:
  - using large areas for the gates
  - without metal overlapping the gates
  - distributed in a interdigitized or common centroid style.
Analog Layout - Transistors
Analog Layout - Transistors
Common-Centroid Layout:
Matching obtained by dividing the gates in two

Topology: $dA_sB_dB_sA_d$
Analog Layout - Matching

Interdigitized

Common centroid
Analog Layout - Matching

Examples of interdigitized MOS topologies:

1. \((D_A S B_D B_S A)_D\) \hspace{1cm} A:B = 1:1

2. \((S_A D A)(S_B D B_S B_D B)(S_A D A_S)\)

3. \((S_A D A_S B_D B_S B_D A_D A_S)\)

4. \((S_A D A_S B_D B_S A_D A_D A_S)\) \hspace{1cm} A:B = 2:1

5. \((S_A D A_S B_D B_S C_D C)_S(C_D C_S B_D B_S A_D A_S)\) \hspace{1cm} A:B:C = 1:1:1
Common-Centroid layout design guidelines:

1. **Placement**: The geometric center of the devices to match must be very near

2. **Symmetry**: The layout of the devices must be evenly distributed in both directions: x and y

3. **Regularity**: Partial devices must be distributes uniformly

4. **Dispersion**: The layout must be as compact and square as possible

5. **Orientation**: The number of partial devices oriented in each direction must be the same for each device to be match.
Analog Layout - Matching

Common-Centroid

Dividing each transistor in two transistors

- $A_S B_D$
- $B_S A_D$

- $A B / B A$ compliant with the orientation guideline
Analog Layout - Matching

Common-Centroid

Dividing each transistor in 4 transistors

\[ \text{D} \text{A}_S \text{B}_D \text{B}_S \text{A}_D \]

\[ \text{D} \text{B}_S \text{A}_D \text{A}_S \text{B}_D \]
Analog Layout - Matching

Common-Centroid
Common Source Stage: Voltage Gain

\[ A_v = \frac{v_{out}}{v_{in}} \]

By KCL @ \( v_{out} \)-node

\[ 0 = g_m v_{gs} + g_{mb} v_{bs} + g_o v_{out} + v_{out}/R_L = g_m v_{in} + g_o v_{out} + v_{out}/R_L \]

\[ A_v = \frac{-g_m}{g_o + 1/R_L} = \frac{-g_m}{1/r_0 + 1/R_L} = -g_m \cdot (r_0 || R_L) \]
Common Drain Stage: Output Resistance

By KCL @ v_{out}-node

\[ v_y/R_L + g_o v_y = i_y + g_m v_{gs} + g_{mb} v_{bs} = i_y + g_m (0 - v_y) + g_{mb} (0 - v_y) \]

\[ R_{out} = \frac{1}{g_m + g_{mb} + g_o + 1/R_L} \approx \frac{1}{g_m + 1/R_L} \approx \frac{1}{g_m} R_L \]
Common Gate Stage: Input Resistance

By KCL @ $v_x$-node
\[ 0 = i_x + g_m v_{gs} + g_m b v_{bs} + g_o (v_{out} - v_x) = i_x + g_m (0 - v_x) + g_m b (0 - v_x) + g_o (v_{out} - v_x) \]

By KCL @ $v_{out}$-node
\[ 0 = g_m v_{gs} + g_m b v_{bs} + g_o (v_{out} - v_x) + v_{out} / R_L \]
\[ = g_m (-v_x) + g_m b (-v_x) + g_o (v_{out} - v_x) + v_{out} / R_L \]
\[ R_{in} = \frac{1 + g_o R_L}{g_m + g_m b + g_o} = \frac{1 + g_o R_L}{g_m} \]
**Single stage basic topologies summary**

![Single stage basic topologies circuit diagram](image)

<table>
<thead>
<tr>
<th></th>
<th>CS</th>
<th>CG</th>
<th>CD</th>
<th>IDEAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_v$</td>
<td>$-g_m(r_0|R_L) \rightarrow -g_m r_0$</td>
<td>$g_m(r_0|R_L) \rightarrow g_m r_0$</td>
<td>$g_m(1/g_m|R_L) \rightarrow 1$</td>
<td>$\infty$</td>
</tr>
<tr>
<td>$R_{in}$</td>
<td>$\infty$</td>
<td>$(1 + R_L/r_0)g_m$</td>
<td>$\infty$</td>
<td>$\infty$</td>
</tr>
<tr>
<td>$R_{out}$</td>
<td>$r_0|R_L \rightarrow r_0$</td>
<td>$r_0|R_L \rightarrow r_0$</td>
<td>$1/g_m|R_L \rightarrow 1/g_m$</td>
<td>$0$</td>
</tr>
</tbody>
</table>
Single stage bandwidth comparison

- CS Amp
  \[ C_{IN} = C_{GS} + A_{vo} C_{GD} \]
  \[ C_{OUT} = C_{GD} \]
  ✓ Poor Freq. Response due to Miller Cap.

- CG Amp
  \[ C_{IN} = C_{GS} \]
  \[ C_{OUT} = C_{GD} \]
  ✓ Good Frequency Characteristics

- CD Amp
  \[ C_{IN} \approx C_{GD} \]
  \[ C_{OUT} \approx C_{GS} \]
Analog Layout – 2 stage AMPOP

Stabilized bias circuit

2 stage ampop
Initial design criteria (after reading process parameter data):

- current budget limited
- overdrive voltage: $V_{GS} - V_T > 200\text{mV}$
- $L_{\text{min}} = 1\mu\text{m}$ (avoid short channel effects and limit sub-threshold current)
- $W \cdot L_{\text{min}}$: Offset limited
- $W/L : g_m$ limited
**Overdrive in the differential the pair**

> overdrive voltage \(\Rightarrow\) > linearity, < \(g_m\)

Bias current \(I\) can be increased to compensate the \(g_m\) reduction at the expense of increased power.
Vos in the differential the pair

\[ V_{OS} = \frac{V_O}{A_d} \]

\[ A_d = g_{m \_diff} r_{o4} \parallel r_{o2} \]

\[ V_{O \_diff} = g_{m \_diff} r_{o4} \parallel r_{o2} \times \Delta V_{T \_diff} \]

\[ V_{OS \_diff \_max} = \Delta V_{T \_diff} = \frac{3 A_{VT}}{\sqrt{W_{diff} L_{diff}}} \]

\[ \sigma(\Delta V_T) = \frac{A_{VT}}{\sqrt{W \cdot L}} \]

99.7%
Vos in the differential the pair (c. mirror)

\[ V_{OS} = \frac{V_O}{A_d} \]

\[ V_{O_{\text{mirr}}} = g_{m_{\text{mirr}}} r_{o4} \parallel r_{o2} \times \Delta V_{T_{\text{mirr}}} \]

\[ A_d = g_{m_{\text{diff}}} r_{o4} \parallel r_{o2} \]

\[ \sigma(\Delta V_T) = \frac{A_{VT}}{\sqrt{W \cdot L}} \]

\[ V_{OS_{\text{mirr max}}} = \frac{3 A_{VT}}{\sqrt{W_{\text{mirr}}} L_{\text{mirr}}} \frac{g_{m_{\text{mirr}}}}{g_{m_{\text{diff}}}} \]

\[ V_{OS} = \sqrt{(V_{OS_{\text{diff}}})^2 + (V_{OS_{\text{mirr}}})^2} \]
Gain between 5,000 and 10,000

Advantage: higher gain
Inconvenient: highly restricted common mode

\[ R_o = \frac{R_{o2C}}{R_{o4C}} = \frac{(g_{m2C} \cdot r_{o2C} \cdot r_{o2})}{(g_{m4C} \cdot r_{o4C} \cdot r_{o3})} \]

\[ A1 = -g_{m1} \cdot R_o \]

Gain between 5,000 and 10,000

- Advantage: higher gain
- Inconvenient: highly restricted common mode
Analog Layout – Cascode dif. pair

Cascode \textit{versus} Folded-Cascode
Ro = Ro2C//Ro4C
A = gm1Ro

Advantage: extended common mode
VBE + Self-biasing Circuit

M₁, M₂: self-biasing circuit ⇒ \( I_o = I_1 \)

Q₁, \( R_S \)

\[ I_o = \frac{V_{BE}}{R} = \frac{V_{th} \ln \frac{I_1}{I_S}}{R} \]

fairly independent of \( V_{DD} \)

\[ \frac{1}{I_o} \frac{dI_o}{dT} = -\frac{1}{R} \frac{dR}{dT} + \frac{1}{V_{BE}} \frac{dV_{BE}}{dT} \]

\( T \uparrow \Rightarrow I_S \uparrow, I_C \text{ fixed} \Rightarrow V_{BE} \sim -2mV/°C \)

\[ \frac{1}{I_o} \frac{dI_o}{dT} = -4300 \text{ ppm/°C} \Rightarrow 0\text{°C to 70°C} \Rightarrow 30\% \text{ variation in } I_o \]

\(-55\text{°C to 125°C} \Rightarrow 75\% \text{ variation in } I_o \)