Dead-Time Control System for a Synchronous Buck dc-dc Converter

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Abstract - The autonomy of battery-operated electronic systems directly depend on the energy conversion efficiency from the battery to the lower voltage levels required by nowadays CMOS technologies. One of the major contributions for power losses in buck dc-dc converters is explained and analyzed. The work presented in this paper focuses on optimizing buck converter efficiency (synchronous rectification) by minimizing body-diode conduction losses. A new control technique, and a drive system that regulates the dead-time to a minimum value of 2 ns, are presented. Converter losses decrease by 19 % to 32 % when compared to the fixed dead-time solution.

I. INTRODUCTION

Nowadays, dc-dc converters play a central role in the performance of electronic systems. Lossless, highly efficient converters are required by the electronic industry mainly due to the increasing demand in autonomy of battery-operated systems. An additional challenge in dc-dc converters design consists in the miniaturization of the filtering components enabled by the rising the switching frequency, \( f_{SW} \), beyond several MHz, leading to an increase in the converter’s power density.

The synchronous buck topology and its operating cycle are illustrated on Fig. 1 (a) and (b), respectively. The control system shown in Fig. 1 (a) is responsible for turning on/off the switches \( Q_1 \) and \( Q_2 \). It guarantees that the switches never conduct simultaneously – shoot-through – which would largely degrade converter’s efficiency. This is accomplished by inserting a \textit{dead time} in each change of state, with both switches off. However, when none of the switches conducts, the parasitic body-diode of the NMOS transistor (\( Q_2 \)) is forward-biased due to the continuity of \( i_L \), thus generating an undershoot voltage of approximately –0.7 V at the \( L_x \) node. Taking into account that this dead time is required twice a period, the corresponding power loss is:

\[
P_{\text{diode}} \approx v_D \cdot i_L \cdot f_{SW} \cdot (t_{\text{diode}1} + t_{\text{diode}2}),
\]

where \( v_D \) is the voltage across the body-diode, \( f_{SW} \) the operating frequency of the converter and \( t_{\text{diode}} \) the duration of each dead-time interval. Converters efficiency is affected by other sources of dissipation, the most critical being the resistive power losses on \( r_{DSon}(Q_1,2) \), switch driving, and the switching losses that occur during voltage transitions on the inverter node – \( L_x \).

To reduce body-diode conduction losses, various techniques can be applied. The simplest one – the \textit{Fixed Dead-Time} technique – consists of generating a fixed delay during both \( v_{Lx} \) transitions. The nonoverlap interval must ensure that, in the operation range of the converter, shoot-through never occurs. This restriction implies a conservative design of the nonoverlap control, optimized for a specific load but with a lower efficiency in different operating points. In order to limit the power losses due to these non-overlapping periods, the converter’s operation frequency must be kept low, increasing the size of the passive filter components, and decreasing power density.
In order to address the limitations cited above, an adaptive dead-time control technique can be applied, in which the gate drive is defined after detecting the zero voltage crossing of node $l_x$ [1]. The main advantage of this technique is its ability to make real-time adjustment to the dead-time for different MOSFET switches, and temperature related delays. However, the propagation delay in the system’s feedback loop ($\approx 20$ ns), cannot be avoided, leading to severe positive dead-time errors.

An alternative approach for adaptive gate driving in a ZVS-QSW converter is proposed on [2]. The presented system sets gate-drive timings assuming that $l_x$ node transitions are linear. Therefore, it is assumed that the midpoint of the nonoverlap interval occurs when $v_{Lx}$ crosses $V_{bus}/2$, after which a delayed transition of a rectangular waveform is generated before the actual zero-voltage crossing. Positive results can be obtained in many switching cycles; however, external trimming is necessary to eliminate timing errors. A similar technique is also proposed in [3] and a successful IC implementation of a ZVS buck circuit is reported in [4].

In order to completely eliminate body-diode conduction, a “predictive” gate-drive solution is proposed in [5]. It is based on the premise that the next inverter node switching cycle is equal to the actual one, therefore enabling the system to predict the minimum dead-time required. The performed control is digital, and it is implemented by the use of a D-flip-flop phase detector, and a digital delay line. Although the system presents reduced dead-time intervals, its digital control limits a fast transient response and originates 8ns dithering when optimal conduction is achieved.

This paper proposes a new, fully analog undershoot voltage detection technique, which allows regulating dead-time into a minimum fixed value, independently of the load conditions. This significantly decreases the body-diode conduction power losses. The control system senses the inverter node voltage and detects the duration and value of negative voltages in this node. The sensor output voltage is used to limit the current in the buffers of the power transistors, thus controlling the dead time based on the undershoot voltage and duration. The system continually operates this way, only stabilizing its feedback loop when the dead time corresponds to a minimum predefined value, thereby optimizing its duration. A similar analog technique, though with a different detection circuit, is proposed in [6].

The paper is organized as follows. In section II, a control system is presented which implements the new proposed technique. Section III reports simulation results. Section IV shows the layout design of a control system’s test-chip and section V presents the conclusions of the work.

II. DEAD-TIME CONTROL SYSTEM

A. General Functioning

In this preliminary study, with the main purpose of validating the methodology, the system was simplified by controlling only one transition of $v_{Lx}$. The other transition of $v_{Lx}$ is controlled by the Fixed Dead-Time technique, as shown in Fig. 2.

The control of the dead-time is accomplished using three elementary functions:

- The identification of the two transitions of $v_{Lx}$
- The translation of the undershoot amplitude and duration into a sensor output voltage, $v_{Detec}$;
- The generation of a rectangular waveform, $v_{Ctrl}$ whose low to high transition delay is adjusted according to the average value of $v_{Detec}$.

The On-off block, the Undershoot Detector block and the Delay Generator block, perform these operation respectively. The On-off block, works as an enable/disable for the sensor, and it is used to distinguish between the two transitions of $v_{Lx}$. The voltage $v_{Detec}$ is the PWM pulse used to control the converter and is also an input signal of this control system. Fig. 3 shows the feedback loop that allows the adjustment of dead-time.

The Undershoot Detector block continuously generates a voltage ($v_{Detec}$) with the difference between $v_{Lx}$ and a reference voltage ($v_{ref}$). The actual output of the sensor consists of this error voltage shifted to half of the power supply voltage of the circuit in order to have always positive voltages and maximum dynamic range. The sensor output voltage establishes the intended dead-time value for the converter. The negative feedback loop will eliminate $v_{Detec}$, making $v_{Detec}$ approximately equal to $V_{dd}/2$.

The Delay Generator block connected to the output of the Undershoot Detector, delays the high to low transition of $v_{Detec}$ as a function of the average value of $v_{Detec}$. As a result, a rectangular waveform, $v_{Ctrl}$, is generated, and its low to high transition is delayed as much as the average value of $v_{Detec}$.

The main function of the gate-driver is to minimize the charge and discharge of the corresponding capacity of $Q1$ and $Q2$. This is accomplished by a chain of inverters that act as...
current buffers. An additional function of the two gate-driver blocks is to ensure non-overlap, avoiding shoot-through of Q1 and Q2.

When the circuit is operating, Q1 and Q2 are controlled as follows: in the high to low transition of \(v_{ld} \) (V_HL to 0V), Q1 is turned off by an instant controlled by the high to low transition of \(v_{sh} \), whereas Q2 is turned on by an instant controlled by the low to high transition of \(v_{sh} \). Conversely, in the other transition of \(v_{ld} \) (0V to 0V), Q2 is turned off by an instant controlled by the low to high transition of \(v_{sh} \), while Q1 is turned on by an instant controlled by the low to high transition of output signal of the circuit that uses the fixed dead-time technique. The Fixed Dead-Time technique consists of a simple RC circuit.

B. Undershoot Detector and On-off block

The Undershoot Detector block, as shown in Fig. 4, is composed by a common gate stage, an output capacitor and current mirrors. The common gate stage – transistor M10 – is responsible for sensing the undershoot voltage at the inverter node of the converter. This voltage is applied to the source of M10 because the undershoot voltage is negative. Transistor M10 thus operates as V/I converter that discharges \(C_{detec} \) capacitor. Transistors M3, M4, M7, M8 and M9 mirror \(i_{bias} \), current to the output node of the block, charging \(C_{detec} \). These two operations lead to the integration of the difference of both currents in \(C_{detec} \), during a switching period of the converter, as expressed in (2).

\[
V_{Cdetec} = V_{Cdetec0} + \int_{0}^{0+T_{sw}} i_{DM9} - i_{DM10} \, dt. \tag{2}
\]

The value of the undershoot voltage can be considered approximately constant, because it is mainly dependent on forward voltage drop of the body diode. Therefore, control is mostly applied to the undershoot time interval, converted by the sensor into the time during which the output capacitor is discharged. As dead-time shortens, M10 is turned off during most of the converter switching period, resulting in an increase of the output voltage of the block. As the undershoot duration becomes higher, M10 discharges the output capacitor, originating a decrease in the output voltage. When the dead time is optimized, for a certain load condition, the output voltage of this block presents a constant average value. This implies that the charging of the capacitor by M9 is balanced with its discharging by M10, resulting in a constant ripple of the output voltage of this block.

A cascode current mirror is also included in the design of this block. It is composed by M3, M4, M5 and M6. An additional resistance in series with M5 and M6 is used to generate the bias voltage applied to the gate of M10, which value is slightly lower than the threshold voltage of the transistor. Hence, M10 is sized to only discharge the output capacitor during the dead time interval.

The On-off switch is used in order to monitor only the high to low transition of \(I_{x} \) node. The topology of the switch and its driver are presented on Fig. 5. The driver only activates the switch in the pretended transition, during 60 ns, enabling the Undershoot Detector to sense the inverter node voltage during this period. The switch is composed by three NMOS transistors. M13 is required in order to force the source of M11 to “0” when the sensor must be off. This way, it is possible to effectively stop sensing \(I_{x} \) node during its low to high transition.

C. Delay Generator

The main function of the Delay Detector block is to control the delay in the low to high transition. Increasing the average value of the Undershoot Generator output voltage, leads to larger delays in the rectangular waveform \(v_{C_{cap}} \). After being regenerated to logical levels, this waveform will enter in a non-overlap block, and a buffer chain. The control of Q2 is then performed. Fig. 6 shows the block diagram of this circuit. Reference [2] presents a similar solution.

In order to convert the detector output voltage into a low to high transition delay, a controlled current source (with a PMOS transistor) is used, which limits pull-up current of Inv1 as a function of the value \(v_{pd} \). At the output of the inverter, the capacitance \(C_{cap} \) is charged with a controllable slope. As a result, the low to high transition of \(v_{C_{cap}} \) is controlled. However, in order to minimize the duration of the transitions in the power stage, the signal with the controlled delay is regenerated back to logic levels by a circuit composed of four inverters and a SR latch (with two NOR gates). Moreover, Inv2, Inv3, and Inv4 limit current consumption during Inv1 pull-up. To correctly control the low to high transition of \(v_{C_{cap}} \), it is necessary to guarantee that during Inv3 low to high transition (reset signal of the latch), Inv4 (set signal of the latch) is at the logical level low. Consequently, the low to high transition of the output voltage of the circuit is uniquely controlled by the low to high transition of \(v_{C_{cap}} \).
D. Gate-Drive

Driving power switches requires charging its parasitic capacitances. A significant current is required to perform the charge/discharge process without significant losses due to the excessive duration of the turn-on/off time of the power stage. A chain of three tapered inverters drives each power switch, as presented in Fig. 7. The buffers design, based in [7], is a tradeoff that minimizes propagation delay throughout the chain, reduces charging time of the power switches, and optimizes wire-bonding related effects due to the fast driving of power switches.

A non-overlap topology is also used in the control system to avoid mutual conductance of the power switches, $Q1$ and $Q2$. In the high to low transition of $lx$ node, $Q2$ is enabled (triggered by the NAND) after $Q1$ is disabled, being the delay period defined by the Undershoot Detector, the Delay Generator block, and the delay associated to the chain of inverters. However, during this transition the system is able to cancel the delay propagation associated to the tapered chain. Noteworthy that this cancellation cannot be carried out by adaptive topologies, or it requires the existence of dithering with predictive gate driving.

During the low to high transition of $lx$ node, $Q1$ is enabled (triggered by the NOR), after $Q2$ is disabled, being the delay period defined by the Delay RC block and the propagation delay associated to the chain of inverters.

III. SIMULATION RESULTS

After the design with the SMIC’s 0.13 µm CMOS technology, in order to verify the correct operation of the control system, transient simulations were executed in HSpice and the results are presented in Fig. 8 and Fig. 9. The simulated specifications (typical corner) are presented in Table I. It is also relevant to highlight that the presented simulations include wire-bonding effects. In Fig. 8 is clear that the dead-time, during the high to low transition of $lx$ node, is regulated, given that the dc component of $v_{\text{Detec}}$ becomes constant approximately after 12 µs. The difference between the two $lx$ node transitions is more visible in Fig. 9 (a) and (b) where the regulated dead-time value is measured and shown in detail. Worth mentioning that as previously explained, $v_{\text{Detec}}$ is only decreased by the detection block during the controlled transition. This is obtained with the On-off circuit’s switch, that connects the $lx$ node and the Undershoot Detector’s input.

The system was also simulated under 192 corners with a constant 0.6 A current load, being registered dead-time values ranging from 2 ns to 22 ns. Simulation results under load variations from 0.1 A to 0.6 A are presented in Table II. These results demonstrate that the system robustly compensates load variations since the dead-time ranges from 8 ns to 15 ns. Nonoverlap interval is reduced as the load current increases due to higher power supplies fluctuation (originated by bonding-wires effects). Hence, undershoot voltage in $lx$ node is increased, which results in a lower $v_{\text{Detec}}$ voltage, and therefore a smaller generated delay.

### TABLE I

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage – $V_{\text{bat}}$</td>
<td>3.7 V</td>
</tr>
<tr>
<td>Output voltage – $V_{\text{out}}$</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Maximum load current – $I_{\text{max}}$</td>
<td>0.6 mA</td>
</tr>
<tr>
<td>Switching frequency – $f_{\text{sw}}$</td>
<td>1 MHz</td>
</tr>
</tbody>
</table>

Fig. 7. Control system with gate-drivers and non-overlap circuit.

Fig. 8. Transient waveforms of $v_{\text{lx}}$ node and $v_{\text{Detec}}$, during power up.
Efficiency improvements brought by the control system, compared to fixed 60ns dead-times are as shown in Fig. 10 (a). In order to yield more accurate results, Delay RC block of the system was adjusted to set a low dead-time during the low to high transition of $x$ node. This way system’s efficiency measurement is not negatively influenced by this transition.

Fig. 10 (b) shows the total losses percentage that the control system is able to diminish. It is clear that the losses are significantly reduced and that as the current increases, the losses reduction percentage is minimized due to the higher predominance of resistive losses in the converter. Fig. 11 shows the losses distribution with and without dead-time control under a 0.2 A load current. It is perceptible that the majority of the losses result from body-diode conduction, which is explained by the low resistive losses on $r_{DS}$ of the power switches.

<table>
<thead>
<tr>
<th>Load current (A)</th>
<th>$v_{\text{detec}}$ (V)</th>
<th>Generated delay (ns)</th>
<th>Dead-time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>1.65</td>
<td>20.3</td>
<td>14.6</td>
</tr>
<tr>
<td>0.2</td>
<td>1.62</td>
<td>17.6</td>
<td>12.5</td>
</tr>
<tr>
<td>0.3</td>
<td>1.60</td>
<td>15.7</td>
<td>11.3</td>
</tr>
<tr>
<td>0.4</td>
<td>1.58</td>
<td>14.5</td>
<td>10.3</td>
</tr>
<tr>
<td>0.5</td>
<td>1.56</td>
<td>13.0</td>
<td>9.1</td>
</tr>
<tr>
<td>0.6</td>
<td>1.53</td>
<td>12.0</td>
<td>7.9</td>
</tr>
</tbody>
</table>
IV. Layout

A test-chip with the control system was submitted for fabrication in the SMIC’s 0.13 μm CMOS process. Its die layout, composed by the control system and the power switches, is presented in Fig. 12. Total die area is 0.4 mm² (500 μm × 800 μm), being mostly occupied by Q1, Q2 and the gate-drivers. The Undershoot Detector, the Delay Generator and the Nonoverlap circuit (Fig. 13) required 0.015 mm² (90 μm × 165 μm), being the remaining area occupied by the gate-drivers. Mentor Calibre was used to verify design rules of SMIC 0.13μm process (DRC) and to guarantee concordance between the layout and the electrical schematic (LVS).

V. Conclusions

This paper introduces an approach to achieve optimal dead times in a synchronous dc-dc converter. An analog automatic dead-time control system is presented for this purpose. This system minimizes losses due to the parasitic body-diode conduction of NMOS power transistor of the converter. The design of the undershoot detection and control system, and the corresponding simulations results are presented. It is concluded that the system controls the dead-time duration between 8 ns and 15 ns, when the load current varies between 600 mA and 100 mA, respectively. As a result the absolute converter efficiency is increased by approximately 3.5 % in all the range of the load current, in comparison with the fixed-dead time technique. This efficiency gain is obtained by decreasing converter losses by 19 % to 32 %.

The described system allows a significant improvement in the performance of the designed buck converter with an area impact below 4 % of the overall power block area. In order to further optimize the system’s efficiency, the following tasks are suggested as future work:

1. Implementation of this control system in the other transition of the $I_x$ node;
2. Increase of Undershoot Detector gain so that the dead-time interval becomes more insensitive to the converter and temperature variations. A dead-time of 5 ns is proposed.

ACKNOWLEDGMENT

The authors would like to thank Prof. Jose Epifanio da Franca and Eng. Nuno Ramalho for the valuable support throughout this work.

REFERENCES