Summary

For the new generation MSTP device, applying LCAS is the extension of VC technology, which allowed the adjustment of link capacity hitless in transmission network without any break to incurrent service or reserved bandwidth resource. The article introduces the operation mechanism of LCAS in SDH/SONET network and point out that even though LCAS really brings us much more advantages in SDH transmission network, it also brings some drawback to us. The paper mainly analysis the time delay problem of SDH network that introduced by LCAS according to the related protocols for LCAS and practical system application. The time delay derives from the LCAS technology itself could take for the necessary cost of flexibility and control [1]. The most practical contribution of the adjustment delay results is in the link delay determination. This knowledge of link delays, at best only loosely estimated today, provides the critical support for rolling out next-generation applications over the transport infrastructure.

1 Introduction

The new generation MSTP device has made good use of VC (virtual concatenation) technology, which advantages are obviously, but the introduction of this kind of technology will greatly have impact on the robustness of SDH/SONET network. So, virtual concatenation does not change the SDH hierarchy through and through, the disadvantage of link bandwidth assignment still exists. If there is happened a failure in one of VC member [2], which will lead to inactivation of the whole VC group.

In the practical application, user’s bandwidth demand is always changing with time. Virtual concatenation technology can not provide the dynamic bandwidth assignment ability to network, the user’s bandwidth assignment is still based on peak rate value, which means the bandwidth is fixed in given time. So, the adjustment of path capacity is static, and the service will be break or even loss. As the multi-SLA network is concern, the ability of dynamic bandwidth adjustment is necessary for the SLA will always limit the service break times.

Link Capacity Adjustment Scheme (LCAS) is the extension of VC technology, which allowed the adjustment of link capacity hitless in transmission network without any break to incurrent service or reserved bandwidth resource. The LCAS enables network service providers to dynamically add STS-n channels to or drop them from a Virtually Concatenated Group (VCG).

LCAS in the virtual concatenation source and sink adaptation functions provides a control mechanism to hitless increase or decrease the capacity of a VCG link to meet the bandwidth needs of the application [1]. A new STS-n channel can be added to the VCG provided that the time delay between the new STS-n channel and the existing STS-n channels in the VCG is within a certain bound that reflects the available memory buffer supported by the EoS system. It also provides the capability of temporarily removing member links that have experienced a failure. The LCAS assumes that in cases of capacity initiation, increase or decrease, the construction or destruction of the end-to-end path of each individual member is the responsibility of the Network and Element Management Systems.

2 The operation mechanism of LCAS in SDH network

The operation of LCAS is uni-directional. This means that in order to bi-directionally add or remove members the procedure has to be repeated in the opposite direction. Note that these actions are independent of each other and are therefore not required to be synchronized. The scheme allows hitless addition and removal of bandwidth under control of a management system. Additionally LCAS will autonomously remove failed members temporarily from the group. Then the failure condition is remedied [1]. LCAS will add the member back into the group. The removal of a member due to path layer fail-

Address of authors:
Beijing Univ. of Posts & Telecommunications (BUPT)
Optical Communication Research Center
P.O. Box 128, BUPT, No. 10
XiFoCheng Road, HaiDian District
Beijing 100876, China
Email: choumao80@263.net
Received 9 March 2006; Accepted 8 August 2006

1) The work of D. Han, X. Li and W. Gu was supported by the National High Technology Research and Development Program of China (Grants No. 2005AA122310), the National Natural Science Foundation of China, Projects No. 60372096 and Science Technology Community of Beijing.
ures will in general not be hitless for the service carried over the virtual concatenated group. The autonomous addition after a failure is repaired is hitless.

2.1 The operation of LCAS are implemented by its Control Packet

Synchronization of changes in the capacity of the transmitter (So) and the receiver (Sk) shall be achieved by a control packet. Each control packet describes the state of the link during the next control packet. Changes are sent in advance, so that the receiver can switch to the new configuration as soon as it arrives.

The control packet consists of fields dedicated to a specific function. The control packet contains information sent from So to Sk and information sent from Sk to So.

The Multi Frame Indicator field (MFI): [1] used to determine the differential delay between members of the same VCG. Sequence Indicator field (SQ): Contains the sequence number assigned to a specific member. Control field (CTRL): used to transfer information from So to Sk and synchronize the Sk with the So. Group Identification bit (GID): Used for identification of the VCG. Member status field (MST): Information from Sk to So about the status of all members of the same VCG. It reports the member status from Sk to So with two states: OK or FAIL. Re-Sequence Acknowledge bit (RS-Ack): The toggling of the RS-Ack bit will validate the MST in the preceding multiframe. The So can use this toggling as an indication that the change initiated by the So has been accepted, and will start accepting new MST information. CRC field: used to protect each control packet. The CRC check is performed on every control packet after it has been received. If the control packet passes the CRC test, then its contents are used immediately.

2.2 Addition procedure of member(s) in LCAS ad-jus-tment

When a member is added it shall always be assigned a sequence number greater than the currently highest sequence number that has EOS in the CTRL code. Following is the sequence of actions for adding a new member:

- The time to “generate” a control word is explained as a constant factor. However, by transforming it into a single operation delay formulation, we can derive effective, practical solutions. Given the rise of next-generation applications such as online games where latency information is critical, this knowledge of link delays, heretofore only loosely approximated [5], enables the telecom infrastructure to be more effective in supporting these applications.

- For a bi-direction path, the source and sink must know the time delay state of each other, otherwise the source might add a member exceed the receive time delay range in the sink while LCAS is operating, which could lead to the failure of LCAS operation. And the source might add成员 continuous, hampered the normal bandwidth.

- For a bi-direction path, the source and sink may be different, even the time delay range is different [6]. So when the source decide to add a bi-direction member in VCG, it must check the time delay range to see if it is a permitted value while transmission.

3 The impact of LCAS dynamic bandwidth adjustment on SDH network

3.1 The time delay to SDH network

LCAS really brings us much more advantages in SDH transmission network. But it also leaves some drawback to us, such as the time delay and interconnection problem.

First of all, the LCAS signaling transmission have to solve the time delay problem when source-sink matching reaction [3, 4]. In VCG, each VC member might have different transmit path, so there will exist time delay between VC member.

The message exchanging causes delay among the paths which can impact service if not accounted for in the network. But it is also provably hard to approximate within a constant factor. However, by transforming it into a single operation delay formulation, we can derive effective, practical solutions. Given the rise of next-generation applications such as online games where latency information is critical, this knowledge of link delays, heretofore only loosely approximated [5], enables the telecom infrastructure to be more effective in supporting these applications.

For a bi-direction path, the source and sink must know the time delay state of each other, otherwise the source might add a member exceed the receive time delay range in the sink while LCAS is operating, which could lead to the failure of LCAS operation. And the source might add member continuous, hampered the normal bandwidth.

Another question is: the time delay between source and sink may be different, even the time delay range is different [6]. So when the source decide to add a bi-direction member in VCG, it must check the time delay range to see if it is a permitted value while transmission.
In different operation mode, the time delay introduced by the LCAS making up steps could be calculated as follows:

In Low order mode:
1. LCAS management SW changes the member state from IDLE to ACTIVE.
2. Source generates and sends an ADD command. 16 ms to generate it, 16 ms to transmit it.
3. Sink sends acknowledgement via MST bits. For HO mode, this can take up to eight multiframes: $8 \times 16 = 128$ ms.
4. Source changes CTRL word from ADD to EOS: 16 ms to generate it, 16 ms to transmit it.
5. Waiting for RS_ACK toggle reception (Sink to Source): 16 ms.

So the total delay is $16 + 16 + 128 + 16 + 16 = 208$ ms.

High order mode:
1. LCAS management SW changes the member state from IDLE to ACTIVE.
2. Source generates and sends an ADD command. 2 ms to generate it, 2 ms to transmit it.
3. Sink sends acknowledgement via MST bits. For HO mode, this can take up to 32 H4 bytes: $32 \times 16 \times 125$ us = 64 ms.
4. Source changes CTRL word from ADD to EOS: 2 ms to generate it, 2 ms to transmit it.
5. Waiting for RS_ACK toggle reception (Sink to Source): 2 ms.

So the total delay is $2 + 2 + 64 + 2 + 2 = 74$ ms.

These delays are due to the LCAS protocol. The add procedure requires to add one single member, then check PRD1, PRD2, aTLCASADDED alarm, then move on to the next tributary. This can be explained by implementation.

When you request 2 members to be added to the same VCG, the source will send ADD on both members at the same time, and PRD1 timer is started for both at the same time.

But even if the Source receives MST = OK at the same time, the Source will effectively add those members sequentially; in other words, Steps 3 and 4 above will be executed in this order:
1. Change CTRL from ADD to EOS for 1st member.
2. Wait for RS_ACK toggle for 1st member.
3. Change CTRL from ADD to EOS for 2nd member.
4. Wait for RS_ACK toggle for 2nd member.

So this procedure (Steps a and b) is reproduced each time you add a member. In the case of an ADD of 8 members at the same time, the PRD1 timer for the last members can expire before the source gets to send EOS or NORM for these last members. That’s why we recommend doing one ADD at a time.

### 3.3 Detecting member with excessive differential delay

Preamble: The VCG will report „excessive differential delay“ in this case: for any two members x and y of this VCG, deduction > maximum differential delay. So this is a per-VCG alarm. (Not per member).

The LCAS system gives some additional alarms that may help you face the situation of excessive differential delay: This reports the maximum differential delay detected among the members of a given virtual concatenated group (VCG). The maximum delay that can be detected is 128 ms.

In case it is needed to detect which member is responsible for the excessive differential delay, you can use the hardware function to detect it. These report the multi-frame count, even for member exceeding the max differential delay allowed.

Here is what can be done:
1. Freeze the multiframe count to their current value
2. Find the member with highest value.
3. The members for which deduction > maximum differential delay are the ones exceeding the maximum differential delay allowed. An increment of 1 hex in minimal value indicates 0.5 ms delay, an increment of 1 hex in maximal value indicates 0.125 ms delay, and you must take into account the roll-over behavior of the MFI counters.
4. At this point, you can simply decide to delete all the members x where the deduction > maximum differential delay.

However, this is not necessarily the best choice. See for example this scenario: imagine a situation where one member is in advance on all others; this brings down the VCG because „all other“ members have excessive differential delay. In that case, it would be judicious to suppress the member in advance instead of all other members.

So a better criteria could be to suppress the member(s) which are too far from the AVERAGE MFI value.

The link delay problem raises a number of protocol issues [7]. Clearly, it requires sharing of link delay information across the network. Being able to achieve it in a distributed manner requires control plane standards to make it happen in a seamless and vendor-neutral manner.

### 4 The effective deployment of LCAS

A key factor in the success of metropolitan-area network (MAN) applications will be the use of LCAS technology to maximize bandwidth efficiency.

#### 4.1 Important technical challenges

The effective deployment of LCAS, however, presents some important technical challenges. Among them is the critical need to tightly manage the control time delay across many traffic streams. At the same time, minimizing time delay for co-routed paths is a critical issue when delay-sensitive protocols such as Fibre Channel, Escon, digital video broadcasting or voice-over-Internet Protocol are mixed together within a VCAT/LCAS environment along with other.
Achieving a balance between the management of dynamic adjustment and time delay is a “ground-level” challenge that has to be solved at the semiconductor level. No amount of design magic at the system level can compensate for inadequate chip-level mapping performance or can overcome inflexibility of the chip’s feature set.

All of the bandwidth adjustment requirements for a network with Sonet/SDH nodes between end points can be handled using efficient memory blocks. The fiber itself is a minor factor in the overall delay equation [8]. This means that the bandwidth adjustment requirements in Sonet/SDH rings traversing many thousands of kilometers can be effectively managed with a small amount of internal memory on the VCAT/LCAS mapping chips used in each node.

In some applications, there is a large percentage of diversely routed (rather than co-routed) VCAT traffic or networks where tributaries are transmitted in opposite directions within a large unidirectional-path switched ring (UPSR) [9]. That may require handling additional delay times between member paths in a VCG.

Experience has shown, however, that these requirements can be met by adding highspeed external memory rather than including the cost of extra internal memory in every VCAT/LCAS mapping device.

4.2 Storage requirement

The amount of storage technology required to support VCAT/LCAS in system architecture depends on the maximum differential delay required. Although the G707 recommends a max of 256 ms, the typical re-quirement will be to support a maximum differential delay of +/- 16 ms, when counting the LCAS dynamic bandwidth adjustment, a 74ms or 208ms controlling time delay should be taken into account.

The storage requirement may be slightly higher, depending on the amount of control information an engineer wants to store externally along with data. This could mean the use of multiple banks of high density RAMs to realize this storage capacity. For high speeds, higher density storage is required. This need may be met using SDRAMs.

As discussed above, equipment delay support requires high-density memories with high bandwidth. This would account for high pin count and power consumption. Designers may also select on-chip memory with whatever density may be accommodated, but at the cost of reducing the amount of time delay supported. The effective deployment of LCAS is obviously based on the chip-level improvement and balancing the control flexibility and hardware cost.

5 Conclusion

LCAS technology could combine with O-UNI, ASON, GMPLS with the strengthen of optical network intellectualization [10, 11], it could fulfill all kinds of dynamic bandwidth assignment on demand in SDH application, thus adapt to the requirement of QoS and SLA of broadband data service as a prosper technology.

As latency becomes key to next-generation applications such as online games, having an end-to-end delay map will be critical information for any service provider. We believe that our insight into how one can leverage the time delay information to derive link delay will provide necessary support to deploy these applications.

References