Tecno-economic Analysis of Thermoelectric recovery of Datacenter Waste Heat

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Portugal, November 2023

Abstract— **The accelerating trend of digitalization of our society is being driven by application areas like blockchain, artificial intelligence, high performance computing, etc. Those computational workloads require computational infrastructure resources, increasingly hosted in large scale Datacenters. Those datacenters are estimated to consume today in more than 1% of the global electricity, generated in traditional gas, coal, nuclear plants or increasingly with renewable sources and then releasing a massive amount of low-grade waste heat after the electricity is used to power mostly semiconductor devices.**

Thermoelectric Generation (TEG) Devices, solid state devices capable of producing electricity based on a temperature differential, are emerging as a potential technology to take advantage of waste heat generated worldwide. Increasing investment and research in applications and new materials is opening new use case opportunities.

The hypothesis of this work is that TEG Devices can take advantage of waste heat generated in Datacenters to produce electricity that can be re-injected in the energy flow, improving efficiency, hence reducing their environmental footprint.

Keywords – Thermoelectric, Datacenter, Waste Heat, Energy Recovery.

I. INTRODUCTION

This work uses a multi-scale approach to organize the concepts around the energy flow in the Datacenter ecosystem:

- Section II concentrates in the global environmental footprint of Datacenters, the context of global waste heat, CO_2 emissions, water consumption and what is happening globally with the Datacenter energy consumption.
- Section III assembles the technical framework to understand how the energy entering the Datacenter is used, how the Datacenter is it cooled, what are the components that generate potentially usable waste heat and what are the characteristics of such waste heat.
- Section IV starts with the Processing Element, PE, identified as the insertion point for this technology/device. The focus is on the thermoelectric energy generation. This section describes the theory of operation of the Thermoelectric Device and analyses the technical viability of building such device.

A. Datacenter Growth Drivers

As the levels of digitalization of the population increase, new global scale applications that are executed for thousands or even millions of people at the same time are driving the computational needs to unprecedented scales:

Social networking, videoconferencing, online gaming, and video-streaming drove an increase of 40 % in internet traffic in 2020. Traffic in turn has increased 15x from 2010 to 2020. By 2022 video streaming and gaming are expected to make up 87 % of consumer internet traffic, according to the International Energy Agency Website. [1]

High Performance Computing impacts almost every area of research and is one of the most important assets in the process of discovery for humanity today. The next generation of challenges include calculations for fusion reactors, next generation materials science for energy storage, advanced grid optimizations, ultra-high fidelity computational fluid dynamics for transportation and combustion models, Multiphysics simulations for electric engines and next generation vehicles, etc. The current generation of supercomputers will be able to deliver Exaflops performance. An overview of the Exascale applications and computational resources to run them can be found in the Exascale Computing Project page at the US Department of Energy, DOE. Frontier, an Exascale system installed at Oak Ridge National lab and the fastest supercomputer in the world today, has an energy envelope of 20 MW and thousands of processing elements. [2]

Big Data applications like **social media, advanced marketing analytics and large-scale e-commerce** keep fast growth and now the combination of massive **genomics** databases, cross analysed with clinical records of patients will open the door for personalized treatments, individual drugs, genomics based predictive medicine, etc. And now **artificial intelligence** and the emergence of **generative AI** are showing explosive growth.

Blockchain is opening news doors in information management. At the same time uses like cryptocurrency, Bitcoin one of them, are raising alarms in energy consumption. The calculations the 'miners' must perform to produce the hash functions that validate the crypto transactions are increasingly energy onerous. In 2018 Jones presents estimates [3] of miners consuming around 20 TWh of electricity per year, around 10% of the global Datacenter consumption.

B. Global Datacenter Energy Consumption

According to the International Energy Agency [1] Datacenters and data transmission networks are responsible for nearly 1% of energy related GHG emissions. Global Datacenter

electricity used in 2021 was 220-320 TWh, or around 0.9-1.3% of global final electricity demand. This excludes energy used for cryptocurrency mining.

The first widely referenced study came from the University of Stanford. [4]Koomey presented a global consumption in Datacenters going from 153 TWh in 2005 to somewhere between 203 and 273 TWh by 2010. In 2020 Shehabi, Masanet and Koomey [5] shows that the accelerated energy consumption increases of the early 2000's slowed down dramatically, stabilizing, for the moment, around 200 TWh annually. The European perspective is presented in [6] Avgerinou projects for 2020 Datacenter consumption in Europe of 104 TWh, 140 TWh for the US and an aggregated global of 269 TWh.

Some local situations point to a more acute problem:

- Denmark Datacenter energy use is projected to triple by 2025 to account for 7% of the country's electricity use. [1]
- At the end of 2021, 11% of Ireland's electricity, more than 900MW, was already being used for Datacenters and projections estimated Datacenter electricity consumption to reach 30% by 2029 making difficult for Ireland to achieve its net zero target by 2050. [7]

C. *Environmental Impact aspects*

The impact of Datacenters operation can be placed in 3 categories:

CO_2 emissions:

Those occur mainly at the electricity generation stage. GHG emissions depend on the generation technology used. According to the International Energy Agency [1], Datacenters and data transmission networks are responsible for nearly 1 % of energy related GHG emissions. The US hosts 30 % of the global Datacenters, consuming 1.8 % of its electricity. In 2021 Shehabi [8]makes a detailed analysis considering the type of datacenters, size, water, and CO_2 footprints and then connects to the specific power plant providing their energy, water treatment facilities, environmental conditions per region and regional water scarcity data. Regarding CO_2 emissions, the study reports 3.15×10^7 tons CO_2-eq in 2018, close to 0.5 % of the total GHG emissions in the US.

Water:

Datacenters consume water on two main fronts; the water associated with cooling thermal plants for their electricity generation and water used for removing heat from the Datacenter itself. On the Datacenter cooling side, very few installations report their data. In the LBNL report [9], Shehabi presents a US national average of 7.6 liters of water per kWh generated including hydro and thermal generating plants. In addition, the study finds an additional use of 1.8 liters per kWh of electricity consumed for Datacenter cooling. Based on the energy consumption pattern and growth projections, Shehabi calculates that Datacenters consumed 626 billion liters of water in 2014, with an expected increase to 660 billion liters by 2020.

Waste heat:

According to the BP Statistical Review of World Energy [10], the global primary energy consumption was almost 600 Exajoules in 2020 with fossil fuels (oil, natural gas and coal) accounting for more than 75%. Primary Energy sources have different final uses: Transportation (22 %), Industrial (15 %), Residential (13 %) and Commercial (5 %) or the generation of electricity (45 %) for final consumption in one of the previous 4 segments. Only 1/3rd of the primary energy ends up in energy services, the vast majority is inefficient use, mostly waste heat. [11]. Each segment has a specific waste heat profile: Electricity generation and commercial activity (where Datacenter buildings are normally located) have high percentages of low-grade waste heat. Transportation has an interesting proportion of high temperature waste heat in the exhaustion gases.

The theoretical conversion efficiency of thermal energy generated from sources like coal, gas or nuclear to electricity is limited by the Carnot cycle. According to the World Energy Council [12] efficiency in combined cycle gas fired state of the art plants is close 60%, and coal fired generation is reaching a 50%, but the estimated average efficiency for installed gas and coal fired plants around the world is 41% and 34% respectively.

D. *Datacenter Green Energy Adoption*

The Datacenter industry has been particularly keen to adopt green energy consumption practices. In 2015, Goiri et al. [13], documented the emergence of renewables in this sector and according to the IEA the technology companies are in the forefront of buying renewable energy via Power Purchase Agreements (PPA)., with the big five tech companies procuring 7.2 GW of renewable in 2020 (Fig. 1), around 3.5% of all the global renewable capacity additions.

II. ENERGY FLOW IN THE DATACENTER

All the electricity entering the Datacenter will be converted to waste heat and the characteristics of such waste heat are key to determine the insertion point for the thermoelectric device and its design parameters.

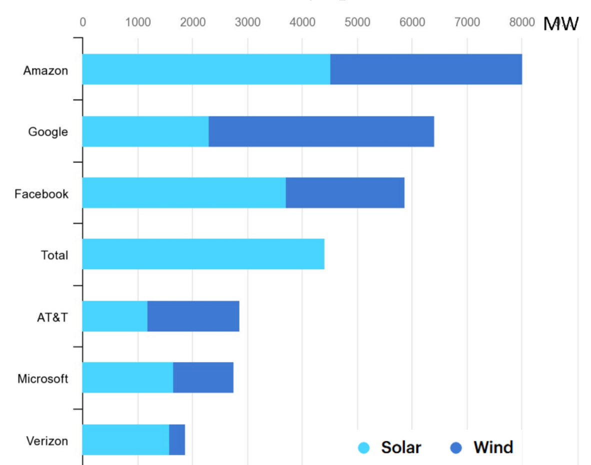


Figure 1. Corporate buyers of renewable energy via PPA. [14]

A. *Power Usage Efficiency, PUE and hyperscaling*

Datacenters consume electricity in two major categories: IT Equipment (Servers, storage, and networking) and Infrastructure Equipment (Cooling, lights, Power Distribution Units and other equipment). The PUE is the ratio between Total Facility Power and Power going to the IT equipment itself [15]. Infrastructure equipment consumption is highly dependent on the space size, scale, and technologies used.

In 2018 Shehabi, Masanet and Koomey [16] shows the decoupling between the growth in Datacenter services and their energy use with a dramatic growth in energy use drivers countered by dramatic improvements in efficiency factors: PUE, energy intensity, number of workloads per server and storage energy use. The key to achieving this dramatic improvement is in scale:

A traditional Datacenter has a typical PUE of 2, but hyperscalers are getting PUEs as low as 1.15 (Table 1) [3]. Large scale operations like Facebook, Amazon, Google, Microsoft, Tencent have more than 400 hyperscale Datacenters. Those operations can take advantage of their massive, dedicated infrastructure. In the Open Compute project, they eliminate video ports and lights in the servers and optimize everything for use and low maintenance, so facilities don't need all the conditioning to keep a massive human operation on the floor.

As organizations close smaller, older, Datacenters and move to managed, collocated infrastructures or hyperscale centers, the gains could be dramatic. The Lawrence Berkely National Report LBNL claimed that if 80% of small Datacenter servers moved to superefficient facilities in the 2016 to 2020 period, there would be a 25% drop in energy use [9]. The IEA is expecting a massive shift in Datacenter energy consumption from Traditional to Hyperscale Datacenters, from 61 TWh and 70 TWh respectively in 2019 to 39 TWh and 93 TWh respectively in 2022. [14]

Hyperscalers are increasingly building their own advanced Datacenters. It has been reported that global hyperscalers had 13777 MW of self-built capacity in 2022 with Amazon Web Services, Google Cloud, Meta and Microsoft Azure accounting for 78% of that capacity (Table 2). [17]

This dramatic improvement in PUE combined with the massive shift of workloads to advanced datacenters is keeping the Datacenter energy consumption from growing exponentially. But with PUEs below 1.1, will be difficult to keep the efficiency gains.

B. *Datacenter Cooling*

For the US, Shehabi estimated that around 40% of the Datacenter energy usage is spent in the infrastructure equipment, mostly removing the heat generated by the IT payload (Datacenter cooling).

Table 1. Typical PUE Ratios in 2014.[15]

Datacenter Type	Typical PUE
Closet	2
Room	2.5
High-End Installations	1.7
Hyperscale	1.2

Table 2. Top Hyperscalers Self-Built Datacenter Capacity 2022.[17]

Hyperscaler	Current Datacenter Capacity	Expansion Capacity Under Development
Google	3,024 MW	2,905 MW
Microsoft	2,176 MW	3,344 MW
Amazon	2,480 MW	2,533 MW
Meta	1,790 MW	2,595 MW

Cooling the computer systems in the Datacenter has been done with three typical approaches:

Air-cooling: is the most common technique for cooling Datacenter servers. A heatsink is installed on top of the processor and air can be forced through the heatsink fins using fans mounted in the computer chassis. The hot air is then expelled into the Datacenter environment and cooled using traditional A/C techniques.

Chilled Doors use a cold fluid, circulated through the rack doors (chilled), improving the capacity to transport the heat released from the servers. The fluid is circulated through an external heat exchanger that can be outside the Datacenter and performs the loop continuously.

Direct Liquid Cooling: is considered the most efficient approach and large-scale systems with higher energy densities are regular users. Here the fluid is circulated into the server, through the heat sink directly, so the heat is removed very early by the fluid. The system is more sophisticated as the possibility of leaks close to the components and increased humidity in the environment are undesirable potential effects. The reduced need of air flow allows closer packaging of components, increasing density, reducing interconnect cost, etc.

NREL – World class Datacenter efficiency

The National Renewable Energy Laboratory in the US has one of the most efficient Datacenters in the world, recognized with the 2018 Data Center Dynamics Data Center Eco-Sustainability Award. Its annualized average power usage effectiveness (PUE) rating of 1.036. [18]

This Datacenter uses warm-water liquid cooling for most of its equipment. Liquid cooling is more efficient and allows NREL to reuse the heat rejected from the equipment, connecting the cooling loop to the campus district heating loop. Water circulates through heat exchangers in the HPC system and is heated to around 100°F and used as a source of heating for laboratory and office spaces.

The hourly IT load average consumption is close to 1 MW. Evaporative coolers could eliminate the traditionally energy intensive chillers, but this solution would consume 2 million gallons of water annually. Instead, NREL solution was to utilize an advanced dry cooler called thermosyphon that uses refrigerant in a passive cycle to dissipate heat.

C. *Procesing Elements (PEs) Energy Consumption Share*

According to the survey presented by Dayarathna, et al. [19], CPUs consumed around 33 % of the used energy in servers in a Google Datacenter Scale operation in 2007. But as servers keep moving to larger number of cores, the power footprint of the PEs is significantly higher, and this is expected to become

the dominant configuration as hyper-scale servers continue hosting increasing number of virtual machines (Fig. 2).

D. Architectural Integration leading to hihger power packaging.

As the computational requirements increase and the technologies to virtualize the components and manage them effectively provide increasing flexibility, the computational elements are moving to higher levels of processing in a single package. The level of integration has implications in the device's power consumption.

a. Single Core Clock frequency

Increasing the clock frequency was the most common approach in the 90's since manufacturing techniques allowed dramatic clock cycle increases. The power dissipation of the devices increases with frequency and as the feature size decreases is harder to dissipate the heat. At some point, higher clock rate becomes impractical. CPUs today are reaching 3-4 GHz. This problem is described as the 'Power Wall'. [20]

b. Multicore Processing

The industry moved in the direction of increasing the number of cores in the package. The latest Intel generation of CPUs, the Ice Lake Platform implements 40 cores with a base clock of 2.4 GHz, that can be boosted temporarily to 3.4 GHz and a power footprint of 280 Watts.

Another multicore approach is used in the GPU by companies like NVidia. In this case, a set of simpler cores is used in parallel (Single Instruction, Multiple Data Model). A latest generation device like the NVidia Hopper H100 launched in 2022 has now 16896 cores running at 1.78 GHz and hits 500 Watts. [21]

c. Multi-Chip-Modules

AMD introduced a methodology based on 'Chiplets'. Each chiplet is a 'tile' with a number of cores; the tiles are put together in the same package with the I/O die to make a complete processor. In the latest generation, Genoa, AMD put together 96 cores using 12 chiplets with 8 cores each, implemented in 5 nm technology, with a total package thermal envelope of 360 Watts.

d. System on Chip (SOC)

Multiple independent cores of functional components like specialized numeric accelerators, memory drivers, network interfaces, can now be co-packaged, integrated in one device.

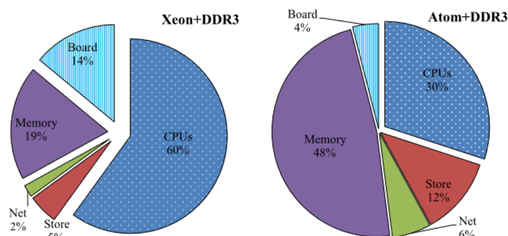


Figure 2. - Power distribution in large vs. small servers. [19]

Arm based SOCs tend to follow this methodology. One of the best SOC designs is the Fogaku A64FX. This SOC is the basic building block for the Fogaku supercomputer, number one system in the top500 during 2021. This SOC integrates in the same package 4 Core Memory Groups, each with 13 Arm cores, memory controller, interconnect controller, PCIe interface. [22]

e. 3D packaging and System in Package

In this emerging package, multiple dies are stacked in a single substrate. It is being used in situations like High Bandwidth Memory, HBM, where co-locating the memory dies reduces the traces length allowing faster signalling. In addition, new system in chips packaging allows to co-locate the CPU or GPU with the stacked HBM, using a shared silicon known as the interposer as shown in Fig. 3.

In the dies stack, heat is flowing vertically through the multiple dies, generating temperature a temperature gradient between dies. Embedded cooling inside the stack is an emerging field to solve this problem. [23]

E.High Performance Microprocessor Cooling

As processing elements increase their power consumption, the constraint of keeping the device at operating temperature becomes increasingly complex. This section is focused on describing the characteristics of the heat generation and cooling process, the operational constraints and some implications that will impact the next stage in the design process.

a. Heat Flux

The heat flux is defined as (Heat dissipated/area of the chip) The study [24]study maps multiple CPU implementations from AMD and Intel and stablish the heat flux in relationship to the CPU Frequency and the Die size, increasing in time trend. While this projection was made in 2012, the recently announced Ampere GPU from NVidia, probably the most advanced processing element today has 3456 cores and occupies a die size of 862 mm², 54.2 billion transistors and a 400 W TDP. [25] With those numbers the heat flux can be calculated in a little under 50 W/cm².

Heat generation in high performance microprocessors is asymmetric, the heat generated is not equally distributed in the semiconductor as different processing areas are normally used in different times and different intensities according to the instruction flow.[26]

The asymmetry in heat generation creates 'Hot Spots', which negatively affect performance and create temperature deltas inside the chip, adding complexity to the cooling process.[27] . The hot-spot power dissipation density is likely to reach 200 W/cm².

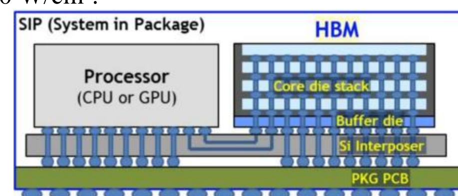


Figure 3. Heterogeneously Integrated Package with 3D stacked HBM dies. [23]

b. Leakage Current

A small current still flows through isolators when there is a voltage difference. As technology nodes are reduced in size, the isolator is thinner, and this leakage current becomes more significant. After the 50 nm nodes static power consumed without load takes a more significant fraction of the power in the devices. Another critical aspect of leakage current is the dramatic increase with temperature. Fig. 4 shows orders of magnitude increase going from 40 to 100 °C in an SRAM memory cell. [28] This imposes a critical constraint in the temperature range of semiconductors operation.

c. Electromigration, Mean Time to Failure and Black's Equation

As current flows through the metal interconnections, the momentum of the electrons can sometimes be transferred to the metal ions, making them drift, in the direction of the current, to a different position to the original. High current densities generate stronger electromagnetic forces making this effect, called Electromigration, become more prevalent.

The effect of electromigration, moving the metallic material, can generate voids (open circuit) or Hillocks (short circuit), which translate to unintended situations in the semiconductor device.[29]

A mathematical model of the Mean Time to Failure, MTTF Black's Equation (1), has been developed in the semiconductor industry. [30]. The MTTF is dependent on the Current Density J, the absolute temperature T in °K, the Boltzmann constant k, the activation energy Ea, a constant based on metal line properties C and the integer constant n.

$$MTTF = \frac{C}{J^n} exp^{(\frac{Ea}{kT})} \quad (1)$$

As the current density increases with smaller technology nodes, the sensitivity to temperature keeps increasing in new devices.

d. Semiconductor Package System

The most critical parameter on the packaging model is the $T_{junction}$, also called T_{jMax}, this is the hottest point in the silicon die. The temperature for the whole package, T_{case} is measured at the Integrated Heat Spreader (IHS). Ambient temperature or "room" temperature is measured at the air intake. Standard Ambient temperature is 22 °C.

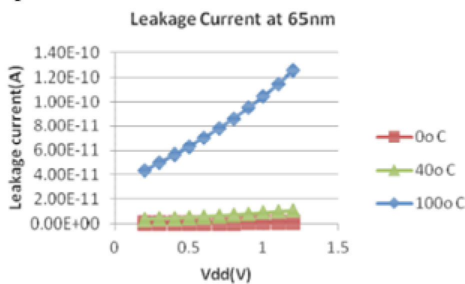


Figure 5. Leakage current, 6T-SRAM Bit-Cell memory, 65 nm [28]

The Thermal Design Power specification, TDP, is the power dissipated as heat as designed at maximum work for a specific processor.

A Thermal Interface Material, TIM, is used to facilitate the transfer of heat between the Die and the IHS, Fig. 5. Finally, a heatsink device is used to increase the heat exchange area if the system is air cooled or including the fluid circulation system is the system is liquid cooled. As shown in Fig. 5 the semiconductor package is then connected to the heat sink using a second TIM (TIM-2).

State of the art case LUMI – HPC Supercomputer

LUMI is today the largest Supercomputer in Europe, and the third globally in the November 2022 Top500 list with 375 Petaflops of sustained performance and 550 Petaflops of peak performance. LUMI is 100 % powered by hydropower and its waste heat is used for district heating. The system uses the HPE-Cray liquid cooling technology. [31]

This system has 2 partitions, one based on GPUS (2560 nodes with 1 AMD EPYC 7A53 CPU and 4 x AMD Instinct MI250x accelerators each) and the other using traditional CPUs (1536 nodes with 2 x 64 cores AMD EPYC 7763 CPUs each). The AMD Instinct MI250X GPUs are Multi-Chip-Modules, fabricated with 6 nm technology, 58.2 M transistors in a 724 mm^2 die. The TDP for the MCM is 560 W. The calculated power density is 38.5 W/cm^2. [32]. The AMD EPYC 7763 is also an MCM, 7 nm technology, 33.2 M transistors. This CPU has 8 computing dies of 81 mm^2 each and one I/O die of 416 mm^2 in 12 nm technology, with a TDP for of 280 W and calculated power density of 26.32 W/cm^2. [33]

III. Thermoelectric Generation

A. *Theory of operation*

If an electric conductor is heated on one side while the other side is cooled, the electrons in the hot side will have more kinetic energy than the electrons on the cooler side. As the hot electrons with more kinetic energy travel faster towards the cooler side than the ones traveling in the opposite direction the hot terminal ends up positively charged, generating a small voltage. An assembly of thermoelectric junctions is known as a TEG module and produces electric DC. As shown in Fig. 6, in a typical TEG one of the terminals contains positive type carriers (p- type, holes) and the other contains negative carriers (n- type, electrons). They are connected in a U-shaped setup and an electrical potential is developed between the terminals. [34].

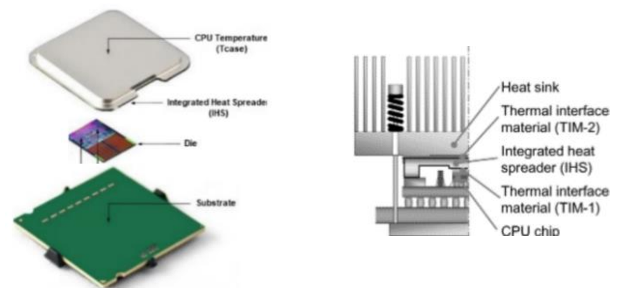


Figure 4. Physical CPU assembly detail.

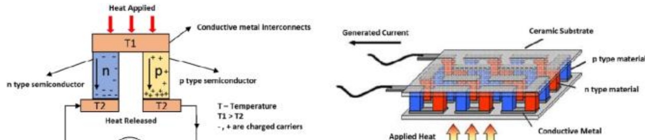


Figure 6. Schematic View of a TEG system setup.[3]

a. Seebeck Effect

The potential of a TEG material to convert heat directly into electric energy is determined by the Seebeck coefficient [V/°K], defined in the 1820s by the German Physicist Thomas Johan Seebeck, (although there seems to be evidence that Volta had observed the effect decades before). The generated voltage is directly proportional to the temperature difference of the junction. The Seebeck coefficient can be positive (for p-type materials that exhibit excess of holes) or negative (n-type materials with excess of electrons), is measured at 0°C and changes with the temperature, (Table 3). [34]

b. The zT Figure of Merit

The Seebeck effect, thermal resistivity and electrical conductivity are combined is in a dimensionless figure of merit, zT (2) that represents the thermoelectric performance of the material and is defined as

$$zT = \frac{Seebeck^2 T}{\rho k} \quad (2)$$

where T [°K] is the average operating temperature, ρ [Ω.cm] the electrical resistivity and κ [W. m^{-1} $°K^{-1}$] the thermal conductivity of the bulk thermoelectric material. [35].

The thermoelectric material is expected to have a large Seebeck coefficient, a low electrical resistivity (or high conductivity) and low thermal conductivity. While it would be ideal to improve the 3 parameters independently, the reality is that they are related in factors like band structure and carrier concentration. Electrical and thermal conductivities increase with the carrier concentration, but the Seebeck presents an opposite effect.

c. Thermoelectric conversion cycle efficiency

The TEG efficiency η_{TEG} is defined as the ratio between the electric output and the heat input. The TEG conversion cycle maximum efficiency η_{TEmax} is limited by the Carnot efficiency and determined by the figure of merit zT as shown in (3).

Table 3. - Example Seebeck coefficients for different materials. [36]

Material	Seebeck Coeff.	Material	Seebeck Coeff.	Material	Seebeck Coeff.
Aluminum	3.5	Gold	6.5	Rhodium	6.0
Antimony	47	Iron	19	Selenium	900
Bismuth	-72	Lead	4.0	Silicon	440
Cadmium	7.5	Mercury	0.60	Silver	6.5
Carbon	3.0	Nichrome	25	Sodium	-2.0
Constantan	-35	Nickel	-15	Tantalum	4.5
Copper	6.5	Platinum	0	Tellurium	500
Germanium	300	Potassium	-9.0	Tungsten	7.5

* Units are μV/°C; all data provided at a temperature of 0 °C.

$$\eta TEmax = \frac{Thot - Tcold}{Thot} * \frac{\sqrt{(1+zT)}-1}{\sqrt{(1+zT)}+\frac{Tcold}{Thot}} \quad (3)$$

B. Thermoelectric Materials

Fig. 7 shows and spectrum of materials and their figures of merit according to temperature. Thermoelectric parameters must be optimized for different applications. Some of the most common or promising materials will be highlighted in this section.

a. Low Temperature TEG Materials

Most commercially available thermoelectric modules are made of Bismuth Telluride (Bi_2Te_3). Bismuth Telluride is a semiconductor material and can be designed to continuously operate as TEG at temperatures below 260 °C, since these materials are easily oxidized and vaporized, they cannot be used for high temperature applications in the air. Bismuth Telluride Seebeck coefficient can be enhanced using different techniques, in particular making alloys with antimony and selenium. The $Bi_{0.4}Sb_{1.6}Te_3$ alloy, with a 4/1 antimony/bismuth ratio, has been widely studied and documented as TEG. Bismuth Telluride (Bi_2Te_3) Figures of Merit for p-type and n-type materials are relatively high at 100 °C, 1.35 and 0.9, respectively, making it a material of choice today for waste heat recovery. Commercial modules for applications such as machine health monitoring, automotive applications, fuel cells and wrist watches have been documented. [35]

b. Mid-Temperature TEG Materials

Going into the Mid-Grade temperature ranges, the denominated group IV Tellurides: PbTe, GeTe and SnTe have been used in the range of 500 °K to 900 °K.

Lead telluride (PbTe) has a high melting point of 1190 °K, decent chemical consistency, low vapor pressure and a solid chemical strength. PbTe reaches a 0,8-1.8 figure of merit above 700 °K [34]. Using advanced materials processing via chemical doping and alloying a zT close to 2.7 at 720 °K can be achieved with GeTe and around 2.57 at 850 °K with PbTe, in both cases for p-type material. SnTe is less toxic than PbTe but the maximum zT obtained at this point is 1.6 at 720 °K [37].

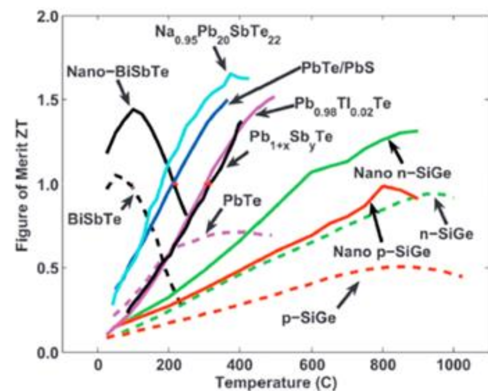


Figure 7, Thermoelectric figure of merit zT vs. Temperature [38]

c. High Temperature TEG Materials

Silicon has been widely studied in the semiconductor industry, and TEG materials have been studied since the 60s and used by NASA in different space missions. Silicon Germanium alloys (Si_xGe_x) are among the best TE materials recorded in high-temperature literature (T_{hot} > 500 °C). Those alloys are some of the simplest non-toxic thermoelectric materials. A documented zT of 1.88 at 873 °K has been achieved with nanostructured $Si_{0.55}Ge_{0.35}(P_{0.1}Fe_{0.01})$ [34].

d. Graphene

A promising thermoelectric material is graphene, a 2-dimensional structure of carbon atoms where each atom has 3 covalent bonds to other carbon atoms, creating the typical hexagonal pattern presented in Fig. 8. This 2D structure, 1 atom thick, is a single graphene sheet, with a height of just a few nanometers, making it very light with a planar density of 0.77 mg/m^2 and at the same time it has a breaking strength of 42 N/m, 100 times better mechanical strength than steel. On the thermoelectrical parameters, graphene is the most highly conductive material at room temperature, with a carrier mobility o about 15000 cm^2 /(V·s), the conduction rate of electrons in it can reach 1/300 of the speed of light, 10 times that of silicon material. The resistivity is 10-^{8}Ω·m, which is lower than the resistivity of copper or silver. The Seebeck coefficient is 100 µV/°K, comparable with other semiconductors. Graphene has a thermal conductivity of 5300 W/m°K, which is ten times the thermal conductivity of copper, but when is supported in an amorphous material, its thermal conductivity drops to around 500–600 W/m°K [39]

While the high conductivity and low electrical resistance are excellent parameters for thermoelectricity, the high thermal coefficient and zero band gap are problematic. Those parameters can be modified by doping the material or with structural modifications, leading to a variety of research paths to improve the overall figure of merit for carbon-based materials. Multiple stacked graphene sheets are denominated multi-layer graphene, and many stacked layers (>30) is common graphite. A graphene sheet can be rolled on itself and closed forming a tube, called nanotube. There is also another 3-dimensional structure based on carbon called fullerene, where instead of hexagonal rings the structure is connected in pentagons, creating a spherical, hollow shape. Carbon nanotubes can be 'unzipped' to produce a flat section known as nanoribbon.

A zT of 1.4 has been reported with graphene and c60 clusters synthesized by chemical vapour deposition (CVD). Experimental analysis showed three peak zT values of 2.0, 2.7 and 6.1 at 300 °K, with a twisted bilayer graphene nanoribbon junction. [34]

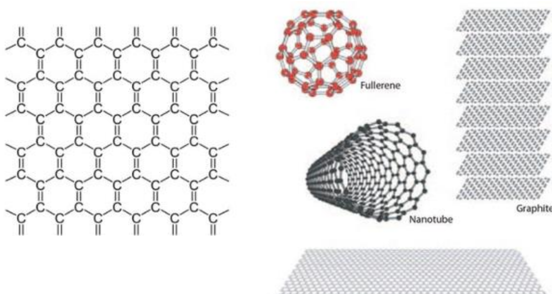


Figure 8. (Left) Graphene hexagonal (honeycomb) pattern. (Right) Graphene is the building block for multiple carbon structures

C. TEG Device for Datacenter PE Analysis

The waste heat of the Datacenter air or liquid cooling fluid has a very low temperature, just a few degrees over the ambient temperature, and any recovered electricity would require re-injecting into the datacenter, while district heating, where possible, is offering a direct route to use this waste heat. On the other hand, most of the heat is released in the electronic components, in particular the PE's with an increasing share. Current devices have an area of a few cm^2 and release a heat flux of ~50 W/cm^2, expected to increase over time. The temperature will be between ambient (0 °C in some cases, most likely 22 °C) and a T_{max} of 100 °C or less.
For the reminder of our study a T_{cold} of 0 °C, T_{hot} of 100 °C and a surface for the cold and hot plates of 1 cm^2 will be used.

The initial approach considered 'bulk' bismuth telluride, a well document material [40], with geometry features in the 100s of micrometers; this type of device has a simple fabrication process with low entry cost. Table 4 shows the thermoelectric parameters and the calculated ideal efficiency for a full device of 3.92 %.

A complete TEG Device was simulated using the Thermoelectric solver of the Ansys Workbench Multiphysics package. The geometry, Fig. 9, used 18 TE pairs, a leg base area of 2.56 mm^2, and leg length = 0.3 mm. for a total TE Area = 92.16 mm^2.

Under ideal conditions, the results show a heat flow of 56W through the TE legs, which satisfies out requirement with an electric output of 2 Watts. In terms of cost for the TE material, bulk Bi2TE3 is found at around €6/gram resulting in a cost of €610/Watt under the most favourable scenario. Under more realistic conditions the device is subject to radiation and convection losses and assuming a $T_{ambient}$ of 22 °C, the device was simulated again: the heat flow fell to 17 W/cm^2, generating only 0.14 W, an efficiency of 0.8 %. With those results, the cost of generation capacity goes to €8980/Watt, making this route unpractical.

Table 4. Efficiency Calculations Bi2Te3

Parameter	Value	Unit
Seebeck Coefficient	0.00022	[V/°K]
Thermal Conductivity	0.00131	[W/mm°K]
Electrical Resistivity	0.0175	[Ω.mm]
$zT=(S^2 \sigma)/\lambda\ T$, @50°C	0.68	---
η_{Carnot}	27%	
η_{zT}	14.6%	
η_{Device}	3.92%	

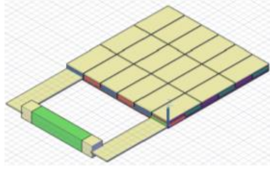


Figure 9. Bismuth Telluride Device Geometry

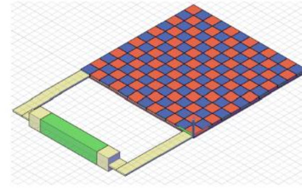
It is desirable to model the response of emerging materials that use nano-structuring to improve the thermoelectric parameters; while many of those efforts are still in the lab and will take a few years to be integrated in larger scale devices, this will give us an idea of what could be possible in a near future. A zT=2.4 figure of merit at 300 °K of,2.4 in p-type Bi_2Te_3/Sb_2Te_3 superlattices has been reported in [41]. In difference to the bulk alloy approach, the superlattice stacks very thin layers of different materials, in this case a few micrometres thick Bi_2Te_3 and Sb_2Te_3, so the electrical properties are kept constant, but the phonons path is disturbed so the thermal coefficient is changed, improving the figure or merit. With the parameters presented in the paper a new set of calculations are made in Table 6.

The same geometry was simulated with the new material. Under ideal conditions the device would produce 2.7 W, but the heat flow with the new thermal coefficient is reduced to 31.9 W/cm^2. When convection, radiation and Tambient of 22 °C conditions are imposed, the generation drops to 0.38 W with a heat flow of 13.58 W/cm^2. The efficiency falls (2.8 %), but less dramatically than in the previous case. Another consideration if that the high levels of current are generating ohmic losses, which could be mitigated increainf the number of TE pairs and reducing the feature sizes.

Based on those simulated results, a new device geometry is propossed (Fig. 10): the length of the TE legs is reduced y 4x, to 75 microns to achieve the >50 W/cm^2 requirement and the number of TE pairs is increased by 4x (72) to increase the ourput voltage and reduce the current generated. With those parameters and assuming that the efficiency of 2.8 % is maintained, the expected output would be ~1.5 W per cm$^{2.}$ There is a 16x reduction in TE material used, on the other hand, the complexity of manufacturing this device may likely require an advanced manufaturing facility, using Chemical Vapour Depositon or Molecular Beam Epitaxy techniques, moving the manufacturing cost more towards the infrastructure side and hence the production volume.

Table 5, Efficiency calculations Superlattice Bi_2Te3/Sb2Te3 material

Parameter	Value	Unit
Seebeck Coefficient	0.000238	[V/°K]
Thermal Conductivity	0.00055	[W/mm°K]
Electrical Resistivity	0.013	[Ω.mm]
$zT=(S^2\sigma)/\lambda$ T, @50°C	2.38	---
η_{Carnot}	27%	
η_{zT}	32.6%	
η_{Device}	8.74%	



Material: **superlattice Bi_2Te_3/Sb_2Te_3**
TE Pairs: 72
TE Legs: 144
TE Base Area: 0.64 mm^2
TE Legs Length: 0.075 mm
TEG Device Area: 1 cm^2

Figure 10. Proposed Design Geometry

IV. CONCLUSSIONS AND FINAL REMARKS

a. Global Datacenter use and environmental footprint

Society will require massive amounts of computational capability, increasingly concentrating in large scale Datacenter facilities. Hyperscalers have successfully rolled out the 'utility' model for computing and is increasingly difficult to support the investment for small scale operations. Those large/hyperscale Datacenters have achieved excellent levels of efficiency leaving minimal room left for PUE improvements. The increasing share of renewable energy and reduced environmental footprint of deployments becomes an attractive value proposition for customers, making this a virtuous cycle. The environmental impact of waste heat and water consumed are still a debate that will emerge over time, but CO_2 emissions are becoming a lesser concern, while the impact in national/regional grids, energy logistics, etc. are the focus of attention now.

District Heating is a major opportunity to reduce the environmental impact of datacenters and decarbonizing in a direct way a segment that according to the IEA, in 2021, accounted for 3.5 % of the global CO_2 emissions. [42] To bridge between Datacenter and the District Heating network, an efficient fluid is necessary, which makes liquid cooling a desirable feature for future large-scale datacenters.

b. Device cooling and waste heat

Architectural integration is driving an upward trend in power consumption that has increased from under 50 Watt per device package in the 80's to the 500-Watt level in today's devices and higher levels moving forward. The progression towards higher power devices is driving a higher share of the Datacenter power, reinforcing the original hypothesis that the best point to insert this technology is in the Processing Elements.

Intelligent devices requiring massive computational capability are becoming more pervasive in industrial and mobile environments where wight and efficiency are critical e.g., autonomous car driving, making the solid-state approach highly desirable.

This combination of factors points towards a dramatic increase in the value of the waste heat harvesting.

c. Thermoelectric Device and Tecno-Economic Analysis

No viable path, today, was found for delivering this device/ application combination. The requirements in space, proximity to the semiconductor, temperature range and specially heat flux

are extremely hard from the technical standpoint and then the cost seems to be prohibitive with current technology. Some observations:

- The heat-flux imposes serious limitations in the thickness of the device. With bulk materials or even with nano-structured ones, the thermal conductivity will be between 0.00131 - 0.0005 W/mm°K, implying that for the expected densities of 50 W/cm^2 it will be necessary to use thick-film devices with thickness under 0.1 mm.
- Bulk Bi_2Te_3 material already has a low potential efficiency (3.92 % for material with a zT of 0.7 under Tc_{old}=0 °C, T_{hot}=100 °C conditions), but once realistic conditions (convection and radiation effects, lower $T_{case,}$ or cooling at $T_{ambient}$ = 22 °C) are applied, that efficiency is reduced well below 1 % making it impractical.
- High area densities with very flat devices simulations point to significant advantages in cost for thin film devices once the economy of scale to pay the infrastructure investment is achieved.

The final design presented shows an encouraging path to keep research on this topic:

- The material efficiency for the nanostructured Bi_2Te_3/Sb_2Te_3 superlattice material is already interesting (8.74 % with a zT of 2.4 under Tcold= 0 °C, Thot= 100 °C conditions). Realistic numbers of efficiency once convection and radiation are introduced, but with the thermal conductivity of 0.0005 W/mm°K and the previously simulated efficiency holding, almost 3 % final efficiency could be reached.
- The device geometry, shown in Fig. 15, has 144 TE legs packed in 1 cm^2. The separation between legs is merely 0.03 mm, requiring micro-fabrication techniques. The 75 microns TE leg length the device would satisfy the heat-flux requirement with a significant advantage in cost.
- The two main manufacturing paths for high performance devices are bulk and thin film. Bulk requires a lower investment while films which require millions of euros in infrastructure. The nanostructured devices path provides an acceptable theoretical path, with lower material cost but the significant film manufacturing investment is a risky proposition, that needs strategic support.

d. Research Direction

This work points to nano-structured superlattices and micro-fabrication techniques for a potential device, but other advances in materials have huge potential: The direction of increasing the mobility of electrons vs. decreasing the mobility phonons makes more sense for this application, making heterogeneous materials with graphene insertions of particular interest, since the thermoelectric material must allow the necessary heat flux.

Embedded cooling for 3D packaging will require advanced thermal exchange at a very small scale, making a combination with microfluidics a desirable research path.

Acknowledgment

Professor Vania Silverio, PhD. at INESC MN (www.inesc-mn.pt), thanks for your mentoring.

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