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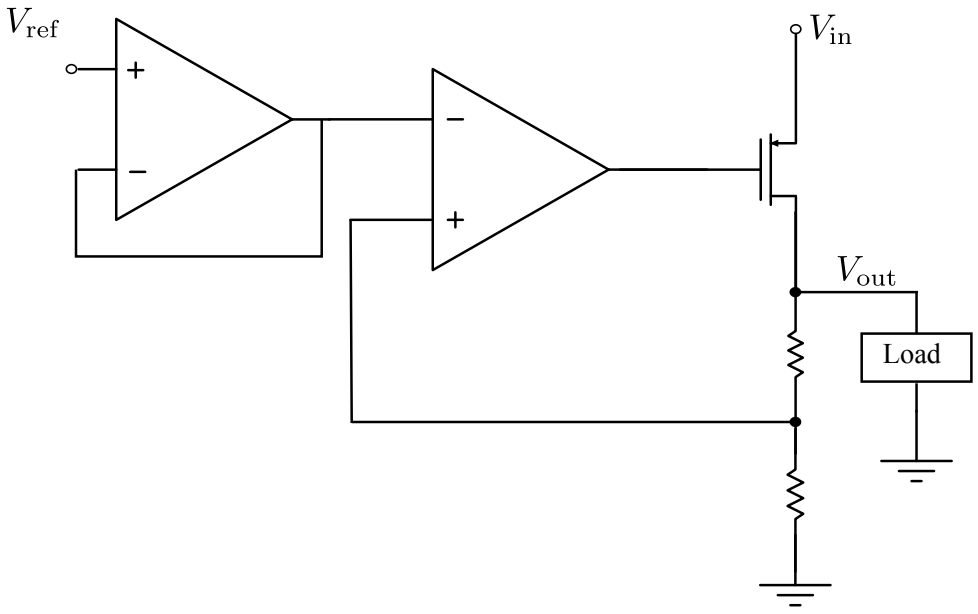

A Low Dropout Voltage Regulator with a Supply Ripple Cancellation Technique

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Thesis to obtain the Master of Science Degree in

Electrical and Computer Engineering

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I declare that this document is an original work of my own authorship and that it fulfills all the requirements of the Code of Conduct and Good Practices of the Universidade de Lisboa.

To my wife

Acknowledgments

This thesis was developed jointly with Synopsys and supervised by Dr. Hugo Teixeira and Prof. Jorge Fernandes. This allowed me to work with state-of-the-art tools and industry knowledge on analog circuits; for all of this, I'm immensely grateful.

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And finally, to my wife, who gave me a push in the right direction when I needed the most, with whom I learned the most valuable lessons of all, and without whom any of this wouldn't have been possible.

Resumo

Os circuitos analógicos necessitam de uma tensão de alimentação desprovida de variações devido à sua natureza sensível. Para esse efeito, são implementados reguladores de baixa queda de tensão com alta rejeição da fonte de alimentação para alimentar esses blocos analógicos.

Este projeto propõe um regulador com uma técnica de Cancelamento de Ruído da Fonte, projetado numa tecnologia de processo CMOS de 16nm. Esta técnica consiste em criar o simétrico do ruído da tensão de entrada e somá-lo de novo à entrada, cancelando-o efetivamente. Este regulador atua em tensões de saída de 0.9 V e para 1 mA de corrente de carga e 1pF de capacitância de carga.

Através de diversas simulações, o regulador proposto mostra ser competitivo entre as arquiteturas do estado-da-arte, oferecendo uma excelente rejeição de ruído em baixas frequências (-113 dB20) e médias frequências (-55 dB20).

São realizadas simulações de corners de processo, tensão e temperatura (PVT) e análises de Monte Carlo para comprovar a robustez do projeto e sua conformidade com a norma ISO 26262.

Palavras-chave: Regulador de baixa queda de tensão, Rácio de Rejeição do Ruído da Fonte, Cancelamento do Ruído da Fonte de Alimentação.

Abstract

Due to their sensitive nature, analog circuits need a supply voltage bereft of voltage ripples. For this end, Low Dropout Voltage regulators (LDO) with high Power Supply Rejection (PSR) are implemented so as to feed these analog blocks.

This work proposes a Supply Ripple Cancellation (SRC) technique LDO designed in a 16nm CMOS process technology. This technique consists in creating the symmetric of the input voltage ripple and summing it to the input once more, effectively cancelling it. This LDO regulates voltages for an output of 0.9 V and for 1 mA of load current and 1pF of load capacitance.

Through simulations, the proposed LDO is shown to be competitive among state-of-the-art architectures, offering excellent PSR in low frequencies (-113 dB20) and mid-frequencies (-55 dB20).

Process, Voltage, and Temperature (PVT) corner simulations and Monte Carlo analysis are performed in order to prove the design's robustness and to comply with the ISO 26262 standard.

Keywords: Low Dropout Voltage Regulator, Power Supply Rejection Ratio, Supply Ripple Cancellation.

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Nomenclature

β	Feedback factor
ΔV	Dropout voltage
ΔV_{out}	Undershoot voltage for a load transient change response
η	Power efficiency
σ	Standard deviation of a Gaussian distribution
A_{LG}	Loop gain
C_L	Load capacitance
g_m	MOS transconductance
I_{SR}	Current slew rate
I_L	Load current
I_q	Quiescent current
I_{ref}	Bias current
R_L	Load resistance
V_{buf}	Buffer output voltage
V_{in}	Input voltage
V_{out}	Output voltage
V_{DD}	Supply voltage
V_{fb}	Feedback voltage
V_{ph}	High voltage supply
V_p	Low voltage supply
V_{ref}	Reference voltage
V_{th}	MOS threshold voltage
dB20	Logarithmic relative unit for voltage ratios

Acronyms

ACCS AC Coupled Shunt

APT Advanced smooth Pole Tracking

ASIC Application-Specific Integrated Circuit

ASRC Adaptive Supply-Ripple Cancellation

CG Common Gate

CGF Common-Gate Feedback

DRC Design Rules Check

EA Error Amplifier

EMNMC Enhanced Multipath Nested Miller Compensation

FFRC Feed Forward Ripple Cancellation

FOM Figure-of-Merit

HBCG Hybrid Bias Current Generator

LDO Low-dropout Voltage Regulator

LVS Layout-versus-Schematic Check

OTA Operational Transconductance Amplifier

PM Phase Margin

PPT Power Pass Transistor

PSR Power Supply Rejection

SoC System-on-a-Chip

SRC Supply Ripple Cancellation

Chapter 1

Introduction

Contents

1.1 Overview

Despite the abrupt silicon shortage entailed by a worldwide pandemic, 2021 saw an increase in smartphone shipments, summing a total of up to 1.35 billion units [1], as can be seen on Table 1.1. Although that trend has slowed down recently due to an inflation rise and the many consequences of an on-going war between Russia and Ukraine [2], the demand for low-powered devices has never seen such heights.

Table 1.1: Top 5 Companies, Worldwide Smartphone Shipments, and Year-Over-Year Growth, Calendar Year 2021. [3]

Company	2021 Shipment volumes [millions]	2020 Shipment volumes [millions]	Year-Over-Year Change
Samsung	272.0	256.6	6.0%
Apple	235.7	203.4	15.9%
Xiaomi	191.0	147.8	29.3%
OPPO	133.5	111.2	20.1%
vivo	128.3	111.7	14.8%
Others	394.3	450.5	-12.5%
Total	**1354.8**	**1281.2**	**5.7%**

To keep up with this ever-growing need, more and more investment has been poured into the manufacturing process industry and R&D for new and more efficient solutions (US CHIPS act and European Chips Act [4]). This includes research on device power management, a facet of evermore importance due to the increasing number of transistors on a single chip.

Voltage regulators are used in a wide array of applications, such as wearable bioelectronics, System-on-a-Chip (SoC)s, or other portable electronics. More specifically, dozens of Low-dropout Voltage Regulator (LDO)s within a mobile phone to support the many different blocks it may have (camera, USB, memory...). Thus, the need for a design of such a device that minimizes power loss and improves regulation on the power supply is critical.

Any equipment that needs constant and stable voltage is suitable for implementing LDOs. It was in the 1980s that interest for these devices grew, specially in the automative industry, where microprocessors were being integrated into vehicles [5]. A modern example of portable application of this type of circuit is wearable bioelectronics, which are becoming increasingly common in these last few years, providing access to personal health monitoring for more and more people. Another common use is in a SoC such as in mobile phones.

As an example, the power source of wearable bioelectronic devices is typically a lithium-ion rechargeable battery with $V_{\mathrm{bat}} = 4.2$ V when fully charged and $V_{\mathrm{bat}} = 2.7$ V when almost discharged. These variations of battery voltages can be seen on Figure 1.1.

Analog circuits usually need a fixed power supply voltage; let's say 1.2 V as an example. The conversion from V_{bat} to V_{DD} V is usually performed by a dc-dc switching converter, which results in a large ripple voltage that affects the performance of subsequent analog circuits. To replace this with only an LDO instead would also be inefficient: as its name implies, an LDO should only be used for low voltage drops, as their efficiency is close to V_{out}/V_{in}. To avoid this, the switching converter would rather

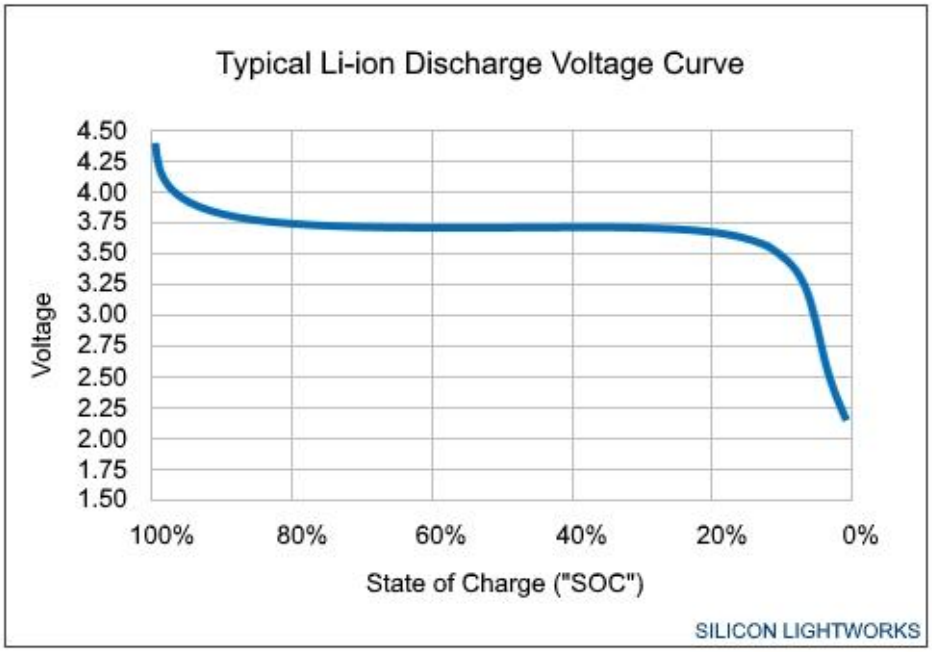


Figure 1.1: Typical Li-ion discharge voltage curve. [7]

take V_{bat} down to a regulated $V_{DD} = 1.4$ V, and then use the LDO to convert V_{DD} to $V_{\mathrm{LDO,out}} = 1.2$ V, suppressing the ripple voltage coming from the switching converter.

In Figure 1.2, a basic implementation of multiple LDO blocks in an SoC can be seen: they provide a stable voltage to each of the circuits' input, ideally bereft of noise.

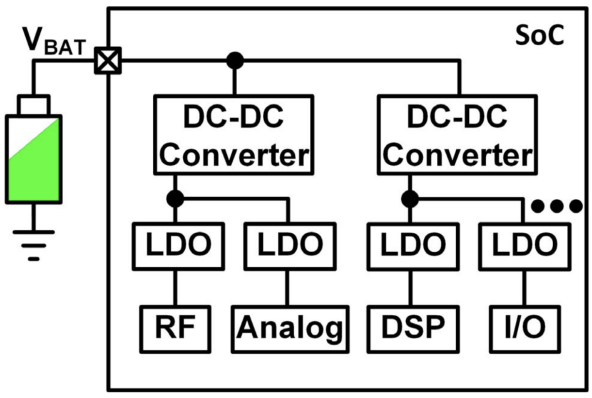


Figure 1.2: Typical power management solution for an SoC. [8]

1.2 Motivation

As described above, the need for stable voltage supplies grows, and the demand for efficient voltage regulators rises with the increase in circuit blocks per chip.

For this end, many different topologies for LDOs exist, each with their own different trade-offs. This work will focus on finding the best solution for a given specification after carefully studying state-of-the-art applications for the same technique.

1.3 Objectives

The main scope of this thesis will be the study, design and implementation (in a simulation environment) of different variants for the same technique and also propose an alternative that presents better results for a specific parameter. The goal is to design an LDO with a high Power Supply Rejection (PSR)[1] (any variation in the power supply should reflect the least possible on the output), and small quiescent current with an Supply Ripple Cancellation (SRC) regulation technique, thus allowing for stable and clean power supply. The regulator should, of course, be able to provide enough current to the load with specified accuracy under worst-case conditions.

A regulator will be proposed so that it can correct medium to high frequency noise at around 1.5 MHz by action of the SRC technique. Large load current range, low dropout voltage and small overshoot/undershoot will also be targeted for. A bulky external capacitor will be avoided, in order to minimize circuit area and to make the LDO suitable for SoC applications.

SoCs work in sleep-mode in most time of a period; LDOs require low-power loss at no load current and fast transient responses to turn ON the system from the sleep-mode immediately. Thus, the LDO should have an optimized trade-off between low power consumption, high PSR, fast transient response and compact area.

The general design of the LDO will be composed of the three following parts: an error amplifier (EA), an output stage with a power transistor, and the SRC block. Its principal parameters may be seen on table 1.2. For this case, the input voltage V_{in} will come from the high voltage supply V_{ph}.

Table 1.2: Expected results from this work's LDO.

Parameter	Symbol	Note	Min.	Typ.	Max.	Units
Technology	-	-	-	16	-	nm
Operating temperature	T	-	-40	25	125	℃
Power Pass transistor	PPT	PMOS	-	-	-	-
Supply voltage	V_{ph}	High voltage	1.030	1.200	2.030	V
	V_p	Low voltage	0.646	0.800	0.985	V
Dropout voltage	ΔV	-	-	300	-	mV
Output voltage	V_{out}	-	-	0.9	-	V
Voltage reference	V_{ref}	-	-	0.45	-	V
Turn-ON Settling time	-	-	-	< 1	-	µs
Bias current	I_{ref}	-	-	5	-	µA
Load capacitance	C_L	-	-	1	-	pF
Load current	I_L	-	-	1	-	mA
Power supply rejection	PSR	@ 1.50 MHz	-	$<$ -40	-	dB20

[1] Also known as Power Supply Rejection Ration (PSRR).

1.4 Outline

The different chapters in this work are described in the following items:

- Chapter 1: Introduction
  In this chapter, a broad contextualization of the thesis' theme, outline, goals, and structure are delivered.
- Chapter 2: LDO overview
  For this part, the basic theory of the regulators, as well as their relevant parameters, are presented.
- Chapter 3: State-of-the-art
  Different papers proposing a similar or relevant technique are examined in this chapter. From these, valuable information is extracted and applied to this work's design.
- Chapter 4: Supply-Ripple Cancellation LDO
  After carefully studying the fundamentals of the LDO and the current state-of-the-art in the previous chapters, a core design is proposed, and an alternative using the same principles of the techniques is proposed.
- Chapter 5: Results
  In this part, simulation results are presented. These results are also compared with the state-of-the-art studied earlier.
- Chapter 6: Conclusion
  An effort is made to sum up the dissertation and to verify that the goals were fulfilled. The author also makes an attempt at what could have been changed in this work for future reference.

Chapter 2

LDO overview

Contents

2.1 Low Dropout Voltage Regulator

In this chapter are introduced the fundamental aspects of regulators, some basic topologies, and many relevant parameters and results we expect from them.

LDOs are DC linear voltage regulators that provide a stable power supply voltage independent of input-voltage variations, load impedance, temperature, and time, while being able to suppress ripple voltage from the noisy input. The dropout voltage is the difference between the input and output voltages, and typical dropout voltages can range from 100 mV to 1.5 V [9].

2.2 Block Level

An LDO is fundamentally a negative-feedback system. In such a setup, there is usually an unpredictable element called the feedforward system, which is embedded in a feedback loop that is compared to a feedback network and a subtractor. Overall, four components are needed: the feedforward system to be improved, $A(s)$; a means of sensing the output $Y(s)$; a feedback network $K(s)$; and finally, a subtractor that subtracts this feedback signal to the input signal. This performs the negative feedback system, as can seen in Figure 2.1.

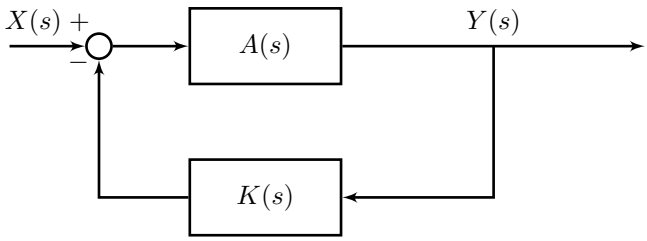


Figure 2.1: Negative-feedback system.

In its most basic form, an LDO is primarily composed of a reference voltage, a means of scaling the output voltage so it can be compared with the reference (the feedback network), an Error Amplifier (EA), and a pass transistor or Power Pass Transistor (PPT), whose source-gate voltage is controlled by the amplifier. This can be seen on Figure 2.2. V_{out} is scaled down by the feedback network, in most cases a voltage divider R_1 in series with R_2, and compared to the reference voltage V_{ref}, the latter being supplied by a bandgap reference, which is a DC voltage that has small dependency on supply, temperature, and process parameters. This bandgap reference also provides the bias current of the EA.

In the LDO's case, there is an unregulated and/or noisy supply voltage for the input, the pass transistor and error amplifier which serve as the feedforward system, and the voltage divider which is the feedback network K(s), as can be seen on Figure 2.3

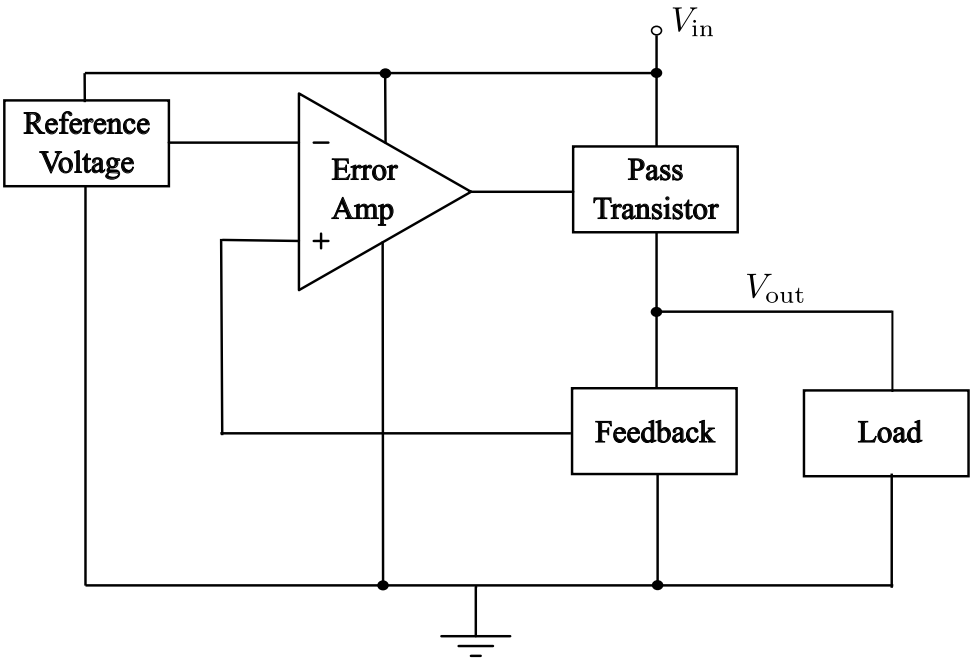


Figure 2.2: Block diagram for a generic LDO.

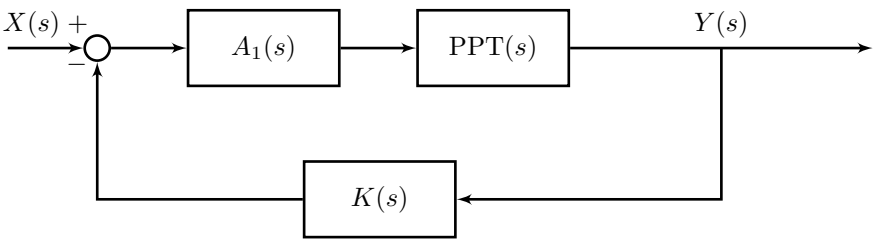


Figure 2.3: LDO feedback system.

2.3 Relevant Parameters

Although an LDO has many relevant parameters to be taken into consideration when designing such a device, the following are those that will require more attention[5]:

- **Power-supply rejection ratio**
  PSRR, or PSR, is defined as the variations in the output voltage over the input voltage $\partial V_{\mathrm{out}}/\partial V_{\mathrm{in}}$. Also known as the line transient, this is the consequence of the ripple voltages coming from the input, and it goes through two paths, the supply of EA and the pass transistor.

- **Output noise**
  The LDO itself produces this output noise $V_{n,\mathrm{out}}$, even in the absence of input noise.

- **Line regulation**
  This is the the system's response to slow variations of the input voltage.

- **Load regulation**
  Defined as $\partial V_{\mathrm{out}}/\partial I_L$, this effect depends on the LDO's output impedance. Transient currents from the load circuits can cause serious voltage ripples at the LDO's output. This effect is more significant at higher frequencies.

- **Power consumption and area**
  In SoCs that make use of several LDOs, these two parameters are of great importance.

- **Stability**
  As the LDO employs a feedback loop, its Phase Margin (PM) should be acceptable enough so as to prevent the degradation of the aforementioned parameters.

As will be seen on section 2.6, there are other metrics the engineer should look out for, but these five usually serve as goalposts for any LDO's design. As described on Chapter 1, this work will specifically focus on optimizing PSR.

2.4 Pass Transistor

The pass transistor can serve as a controlled current source or as a source follower, each implementation having its advantages and drawbacks in terms of circuit parameters and performance. It can also serve as a controlled resistor, but this leads to PSR degradation amongst other negative results, which is why it isn't a usual choice [5].

In this section, a careful analysis of the pass transistor implementation is produced, with the goal to extract as much valuable information that may later serve for this work's design.

2.4.1 Source Follower

Selecting an NMOS pass transistor results in a source follower topology for the LDO. It has in fact higher PSR than its PMOS counterpart, as the drain voltage variations don't affect the source voltage if channel-length modulation is neglected[5].

The transistor has practically no Miller effect; it has a quick transient response. It works almost as a common gate amplifier. As the load voltage $V_{\rm out}$ increases, the source's increases, V_{GS} is reduced, which pumps less output current, and in turn less output voltage. It has a "natural" negative feedback.

However, for the same dropout voltage, and since the gate voltage is $V_{\rm out} + V_{\rm th,PPT}$, a higher supply voltage ($> V_{ph}$) would be needed for the EA in order to keep it in a good operating point.

Thus, this structure may only be possible if an additional charge pump is placed to the opamp's supply, which in turn compromises area overhead, power efficiency, and startup times. This is why, in practice, few examples of NMOS LDOs are encountered, and why it won't be a subject of analysis for this thesis.

2.4.2 Current Source

An EA paired with a PMOS pass transistor operating in the saturation region form a voltage-controlled current source. The dropout voltage, which is the source-drain voltage of the transistor $|V_{DS}|$, is minimized by selecting a wide transistor [5]. In Figure 2.4, a basic LDO with a controlled current source can be observed.

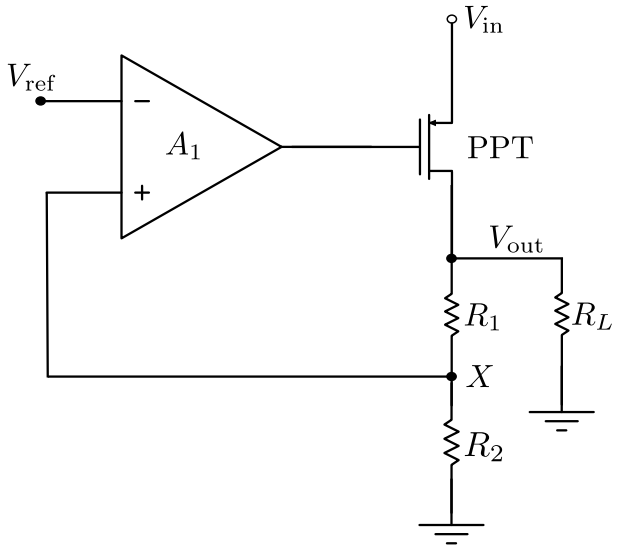


Figure 2.4: Conventional LDO using a PMOS transistor, with a load resistance.

The output voltage $V_{\rm out}$ is equal to $V_{\rm ref}/\beta = V_X/\beta$, where β is the resistor string ratio $R_2/(R_1 + R_2)$, and V_X is the feedback voltage coming from the voltage divider.

To determine the load and line regulation expressions, the loop gain A_{LG} must first be found. For now, it is assumed that the opamp has a gain A_1 and infinite supply rejection. To find the expressions for $\partial V_{\rm out}/\partial V_{\rm in}$ and $\partial V_{\rm out}/\partial I_{\rm L}$, the loop will be broken at the point X on Figure 2.4, cutting off the feedback

network from the output. By assuming a certain small-signal resistance R_L to the load, the following equation can be obtained:

$$A_{LG} = A_1 g_{m,PPT} \left[R_L \parallel (R_1 + R_2) \right] \frac{R_2}{R_1 + R_2}. \tag{2.1}$$

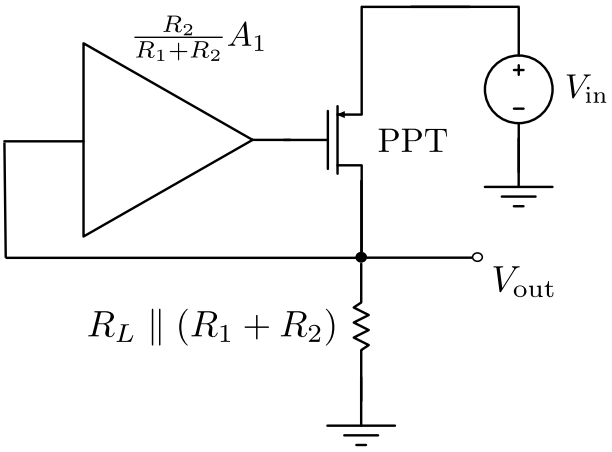


Figure 2.5: A model for finding PSR. [5]

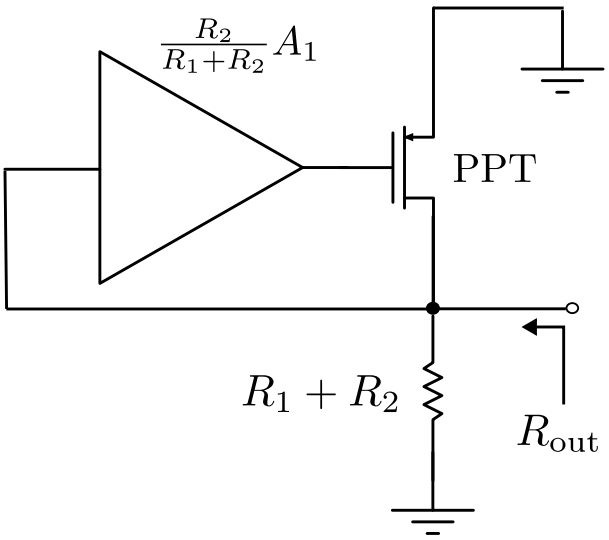


Figure 2.6: A model for finding the output resistance. [5]

From this, it can be stated that the opamp's gain amplifies that of the PPT. To find the PSR expression, a small-signal model is needed to be built, as in Figure 2.5. From here, it is observed that the gate-source voltage of the pass transistor is:

$$V_{GS,PPT} = \frac{A_1 R_2}{R_1 + R_2} V_{out} - V_{in}, \tag{2.2}$$

turning the small-signal current flowing through the pass transistor to:

$$I_{D,PPT} = g_{m,PPT} \left(\frac{A_1 R_2}{R_1 + R_2} V_{\text{out}} - V_{\text{in}} \right). \tag{2.3}$$

This current then flows into the equivalent output resistance $R_L \parallel (R_1 + R_2)$, and therefore:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{g_{m,PPT}\left[R_L \parallel (R_1+R_2)\right]}{1 + A_1 g_{m,PPT}\left[R_L \parallel (R_1+R_2)\right]\frac{R_2}{R_1+R_2}} \tag{2.4}$$

$$= \frac{g_{m,PPT}\left[R_L \parallel (R_1+R_2)\right]}{1+A_{LG}}. \tag{2.5}$$

As $A_{LG} >> 1$:

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \left(1+\frac{R_1}{R_2}\right)\frac{1}{A_1}, \tag{2.6}$$

which means that the line regulation can be enhanced by increasing the opamp's gain A_1.

It can also seen that load regulation $\partial V_{\text{out}}/\partial I_L$ is the output impedance R_{out} of the LDO. This means that drawing the circuit as in Figure 2.6:

$$R_{\text{out}} = \frac{1}{g_{m,PPT} A_1 \frac{R_2}{R_1+R_2}} \parallel (R_1+R_2). \tag{2.7}$$

As the first term of the parallel combination is much inferior to the second:

$$R_{\text{out}} \approx \left(1+\frac{R_1}{R_2}\right)\frac{1}{g_{m,PPT}A_1}. \tag{2.8}$$

So as it was for the line regulation, for the load regulation high A_1 will be needed.

The PMOS pass transistor has an output resistance $r_{o,\text{PPT}}$, which allows V_{in} to pass to V_{out} and degenerate the PSR. This degradation worsens if the transistor passes from saturation to the linear region, which is one of the reasons why it needs to be guaranteed that the output transistor has enough saturation margin.

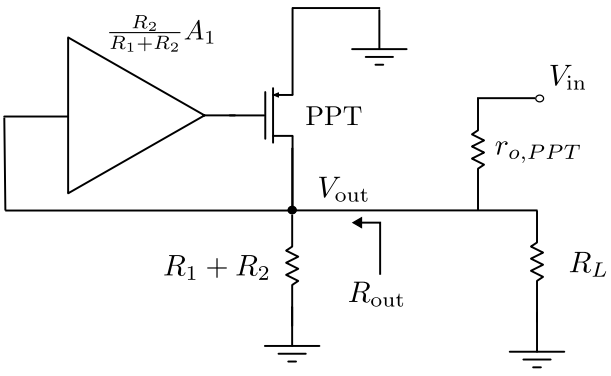


Figure 2.7: The effect of transistor output resistance on PSR. [5]

From Figure 2.7, this can be seen as a simple voltage division between $r_{o,\text{PPT}}$ and R_{out}:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_{\text{out}}}{r_{o,\text{PPT}} + R_{\text{out}}} \tag{2.9}$$

$$= \frac{1+R_1/R_2}{g_{m,PPT} r_{o,\text{PPT}} A_1 + 1 + R_1/R_2}, \tag{2.10}$$

assuming $R_L >> R_{\text{out}}$. As 2.9 is much lower than 2.6 (by a factor of $g_{m,PPT}r_{o,\text{PPT}}$), the former equation can be discarded, but only when the transistor works in saturation, as previously mentioned.

The output noise can be extracted by modeling the two appropriate noise sources as voltage sources, as can be seen on Figure 2.8: the noise from PPT $\overline{V^2_{\text{n,PPT}}}$, and the noise coming from the voltage reference, the voltage divider, and the amplifier, $V_{\text{n,A}}$. The noise of PPT can be divided by A_1^2 and put in series with the noise source from the reference voltage. Assuming a high loop gain:

$$\overline{V^2_{n,\text{out}}} = \left(1 + \frac{R_1}{R_2}\right)^2 \left(\overline{V^2_{n,A}} + \frac{\overline{V^2_{n,\text{PPT}}}}{A_1^2}\right). \tag{2.11}$$

From this equation, it can be gathered that by increasing the gain of the amplifier, the noise effect from PPT can be minimized.

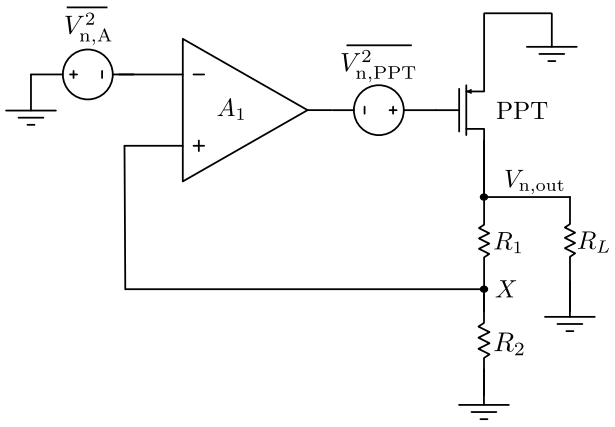


Figure 2.8: The LDO circuit including noise sources. [5]

If ripples exist at high frequencies at either input or output, then the equations (2.6) and (2.8) need to be revisited. This is mainly because the opamp will have at least one pole, rendering:

$$A_1 \rightarrow \frac{A_0}{1 + \frac{s}{\omega_0}}, \tag{2.12}$$

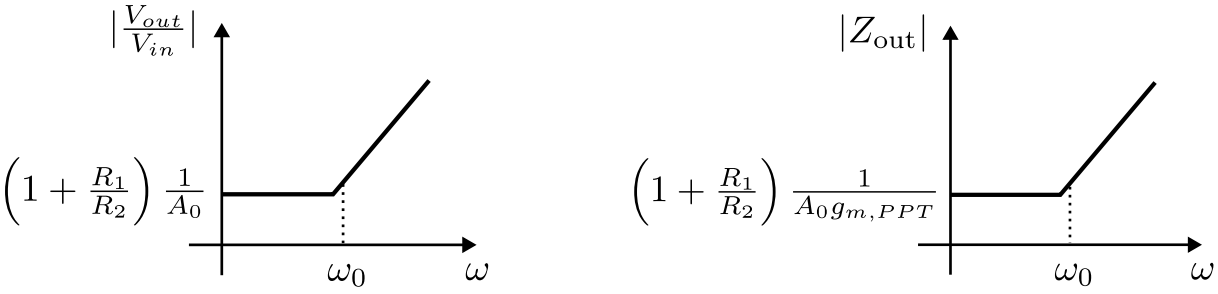
and as a consequence the previous PSR equation changes to:

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \left(1 + \frac{R_1}{R_2}\right) \frac{1}{A_0} \left(1 + \frac{s}{\omega_0}\right), \tag{2.13}$$

while the output impedance turns into:

$$R_{\text{out}} \approx \left(1 + \frac{R_1}{R_2}\right) \frac{1}{g_{m,PPT}A_0} \left(1 + \frac{s}{\omega_0}\right). \tag{2.14}$$

With this in mind, the LDO's frequency response to supply noise (PSR) and output impedance can be sketched, as in Figure 2.9: beyond ω_0, PSR and load regulation degrade. This is where this work's proposed design should develop on.



(a) PSR.

(b) Output impedance.

Figure 2.9: LDO frequency response for a one-pole opamp.

2.5 Error Amplifier

The EA shall be implemented as an Operational Transconductance Amplifier (OTA): these blocks usually drive capacitive or high impedance loads (unlike opamps, which drive resistive or low impedance loads). In this case, it will have a MOS gate as load.

2.5.1 One-stage OTA

For a single-stage OTA, there are many possible architectures: among these, the most simple and most familiar to us is the differential pair with an active load. However, this topology doesn't offer nearly enough gain needed for this context.

Another possibility would be to use cascode amplifiers: among these, the telescopic and folded-cascode architectures are a possibility. Although the voltage headroom is very low due to the stacked transistors (5 in the telescopic and 4 in the folded-cascode), these usually offer high gain for a given bandwidth.

2.5.2 Two-stage OTA

Using a two-stage circuit architecture for the amplifiers' design has been a popular approach for many years. Designs with three or more stages, however, can become a challenge, as it becomes harder to reduce the number of poles. In a two-stage configuration, the first stage is configured so that it offers high gain, while the second supplies high swing. The first stage can be incorporated according to many different topologies, usually a differential pair with an active load; the second stage is most commonly set up as a common-source stage so as to allow maximum output swings [6]. This architecture is usually coupled with an output buffer, as can be seen in Figure 2.10; this stage is only present when the circuit needs to drive resistive loads. Amps such as OTAs have no need for the buffer stage.

These OTAs are useful for when the circuit cannot afford have as many stacked transistors as the cascode topologies (when you have a low supply voltage).

A typical two-stage amp may be seen on Figure 2.11.

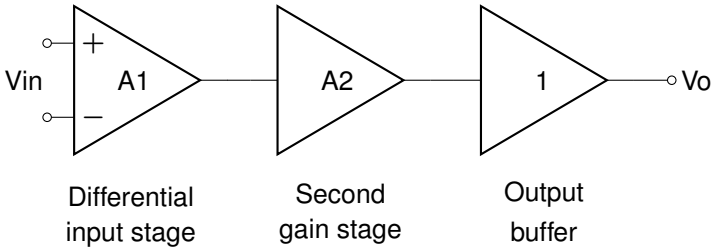


Figure 2.10: Typical OpAmp stages.

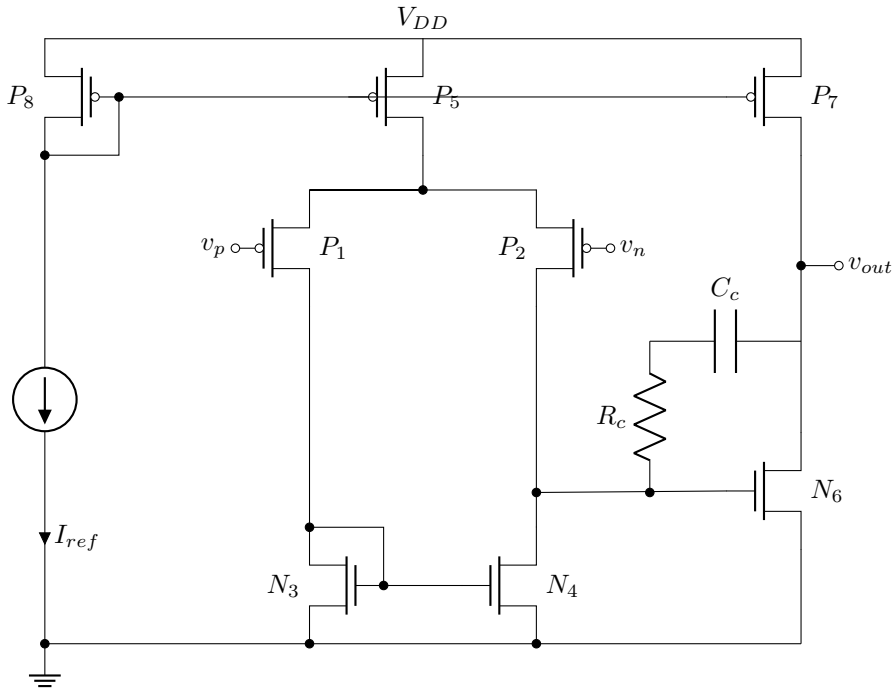


Figure 2.11: Two-stage CMOS OTA design.

2.5.3 Amplifier Comparison

As can be seen on table 2.1, the many amplifier topologies offer different tradeoffs.

Table 2.1: Comparison of performance for various amps. [6]

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-stage	High	Highest	Low	Medium	Low
Gain-boosted	High	Medium	Medium	High	Medium

As for an LDO, the key component is a wide bandwidth for a given gain [5], which is why a cascode topology will be selected. As a high supply voltage is on the table, the voltage headroom will not be so easily exceeded. A one-stage topology also avoids the compensation issues that appear in two-stage configurations. A telescopic architecture would nevertheless be too close for even a high supply voltage (5 stacked transistors). Input and output common-mode (CM) levels can also be the same without

limiting output swings, and they have wider input CM range. Therefore, it is the folded-cascode that will be implemented for this thesis.

2.5.4 Folded Cascode

For this subsection, a swift analysis shall be done on this topology. A simple schematic can be seen in Figure 2.12.

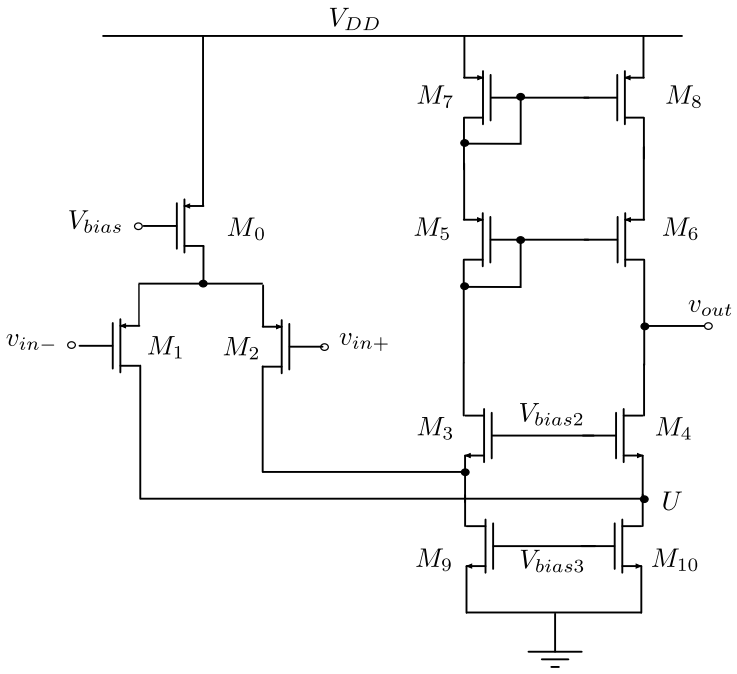


Figure 2.12: Schematic for a single-output folded cascode amp.

The first matter to evaluate in this amp is the current biasing: to put it simply, the current that flows in M_9 will be the same that flows through M_7 and M_8, and double of that for each remaining transistor:

$$I_0 = 2I_{1,2} \tag{2.15}$$

$$= 2I_{3,4,5,6,7,8} \tag{2.16}$$

$$= I_{9,10}. \tag{2.17}$$

To simplify matters, symmetry will be assumed, with $M_1 = M_2$, $M_3 = M_4$, $M_5 = M_6$, $M_7 = M_8$, and $M_9 = M_{10}$.

Its input impedance $R_{i,EA}$ being obviously very large (so much so that $R_{id} = \infty$ can be considered), the analysis moves to its output impedance.

It can be easily seen that $R_{o,EA}$ will be the parallel of the two nets branching from the output. From the branch coming from M_1 to the node U, the equivalent resistance would be $r_{o1} \parallel R_{o10}$; this in turn would be multiplied to $g_{m4}r_{o4}$. On the upper output branch, it is simply $g_{m6}r_{o6}r_{o8}$. The following equation can be formulated:

$$R_{o,EA} = \left[g_{m4} r_{o4} \left(r_{o1} \parallel r_{o10}\right)\right] \parallel \left[g_{m6} r_{o6} r_{o8}\right]. \tag{2.18}$$

The total voltage gain of this structure will be:

$$A_{EA} = g_{m1} R_{o,EA}. \tag{2.19}$$

The following dominant pole defines the GBW product:

$$\mathrm{GBW} = \frac{g_{m1}}{2\pi C_{L,EA}}, \tag{2.20}$$

and the second pole

$$f_{nd} = \frac{g_{m3}}{2\pi C_n}, \tag{2.21}$$

where

$$C_n \approx C_{GS3} + C_{DB2} + C_{DB9} \approx 3C_{GS3}. \tag{2.22}$$

This amp can have high GBW, which will mater for this work's case, as maximum gain and bandwidth are needed in order to increase overall PSR.

It has the drawback of necessitating more transistors than other amp topologies, which undermines voltage headroom and power consumption. These points will be taken into consideration when designing the amplifier.

2.6 Other Important Aspects

Beyond the aforementioned critical parameters, the designer should also strive for optimal results in other metrics.

2.6.1 Efficiency

The power efficiency of any circuit is the output power over the input power, and for the LDO's case it can be expressed as follows [10]:

$$\eta = \frac{I_L V_{\mathrm{out}}}{(I_L + I_{\mathrm{I_q}}) V_{\mathrm{in}}} \leq \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}, \tag{2.23}$$

where I_L is the load current and I_q is the current drawn by the LDO while enabled and with no load. The biggest contributor for the quiescent current will be the EA [13].

From (2.23), it can be gathered the LDO's dropout voltage should be as low as possible in order to obtain an efficient LDO, as the top ceiling for it will be determined by $V_{\mathrm{out}}/V_{\mathrm{in}}$. Nowadays, it's considered good practice to keep the dropout voltage lower than 100 mV [5], but that could force the pass transistor into the linear region.

If the input and output voltages are fixed by the specifications, then from 2.23 a current efficiency equation is obtained, from which it is also acknowledged that I_q should be minimised.

2.6.2 Figure of Merit

As may be expected, there are many different performance parameters to compare between different ICs. It is no wonder, then, that engineers have often resorted to Figures of Merit (FOM) to evaluate different designs: the most important parameters are weighed in and grouped within a single metric. There are many different definitions for it, but in general, the lower the FOM, the better the LDO's performance.

G. Rincon-Mora states [14] that a good FOM for an LDO has to account for the following characteristics:

- high output current or I_L
- worst-case power supply rejection, $\mathrm{PSR}_{\min}$
- low steady-state errors ΔE_0
- low ground current or quiescent current I_q
- low dropout-voltage ΔV
- low output capacitance or C_L
- response time Δt_r

and that a good FOM to resort to should then be:

$$\mathrm{FOM}_1 = \frac{I_{L,max}\,\mathrm{PSR}_{\min}}{\Delta E_0\, I_q\, \Delta V\, C_L\, \Delta t_r\, 10^{20}}. \tag{2.24}$$

Another commonly used FOM [8] for LDO performance is:

$$\mathrm{FOM}_2 = \frac{C_L \Delta V_{\mathrm{OUT}}}{I_{\mathrm{MAX}}} \frac{I_{\mathrm{q}}}{I_{\mathrm{MAX}}}, \tag{2.25}$$

where ΔV_{OUT} is the undershoot voltage for a load transient change response. However, this equation assumes that the load current changes instantaneously; in truth, the load current slew rate I_{SR} for a load change is finite [15], and thus a more accurate version for (2.25) would be:

$$\mathrm{FOM}_3 = \sqrt{\frac{2C_L \Delta V_{\mathrm{OUT}}}{I_{\mathrm{SR}}}} \frac{I_{\mathrm{q}}}{I_{\mathrm{MAX}}}, \tag{2.26}$$

with

$$I_{\mathrm{SR}} = \frac{\Delta I_L}{T}, \tag{2.27}$$

where T is the time for the maximum ΔV_{out} for a given ΔI_L load current change in a transient response.

These and many more FOMs have been produced in order to compare different LDOs: in this thesis, equation (2.26) will be selected.

2.6.3 PVT Variability

The IC can suffer many unintended consequences from the fabrication process; it must, nevertheless, still operate as intended. That is why the designer must also take into account the different corners the circuit may be found in. These corners are separated into three categories: Process, supply Voltage, and operating Temperature (PVT). The engineer must make sure that their circuit is robust against PVT variations.

Process

Process variations are primarily brought on by lithographic restrictions, potentially increasing leakage and propagation delay. Lithographic exposure and defocus aberrations are two examples of systematic deviations in such process variations[16]. With these changes, they are categorised as Fast (F), Slow (S), or Typical (T). The corners one would have to evaluate would be as seen on Table 2.2:

Table 2.2: Process corners.

NMOS	PMOS	Corner
Typical	Typical	TT
Slow	Slow	SS
Slow	Fast	SF
Fast	Slow	FS
Fast	Fast	FF

Supply voltage

The supply voltage can suffer variations because of IR drops in the supply rail and supply noise [17]. For this work, the supply voltage variation corners are shown in Table 2.3.

Table 2.3: Supply voltages corners.

	MIN	TYP	MAX
V_{ph} [V]	1.03	1.2	2.030
V_p [V]	0.646	0.8	0.985

Operating temperature

Temperature affects the threshold voltage and the carriers' mobility for the transistors, which means the drain current I_D will change, and in turn the system will have a different operating point. Thus, running corners on different temperatures, as shown in Table 2.4, becomes relevant.

Table 2.4: Temperature corners.

	MIN	TYP	MAX
Temperature [℃]	-40	25	125

Worst-case corners

There are many more parameters that vary due to process, but the three mentioned above are the ones that will be experimented with during the simulations.

To prove the robustness of the circuit, the designer would benefit to cross all the different corners, but simulating that many different scenarios may easily become unmanageable; to make most of the engineer's time, the worst-case scenarios for these corner crossings are selected, as presented on Table 2.5.

Table 2.5: Worst-case corners selected for this thesis' simulations.

	MOSFET	Supply voltages	Temperature
Corner 1	TT	TYP	TYP
Corner 2	SS	MIN	MIN
Corner 3	SS	MIN	MAX
Corner 4	SF	MIN	MIN
Corner 5	SF	MIN	MAX
Corner 6	FS	MIN	MIN
Corner 7	FS	MIN	MAX
Corner 8	FF	MAX	MIN
Corner 9	FF	MAX	MAX

2.6.4 Monte Carlo

After running through the most extreme of PVT corners, the Monte Carlo analysis can then be run to check for the effect of these corner changes. From the worst corner simulated in PVT, the MC analysis produces a random variation in the MOSFETs parameters, causing mismatches between them, so that it would portray a more faithful reality.

This analysis follows a Gauss deviation, on which the designer defines a target σ to check if the circuit may fulfill a specific yield. This model is illustrated on Figure 2.13.

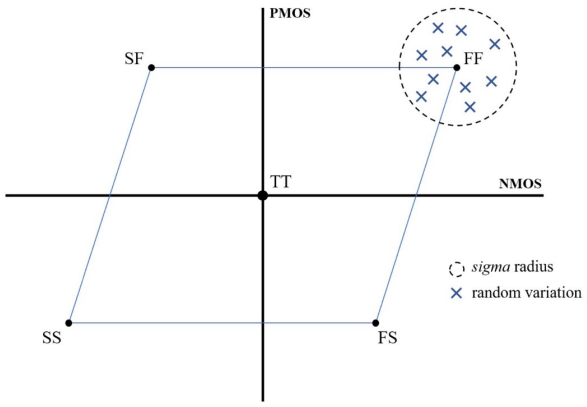


Figure 2.13: Monte Carlo analysis setup illustration[18].

2.6.5 Other Considerations

To have a low dropout voltage, the power transistor needs to be large, which introduces a low-frequency nondominant pole at the output of the error amplifier [12]: as the load current increases, so does the loop bandwidth, and the nondominant pole closes in within range of the UGB, leading to a stability problem. To compensate this, designers usually use ESR compensation to place a zero on the left half plane, which consists on placing a resistor and capacitor in series on the output. However, this deteriorates transient response, and wastes area usage, which is why this will not be considered for this project. Instead, internal compensation and pole splitting is focused on if needed, as will be seen on Chapter 4.

Chapter 3

State of the art

Contents

3.1 Overview

The study of LDOs is the core of many papers; it isn't hard to find different applications and techniques regarding this subject. In this chapter, a broad view is taken at selected state-of-the-art LDOs from the last years and compare their overall performance and parameters. These papers were selected for implementing some form of supply ripple cancellation on their architecture and using a PMOS pass transistor. Here, alternative designs are briefly explored; the basis of SRC is then developed in section 4.2.

3.2 Adaptive Supply-Ripple Cancellation

The LDO [22] is an external capacitorless regulator that provides high PSR at all frequencies. Not using an external capacitor can be a great advantage due to the sheer size it can occupy in circuit area. To compensate for the instability of a design with no capacitor, the electronic designer places a dominant pole at the gate of the pass transistor. Because of this design choice, the LDO must also make use of an adaptive supply-ripple cancellation technique (ASRC) to suppress the PSR hump of conventional gate-pole-dominant LDOs: this allows to cancel supply ripples through $\mathrm{g_{ds}}$ as well as through $\mathrm{g_m}$ of the transistor. High PSR is firmly maintained thanks to the ASRC continuously optimizing the magnitude of injecting ripples, despite PVT variations as well as during changes of $\mathrm{I_L}$ and $\mathrm{V_{DO}}$. A block diagram of this circuit can be seen in Figure 3.1.

This paper proposes injecting the supply ripple to the pass transistor's body terminal through a Body-Ripple Injector (BRI). The g_{ds}-to-g_{mb} sensor (GTGS) determines the necessary magnitude needed for v_{SRC} to compensate for the supply ripple, hence the 'adaptive' on the paper's title 'Adaptive Supply Ripple Cancellation'.

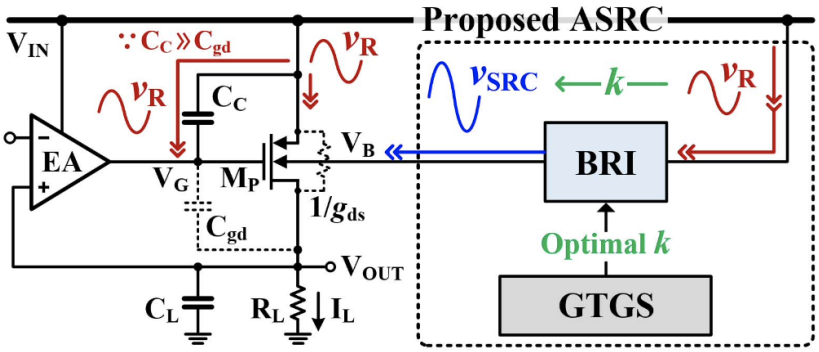


Figure 3.1: Conceptual block diagram of the LDO with ASRC. [22]

3.3 Scaled Replica

The regulator [24] is a 180-nm process LDO that uses a scaled replica technique: PSR performance improvement is achieved by use of a scaled replica circuit of the pass transistor. This calibration scheme

tracks all loading current conditions, such that the supply noise is compensated even under PVT variations. The on-chip capacitors are used for internal frequency compensation and DC offset current cancellation. A block diagram of this circuit can be seen in Figure 3.2.

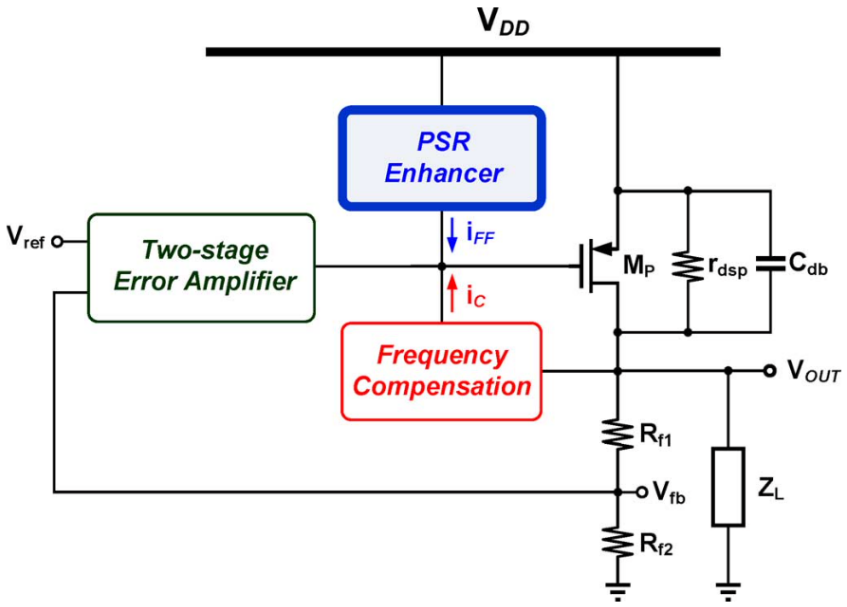


Figure 3.2: Conceptual block of the scaled-replica LDO. [24]

3.4 Enhanced Multipath Nested Miller Compensation

The LDO [25] is a 130-nm CMOS process output-capacitorless regulator that uses an enhanced multipath nested Miller compensation (EMNMC) with embedded feedforward path. This allows for a considerably high response time for a load transient, while keeping an excellent PSR performance over a wide frequency range. A schematic of this circuit can be seen in Figure 3.3.

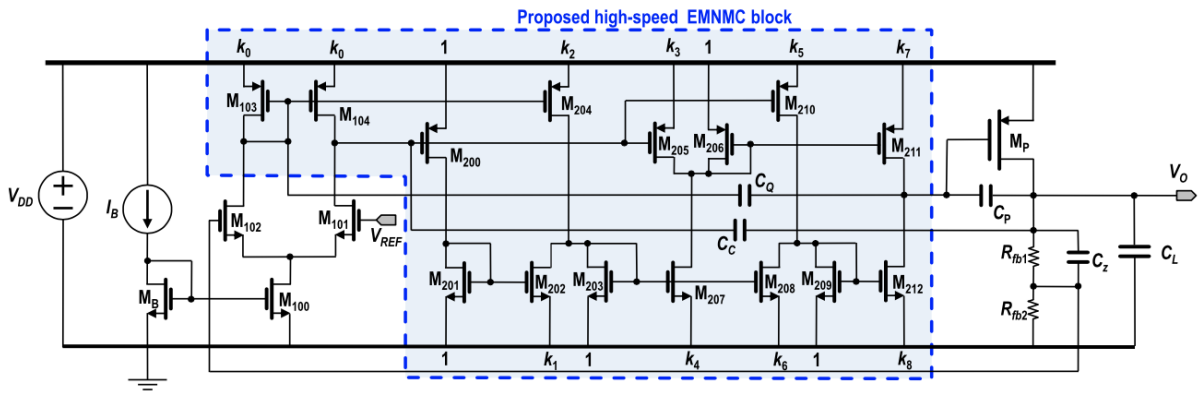


Figure 3.3: Schematic of the EMNMC LDO. [25]

3.5 Reference buffer

In short, the LDO [28] makes use of a buffer for the reference voltage which reverses the supply voltage ripple. Summed with the normal-phase PSR from the EA, this allows for great supply ripple subtraction on DC (-59.8 dB) and frequencies up to 1 MHz.

The buffer has two symmetric branches, and in each one there is a supply ripple amplifier (M_{R1} and M_{R2}; M_{L1} and M_{L2}). Its output is connected to the gate of a transistor (M_{R3}; M_{L3}) which will generate a small-signal current with negative phase (when the design is such that $g_{m,R2} > g_{m,R1}$; $g_{m,L2} > g_{m,L1}$).

The DC PSR of this buffer is thus defined by:

$$PSR_{BUF} = -\frac{(g_{m,R3} + g_{m,L3})\left(\frac{g_{m,R_2}}{g_{m,R_1}} - 1\right)}{2g_{m,F1}g_{m,F3}r_{ds,F1}}. \tag{3.1}$$

The LDO PSR is at its peak when:

$$PSR_{BUF} = -\frac{1}{g_{m,P}g_{m,A1}R_oR_{o,EA}}. \tag{3.2}$$

Furthermore, the buffer relies on adaptive biasing currents so that it may hold high PSR on a wide load current range.

Moreover, it employs a common-gate feedback (CGFB) loop, which enhances the DC gain of the EA. It also implements a pole-tracking compensation (PTC) technique to maintain a high PM over a wide load current range. A current-controlled nulling resistor tracks the operating points of the power transistor through linear, saturation and even subthreshold regions.

A schematic of this circuit can be seen in Figure 3.4. The simulated PSR results from the paper can be seen in Figure 3.5: here, we can see how the buffer effectively enhances the PSR, practically doubling it.

3.6 Comparisons Table

The different LDOs specs can be seen on Table 3.1. A succinct summary of all advantages and disadvantages from the previous LDOs was placed on Table 3.2.

For this work, the final state-of-the-art LDO will be implemented and elaborated on the following sections.

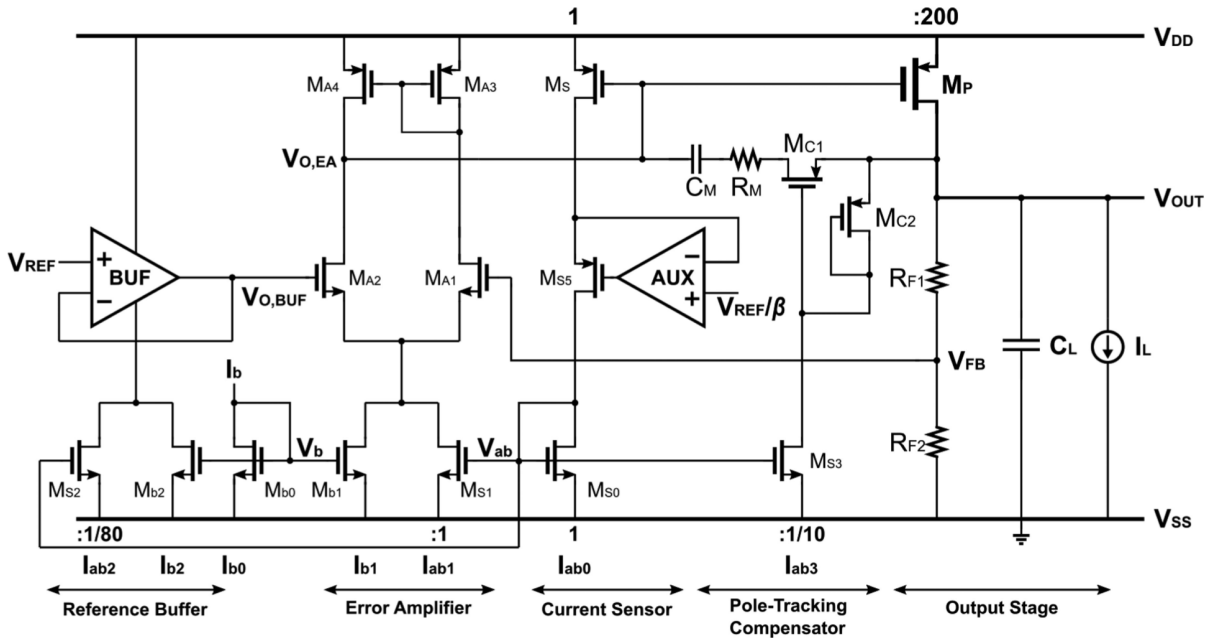


Figure 3.4: LDO with phase-reversed PSR buffer and PTC. [28]

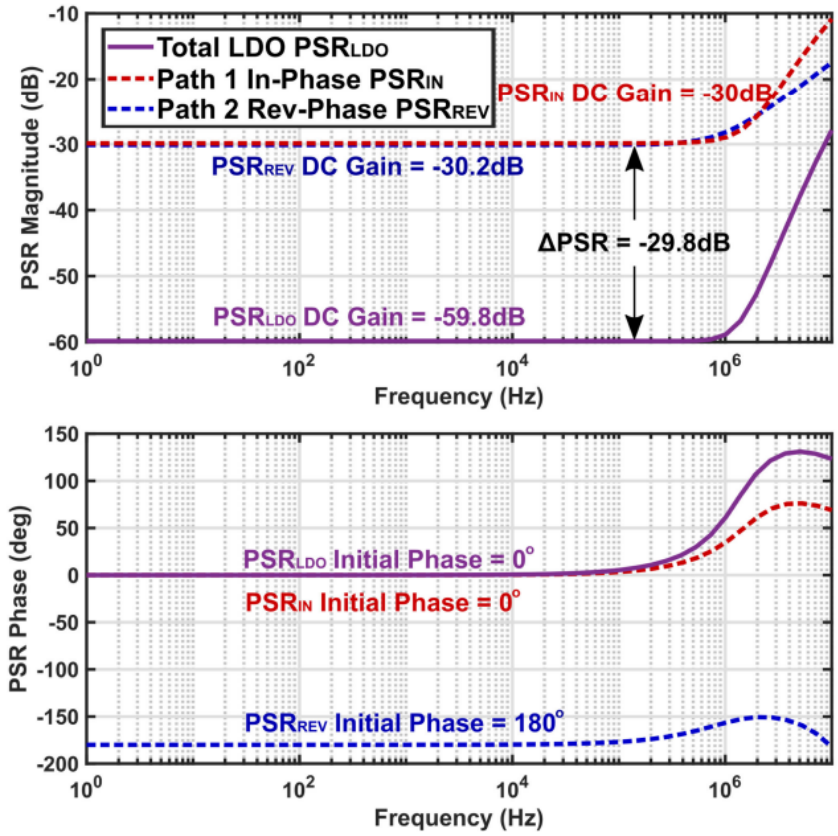


Figure 3.5: Simulated PSR frequency response for LDO and the two opposite PSR paths with 20 mA load current.[28]

Table 3.1: Comparison of state-of-the-art LDOs.[28]

Parameter	[22]	[24]	[25]	[28]
Process [nm]	65	180	130	180
$\mathrm{V_{OUT}}$ [V]	1	1.6	0.8	1.2
ΔV [mV]	200	200	200	200
$\mathrm{I_{MAX}}$ [mA]	25	50	25	20
$\mathrm{I_q}$ [µA]	8 - 297.5	55	120	8.6 - 241
$\mathrm{C_L}$ [pF]	120	100	25	100
$\Delta\mathrm{V_{OUT}}$ [mV] / $\mathrm{T_f}$ [ns]	225 / 100	75 / 100	284 / 0.3	117.7 / 70
Turn-ON Settling time [µs]	1 mA - $\mathrm{I_{MAX}}$, < 3	0 - $\mathrm{I_{MAX}}$, < 6	120 µA - $\mathrm{I_{MAX}}$, < 0.19	0 - $\mathrm{I_{MAX}}$, < 0.35
Load Regulation [µV/mA]	42	140	170	930
PSR [dB] @ 100 kHz	-68	-61	-64	-57
@ 1 MHz	-61	-70	-57	-63
Area [mm^2]	0.087	0.14	0.008	0.0113
FOM [ps]	6.79	6.02	1.98	3.90

Table 3.2: Comparison table of the aforementioned LDOs.

LDO	Pros	Cons
[22]	High PSR at high frequencies	Low process size (more expensive)
[24]	Highest $\mathrm{V_{OUT}}$	Low I_q, slow transient response
[25]	Lowest area, fastest settling time, low FoM	Lowest $\mathrm{V_{OUT}}$
[28]	Low I_q	Lowest $\mathrm{I_{MAX}}$, highest load regulation

Chapter 4

Supply-Ripple Cancellation LDO

Contents

4.1 Basic Design Choices

The art of analog design is based on finding the right tradeoffs between many parameters for the right context, as illustrated on Figure 4.1 specifically for opamps.

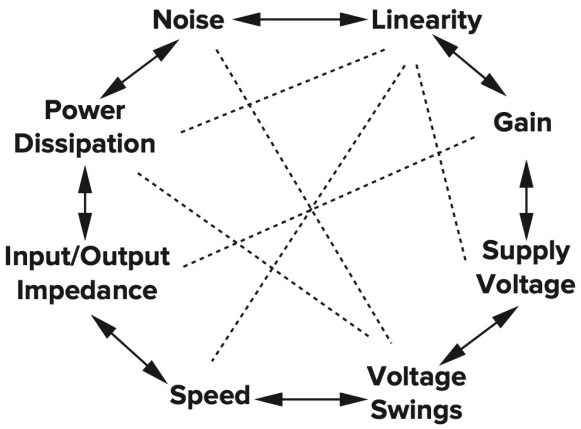


Figure 4.1: Analog design octagon [31].

The transistor size selection can be summarised as follows: first, the minimum sizing is selected, and the results are evaluated; if the results are not satisfactory, then the equations are revisited so that it may known which parameters and transistors to change. These parameters are then varied through a sweeping until an adequate result is reached. If the general outcome is positive, only then is the final size selected. This process is illustrated on Figure 4.2.

4.1.1 General Considerations

The LDO is usually tailored to the circuit it supplies voltage to. Let's recall the basic design described in Chapter 2 with Figure 4.3:

and some of the initial specifications from Table 1.2:

- $V_{\text{in}} = 1.2$ V;
- $V_{\text{out}} = 0.9$ V;
- $V_{\text{ref}} = 0.45$ V;
- $I_L = 1$ mA;
- PSR < -40 dB @ 1.5 MHz.

From these items, it can be gathered that within 40 dB of attenuation, any periodic perturbation on V_{DD} needs to be extremely small in order to properly supply the loading circuit.

From that same equation, it can see that quiescent current I_q. should also be minimised.

If the circuit designer had $V_{\text{ref}} = V_{\text{out}}$ at their disposal, then the LDO's output could be directly connected to the non-inverting input of the EA, making it possible to dismiss the voltage divider R_1 and

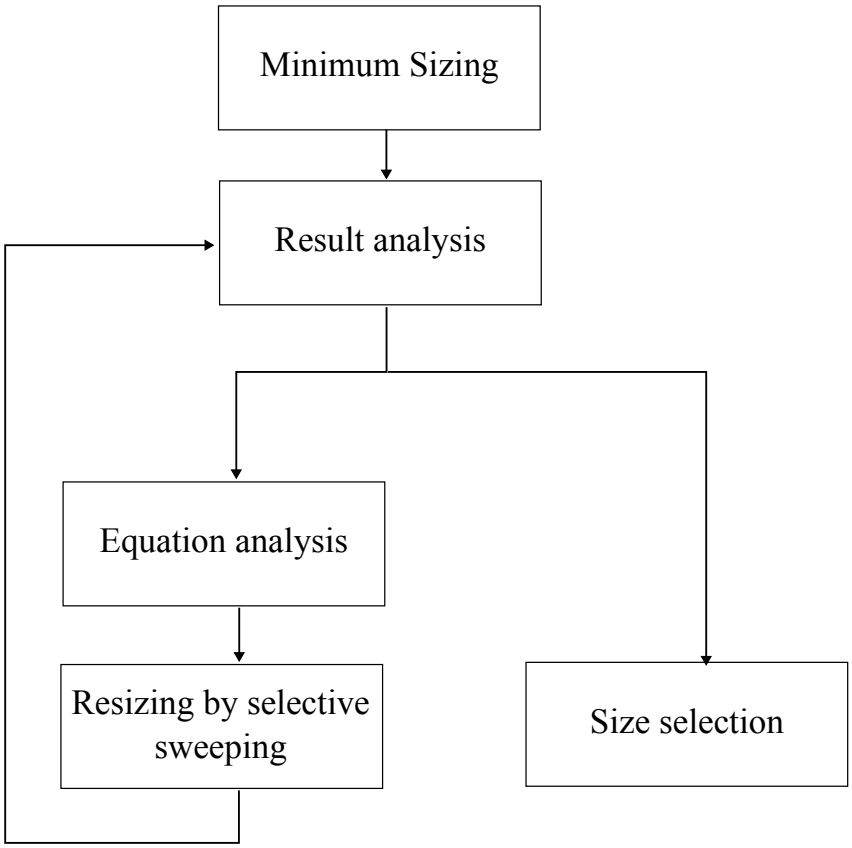


Figure 4.2: Sizing flow used to select components' dimensions of the circuit at hand. [18]

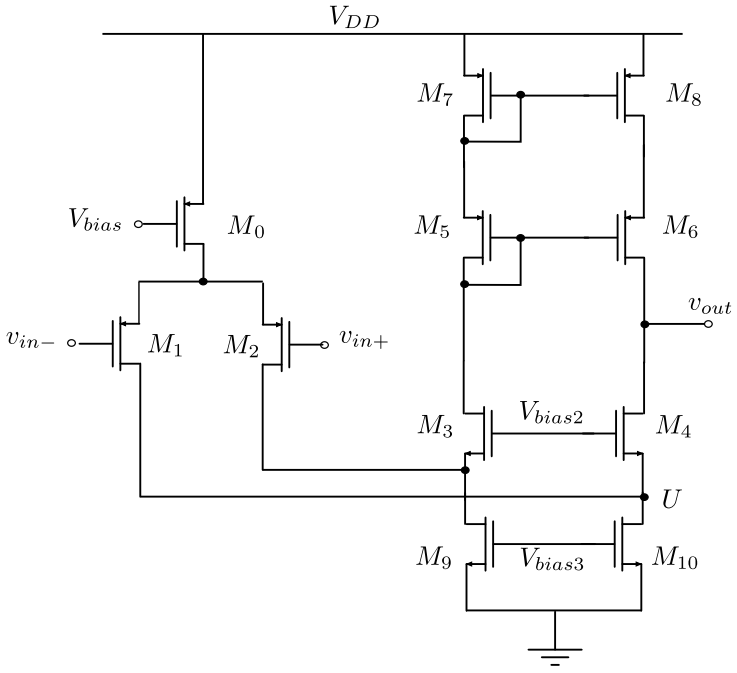


Figure 4.3: Schematic for a single-output folded cascode opamp.

R_2 entirely, which in turn would cause a small decrease on I_q. As this isn't the case for this work, the following feedback factor is imposed:

$$V_{\text{out}} = \frac{V_{\text{ref}}}{\beta} \tag{4.1}$$

$$\Leftrightarrow \beta = \frac{1}{2}, \tag{4.2}$$

which means that:

$$\beta = \frac{R_2}{R_1 + R_2} \tag{4.3}$$

$$\Leftrightarrow R_1 = R_2. \tag{4.4}$$

Some quiescent current will flow through these resistors, so it is in the designer's best interest to have these as large as possible, while taking into account the area used. Thus, for this output and reference voltages, a voltage divider of $R_1 = R_2 = 10\ \text{k}\Omega$ is selected, for which is obtained a respectable $I_{q,Rf} = V_{\text{out}}/(R_1 + R_2) = 45\ \mu$A.

4.1.2 Pass Transistor Design

As previously said, the low voltage drop from V_{ph} to V_{out} imposes a PMOS to be used as pass device. The transistor's overdrive voltage cannot exceed $|V_{DS,\text{PPT}}| = 300$ mV: a $(W/L)_{\text{PPT}}$ is needed to be large enough so that a reasonable V_{GS} is obtained. Ignoring body effect, it is obtained from the saturation equation:

$$(W/L)_{\text{PPT}} = \frac{2}{k_p V_{ov}^2}\ I_{D,\text{PPT}}, \tag{4.5}$$

where

$$k_p = \mu_p C_{ox} \tag{4.6}$$

$$= \mu_p \frac{E_{ox}}{t_{ox}} \tag{4.7}$$

$$= \mu_p \frac{E_o \cdot E_r}{t_{ox}}. \tag{4.8}$$

From these technology parameters, and with a reasonable load current of $I_{D,\text{PPT}} = 1$ mA, the pass transistor's size may be projected as shown on Table 4.1. Coupling the supply voltage V_{DD} with the power transistor's output resistor $r_{o,\text{PPT}}$ to the output voltage V_{out} has a negligible effect on overall PSR, which is why minimum length can be selected for this component; this will also mitigate the contribution of the capacitances of PPT to the poles at the output of the opamp and the output of the regulator.

Table 4.1: Pass transistor size.

	M_{PPT}
W/W_{min}	1
L/L_{min}	1
Multiplicity	225

4.1.3 OTA Design

As stated before, the LDO's performance will mostly rely upon the OTA's. Low-frequency PSR can be obtained from :

$$\mathrm{PSR}_{DC} = \frac{V_{\mathrm{out}}}{V_{\mathrm{DD}}} \approx \left(1 + \frac{R_1}{R_2}\right) \frac{1}{A_1}, \tag{4.9}$$

where the open-loop gain is $A_1 >> 1$.

For $V_{\mathrm{ref}} = 0.45$ and $V_{out} = 0.9$ V:

$$V_{\mathrm{out}} = \frac{V_{\mathrm{ref}}}{\beta} \tag{4.10}$$

$$\Leftrightarrow 1 + \frac{R_1}{R_2} = \frac{0.9}{0.45} = 2, \tag{4.11}$$

and from (4.9), for a PSR $= -40$ dB:

$$A_1 > 2 \times \frac{1}{10^{-40/20}} = 2 \times 100 = 200 \approx 46\ \mathrm{dB}. \tag{4.12}$$

As the specifications demand for a rejection up to 1.5 MHz, the amp's open-loop 3-dB bandwidth point must be greater than this value. The Unity-Gain Bandwidth (UGB) for a one-pole design would be:

$$\mathrm{UGB} = 200 \times 1.5\mathrm{MHz} = 300\mathrm{MHz}. \tag{4.13}$$

Because these settings impose such a wideband opamp, thin-oxide (low-voltage) transistors will be used for the signal path [20].

Many poles can be identified in the feedback loop; these will eventually require frequency compensation. A capacitance could be added at the output node to improve PSR at high frequencies, but that comes at the cost of introducing instability in the loop, which can be seen on the increase of peaking in PSR. The value of the feedback resistors could be reduced, increasing their pole frequency, but that would only raise power consumption. Thus, there exists an upper limit for the pole frequency at the output. Having $C_{\mathrm{load}} = 1$ pF and $(R_1 + R_2) \parallel r_{o,\mathrm{PPT}} \approx 20$ kΩ, then $\omega = 20 \times 10^9\ \mathrm{rad.s}^{-1}$ or $f = 3.18$ GHz. Considering this as the first nondominant pole, then UGB cannot be greater than this value.

In order to have the widest bandwidth for a high gain, a folded-cascode opamp is implemented, as illustrated on Figure 4.3.

In this configuration, you'd have $V_{D5} = V_{DD} - |V_{GS5}| - |V_{GS7}|$, which limits the maximum value of

$V_{o,EA}$ to $V_{DD} - |V_{GS5}| - |V_{GS7}| + |V_{th6}|$, which adds a PMOS threshold voltage to the swing. To solve this, the PMOS load will be replaced by a low voltage cascode so that M_7 and M_8 are biased at the edge of the triode region. This is illustrated on Figure 4.4.

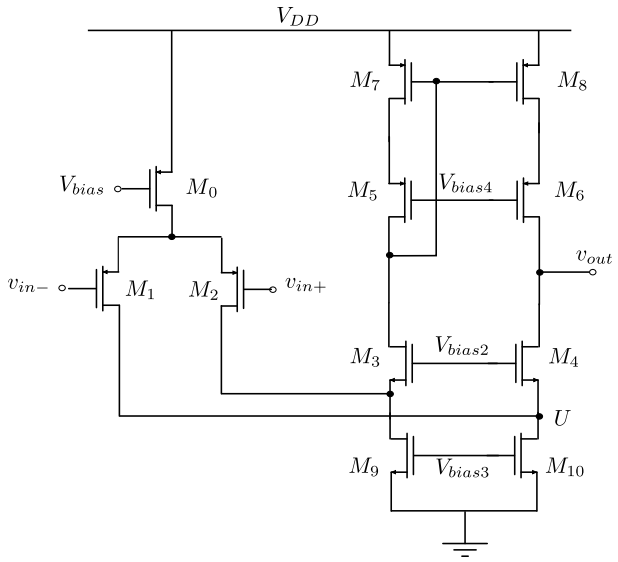


Figure 4.4: Folded-cascode with low voltage cascode PMOS load.

As previously said, the signal path will be comprised of ultra-low-voltage transistors ($M_{1,2,3,4}$) so as to also help to give saturation margin to the CS (M_9), with PMOS bulk connected to $V_p = 0.8$ V), and all loads and current sources will be high-voltage (PMOS bulk connected to $V_{ph} = 1.2$ V). Furthermore, $M_{5,6}$ will also be low-voltage so as to have higher g_m for the voltage gain. Their sizing can be seen on Table 4.2.

Table 4.2: EA transistors size.

	$M_{1,2,3,4}$	$M_{5,6}$	$M_{7,8}$	$M_{9,10}$
W/W_{min}	1	1	1	1
L/L_{min}	1	1	1	1
Multiplicity	1	1	4	8

4.1.4 Bias Circuitry

For the EA, simple current mirrors will be implemented, as shown on Figure 4.5. The current reference will be extracted from a voltage bandgap circuit. A cascode current mirror would reproduce the reference current more faithfully; however, that would in turn increase area usage. As the need for accuracy for this biasing current isn't indispensable, the cascode current mirror will not be implemented.

Table 4.3: EA bias transistors size.

	M_{b0}	$M_{b1,2,3}$	M_{b4}	M_9	M_{10}
$W/W_{min,hv}$	1	1	1	1	1
$L/L_{min,hv}$	1	1	1	1	1
Multiplicity	1	8	4	8	8

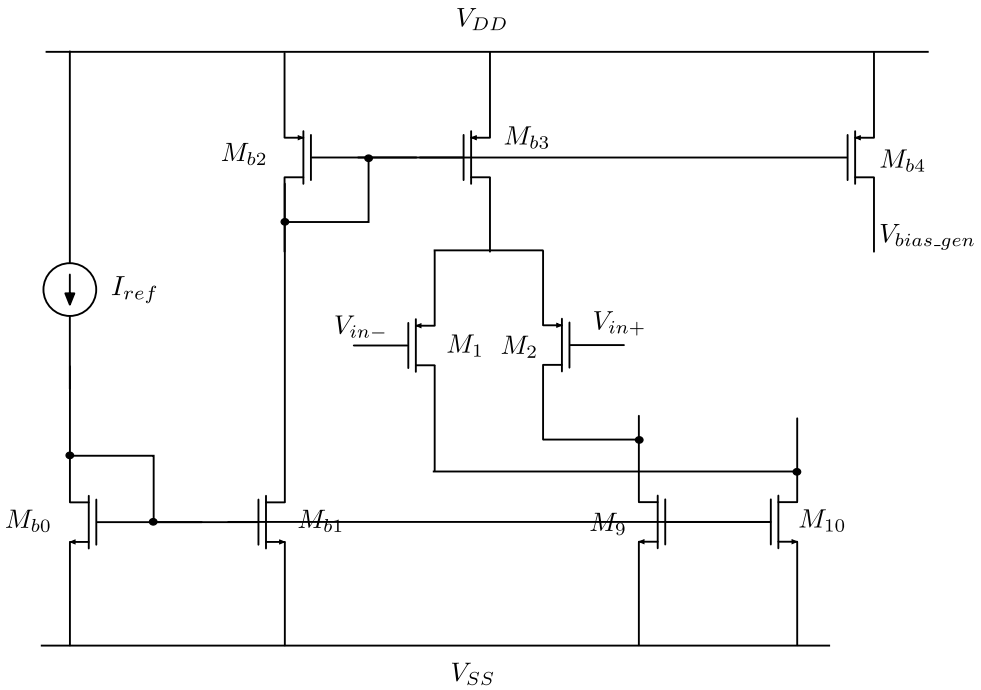


Figure 4.5: Current source and current mirrors for the EA.

To generate the gate voltages for the cascode loads in the EA, some biasing technique will be implemented, depicted in the case for V_{bias4} in Figure 4.6.

If it's to be expected to consume as little voltage headroom as possible, then $V_A = V_{GS1} - V_{th1}$, and $V_b \geq V_{GS0} + (V_{GS1} - V_{th1})$. In this implementation, the diode-connected M_4 gives enough V_{GS} and M_3 generates a V_{DS} equal to the necessary overdrive. The current I is generated with a PMOS load biased with the reference current (such as M_{b4} on Figure 4.5).

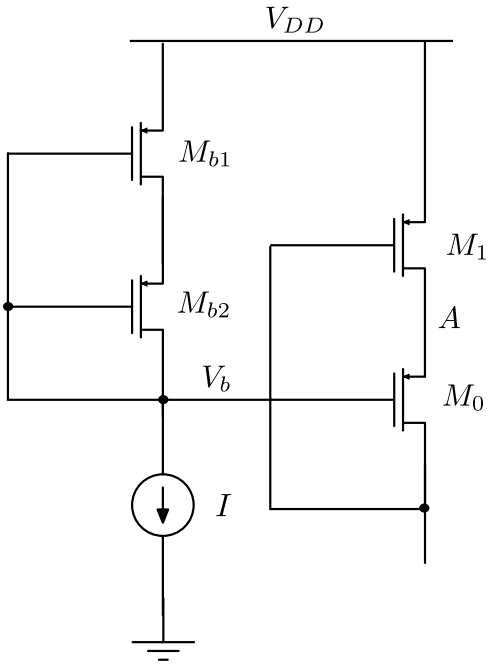


Figure 4.6: Generation of gate voltage V_b for cascode mirrors [33].

4.1.5 Enable Signal Circuitry

For this LDO, a simple startup system was implemented, where an enable signal could turn on and off the regulator as needed. This enable signal flows through a CMOS inverter; these two logic signals control PMOS/NMOS switches and CMOS transmission gates.

PMOS switches connected to V_{DD} are used to power down PMOS current sources and NMOS connected to ground to power down NMOS current sources. The CMOS transmission gates are used to power down bias voltages that are not either V_{DD} or ground.

This is exemplified in Figures 4.7, where the enable signal circuity for the EA is shown.

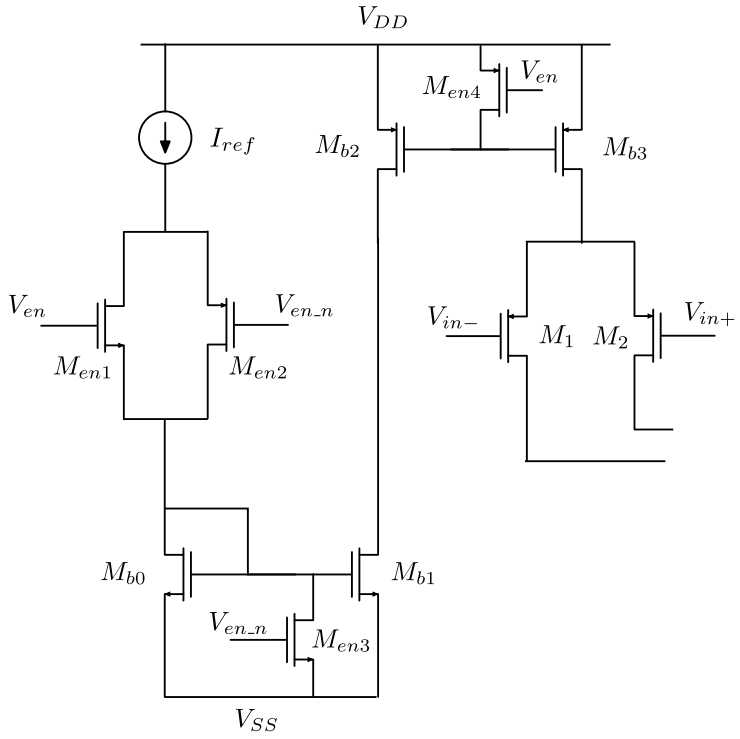


Figure 4.7: Example of enable signal implementation within the EA.

4.2 Supply Ripple Cancellation Technique

Based on the last LDO of Table 3.2, this technique is based on suppressing as much as possible input ripples by replicating it, creating its symmetric, and summing it to the original ripple.

Going back to eq. (2.5):

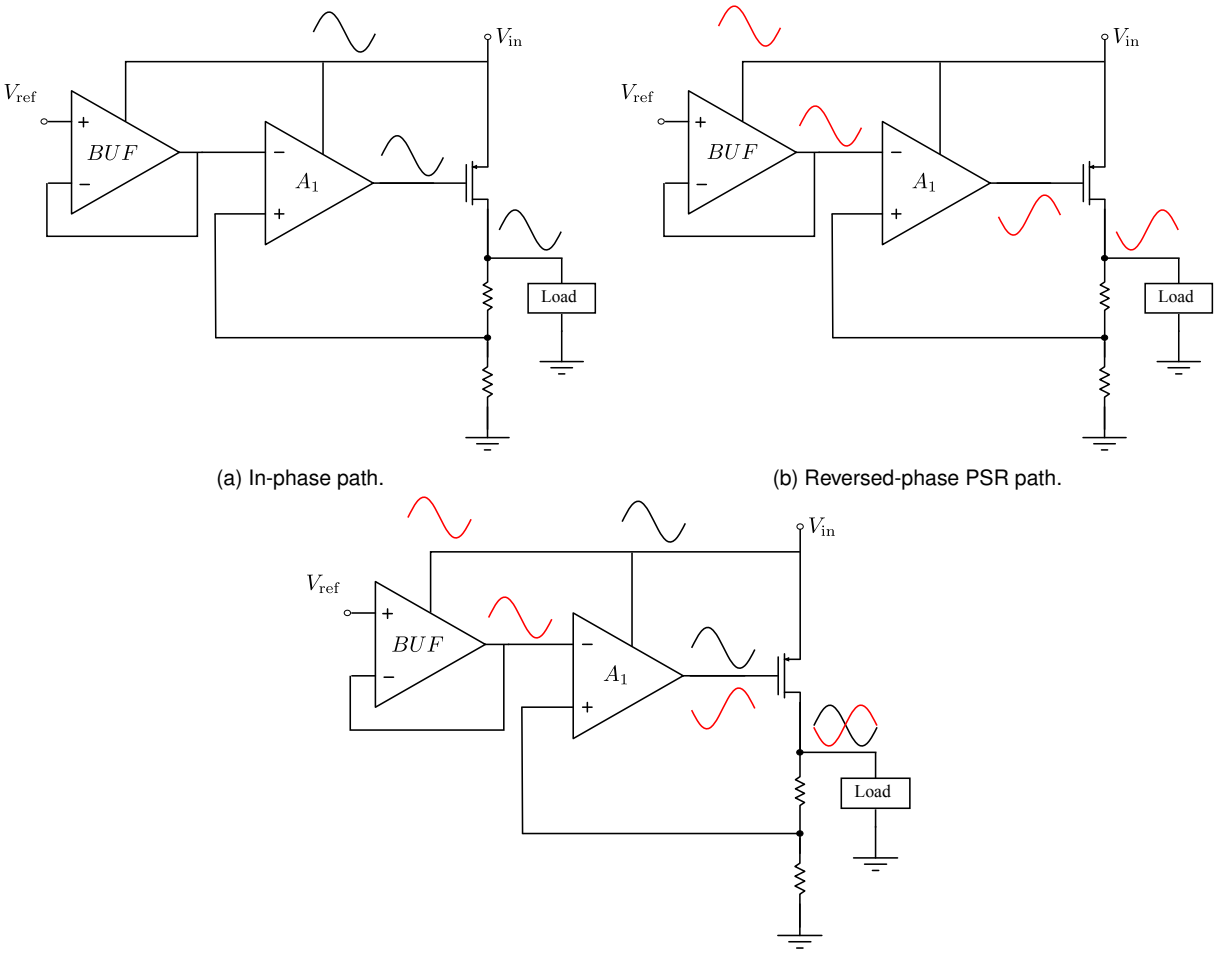
$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{g_{m,PPT}\left[R_L \parallel (R_1 + R_2)\right]}{1 + A_{LG}} \tag{4.14}$$

$$= \frac{K}{1 + A_{LG}} \tag{4.15}$$

For this technique, it can be gathered that a K_{psr} factor is needed so that multiplied with (4.14), PSR is improved as much as possible. To make this possible, a secondary path for the ripple is necessary,

as seen from the previous state-of-the-art LDOs; in this case, a buffer will be placed on the reference voltage path, in which the ripple will be injected and then reversed.

Considering an example where there's a small increase on the supply voltage, this forces an increase on $V_{SG,PPT}$ in the original PSR path, which results in an increase in output current, as well in the output voltage. The proposed reference buffer takes this supply variation and inverts its phase, then injects it into the reference voltage. This causes a small decrease on the buffer output; the opamp has to compensate this decrease on the non-inverting input, decreasing in turn the voltage on the output, compensating for the original ripple path. Another way to see this is as the buffer output decreases, the opamp output increases, which in turn decreases the pass transistor source-gate voltage, and compensates the increase at the output. This is illustrated on Figure 4.8.



(a) In-phase path.

(b) Reversed-phase PSR path.

(c) The two PSR paths summed together.

Figure 4.8: Diagram of the two opposite-phase PSR paths in the proposed LDO with the reference buffer.

Considering the two paths, the total PSR in dB is defined as:

$$PSR = PSR_{in} + PSR_{rev}, \tag{4.16}$$

where PSR_{in} is the ripple in phase with the input ripple, and PSR_{rev} is the reversed-phase ripple, with

$$PSR_{rev} = PSR_{buf}(s)\frac{A_{LG}(s)/\beta}{1 + A_{LG}(s)}. \tag{4.17}$$

If:

$$PSR_{DC6} = \frac{K \cdot K_{psr}}{1 + A_{LG}}, \tag{4.18}$$

then:

$$K_{psr} = 1 + A_0 g_{m,PPT} \left[R_L \parallel (R_1 + R_2)\right] \cdot PSR_{buf,DC}. \tag{4.19}$$

The overall maximum PSR in DC is achieved if $K \cdot K_{psr} = 0$, or:

$$\frac{\partial V_{\text{ref}}}{\partial V_{ph}} = \text{PSR}^{\text{max}}_{\text{BUF,DC}}, \tag{4.20}$$

where

$$\text{PSR}^{\text{max}}_{\text{BUF,DC}} = -\frac{1}{A_{EA} g_{m,PPT} \left[R_L \parallel (R_1 + R_2)\right]}. \tag{4.21}$$

This buffer is implemented as illustrated on Figure 4.9. It's constituted of a simple PMOS input differential pair $M_{1,2,3,4}$ with its bias current supplied by M_b. This buffer takes the reference voltage at the gate voltage of M_1 and delivers it at the gate voltage of M_2.

M_5 and M_6 form a supply ripple amplifier with the supply voltage as input and V_{G7} as output. M_7 takes these variations and forms a small-signal current when $g_{m6} > g_{m5}$. This current will have an inverted phase compared to the input ripple, and is injected into the differential pair, where it flows to the buffer output V_{buf} and to the EA's inverting input. M_5 and M_6 are biased from the bandgap reference voltage and are in saturation.

Analysing Figure 4.10, the following PSR analysis equations are obtained:

$$PSR_{bufDC} = -\frac{g_{m7}\left(g_{m6}/g_{m5} - 1\right)}{2 g_{m1} g_{m3} r_{ds1}}, \tag{4.22}$$

$$p_{1,buf} \approx -\frac{g_{m1}}{C_{g,A1}}, \tag{4.23}$$

$$p_{2,buf} \approx -\frac{g_{m3}}{2C_{g3}}, \tag{4.24}$$

$$z_{1,buf} \approx -\frac{1}{r_{o,buf} C_{o,buf}}, \tag{4.25}$$

where

$$\frac{g_{m6}}{g_{m5}} > 1, \tag{4.26}$$

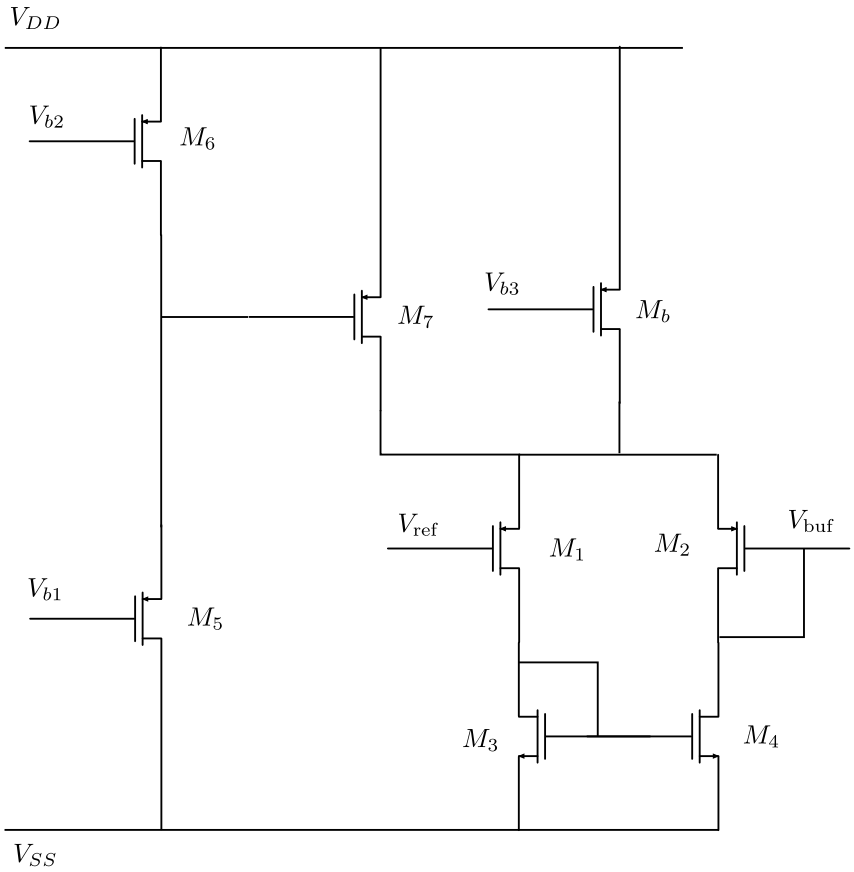


Figure 4.9: Reference buffer schematic.

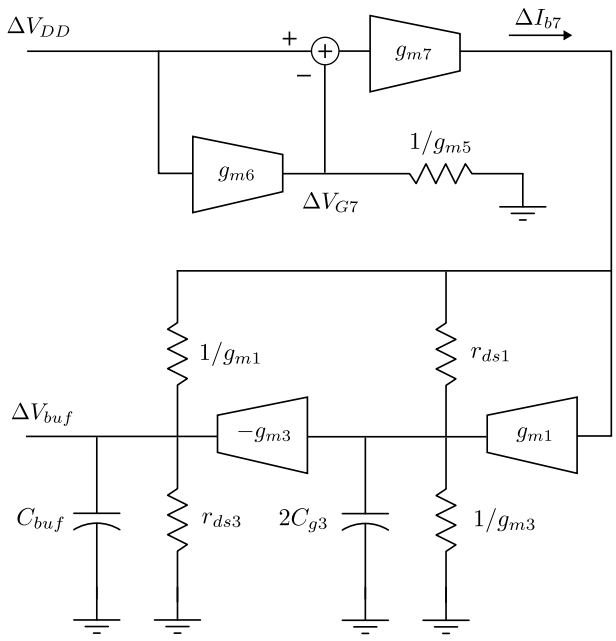


Figure 4.10: Small-signal model of the reference buffer

and $r_{o,buf}$ and $C_{o,buf}$ are the output resistance and capacitance of the buffer.

Chapter 5

Results

Contents

5.1 Testbench Setup

The simulations were performed with a load block composed by an ideal resistor $R_L = 900\,\Omega$ so as to represent the loading current $I_L = 1$ mA, and a loading capacitor $C_L = 1$ pF.

5.2 Basic LDO

For the basic LDO designed in Chapter 4.1, the following results were extracted from simulations in the typical corner.

Table 5.1: Some OP measurements from basic LDO simulations.

Parameter	Value
V_{fb}	450.13 mV
V_{out}	900.261 mV
I_q	208.91 µA
I_L	1.00029 mA

Stability results can be extracted from this design, as it will be relevant to compare with the final design. Here, the unit 'dB20' is simply used as the logarithmic relative unit of a voltage ratio, which is Vout / Vin in the case of the PSR.

The AC analysis was performed by opening the loop at the common node of the feedback network, and the results for both the open loop gain and phase can be seen on Figure 5.1. From this, the open loop gain, bandwidth, and phase margin can be extracted, which are 58 dB20, 315.47 kHz, and 57°respectively.

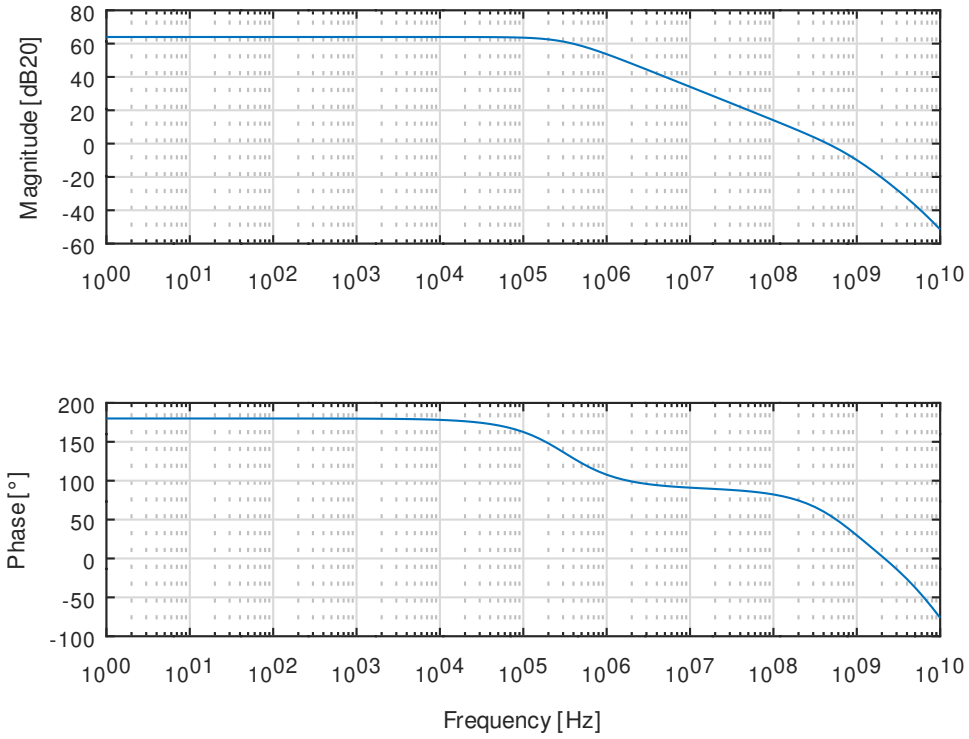


Figure 5.1: AC simulation results for simple LDO.

The PSR was simulated with an AC supply voltage with $V_{ph} = 1.2$ V and AC magnitude of 1. The result can be seen on Figure 5.2.

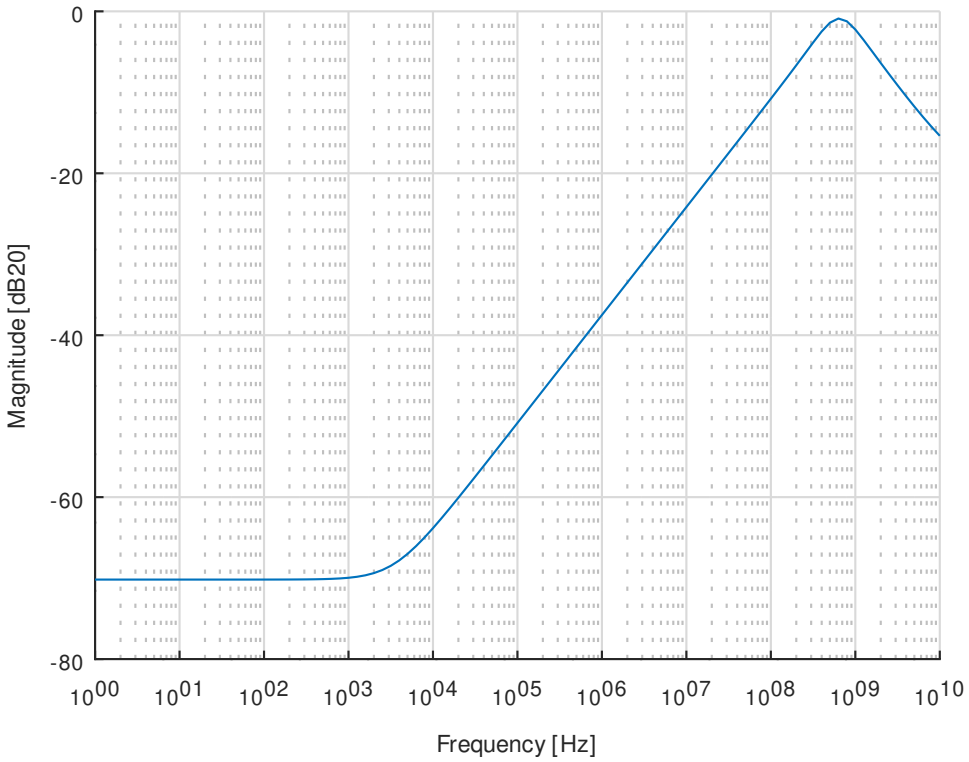


Figure 5.2: PSR simulation results for simple LDO.

A rejection of -73 dB20 at DC can be seen, and around -38 dB20 at 1.5 MHz.

5.3 LDO with Reference Buffer

The main operating point simulation results in the typical corner for the SRC LDO from Chapter 4.2 are shown in Table 5.2.

Table 5.2: Some OP measurements from LDO simulations.

Parameter	Value
V_{fb}	450.001 mV
V_{out}	900.002 mV
I_q	264.047 µA
I_L	1 mA

After implementing the reference buffer, the overall quiescent current suffered an increase of 56 µA.

5.3.1 DC Behavior

Dropout voltage

A parametric sweep over the input voltage was performed on the typical corner, as seen on Figure 5.3 so as to establish the necessary V_{in} for this LDO to start correctly regulating for $V_{\text{out}} = 0.9$. From

this analysis, it can seen that the minimum V_{in} is 946 mV, resulting in a minimum dropout voltage ΔV of 46 mV.

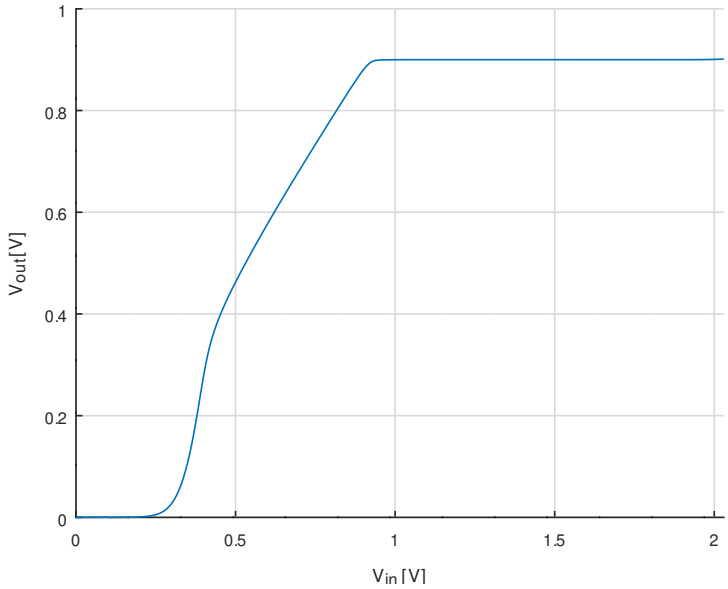


Figure 5.3: Dropout voltage simulation.

Line regulation

A line regulation analysis can also be extracted from this result if analysed for the input range 1 V to 1.4 V, where a regulation delta of around 0.12mV is obtained. This can also be measured in voltage percentage by dividing this value by the nominal output voltage, giving a line regulation of $0.01\%/\text{V}$.

Load regulation

The simulation for the load regulation was performed by running a parametric sweep of the load current from 0 mA to 1 mA, as can be seen on Figure 5.4, for a V_{in} of 1.2 V. From this analysis can be defined the load regulation delta, set around 1.4 mV, or $0.16\%/\text{V}$.

Efficiency

With minimum input voltage of $V_{ph} = 946$ mV for a $V_{\text{out}} = 0.9$ V, and $I_q = 264.047$ µA, and $I_L = 1$ mA, then the LDO's efficiency can be computed as follows:

$$\eta = \frac{1 \times 10^{-3} \times 0.9}{(1 \times 10^{-3} + 264.047 \times 10^{-6}) \times 0.946} = 75.26\%, \tag{5.1}$$

which is around 20% below the maximum efficiency possible for this LDO ($0.9/0.947 = 95.04\%$).

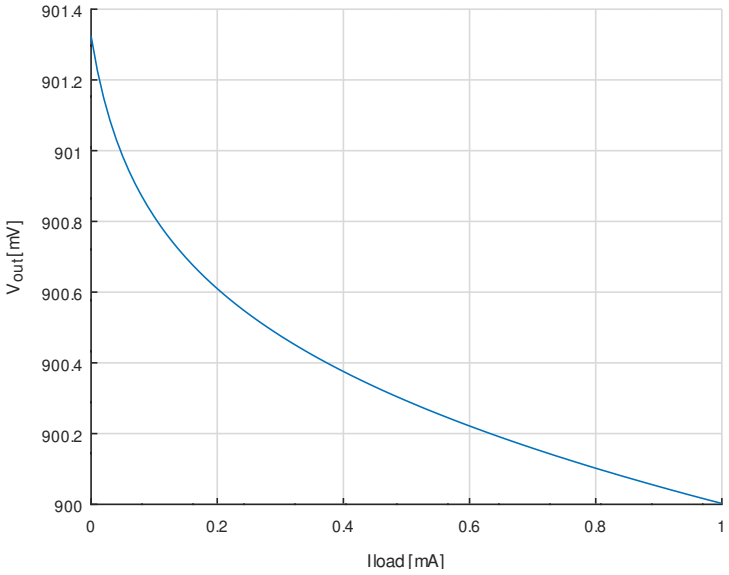


Figure 5.4: Load regulation simulation results.

5.3.2 Transient Behaviour

Startup

The following simulation quantifies the power up of the LDO. As seen on Figure 5.5, for an error band of 2%, the measured settling time is about 4.74 ns.

Load transient

The load transient behaviour was simulated with load current variations from 0 to 1 mA with rise and fall times of 1 ns. This is represented in Figure 5.6, which shows an overshoot and undershoot of 0.18 V and 0.21 V respectively.

Line transient

The line transient behaviour was simulated with input variations of $+/-10\%V_{ph}$, with rise and fall times of 1 ns. From Figure 5.7, the overshoot and undershoots can be extracted, which are 31 mV and 34 mV respectively.

FoM

From equation (2.26) and the previous results, the LDO's FoM can be extracted:

$$\mathrm{FoM} = \sqrt{\frac{2 \times 1 \times 10^{-12} \times 21 \times 10^{-3}}{0.764 \times 10^{-3}/0.4 \times 10^{-9}}} \frac{264.047 \times 10^{-6}}{1 \times 10{-}3} \tag{5.2}$$

$$\approx 39.16 \text{ ps}. \tag{5.3}$$

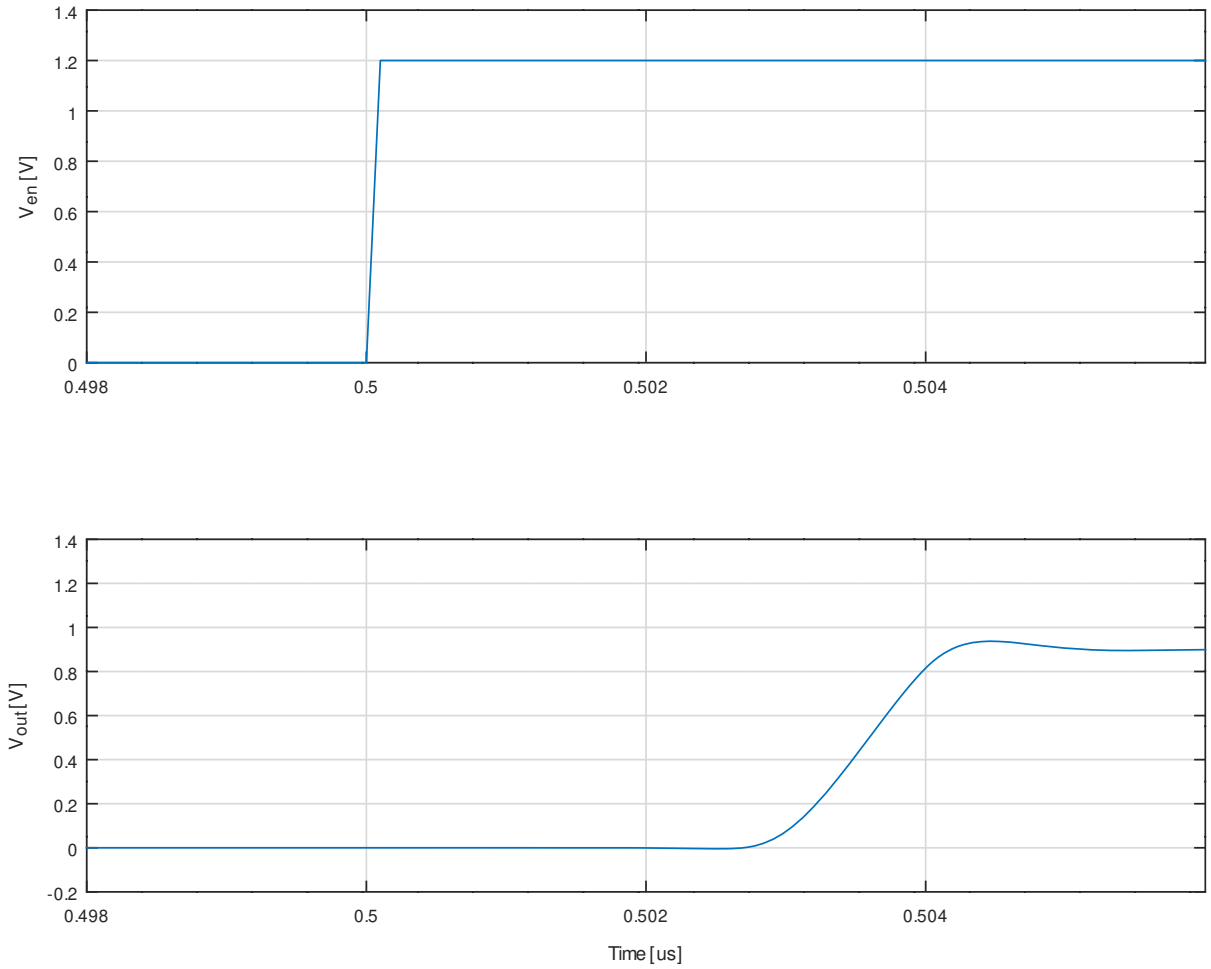


Figure 5.5: Startup simulation results.

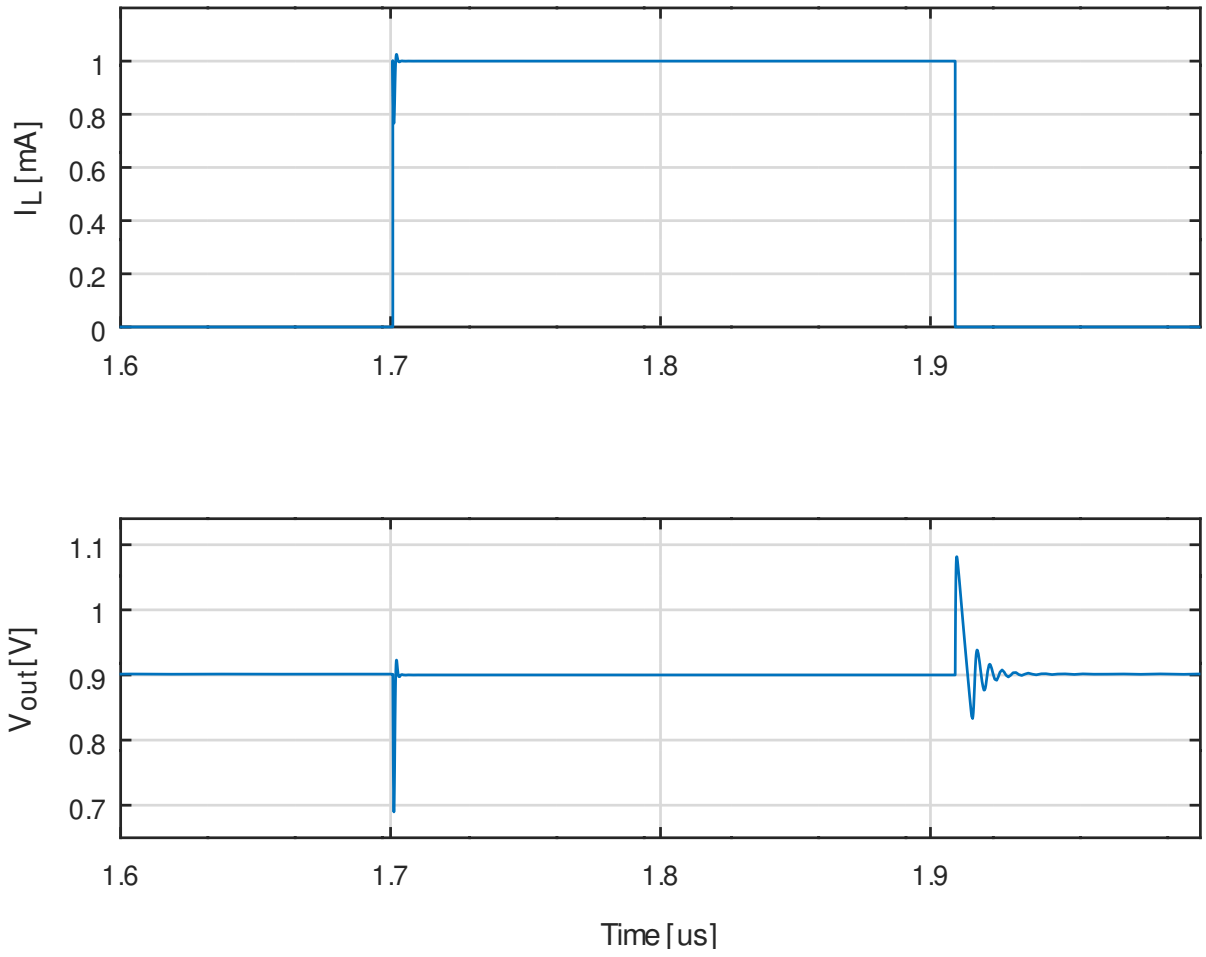


Figure 5.6: Load transient simulations.

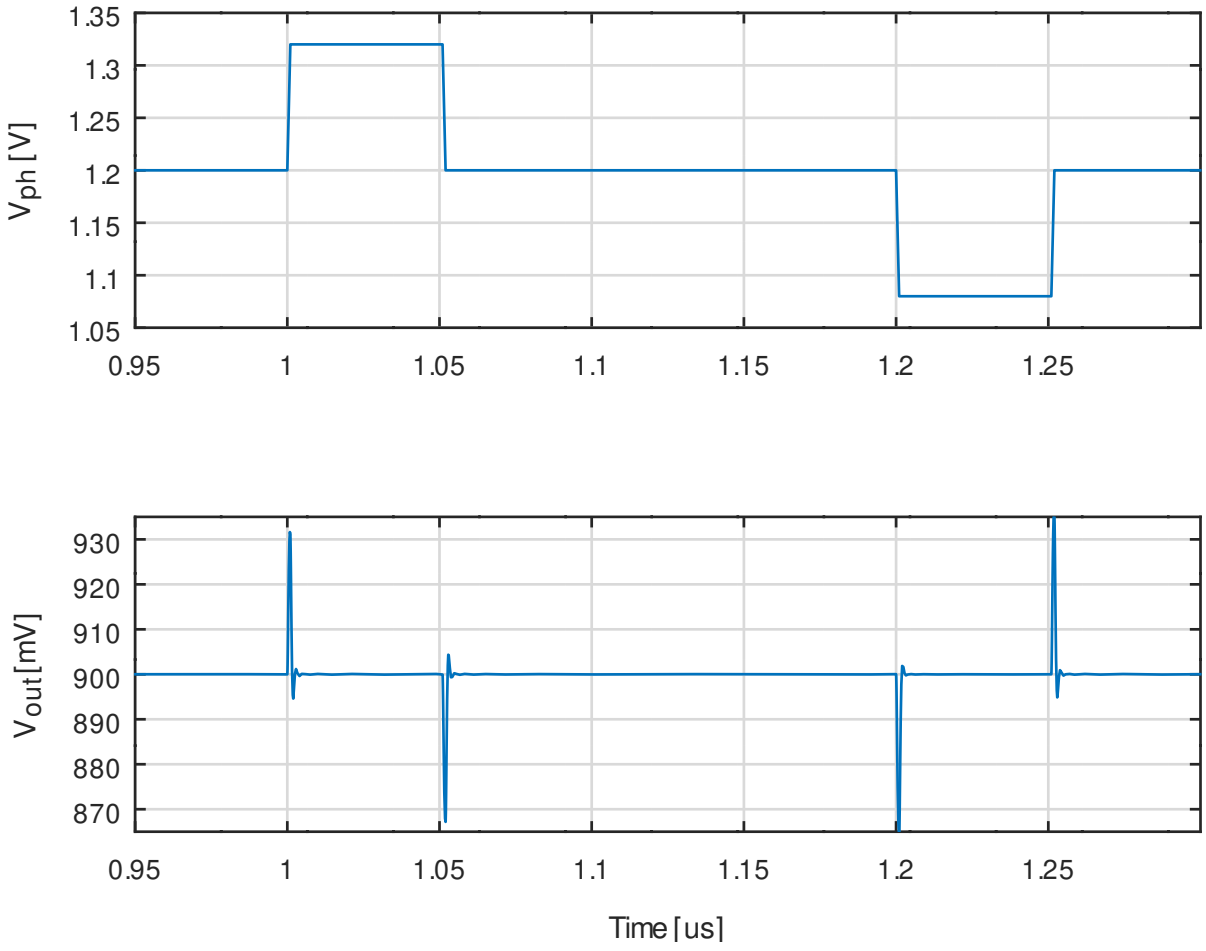


Figure 5.7: Line transient simulations.

5.3.3 AC Analysis

As with the basic design for the LDO, an AC and PSR analysis was performed, presented on Figures 5.8 and 5.9.

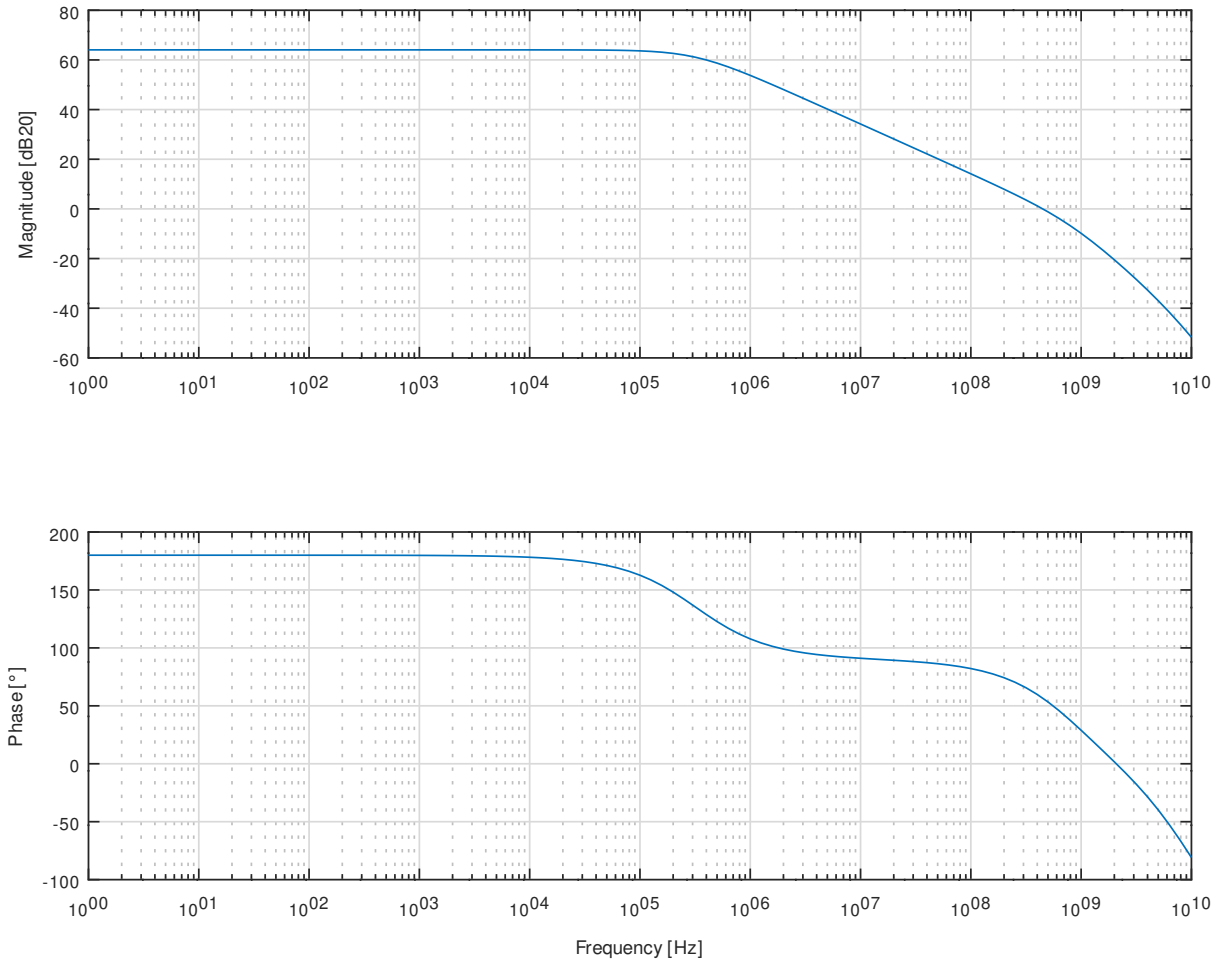


Figure 5.8: AC analysis.

From these figures, it can be extracted that the amp has, in the typical corner, an open loop gain of 61.3 dB20, bandwidth 321 kHz, and phase margin of 56°. The PSR is substantially increased with the reference buffer: in the typical corner, at DC, it is around -113 dB20, and -55 dB20 at 1.5 MHz.

The AC analysis was run with $I_L = 1$ mA only; for a more rigourous analysis, it should be run with a wide range of load current.

5.3.4 PVT Corner Variations

The following PVT measurements from Figure 5.10 to Figure 5.14 were simulated with parameters set as described in section 2.6.3.

Most plots roughly follow the same trend as the typical corner, except for some outliers.

In Figure 5.11, there is a failed corner for which the LDO could not properly regulate for an increase in supply voltage.

In Figure 5.14, some more variation can be seen, mostly explained by the fact that the voltage bias

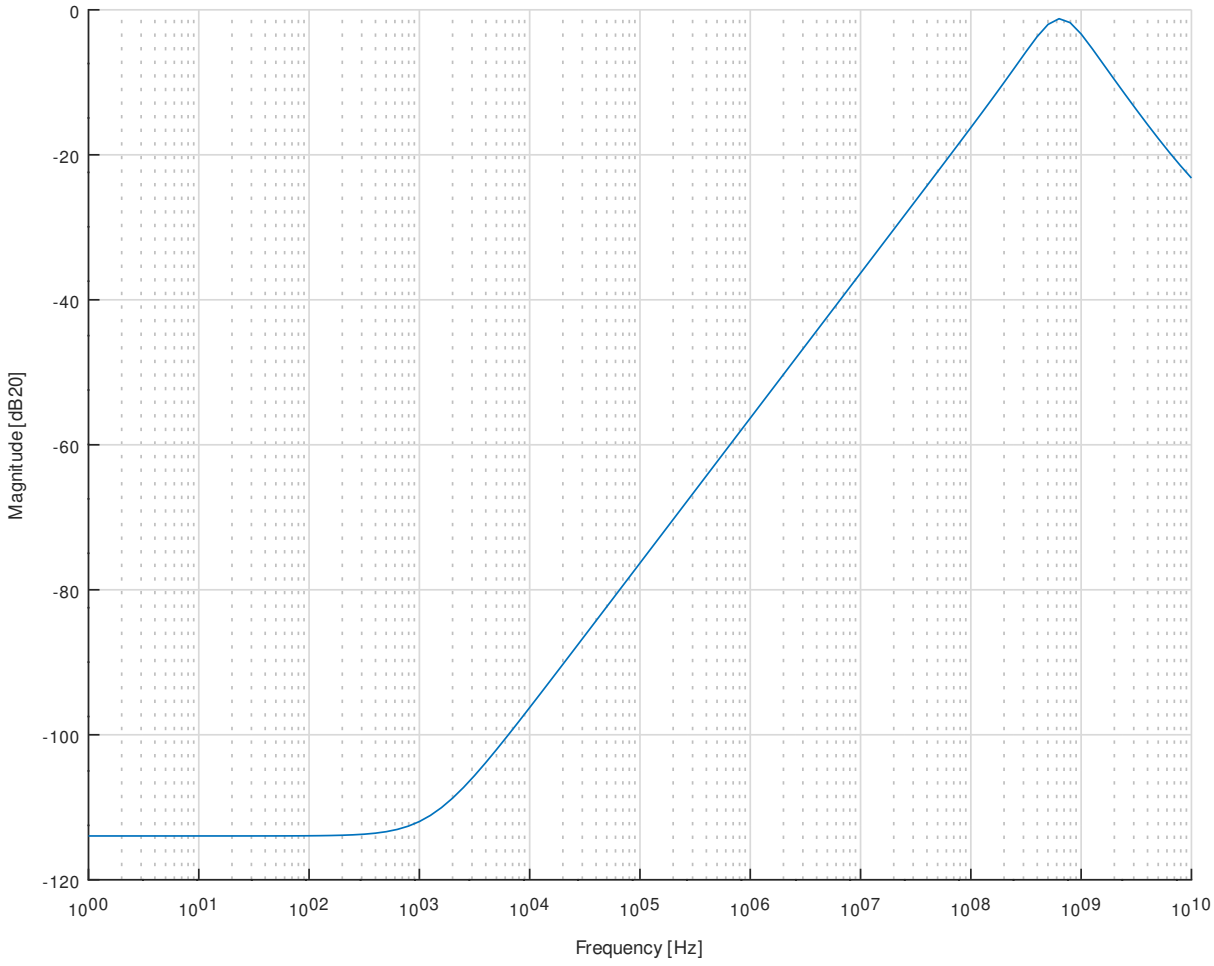


Figure 5.9: PSR analysis.

for $M_{5,6}$ in the reference buffer was supplied by an ideal voltage source, which means it wouldn't properly track the necessary voltage to bias these PMOS as their supply voltages vary. This should be resolved by replacing the ideal voltage sources by the bias voltage generator as defined in Figure 4.6.

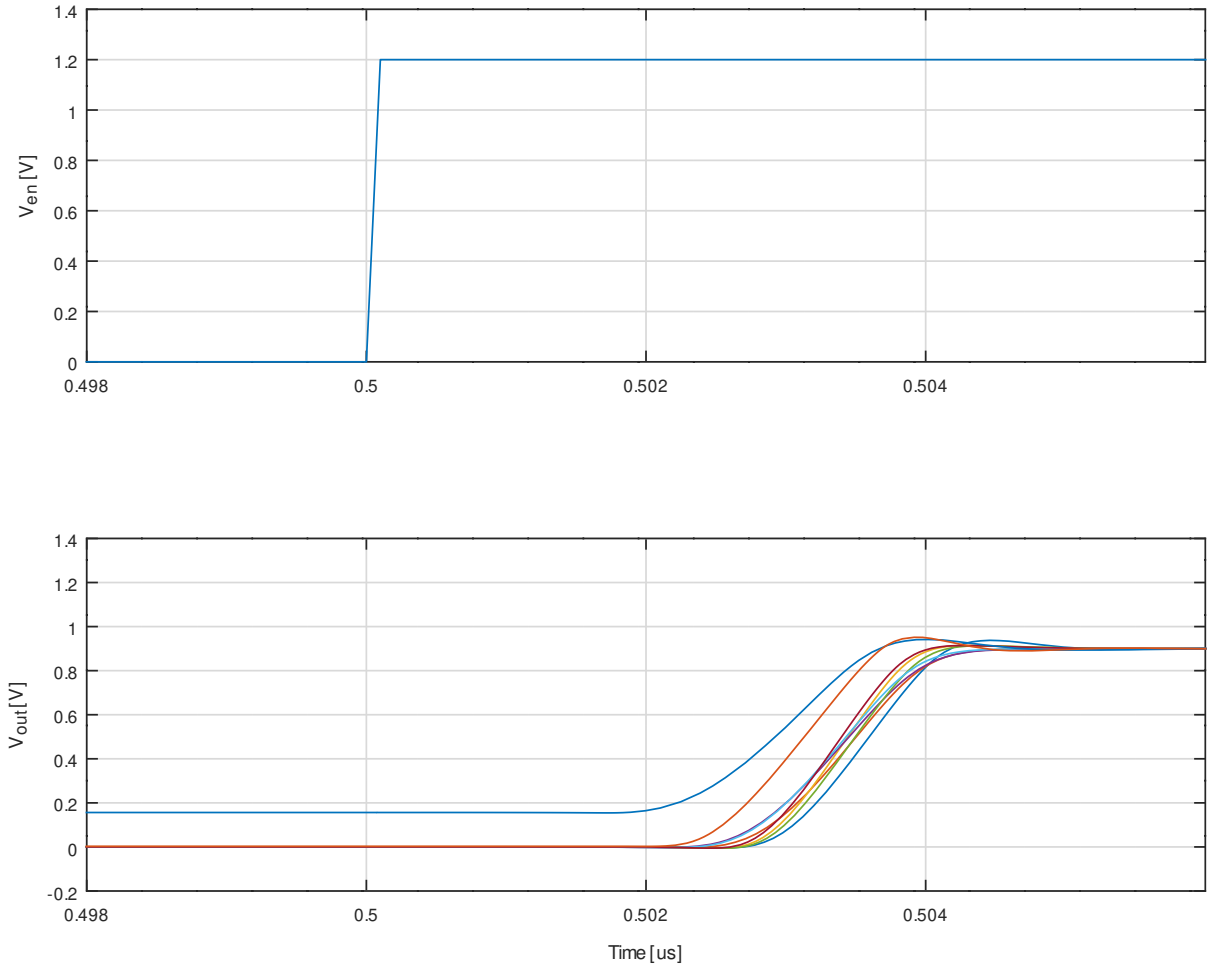


Figure 5.10: Startup PVT simulation results.

5.3.5 Monte Carlo Analysis

Monte Carlo analysis was performed on the worst PVT corners for each analysis. In order to comply with ISO26262 safety and reliability standards, the measured device should have a maximum of 1000 *dppm* [34], (defective parts per million), which corresponds to a 3.09 sigma deviation. To cover a yield percentage of 99.997%, or 3.4 dppm, Monte Carlo simulations were run with a 4.5 sigma for 330 iterations.

All results may be seen on Figures 5.15 to 5.19.

In Figure 5.15, a Monte Carlo (MC) analysis can be seen for the line regulation, outputting a median V_{out} of 927.99 mV, with a standard deviation of 199.92 mV. As around 66.7% of samples will be around this value, this is obviously not ideal, and a possible solution for this could be increasing the area of the EA's differential pair.

As for the load regulation in Figure 5.16, the Gaussian distribution is centered around 879.56 mV

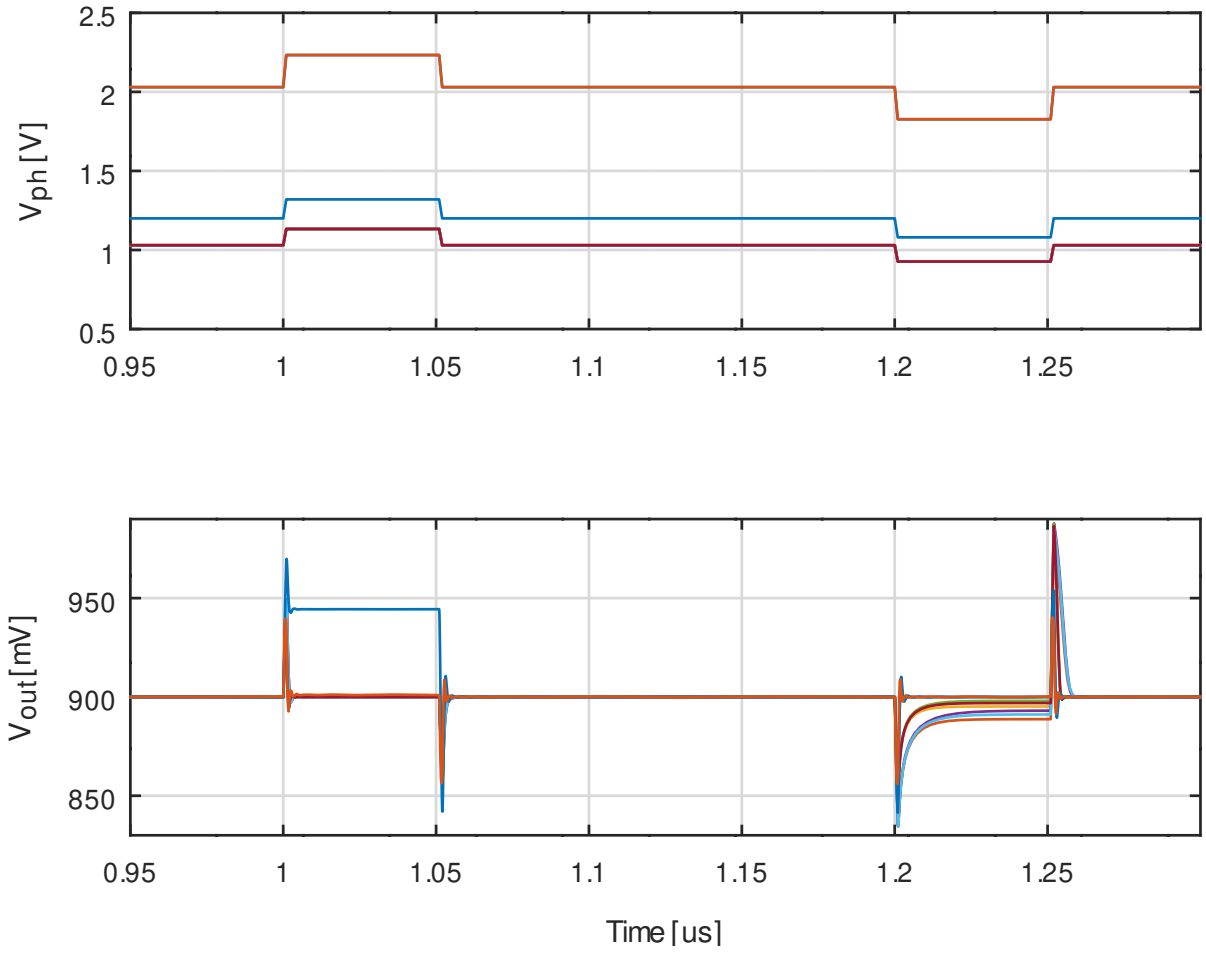


Figure 5.11: Line transient PVT simulation results.

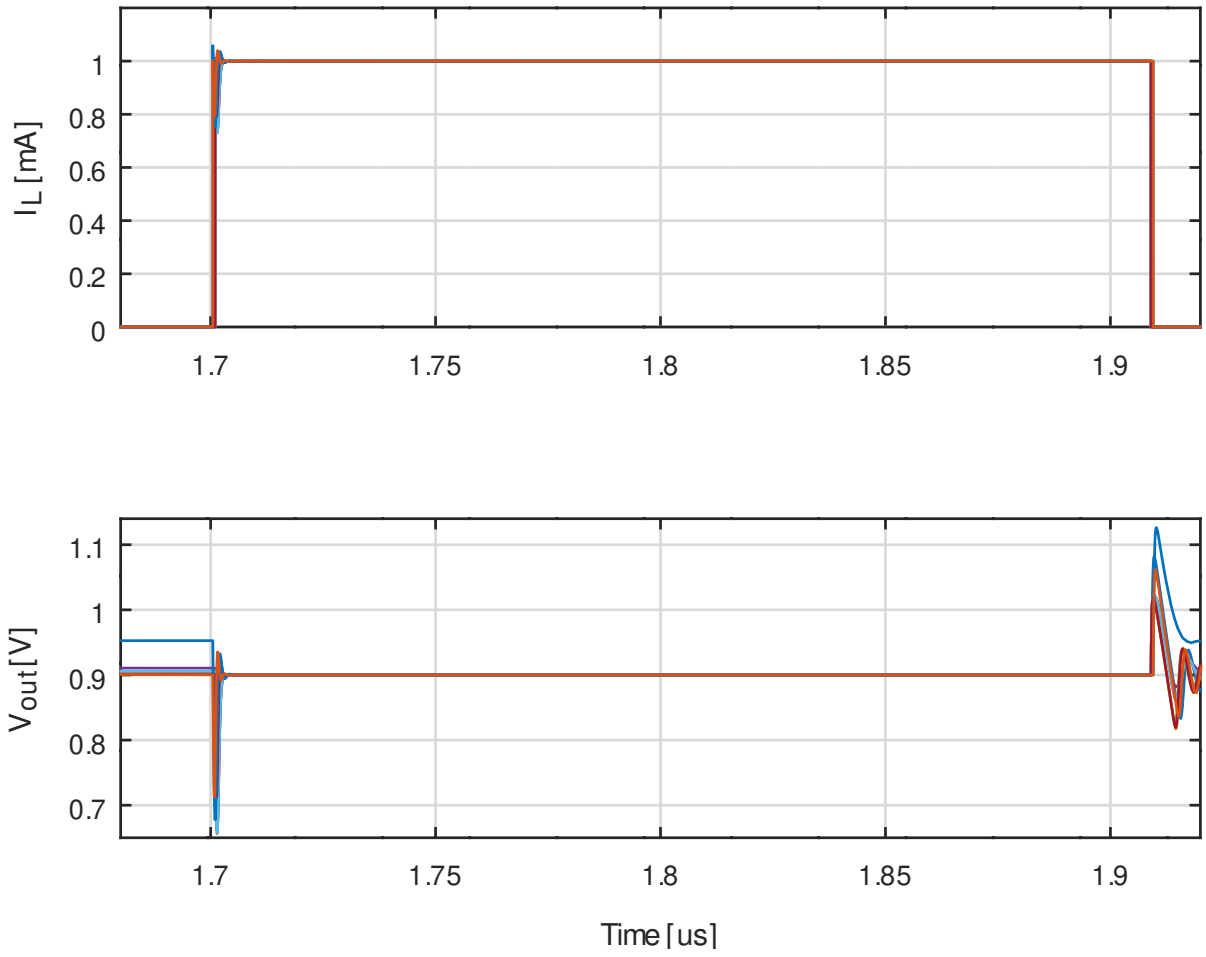


Figure 5.12: Load transient PVT simulation results.

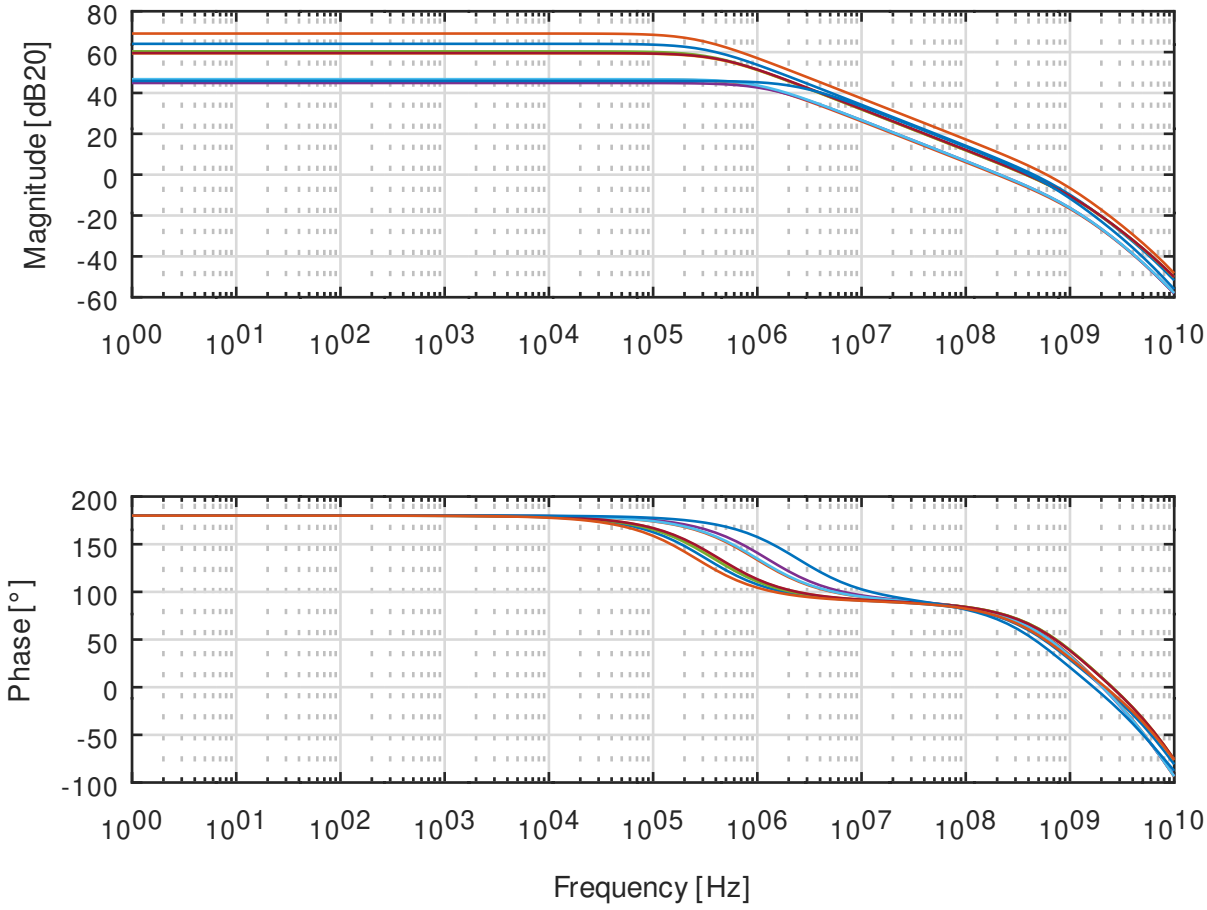


Figure 5.13: AC PVT simulation results.

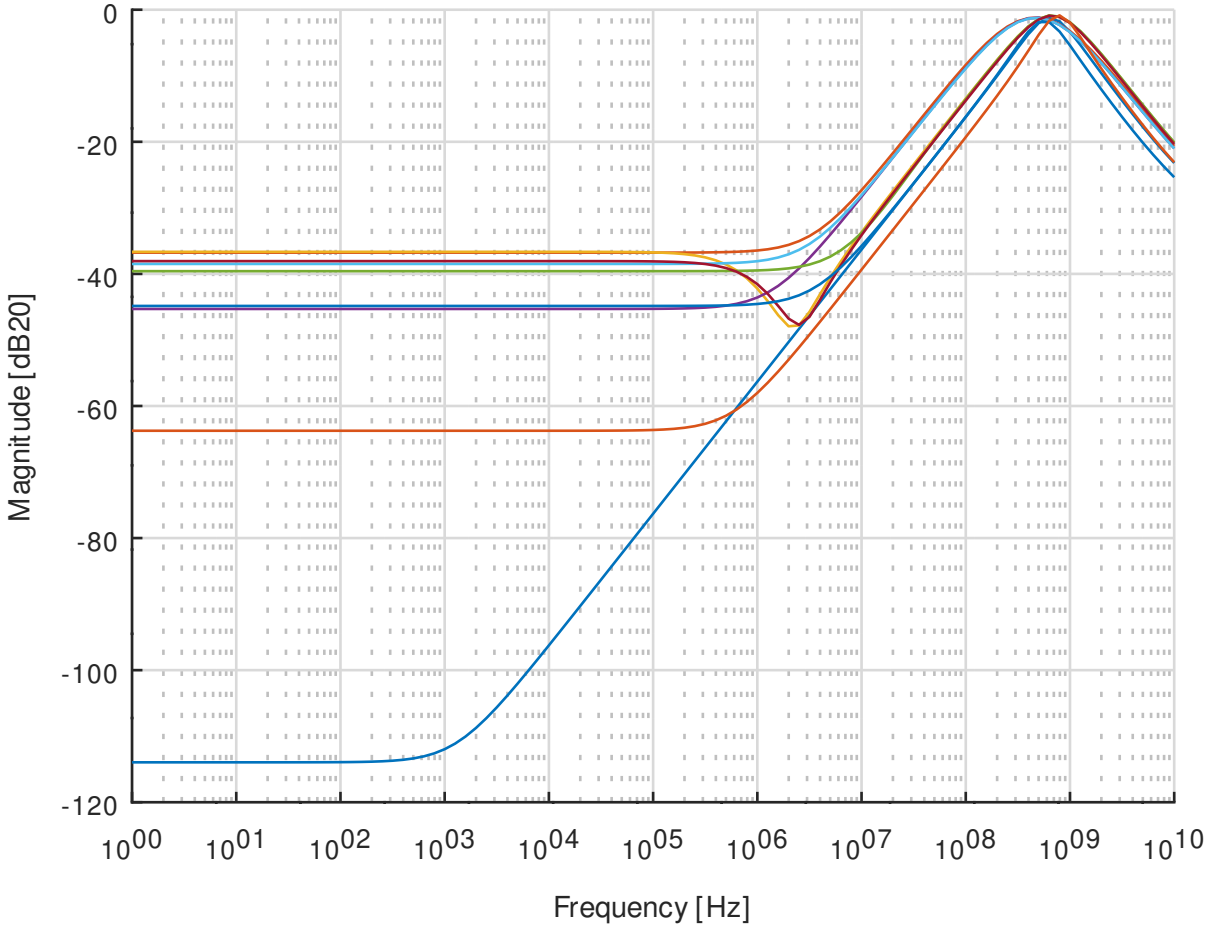


Figure 5.14: PSR PVT simulation results.

with a standard deviation of 66.16 mV.

For the Figures 5.17a and 5.17b, the MC analysis for the AC gain and phase margin can be seen, where their median is at 41.23 dB20 with standard deviation of 11.95 dB20, and 48.67 degrees with standard deviation of 3.97 degrees, respectively. This ensures the stability of the system. The increase in phase margin for some MC runs is explained by the DC gain increase in certain PVT corners.

As with the PVT simulations, there are large standard deviations on the PSR MC analyses, in Figures 5.18 and 5.19. As it was for PVT, this is explained by the fact that the bias voltage is not properly tracked for the $M_{5,6}$ transistors in the reference buffer. Nevertheless, large medians for PSR in low-to-medium frequencies can be verified for what is the worst PVT corner.

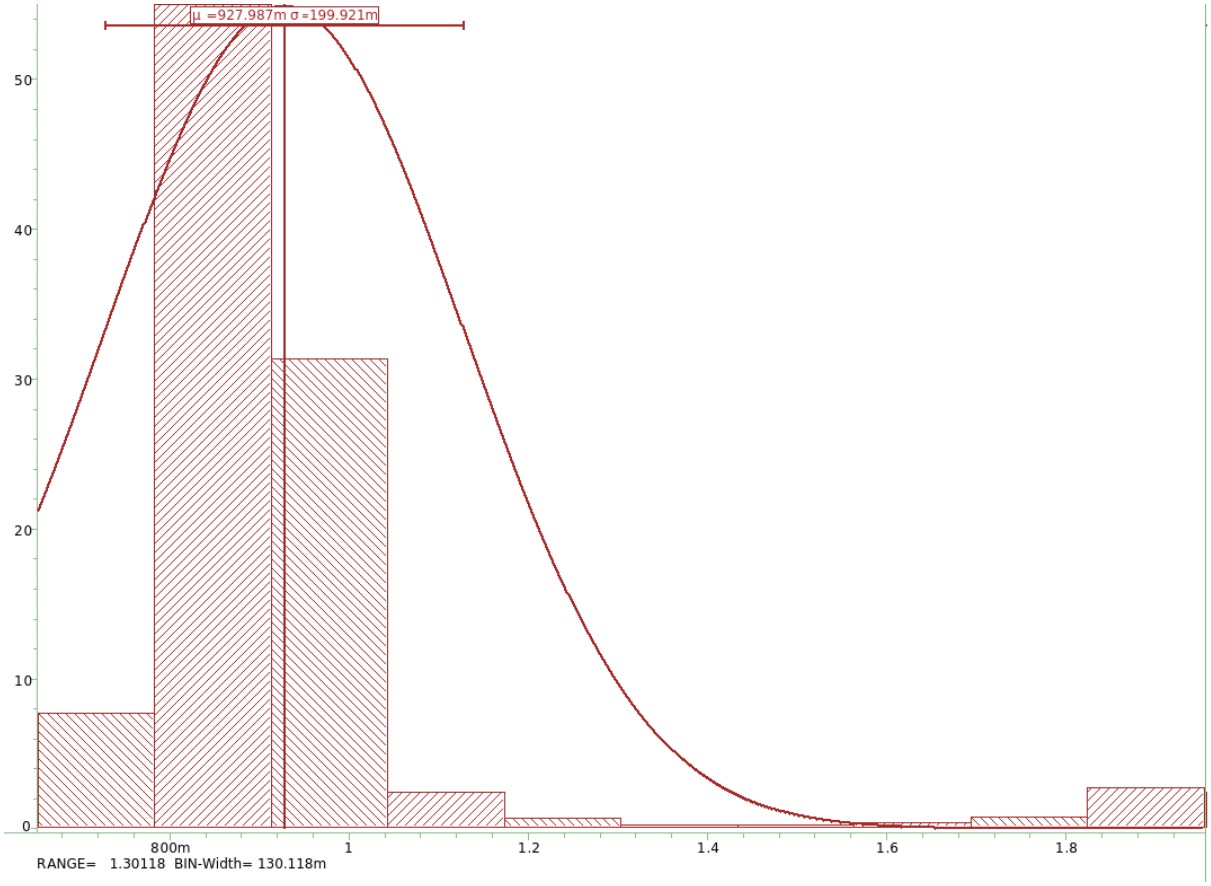


Figure 5.15: Worst case Line Regulation Monte Carlo simulation results.

5.4 Circuit Validation and Datasheet

From the previous simulation results, a datasheet of the proposed Supply Ripple Cancellation LDO is presented on Table 5.3.

Table 5.3: Datasheet of the electrical characteristics for the SRC LDO.

Parameter	Symbol	Min.	Typ.	Max.	Units
Input voltage	V_{in}	0.946	1.2	2	V
Low voltage supply	V_p	646	800	985	mV
Dropout voltage	ΔV	0.046	0.3	1.1	V
Output voltage	V_{out}	899.88	900	902.11	mV
Voltage reference	V_{ref}	-	0.45	-	V
Turn-ON Settling time	T_s	-	4.74	-	ns
Quiescent current	I_q	-	264.047	-	µA
Load capacitance	C_L	-	1	-	pF
Load current	I_L	-	1	-	mA
Load regulation	-	-	1.4	-	mV/mA
Load transient overshoot	-	118.6	180	226	mV
Load transient undershoot	ΔV_{out}	186	210	245	mV
Line transient overshoot	-	30.7	31	87.8	mV
Line transient undershoot	-	31	33	65.6	mV
Power supply rejection	PSR@1kHz	-38.1	-113.2	-113.2	dB20
	PSR@1.5MHz	-37.8	-55.4	-58.6	dB20
	PSR@1GHz	-2	-4	-4	dB20
Efficiency	η	-	75.26	-	%
Figure-of-merit	FoM	-	39.16	-	ps

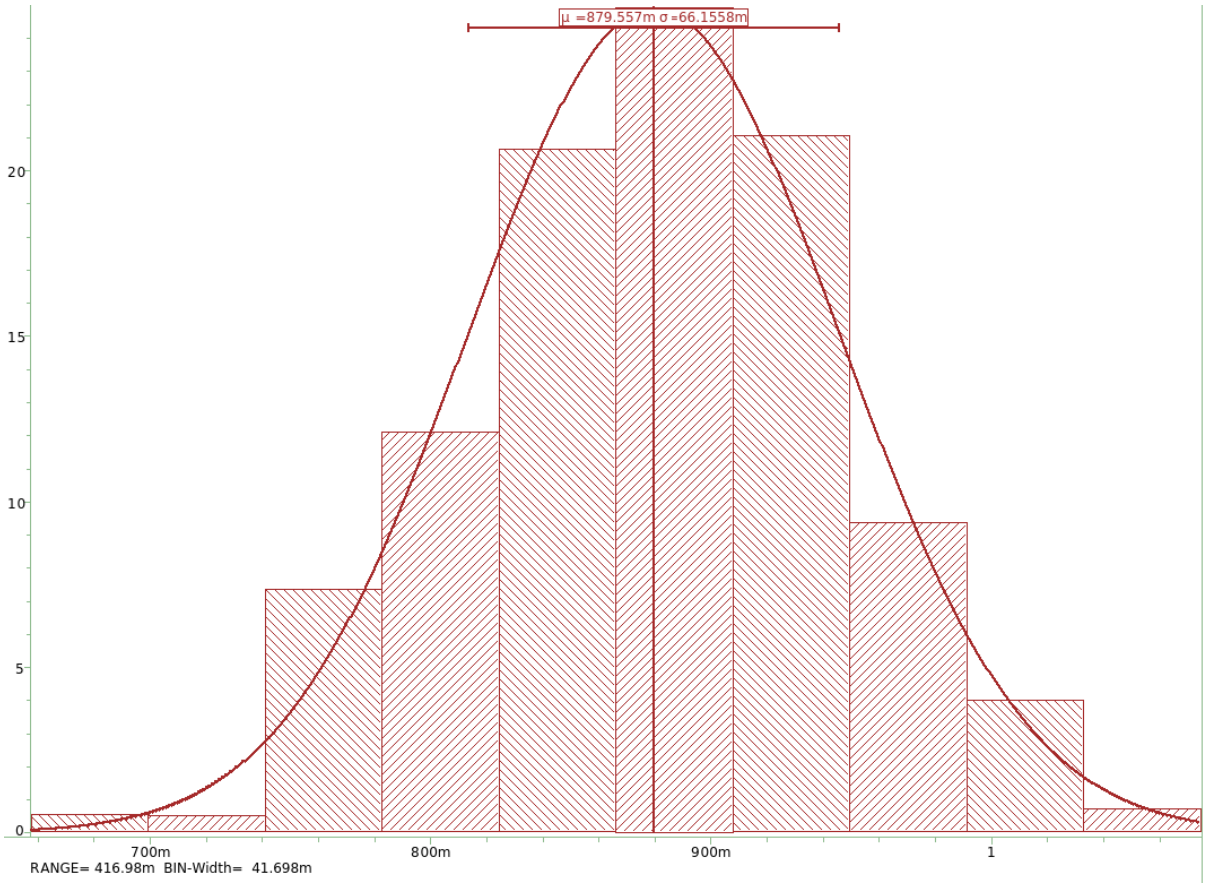
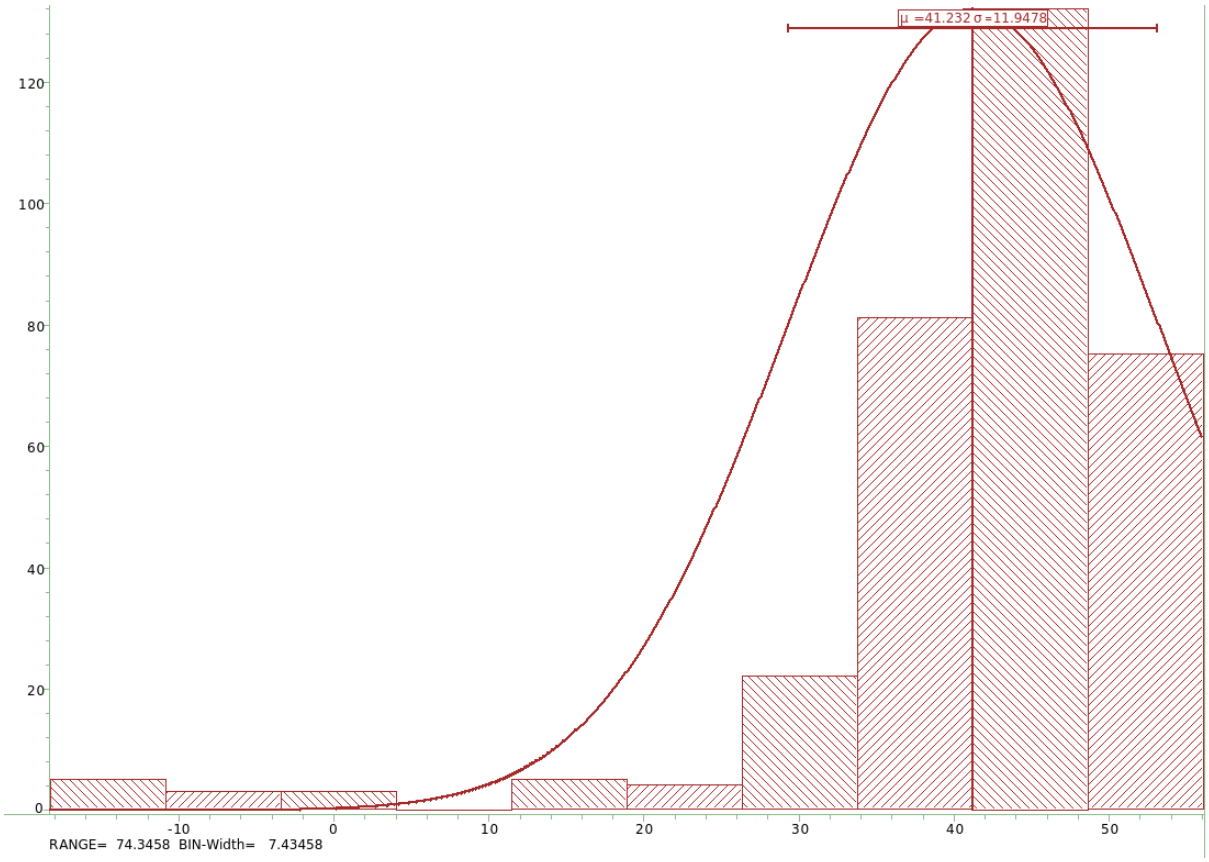
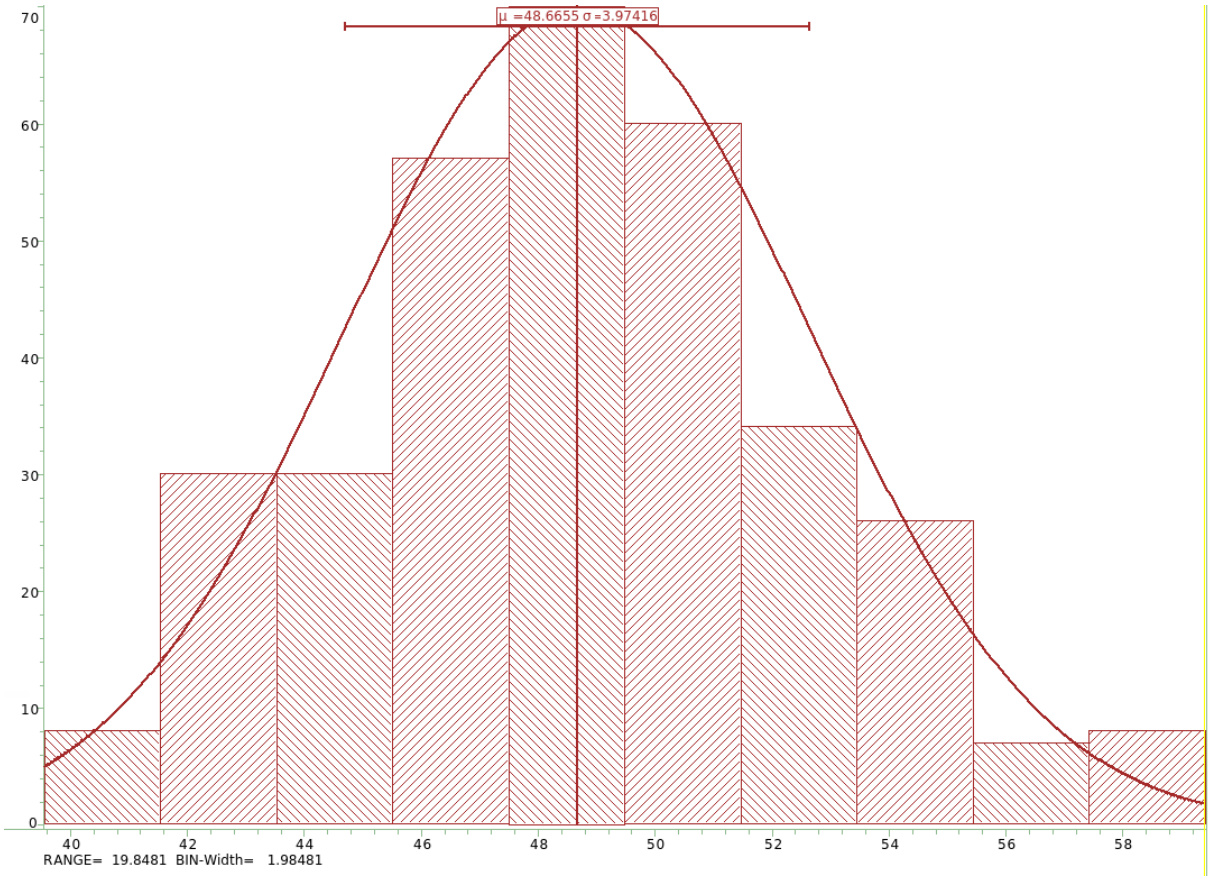


Figure 5.16: Worst case Load Regulation Monte Carlo simulation results.

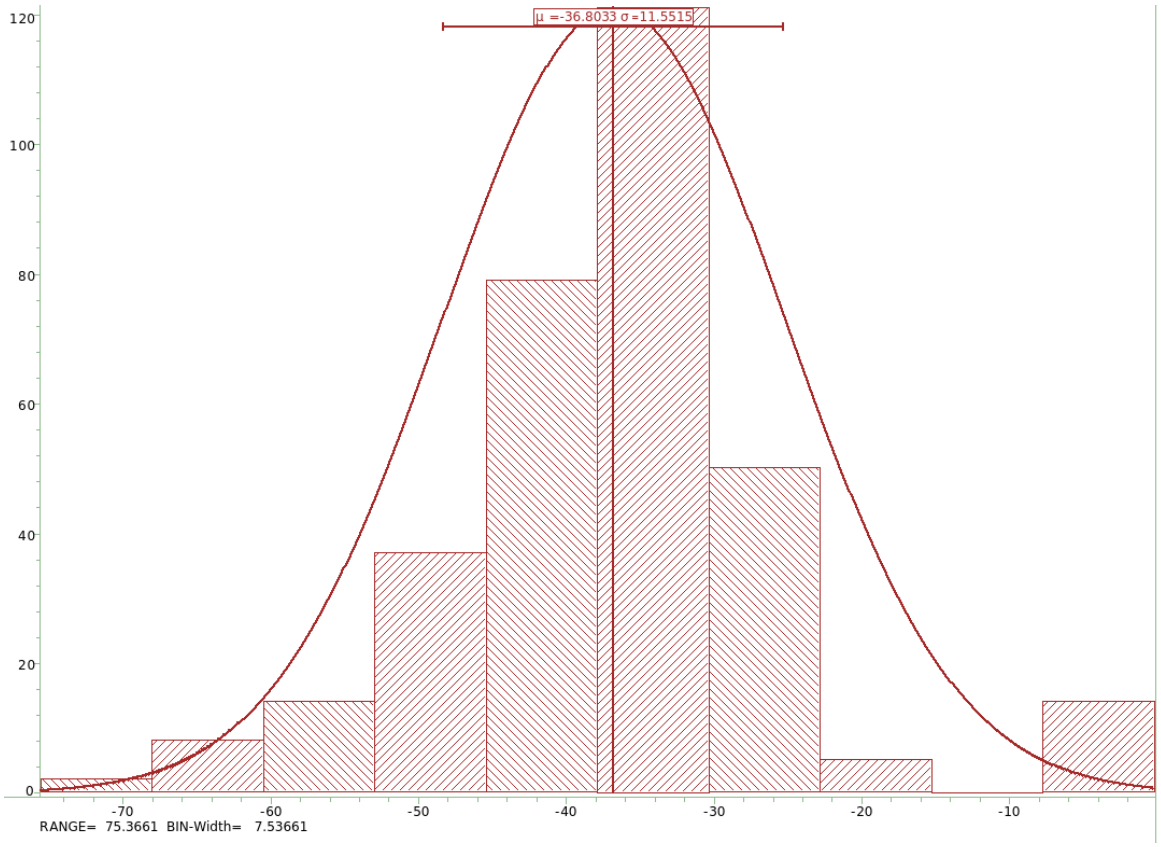


(a) AC gain.

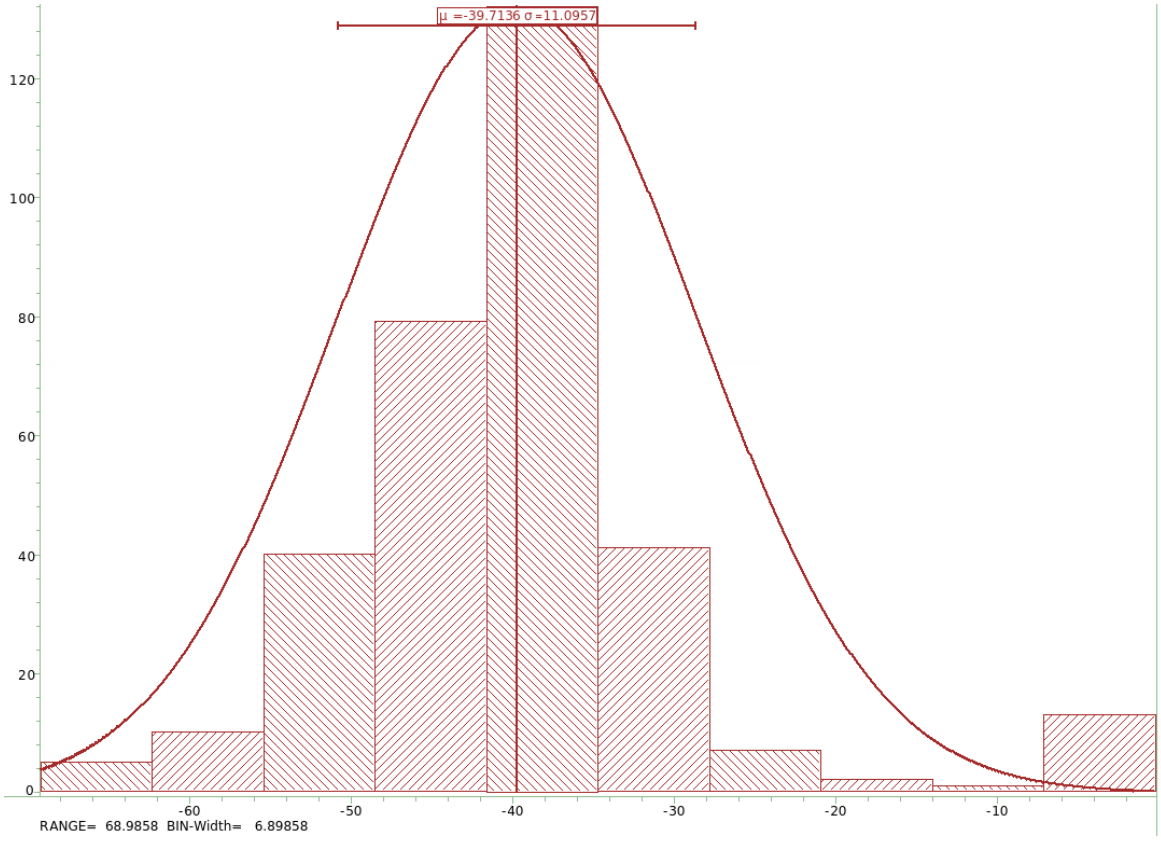


(b) Phase margin.

Figure 5.17: Worst case AC Monte Carlo simulation results.

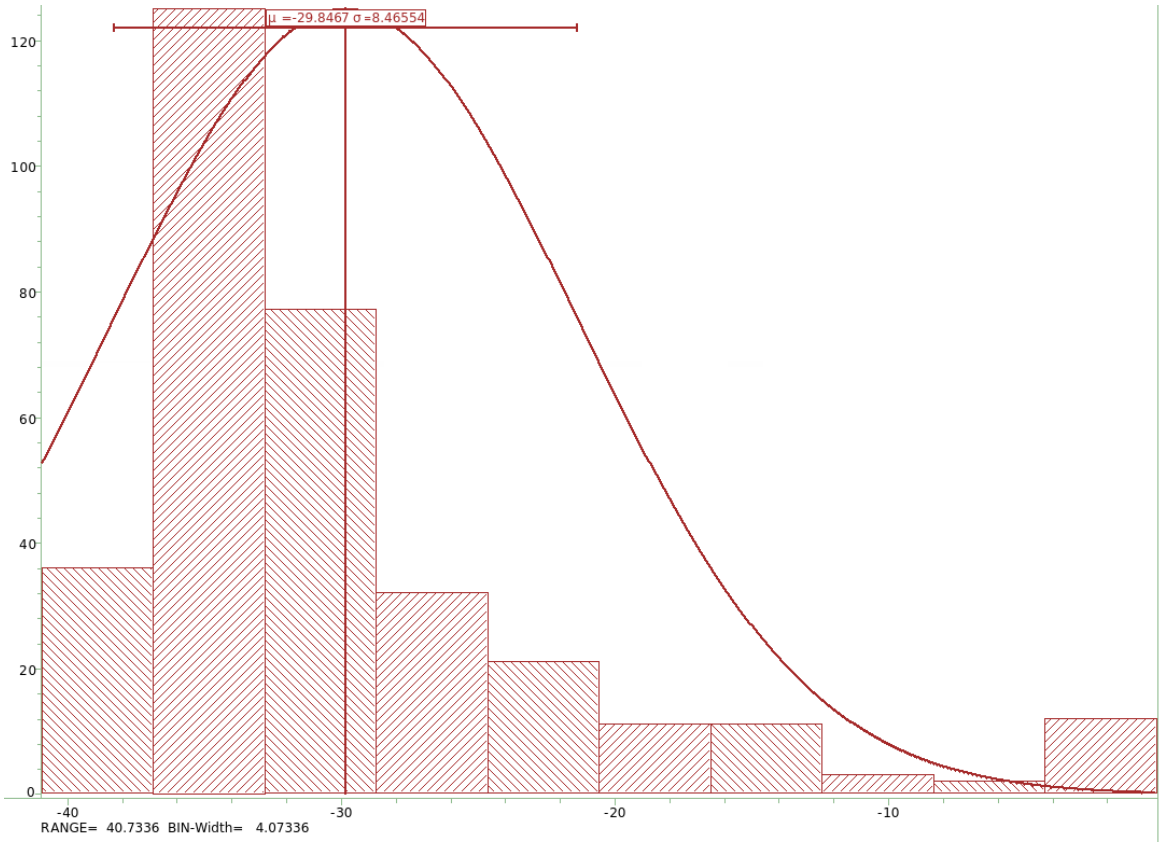


(a) PSR@1kHz.

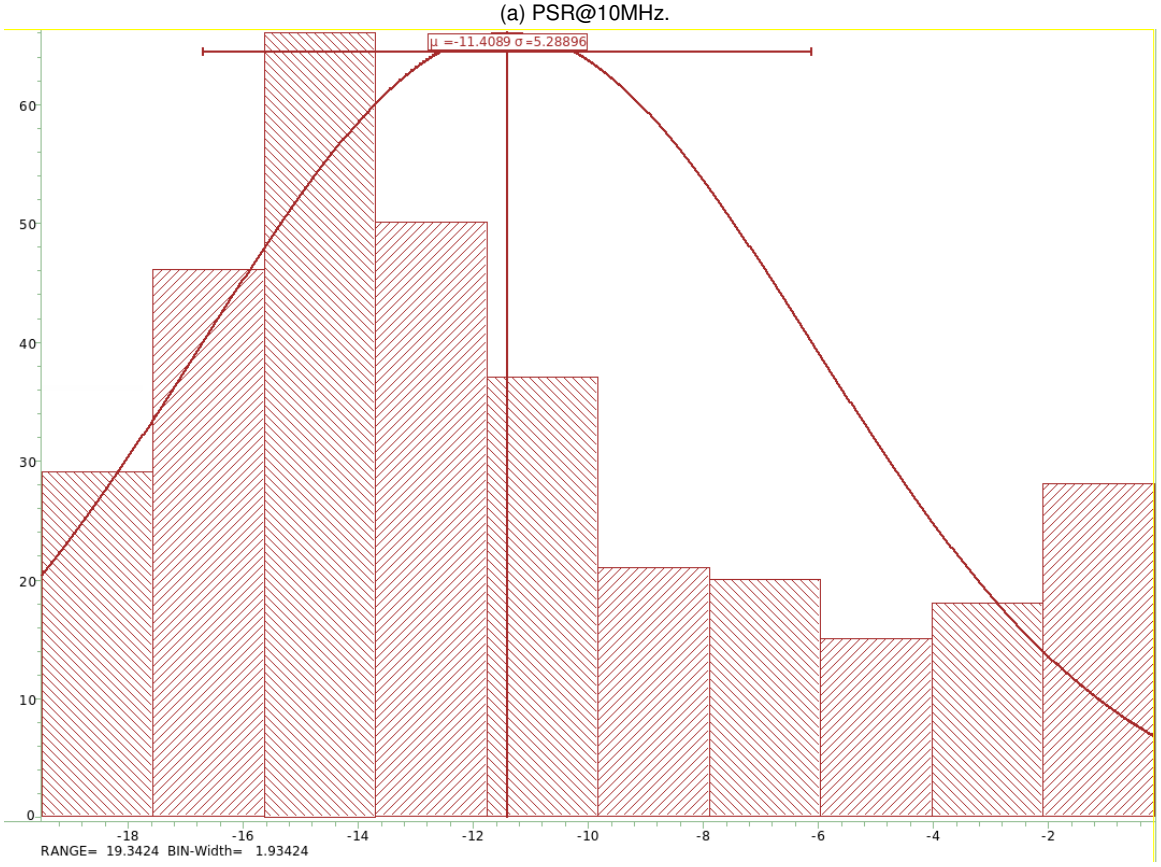


(b) PSR@1MHz.

Figure 5.18: Worst case PSR Monte Carlo simulation results for low-to-medium frequencies.



(a) PSR@10MHz.



(b) PSR@100MHz.

Figure 5.19: Worst case PSR Monte Carlo simulation result for medium-to-high frequencies.

Chapter 6

Conclusion

This work introduced the concept of an LDO, its most relevant parameters, and various LDO topologies, highlighting advantages and disadvantages for each design. Simulated results for a simple PMOS LDO were quantified.

After careful research and consideration on state-of-the-art LDOs, a Supply Ripple Cancellation technique was applied, in which the supply ripple is sensed, inverted, and finally summed to the original supply ripple. Total PSR cancellation is achieved with the tradeoff of PSR bandwidth. Robust PVT results in PSR, overshoot, and undershoot line transients are achieved.

On this work, the schematic section of the analog design flow was delivered. To build upon this thesis, a layout could be designed, and an LVS could be realized; only after good results from the latter should this circuit enter prototype fabrication, after which, if the specs are met, it should enter production. This flow is summarised on Figure 6.1.

Beyond this, a more rigorous analysis of flicker noise could be performed upon the simulations and results, as it is an important parameter that could degrade the PSR from the buffer.

A thorough study on this technique applied to frequencies outside the EA's bandwidth should also be performed.

To increase current efficiency, higher output current should be considered, and quiescent current should be reduced. More corners should also be realized in order to render this circuit more robust. Finally an Electromigration and voltage drop (EMIR) analysis should be done after layout and then again after design of the IC chip, so that power integrity should cause no issues.

To further improve the LDO's performance, an impedance attenuation technique buffer [21] could be implemented, so as to push the pole at the gate of the PPT beyond the UGF of the loop, increasing PSR bandwidth.

In order to alleviate load transients and decrease FoM, an output capacitor could also be introduced.

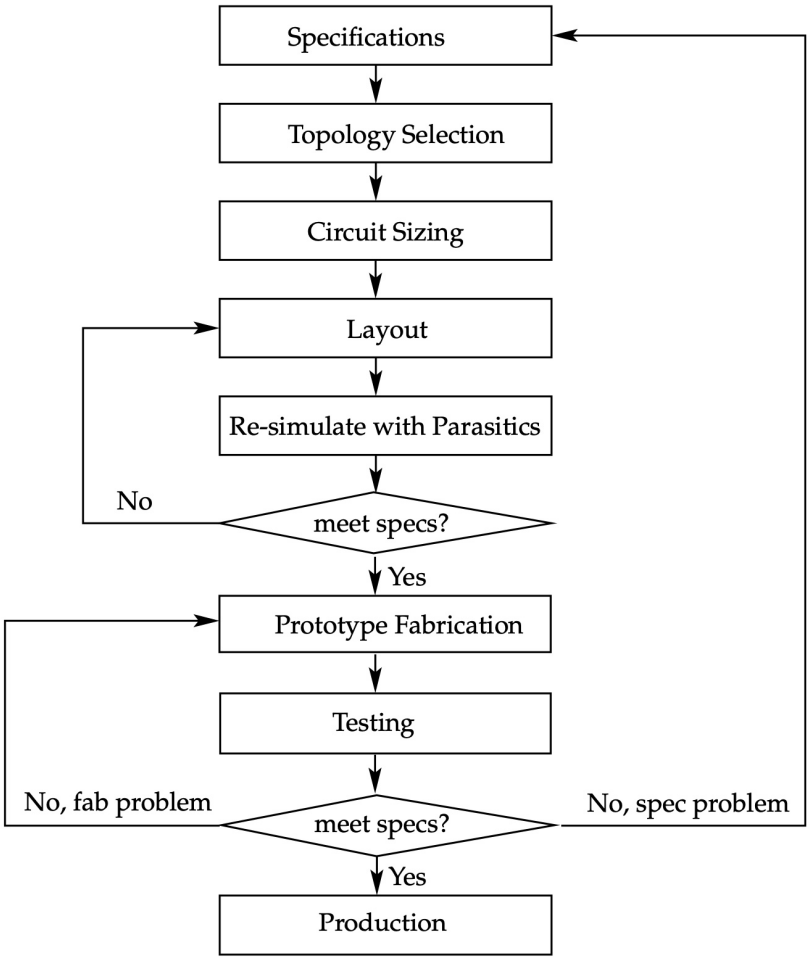


Figure 6.1: Simplified typical design flow of analog integrated circuits. [32]

Bibliography

[1] C. Reichert, ”Samsung led smartphone shipments for 2021, beating out Apple,” CNET, Jan. 2022.

[2] S. Mukherjee, ”Gartner revises 2022 mobile sales estimates to fall 7.1%,” Reuters, June 2022.

[3] ”Top 5 Companies, Worldwide Smartphone Shipments, Market Share, and Year-Over-Year Growth, Calendar Year 2021,” IDC Quarterly Mobile Phone Tracker, Jan. 2022.

[4] S. Venkatesan, ”How The CHIPS Act Benefits Semiconductor Companies Of All Sizes,” Forbes, Sep. 2022.

[5] B. Razavi, “The low-dropout regulator,” IEEE Solid-State Circuits Mag., vol. 11, no. 2, pp. 8–13, Spring 2019.

[6] B. Razavi, ”Design of Analog CMOS Integrated Circuits,” McGraw Hill Education, Second Edition, Chap. 9: ”Operational Amplifiers”, 2017.

[7] ”Li-ion Voltage Analysis,” Silicon Lightworks.

[8] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, “Area-efficient linear regulator with ultra-fast load regulation,” IEEE J. Solid-State Circuits, vol. 40, no. 4, pp. 933–940, Apr. 2005.

[9] F. Goodenough, ”Low Dropout Linear Regulators”, Electronic Design, May 13 1996.

[10] G. A. Rincon-Mora, “Current Efficient, Low Voltage, Low Dropout Regulators,”, Georgia Institute of Technology, Chap. 1, p. 4, Nov. 1996.

[11] Q. H. Duong *et al.*,“Multiple-loop design technique for high-performance low-dropout regulator,” IEEE J. Solid-State Circuits, vol. 52, no. 10, pp. 2533–2549, Oct. 2017.

[12] X. Zhao, Q. Zhang, Y. Xin, S. Li, L. Yu, ”A High-Efficiency Fast-Transient LDO With Low-Impedance Transient-Current Enhanced Buffer,” EEE Transactions on Power Electronics, vol. 37, no. 8, Aug. 2022.

[13] W. Fwu, ”Understanding the Foundations of Quiescent Current in Linear Power Systems,” Texas Instruments, Mar. 2021.

[14] G. A. Rincon-Mora, “Analog IC Design with Low-Dropout Regulators,” McGraw Hill, Second Edition, Chap. 2, p. 38, 2014.

[15] C. Lim, D. Mandal, B. Bakkaloglu, and S. Kiaei, “A 50-mA 99.2 peak current efficiency, 250-ns settling time digital low-dropout regulator with transient enhanced PI controller,” IEEE Trans. on Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 8, pp. 2360–2370, Aug. 2017.

[16] A. Tang, Y. Yang, C.-Y. Lee, N. K. Jha, ”McPAT-PVT: Delay and Power Modeling Framework for FinFET Processor Architectures Under PVT Variations,” IEEE Trans. on VLSI Syst., vol. 23, no. 9, pp. 1616-1627, Sep. 2015.

[17] N. H. E. Weste, D. M. Harris, ”CMOS VLSI design: a circuits and systems perspective,” Noida: Pearson, 2015.

[18] F. de O. Barros, ”Fast loop for a capless LDO”, Master thesis, Oct. 2022.

[19] Y. Lu, W.-H. Ki, and C. P. Yue, “An NMOS-LDO regulated switched capacitor DC–DC converter with fast-response adaptive-phase digital control,” IEEE Trans. Power Electron., vol. 31, no. 2, pp. 1294–1303, Feb. 2016.

[20] B. Razavi, ”The Design of An LDO Regulator,” IEEE Solid-State Circuits Mag., vol. 14, no. 2, pp. 7-17, Spring 2022.

[21] M. Al-Shyoukh, H. Lee, ”A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator With Impedance Attenuation,” IEEE Journal of Solid-State Circuits, vol. 42, no. 8, Aug. 2007.

[22] Y. Lim, J. Lee, S. Park, Y. Jo, and J. Choi, “An external capacitorless low-dropout regulator with high PSR at all frequencies from 10 kHz to 1 GHz using an adaptive supply-ripple cancellation technique,” IEEE J. Solid-State Circuits, vol. 53, no. 9, pp. 2675–2685, Sep. 2018.

[23] J.Jiang, W.Shu, and J.S.Chang, “A 65-nm CMOS low dropout regulator featuring $>$ 60-dB PSRR over 10-MHz frequency range and 100-mA load current range,” IEEE J. Solid-State Circuits, vol. 53, no. 8, pp. 2331–2342, Aug. 2018.

[24] C. J. Park, M. Onabajo, and J. Silva-Martinez, “External capacitor-less low drop-out regulator with 25 dB superior power supply rejection in the 0.4-4 MHz range,” IEEE J. Solid-State Circuits, vol. 49, no. 2, pp. 486–501, Feb. 2014.

[25] S. Bu, J. Guo, and K. N. Leung, “A 200-ps-response-time output-capacitorless low-dropout regulator with unity-gain bandwidth $>$100 MHz in 130-nm CMOS,” IEEE Trans. Power Electron., vol. 33, no. 4, pp. 3232–3246, Apr. 2019.

[26] R. Magod, B. Bakkaloglu, and S. Manadhar, “A 1.24 µA quiescent current NMOS low dropout regulator with integrated low-power oscillator-deriven charge-pump and switched-capacitor pole tracking compensation,” IEEE J. Solid-State Circuits, vol. 53, no. 8, pp. 2356–2367, Aug. 2018.

[27] X. Ming, H. Liang, Z.-W. Zhang, Y.-L. Xin, Y. Qin, and Z. Wang, “A high-efficiency and fast-transient low-dropout regulator with adaptive pole tracking frequency compensation technique,” IEEE Trans. Power Electron., vol. 35, no. 11, pp. 12401–12415, Nov. 2020.

[28] X. Han, L. Wu, Y. Gao, and W.-H. Ki, ”An Adaptively Biased Output-Capacitor-Free Low-Dropout Regulator With Supply Ripple Subtraction and Pole-Tracking-Compensation,” IEEE Trans. Power Electron., vol 36, no. 11, pp. 12795-12804, Nov. 2021.

[29] J. Patoux, ”Low-Dropout Regulators,” Ask The Applications Engineer—37, Analog Dialogue 41-05, May 2007.

[30] J. Fernandes, ”Ultra Low Power Circuits” course slides, Instituto Superior Técnico.

[31] B. Razavi, ”Design of Analog CMOS Integrated Circuits,” McGraw Hill Education, Second Edition, Chap. 3: ”Single-stage Amplifiers”, pp. 46-47, 2017.

[32] R. J. Baker, ”CMOS circuit design, layout and simulation,” IEEE Press, John Wiley & Sons, Inc., 2nd edition, 2008.

[33] B. Razavi, ”Design of Analog CMOS Integrated Circuits,” McGraw Hill Education, Second Edition, Chap. 5: ”Cascode Current Mirrors”, pp. 144-145, 2017.

[34] Synopsys, Inc., ”PrimeSim Reliability Analysis,” p. 2, 2021.