Silicon Wafer Processing

PAKAGING AND TEST

- Parametrical test using test structures regularly distributed in the wafer
- Wafer die test marking defective dies
- dies separation
- die fixing (not marked as defective) and connection to package by:
  - *Wire bonding* or
  - *Flip-chip*
- Final test
Packaging purposes:

- Heat transfer from the die to the exterior
- Protect the die from the exterior environment
- Allow interface for production test
- Implement an interface with PCB
  - Mechanical
  - Electrical

Goals:

- Minimum dimensions
- Lowest price possible
Connection between die and packaging:

- **Wire bonding**
  - Only the *die* boundary is available for connection
  - Sequential pin connection
  - Heat transfer through the substrate
  - $L \approx 1 \, \text{nH}$

- **Flip-chip**
  - All the die area is available for interconnections
  - All pins are connected simultaneously
  - Heat transfer through the connections (and subs. if required)
  - Even thermal physical properties required
  - $L \approx 0.1 \, \text{nH}$
## Types of packaging:

<table>
<thead>
<tr>
<th>Type</th>
<th>Good Thermal Properties</th>
<th>Expensive</th>
<th>Bad Thermal Properties (can be improved with metallic heat dissipation)</th>
<th>Cheap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ceramic</td>
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<tr>
<td>Plastic</td>
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## Interface with PCB:

- **Pin through hole**
  - Easy manual assembly
  - Each pin is available in all PCB levels
  - Limited density
- **Surface Mount Devices (SMD)**
  - Requires dedicated equipment for PCB assembly
  - Only the surface of the PCB is available (it doesn’t interfere with bottom PCB levels)
  - Higher density

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**Silicon Wafer Processing**

**PAKAGING AND TEST**
Traditional packaging:
Inductances: 1 - 20 nH

- **DIL (Dual In Line)**
  - Small number of pins
  - Large space
- **PGA (Pin Grid Array)**
  - until 400 pins
  - frequently used in old CPUs
- **PLCC (Plastic Leaded Chip Carrier)**
  - until 84 pins
  - Requires large space
  - SMD
- **QFP (Quarter Flat pack)**
  - until 300 pins
  - Requires large space
  - SMD
More recent packages:
Inductances: 1 - 5 nH

• **BGA (Ball Grid Array)**
  – Small balls for PCB connection
  – Large number of pins
  – Small space required
  – Lower inductance

• **CSP (Chip scale Packaging)**
  – Like BGA but smaller

• **MCP (Multi Chip Package)**
  – Allows different technologies in the same device
  – Increases yield since each chip is tested before packaging
In a N well process the wafer must have P type impurities.

- The wafer typical diameter is between 75 mm and 300 mm, with a thickness <1 mm (typically between 500 µm and 800 µm).

- Can be obtained building an epitaxial layer P- (about 2 µm, smaller concentration, more pure, smaller latch-up risk).
2 – N Well

- The first mask used defines the N wells position.
- The N wells can be obtained by diffusion or ion implant (better since it has smaller lateral diffusion).
- The N well is very deep: 30000 Å.
3 – Active area definition

- Areas for the implementation of transistors (gate, source and drain) and other diffusions (biasing the substrate and well, guard rings).
- This area will receive the thin oxide
- Is protected with SiO$_2$ ($\approx 200$ Å) and Si$_3$N$_4$ ($\approx 2500$ Å)
4 – Devices isolation

- There are parasitic MOS transistors besides the ones designed:
  - The implemented diffusions form drains and sources
  - The gates are the metal and poly interconnections
  - It is mandatory to force the Vth of these parasitic MOS to be higher than the supply voltage:

  - Increasing the bulk concentration between diffusions of different transistors (*channel-stop*)
  - Increasing the thickness of the FOX.
The channel-stop is obtained by ion implant, customized using Si$_3$N$_4$ (in the P substrate) and *photoresist* (in the N well).
4 – Devices isolation (LOCOS)

- Growing of the thick oxide - *Local oxidation of silicon (LOCOS)*:
  - *photoresist* is removed
  - $\text{Si}_3\text{N}_4$ and $\text{SiO}_2$ are the masks
  - $\text{SiO}_2$ grows: $1000^\circ\text{C} + \text{H}_2\text{O}$ ou $1200^\circ\text{C} + \text{O}$
  - The oxide grows in all directions reducing the original masked active area
5 – Thin oxide

- The active area masks (Si$_3$N$_4$ over SiO$_2$) are removed
- The concentration at the surface is adjusted in order to obtain the desired $V_{th}$
- The thin oxide grows with a thickness that varies from $t_{ox} = 20 \text{ Å}$ to 100 Å

Is one of the most critical steps in the process!
The wafer is covered with a layer of polysilicon (*poly thickness*: 1500-3000 Å)
- Polysilicon is lithographically customised (in the most critical lithographical step of the process)
- The polysilicon is usually doped (N+) while deposited in order to reduce its resistivity
7 – P type diffusion

- Lithographic selection of the target areas
- Ion implant is carried out with a beam of boron ions
- The transistors are formed using poly as a mask that creates a gap between the implant of the drain and source areas:
  - Called self-aligned process
  - The poly of the P type transistors gets P type impurities over the N type received during deposition. The final type depends on the dominant doping.
8 – N type diffusion

- Lithographic selection of the target areas
- Ion implant is carried out with a beam of phosphorous ions
- The transistors are formed using *poly* as a mask that creates a gap between the implant of the drain and source areas:
  - *Called self-aligned process*
  - The *poly* of the N type transistors gets more N type impurities.
9 – Annealing

- After ion implant a cycle of *thermal annealing* is required
  - The crystalline structure is reorganized (after the damages caused by ion implant) and additional diffusion of implanted impurities takes place

- After this step the temperature must stay low in order to preserve the distribution of impurities

Silicon Wafer Processing – Details
The wafer surface is covered with SiO₂ using CVD (≈ 1µm, at low temperature)
A lithographical process is used to open slots in the previously deposited SiO₂ allowing access to the lower level electrical nodes (poly or diffusion)
Metal 1

- The wafer surface is covered with metal ($\approx 5000 \, \text{Å}$)
- A lithographical process is used to selectively remove the metal

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metal 1

metal 1 mask

n+  p+  n-well

p-type
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The wafer surface is covered again with SiO₂ using CVD (at low temperature, thickness ≈ 1µm)
A lithographical process is used to open slots in the SiO₂ in order to allow access to the metal 1 nodes (vias)
The wafer surface is covered with metal (2)
A lithographical process is used to selectively remove the metal
13 – Passivation

- The top protection of the circuit consists of:
  - $\text{SiO}_2$ and
  - $\text{Si}_3\text{N}_4$

- A lithographical process is used to open large slots in the passivation in order to allow access to the top metal nodes (pads)