A 12-bit, 35 MS/s, 0.38 mW SAR ADC with Digital Calibration

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***Abstract*—This paper presents a low power sub-radix-2 SAR ADC that uses digital calibration to correct static non-linearities of the converter created by mismatches in the DAC capacitors. The redundancy built in the DAC not only allows digital calibration, but also helps to reduce impacts of dynamic errors during the conversion. Instead of using only one comparator, this ADC uses four different comparator designs with different noise specifications to optimize power consumption. The IMCS switching scheme requires one less DAC capacitor while allowing the DAC to have a very low power consumption. The DAC size is further minimized by using a split-capacitor. The circuit was designed in a 130 nm technology. The converter was validated by simulation, achieving an estimated SNDR of 71.5 dB and a SFDR of 85.5 dB at 17.5 MS/s while consuming 380 µW and occupying an area of 0.04 mm^2. The estimated figure of merit (FoM) of the ADC is 11.2 fJ/step at 17.5 MS/s and 7.9 fJ/step at 35 MS/s.**

***Index Terms*—SAR ADC, redundancy, digital calibration, multiple comparators, IMCS, low power.**

I. Introduction

Electronic systems nowadays use some sort of digital data storage and processing. Digital systems are becoming faster and smaller as science and technology progress and this has led to a shift in the way signals are handled and processed. Although analog circuits continue to be used, much of the signal path in many systems is now implemented in the digital domain, creating a demand for data converters, which bridge the analog and digital domains.

The Successive-Approximation-Register (SAR) ADC is becoming a popular architecture for high-accuracy and high-speed applications. Being a switching intensive and free of precision amplification architecture allows it to benefit greatly from faster transistor speed of scaled CMOS technologies. The key linearity limiting factor in SAR ADCs is capacitor mismatch of the DAC caused by production process non-idealities. Laser trimming and precision layout techniques can be used to reduce these mismatches. Alternatively, SAR ADCs employing digital calibration to correct static non-linearities caused by DAC mismatches have been proposed recently [1]–[4], presenting very good dynamic performance with minimum area overhead, since the DAC can be sized to the kT/C limit.

A common characteristic of these reported ADCs is the usage of redundancy. A redundant ADC is one in which several output codes have an overlap with respect to the analog range of the input signal that they cover. This means that errors early in the conversion process can be absorbed in the redundant ranges of the later steps. In fact, redundancy is a key ingredient that makes digital calibration possible, since it allows some amount of mismatch in the DAC capacitors. If the amount of redundancy is correctly chosen, the linearity of the transfer function of the ADC can be recovered by learning the true bit weights built into the DAC.

A recent study suggested that the power consumption of SAR ADCs could be optimized by using multiple comparators instead of only one as in a typical implementation [5]. Since the differential voltage at the comparator input is reduced from the MSB to the LSB, a higher noise can be tolerated when resolving the MSB while a lower noise is desired when resolving the LSB. As the comparator input-referred noise variance is inversely proportional to its power consumption, using different comparator noise specifications in resolving each bit improves the overall power consumption of the ADC. In fact, a close to optimal performance is achieved with only two comparator designs for a 10-bit ADC while the comparator power is reduced by 40% [5].

This paper describes a 12-bit sub-radix-2 SAR ADC with perturbation-based digital calibration employing four different comparator designs to optimize power consumption. In a typical implementation, the comparator offset only introduces an offset in the transfer function of the converter. However, when multiple comparators are used, their different offset values generate non-linearity, reducing the dynamic performance of the ADC. To solve this problem, the offset of each comparator is calibrated. Power consumption is further optimized by using the IMCS switching scheme proposed in [6]. This switching scheme consumes 94% less energy compared to the conventional one and does not require the MSB DAC capacitor, reducing the DAC size. The ADC was implemented in a 130 nm process, fitting in an area of 260 × 155 µm^2. Simulation results show that the ADC consumes only 380 µW while sampling at 17.5 MS/s, having an estimated SNDR of 71.5 dB, which corresponds to an ENOB of 11.6 bit. After learning the bit weights, the sampling frequency can be doubled at the expense of twice the quantization and comparator noise power, losing 0.5 bit of ENOB.

The organization of this paper is as follows. Section II describes the architecture and implementation of the proposed

SAR ADC. Section III shows the simulation results. Finally, conclusions are given in Section IV.

II. ADC Architecture and Implementation

A. Redundancy

With limited on-chip bypass capacitance, reference voltage bouncing increases the DAC settling time in conventional binary search SAR ADCs. This happens especially when large DAC capacitors are used, either for good matching or to have low kT/C noise. An approach to alleviate this issue is to use redundancy in the conversion steps [1]. A redundant ADC is one in which several output codes have an overlap with respect to the analog range of the input signal that they cover. This means that errors early in the conversion process can be absorbed in the redundant ranges of the later steps, as demonstrated in Fig. 1. Thus, the DAC settling accuracy of the most MSB conversion steps can be relaxed. There are several ways of implementing redundancy in the ADC. The simplest one, which was the one used in this work, is to build it in the DAC by sizing the capacitors in a sub-binary way, leading to a sub-radix-2 approach. In a sub-radix-2 ADC more conversion steps are required to achieve a certain SNR due to the smaller sub-binary step sizes. For this reason, to achieve a 12-bit resolution 14 conversion steps are used and the DAC is sized with a radix of 1.86, which allows digital calibration to restore the static linearity of the converter in the presence of up to 5% mismatch standard deviation in the DAC capacitors.

B. Digital Calibration

If the amount of redundancy is correctly chosen, the linearity of the transfer function of the ADC can be recovered by learning the true bit weights built into the DAC. This SAR ADC uses the perturbation-based digital calibration algorithm described in [1]. The correct bit weights are obtained by performing two conversions on the sampled signal. In each of the conversions an offset is added with opposite polarity. This technique is called Offset Double Conversion (ODC). This offset or perturbation added in the analog domain shall have a small amplitude such that the dynamic range of the ADC is not significantly reduced. A block diagram showing the working principle of the ODC algorithm is presented in Fig. 2. If the correct bit weights (W) are known, the perturbation added in the analog domain ($+\Delta_a$ and $-\Delta_a$) can be subtracted in the digital domain, obtaining the result of the conversion d_{out}. However, if the correct bit weights are unknown, two different results (d_+ and d_-) would be obtained, depending on whether a positive or negative perturbation was applied to the sampled signal. The difference between these two results is the error, as expressed in (2), and the goal of the calibration algorithm is to minimize the square of this error. The result of the conversion d_{out} is obtained by averaging the d_+ and d_-, as expressed in (1).

$$d_{out} = \frac{d_+ + d_-}{2} = (D_+ + D_-)\cdot\frac{W}{2} = \sum_{i=0}^{N-1}\left(b_+^i + b_-^i\right)\frac{w^i}{2} \quad (1)$$

$$error = d_+ + d_- - 2\Delta_d = \sum_{i=0}^{N-1}\left(b_+^i + b_-^i\right)w^i - 2\Delta_d \quad (2)$$

The least-mean-square (LMS) algorithm is used to learn the bit weights. The LMS update equations are given by:

$$w^i[n+1] = w^i[n] - \mu_w error[n]\left(b_+^i[n] - b_-^i[n]\right) \quad (3)$$

$$\Delta_d[n+1] = \Delta_d[n] + \mu_\Delta error[n] \quad (4)$$

C. Multiple Comparators

One of the key differences between this SAR ADC implementation and a typical one is the usage of multiple comparators to optimize power consumption. In a typical SAR ADC, the input-referred noise of the comparator should be at least 4 to 6 times lower than one LSB voltage to ensure that the ADC performance will not be limited by the noise of the comparator [5]. Since the differential voltage at the comparator input is reduced from the MSB to the LSB, a higher noise can be tolerated when resolving the MSB while a lower noise is desired when resolving the LSB. As the comparator input-referred noise variance is inversely proportional to the comparator power consumption, it becomes obvious that using the same comparator noise for each bit cycle is not optimal. For a 10-bit ADC, close to optimal performance regarding power consumption is achieved with only two different comparator designs. Since this is a sub-radix-2 ADC with 14 conversion steps and targets a resolution of 12-bit, four different

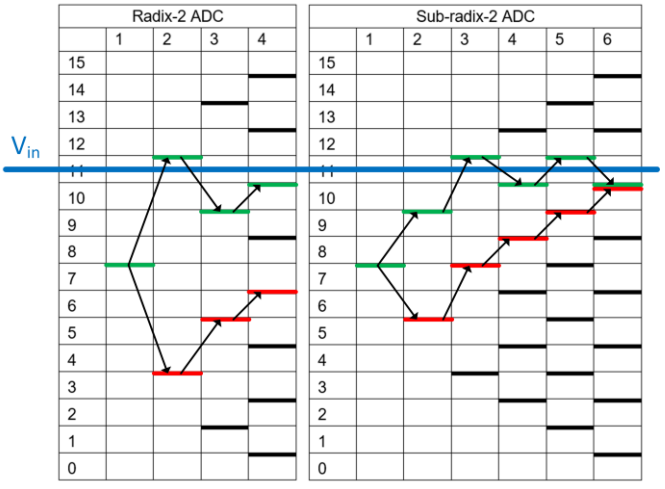

Fig. 1. Comparison of error resilience in a 4-bit radix-2 ADC and a 6 raw bit sub-radix-2 ADC. The thicker lines represent the decision levels. The green decision levels are the ones used in an errorless conversion and the red ones are used when an error is introduced in the determination of the first bit. In this case, the redundant ADC still has a correct output, whereas the radix-2 ADC is not able to recover.

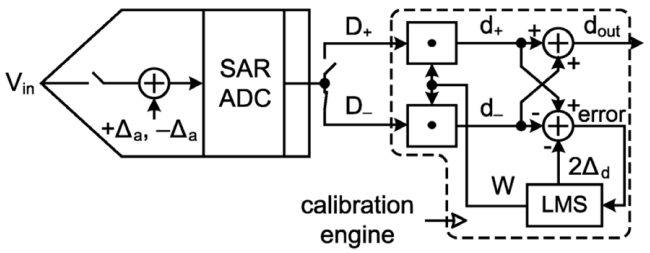

Fig. 2. Block diagram exemplifying the working principle of the ODC algorithm [1].

comparator designs were used with different noise and power specifications.

The StrongARM latch was the chosen topology. It has no static power consumption and its latching nature allows the ADC to operate without flip-flops, increasing its speed. In a typical SAR ADC, the comparator input offset voltage only introduces an offset in the transfer function of the converter. However, when multiple comparators are used, their different offset values generate non-linearity, reducing the dynamic performance of the ADC. The offset calibration circuit described in [7] was used with slight modifications. The schematic of the StrongARM latch is depicted in Fig. 3a and the schematic of the offset calibration circuit used in this work is depicted in Fig. 3b. A comparison is triggered when the *CLK* or *CAL* signals go high. If the *CLK* signal triggers a comparison, the *READY* signal goes high as soon as an output is available. The *CAL* signal is used to calibrate the offset of the comparator and should not change the state of the DAC switches. For this reason, the *READY* signal remains low if the comparison is triggered by the *CAL* signal. The capacitors C_{os+} and C_{os-} are discharged if the *RESET* is asserted or *CAL_EN* is low. To calibrate the offset of the comparator, a comparison is triggered through the *CAL* signal when an equal input voltage is present at V_{IN+} and V_{IN-}, i.e. during the sampling phase. When the *CAL* signal is low, charge is stored in the parasitic capacitances C_{par}. After *CAL* goes high and an output is available, the *CHARGE* signal goes low and one of the signals S_+ or S_- goes high, sharing charge between C_{par} and C_{os+}/C_{os-} and changing V_{os+}/V_{os-} to counteract the comparison result caused by the offset voltage. After a maximum of 1000 calibration cycles, the offset voltage of the comparator is calibrated.

Comparators 1 and 2 have the lowest input-referred noise value. The sizing of those comparators was done according to [8]. For comparators 3 and 4, minimum size transistors were used and the size of the input pair was tuned to achieve the noise goal. The noise of each comparator was obtained with a transient simulation with noise by calculating the probability of '1's for different differential input voltages and fitting these values to a cumulative distribution function (CDF) of a normal distribution. An example with the comparator 1 is depicted in Fig. 4. The characterization results for each comparator design is summarized in Table I.

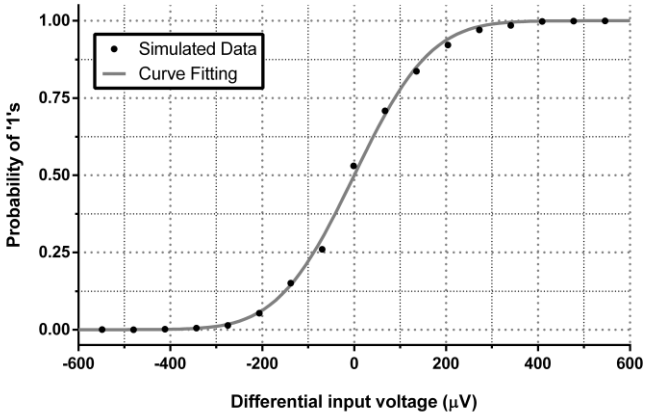

Fig. 4. Probability of '1's simulated at different differential input voltages for comparator 1 with fitted CDF.

TABLE I
CHARACTERIZATION PARAMETERS OF THE DESIGNED COMPARATORS

Parameter	Comp. 1	Comp. 2	Comp. 3	Comp. 4
Noise	126 μV	243 μV	368 μV	971 μV
Energy	496.7 fJ	118.9 fJ	70.3 fJ	60.7 fJ
Offset	4.5 mV	7.2 mV	12.0 mV	46.1 mV
Bit Allocation	0-1	2-4	5-7	8-13

D. Split-Capacitor DAC

In a SAR ADC typical implementation, the total capacity of the DAC increases exponentially with the resolution. To avoid this, a split-capacitor was used in this ADC, as shown in the single-ended DAC of Fig. 5. The split-capacitor divides the DAC in two sub-DACs, the MSB and the LSB DACs. As required by the IMCS switching scheme, the input signal is sampled into the bottom plate of each capacitor. During the sampling phase, the top plates should be connected to V_{CM}. The sampling ends when the top plate V_{CM} switches open. These switches should open first to inject a constant and signal-

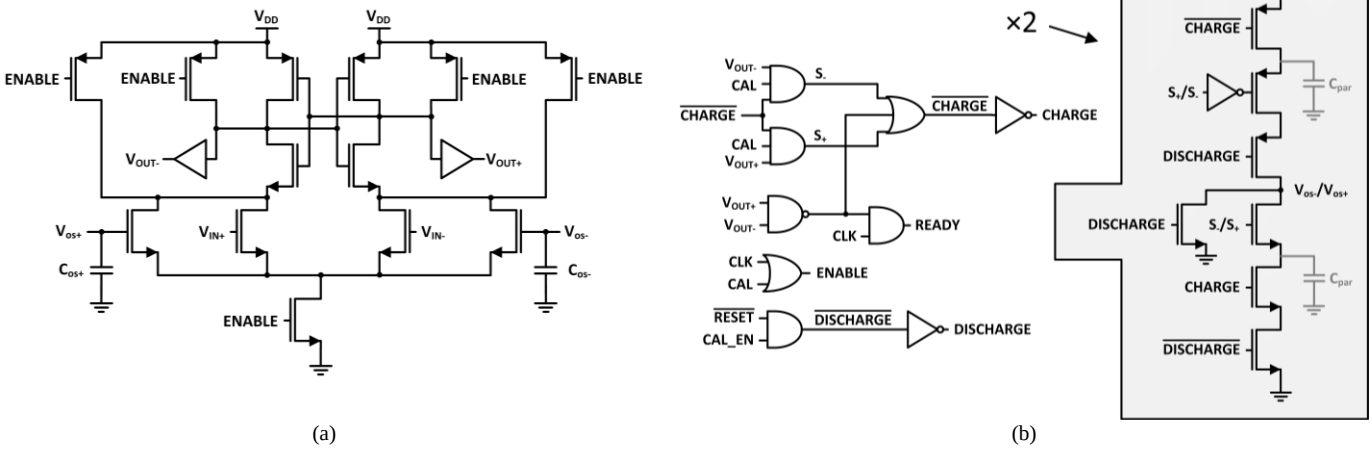

Fig. 3. (a) StrongARM latch schematic and (b) offset calibration circuit schematic.

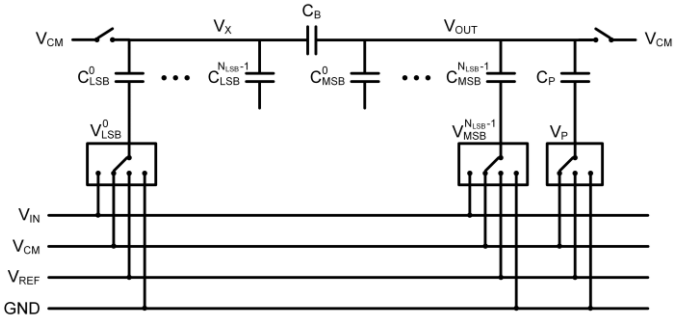

Fig. 5. Single-ended split-capacitor DAC with perturbation capacitor C_P in the MSB array.

independent charge into the DAC. The V_{IN} switches should open after the top plate V_{CM} switches. Since the top plates are floating, the non-linearly signal-dependent charge accumulated in the V_{IN} switches is not released into the DAC. This technique is known as "bottom-plate sampling". A perturbation capacitor C_P is used to apply the offset to the sampled signal as required by the ODC algorithm. The perturbation capacitor should be connected to V_{CM} during the sampling phase and to V_{REF} or GND during the conversion phase depending on the perturbation polarity. The conversion phase follows according to the IMCS switching scheme as described in [6]. Simple NMOS and PMOS were used to implement the GND and V_{REF} switches, respectively. The V_{IN} switches were implemented with bootstrapped NMOS transistors to achieve a signal-independent on-resistance and, consequently, a high linearity. The bootstrapping circuit is only instantiated twice, one for the positive DAC and one for the negative DAC. The bootstrapping capacitor was implemented using a MOSCAP to achieve a high capacitance value with a small area. For the V_{CM} switches, the same bootstrapping circuit was used to achieve a low on-resistance. The bootstrapping circuit was replicated for each switch, because they must turn off at different time instants.

For a differential split-capacitor DAC, the output voltage can be described as:

$$\begin{aligned} V_{OUT+} - V_{OUT-} = & \sum_{i=0}^{N_{LSB}-1} w_{LSB}^{i}\left(V_{LSB+}^{i} - V_{LSB-}^{i}\right) + \\ & + \sum_{i=0}^{N_{MSB}-1} w_{MSB}^{i}\left(V_{MSB+}^{i} - V_{MSB-}^{i}\right) + \\ & + w_P\left(V_{P+} - V_{P-}\right) - \left(V_{IN+} - V_{IN-}\right) \end{aligned} \tag{5}$$

The weights *w* can be defined as in (6)-(8) when C_P is placed in the MSB array:

$$w_{LSB}^{i} = \frac{C_{LSB}^{i} C_B}{C_B C_{LSB} + C_B C_{MSB} + C_{LSB} C_{MSB}} \tag{6}$$

$$w_{MSB}^{i} = \frac{C_{MSB}^{i}\left(C_B + C_{LSB}\right)}{C_B C_{LSB} + C_B C_{MSB} + C_{LSB} C_{MSB}} \tag{7}$$

$$w_P = \frac{C_P\left(C_B + C_{LSB}\right)}{C_B C_{LSB} + C_B C_{MSB} + C_{LSB} C_{MSB}} \tag{8}$$

For the case where C_P is placed in the LSB array, the weights *w* are defined as in (9)-(11):

$$w_{LSB}^{i} = \frac{C_{LSB}^{i} C_B}{C_B C_{LSB} + C_B C_{MSB} + C_{LSB} C_{MSB} + C_{MSB} C_P} \tag{9}$$

$$w_{MSB}^{i} = \frac{C_{MSB}^{i}\left(C_B + C_{LSB} + C_P\right)}{C_B C_{LSB} + C_B C_{MSB} + C_{LSB} C_{MSB} + C_{MSB} C_P} \tag{10}$$

$$w_P = \frac{C_P C_B}{C_B C_{LSB} + C_B C_{MSB} + C_{LSB} C_{MSB} + C_{MSB} C_P} \tag{11}$$

In this work, a unitary capacitance value of 60 fF was used. C_P was designed 16 times larger than the unit capacitance and was placed in the LSB array, resulting in a perturbation amplitude of 16 LSBs. The capacitors were sized to have a radix of 1.86 and to have the same unitary capacitance value in both sub-DACs. The used DAC capacitance values are summarized in Table II.

TABLE II
DAC CAPACITOR VALUES

i	C_{LSB}^{i} (fF)	C_{MSB}^{i} (fF)	C_B (fF)	C_P (fF)
0	60	60		
1	60	111.6		
2	111.6	207.6		
3	207.6	385.8	94.8	960
4	385.8	718.2		
5	718.2	1335.6		
6	1335.6	2484.6		

E. Asynchronous Operation

To have a higher sampling rate, an asynchronous operation is used. Each comparator outputs a *ready* signal as soon as a decision is available. The DAC is reconfigured after each bit is resolved. The next comparison is triggered by the *ready* signal of the previous comparator. To allow the DAC output to settle, a tunable delay of 140 to 400 ps is introduced to the *ready* signal of the previous comparator before it triggers the next comparison. The *ready* signal of the last comparator is used to indicate that a conversion has finished. The delay is achieved with a simple voltage-controlled current starved inverter. Fig. 6 shows the variation of the delay with the tuning voltage and Fig. 7 shows the waveforms of the *ready* and *enable* signals during one conversion.

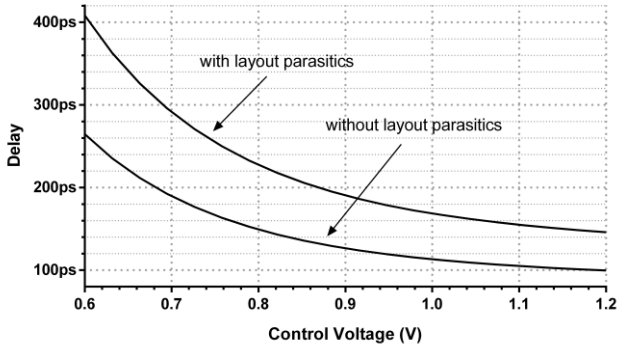

Fig. 6. Delay as a function of control voltage with and without layout parasitics, showing the increased delay due to the parasitic capacitances added by the layout.

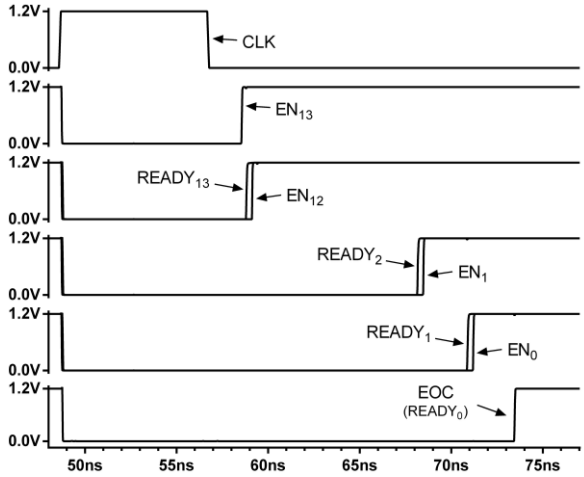

Fig. 7. Waveforms of *ready* and *enable* signals during one conversion.

F. Layout

The complete layout of the SAR ADC is depicted in Fig. 8. Since digital calibration is used to correct mismatch errors of the DAC capacitors, the layout is very straightforward and matching improvement techniques like "common centroid" were not used. The DAC is designed with MOM capacitors. Although they have worse matching compared to MIM capacitors, they do not require any special process option. The ADC occupies an area of 260 × 155 µm^2.

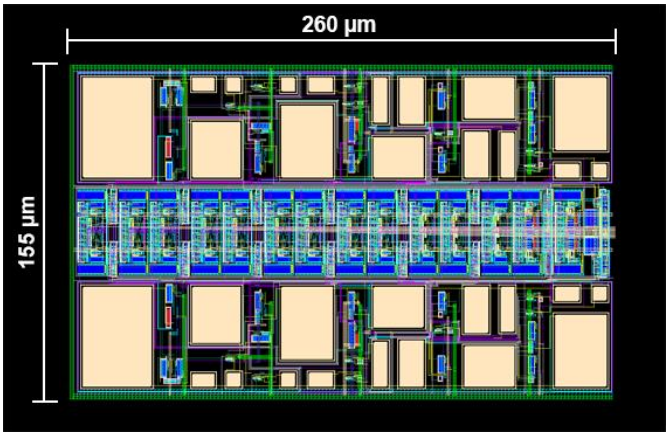

Fig. 8. SAR ADC layout.

III. Simulation Results

A high-level model of the ADC was built in MATLAB. This model was used to estimate the output noise of the ADC. This accelerated the simulations, since noise was not included. Table III shows the obtained noise values of the ADC. When ODC is enabled, two conversions are done for the same sampled signal. The averaging of the two conversions halves both the quantization noise power and the contribution of the comparators to the output noise power. However, the sampling noise is the same, since the two conversions are done with the same sampled signal. For this reason, when ODC is disabled the quantization noise power and the comparators equivalent output noise power doubles.

TABLE III
ADC NOISE BUDGET

	Sampling	Quantization	Comparators
ODC enabled	39.2 µV	63.5 µV	108.9 µV
ODC disabled	39.2 µV	89.8 µV	154.0 µV

To verify the effectiveness of the offset calibration and digital calibration of the DAC mismatches, a random 1 run Monte Carlo simulation was performed, including mismatch and process variations. Fig. 9 shows a 512 points FFT of the output signal before digital calibration. An input frequency of approximately 1.06 MHz and a clock frequency of 35 MHz were used, resulting in a 17.5 MHz sampling frequency with ODC enabled. A SNDR of 37.6 dB, corresponding to an ENOB of 6.0 bit, SFDR of 41.0 dB and THD of -38.7 dB were measured. After applying the digital calibration, the results depicted in Fig. 10 were obtained. A SNDR of 73.1 dB, ENOB of 11.9 bit, SFDR of 85.5 dB and THD of -80.4 dB were obtained, representing, respectively, an improvement of 35.5 dB, 5.9 bit, 44.5 dB and -41.7 dB compared to when digital calibration is not used. Regarding power consumption, an average power consumption of 380 µW was obtained. A power breakdown of the ADC is presented in Fig. 11. A SNDR of 71.5 dB is estimated with the noise values of Table III, equivalent to an ENOB of 11.6 bit. An ENOB of 11.1 bit is estimated when the ADC operates with frozen bit weights. In this thesis, a dedicated calibration circuit was not designed. However, Liu *et al.* [1] estimates an area of 0.03 mm^2 and a power consumption of 230 µW for the calibration circuit in a similar 130 nm CMOS process. Finally, a FoM as defined in (12) of 11.2 fJ/step at 17.5 MS/s and 7.9 fJ/step at 35 MS/s can be estimated having into account the estimated total power consumption and the estimated ENOB values.

$$FoM = \frac{Power}{f_s \times 2^{ENOB}} \tag{12}$$

IV. Conclusion

SAR ADCs have seen an increase in popularity because they benefit greatly from technology scaling. However, the DAC mismatches are still the linearity limiting factor of this topology. The SAR ADC described in this paper tackles this

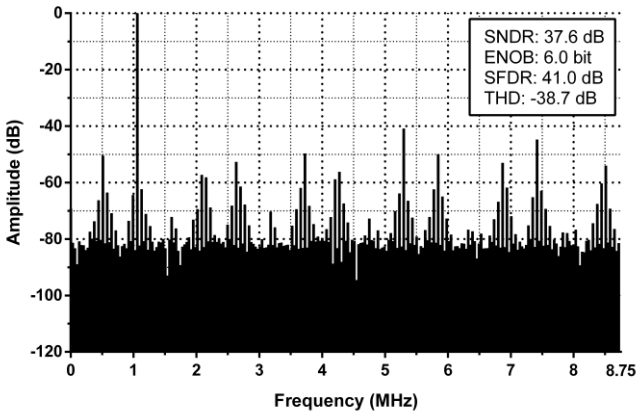

Fig. 9. Spectrum of the output of the ADC before digital calibration.

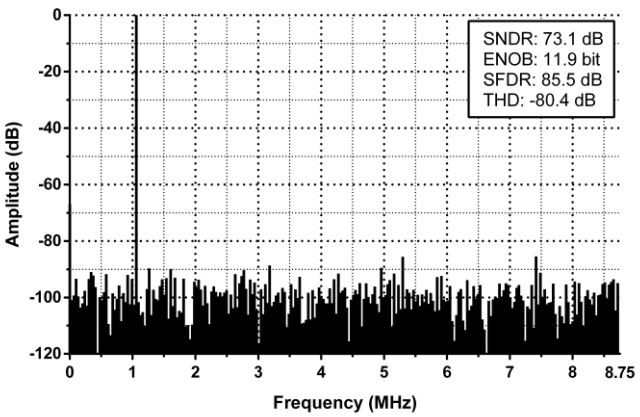

Fig. 10. Spectrum of the output of the ADC after digital calibration.

problem using digital calibration. With this technique, the bit weights built into the fabricated ADC are learned. To achieve this, the ODC algorithm was used. Several techniques were used to optimize the power consumption of the circuit, namely the usage of multiple comparators and the usage of the IMCS switching scheme, resulting in a low power ADC. The offset of each comparator was calibrated to avoid introducing non-linearities. A comparator offset calibration cycle can be triggered during the sampling phase without slowing down the ADC. The usage of a split-capacitor allowed the DAC to be small even with a significantly large unitary capacitance, minimizing the sampling noise. The unitary capacitance value can be further reduced, since there is enough room to increase the sampling noise with little ENOB loss, further reducing the power consumption and increasing the speed of the ADC.

The implemented SAR ADC achieves an estimated ENOB of 11.6 bit at a sampling rate of 17.5 MS/s, only dissipating 380 µW. After calibration, the ADC can achieve a sampling frequency of 35 MS/s with frozen bit weights, losing 0.5 bit of ENOB.

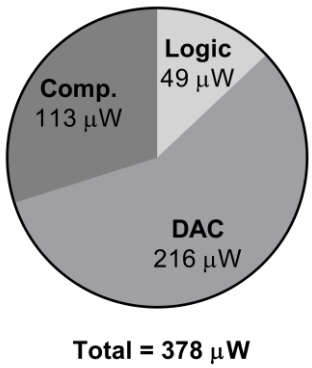

Fig. 11. ADC power breakdown.

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