DC-DC Converters for Organic Photovoltaic Cells

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***Abstract*—This paper describes the design of step-up DC-DC converters supplied by an organic photovoltaic cell. Three topologies were under study, namely a hard switch boost and two hybrid configurations, based on inductive and switched capacitors topologies. The MOSFET switches were driven by a Colpitts oscillator at 1,2 MHz, allowing the implementation of a completely autonomous conversion system, making way to the final PCBs, where output voltages higher than 1,2 V were obtained. Each prototype was designed with an area bellow 2,3 cm^2.**

I. Introduction

The functionalities of modern portable electronic systems are becoming increasingly complex, resulting in an increase in the processing capacity of the devices and, consequently, in a reduction of autonomy. The advancements in the field of wireless sensor networks implies that some of these applications demand long lifetime, which turns the use of conventional batteries a disavantadge, since they require regular human intervention. In this way, there is an increasing interest in using the available energy from the environment, commonly known as energy harvesting, allowing the supply of almost unlimited energy for the useful life of the devices [1]. The use of DC-DC converters is a solution used to increase the typically low voltage values of energy harvesting sources [2] to standard values.

The goal of this work is the design of a step-up DC-DC converter in Surface-Mount Technology (SMT), that can raise the voltage supplied by an organic photovoltaic cell, that is typically in the range of a few hundred milivolt, to a voltage above 1,2 V.

The paper is divided in six sections. Section II presents the state of the art of some systems already developed for low power energy harvesting applications. Section III presents the models used for the characterization of an organic photovoltaic cell. Section IV focuses on the implementation of the proposed converters, where the simulated and experimental results are shown and compared. An LC Copitts oscillator is also design in this section. Section V includes the results obtained from the prototypes. Finally, the conclusions are presented in section VI.

II. State of the art

The vast majority of switch-mode DC-DC converters are designed for medium/high power applications, with high conversion rates and with no limitation in the component count or system volume. Several architectures were already naturely tested and studied. The circuit proposed in [3] is based in a charge-pump topology, turning an input voltage of 0,6 V into an output voltage of 2 V, with a variable number of capacitors. Switching frequency is also variable and the circuit must be started by an external 2 V supply. In [4] a DC-DC converter composed of two different architectures is presented. In the first stage it is composed by two boost converters that raise the input voltage from 0,4 V to 0,8 V, wich is later converted to 2,4 V by a two-stage charge-pump converter. The project presented in [5] is a boost converter wich converts an input voltage of 20 mV into 5 V. Although the conversion coefficient is high, the circuit uses a transformer at the input in order to raise the input voltage to higher values to make the operation of the circuit possible. The DC-DC converter presented in [6] includes an integrated Maximum Power Point Tracking (MPPT), allowing the maximization of the power extracted from the OPV. The work presented in [7] resorts to the use of an energy storage system (super capacitor), to store energy that is collected in excess during the day, supplying it to the load when it is not possible to achieve desired and sufficient levels of collected energy.

III. Organic Photovoltaic Cell Model

Solar cells can convert directly solar energy into electrical energy. These can be represented for two distinct cases, with and without solar irradiation [8].

Figure 1 shows the equivalent circuit of an OPV without solar irradiation.

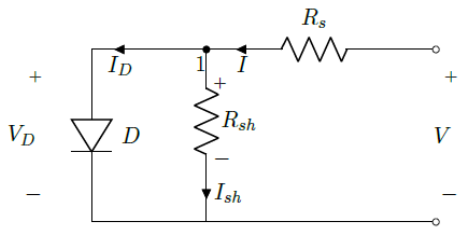


Fig. 1: Equivalent circuit of an OPV without solar irradiation.

The I(V) characteristic equation of an OPV without irradiation is given by:

$$I = I_S \left(e^{\frac{V - IR_S}{nV_T}} - 1 \right) + \frac{V - IR_s}{R_{sh}} \tag{1}$$

Where I is the output current, I_S is the reverse saturation current, n is the diode ideality factor, V_T is the thermal voltage, and R_s and R_{sh} are the parasitic series and shunt resistances.

Figure 2 shows the equivalent circuit of an OPV with solar irradiation.

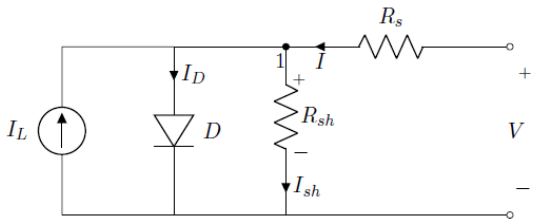


Fig. 2: Equivalent circuit of a OPV with solar irradiation.

The I(V) characteristic equation of an OPV with irradiation is given by:

$$I = I_S \left(e^{\frac{V - IR_S}{nV_T}} - 1 \right) + \frac{V - IR_s}{R_{sh}} - I_L \qquad (2)$$

Where I_L is the photocurrent.

The organic cells used in this work were fabricated in glass substrates, with two different cells per substrate. Figure 3 shows two pixels (P_1 e P_2) implemented in the referred glass substrate, each corresponding to a different cell.

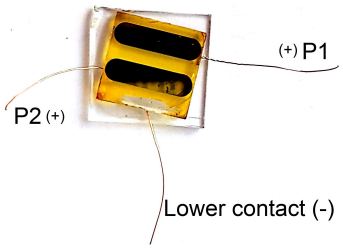


Fig. 3: Two organic photovoltaic cells.

Each substrate contains two upper aluminum contacts and one lower tin contact, the lower electrode, which is common to both pixels.

Table I shows the electrical parameters of the OPVs, obtained from simulation comparison with the I(V) characteristics of eight cells.

TABLE I: OPV's Electrical Parameters

I_{sc} (mA)	n (ideality factor)	R_s (Ω)	R_{sh} (kΩ)	I_S (nA)
1	3,88	49,5	2,5	64

IV. Proposed Topologies

In this section a detailed description of the three topologies implemented will be presented. The design of the circuits was based on an input voltage of 0,4 V and an output voltage of 2,6 V. Preliminary experimental results were obtained with an external oscillator.

A. Boost converter with switched capacitors at the output

The first topology, shown in figure 4, is a boost converter with switched capacitors at the output. The operating principle of this circuit is based on the charge and discharge of the inductor and switched capacitors [9].

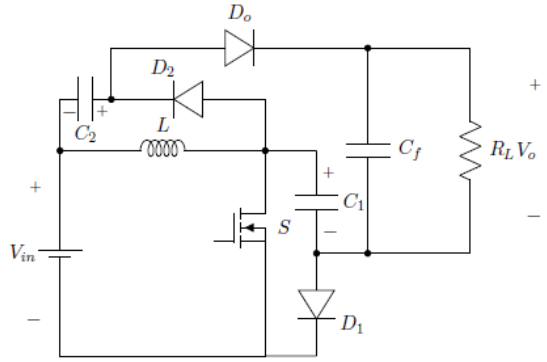
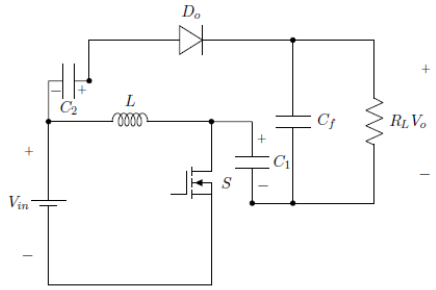
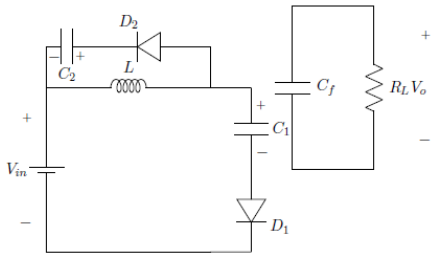


Fig. 4: Boost converter with switched capacitors at the output.

This circuit has two stages of operation, as can be depicted in figure 5.



(a) Stage 1, Switch (S) in ON.



(b) Stage 2, Switch (S) in OFF.

Fig. 5: Operation stages of boost converter with switched capacitors at the output topology.

In stage 1, when switch S is ON, the inductor starts charging by the current of the voltage source and the capacitors C_1 and C_2 supply the load. At this time diodes D_1 and D_2 are OFF.

In stage 2 switch S is OFF and the inductor stars discharging. The energy from the inductor charges the capacitors C_1 and C_2. In this stage the load is supplied by the filter capacitor C_f.

The input/output voltage ratio can be expressed as,

$$V_o = \frac{2V_{in}}{1-D} \tag{3}$$

where D is the switch duty cycle.

The current ripple in the inductor can be expressed as

$$\Delta i_L = \frac{V_o(1-D)DT}{L} \tag{4}$$

where, L is the inductor value and T is the time in μs.

The voltage ripple of capacitors C_1 and C_2 is given by

$$\Delta V_{C_n} = \frac{I_o T}{C_n} \tag{5}$$

where I_o is the output current and n the number of capacitor, 1 or 2.

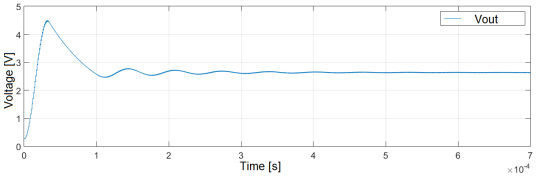
The filter capacitor C_f was obtained from simulation in order to eliminate the ripple of output voltage. The capacitor has a value of 4,8 nF.

The values calculated from the above analysis can be observed in Table II.

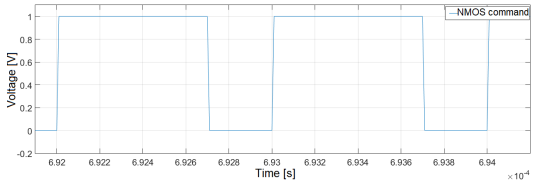
TABLE II: Specifications for the boost converter with switched capacitors at the output topology.

Components	Values
Inductor (L)	250 μH
Capacitor (C_1 and C_2)	9,62 nF
Filter Capacitor (C_f)	4,8 nF
Switching frequency (f_s)	1 MHz
Duty cycle (D)	70 %
Load resistance (R_L)	10 kΩ

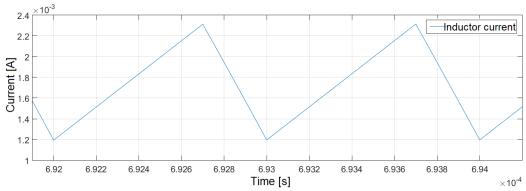
1) Simulated results: The simulated waveforms are shown in figure 6. It has been observed that the value obtained for the output voltage in steady state is 2,62 V. It is possible to observe that when the NMOS transistor is ON, the value of the inductor current increases, it is charged by the current from the voltage source. When the NMOS transistor cuts-off, the current value decreases, with the discharge of the stored energy occurring, to charge C_1 and C_2. Trough figure 6(c) it is possible verify that the current in the inductor is always above to zero, which means that the converter is in continuous-conduction mode (CCM).



(a) Output voltage.



(b) NMOS transistor command.



(c) Inductor current.

Fig. 6: Waveforms obtained by simulation.

2) Experimental results: Figure 7 shows the output voltage obtained experimentally. The achieved voltage is 1,75 V. The difference compared to the value obtained by simulation is due to the non-idealities of the components of the circuit, especially the voltage drop across the diodes.

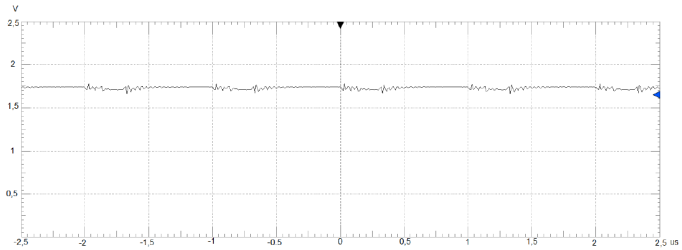


Fig. 7: Output Voltage.

The change in output voltage with respect to duty cycle is shown in figure 8. It is observed that the output voltage increases for a maximum duty cycle around 80%.

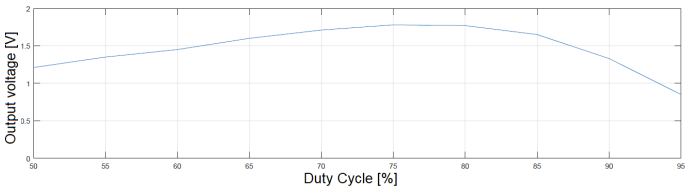


Fig. 8: Output Voltage vs Duty Cycle.

Figure 9 shows the variation of the output voltage versus the increase of the switching frequency, where it is possible

to observe that the output voltage decreases with the increase of the switching frequency, due to an increase in switching losses.

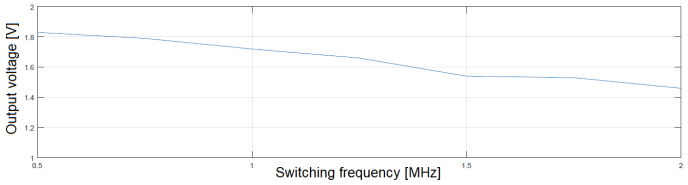


Fig. 9: Output Voltage vs Switching frequency.

Since the converter is designed to be supplied by an OPV, it is fundamental to simulate the possible variations of the supply voltage. Figure 10 shows that the circuit guarantees a minimum voltage of 1,2 V for the entire input voltage range and 2,4 V for a range of input voltages from 0,7 V to 1 V.

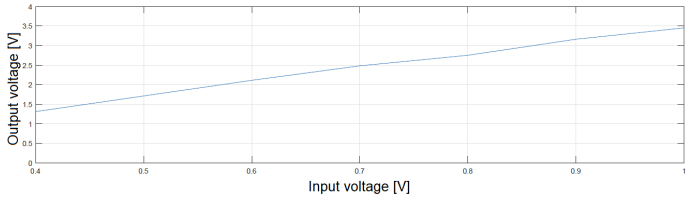


Fig. 10: Output voltage vs Input voltage.

B. Boost converter

The second topology is the classical hard-switching boost converter [10], as shown in figure 11. This circuit has two stages of operation defined by the state of the transistor, $0 < t < t_{on}$ and $t_{on} < t < T$.

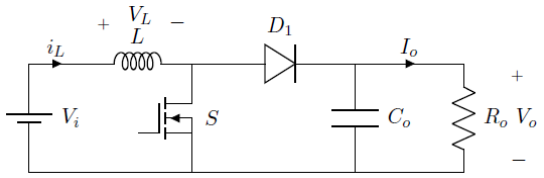


Fig. 11: Boost converter.

Stage 1, $0 < t < t_{on}$: In this stage the transistor is ON and the input voltage is across the inductor, leading to a linear ramp up of i_L, and increasing the energy in the inductor.

Stage 2, $t_{on} < t < T$: In the second stage the transistor is OFF forcing the inductor current to flow trough the diode. The stored energy in the inductor is transferred to the output that consists of the filter capacitor and the output load.

The relation between input voltage and output voltage, is given by,

$$V_o = \frac{1}{1-D} \times V_i \tag{6}$$

The average current delivered to the load can be written as,

$$I_o = \frac{V_o}{R_o} = \frac{1}{1-D} \times \frac{V_i}{R_o} \tag{7}$$

The peak-peak value of the ripple in the inductor can be calculated by using the expression,

$$\Delta i_L = \frac{1}{L}(V_o - V_{in})(1-D)T \tag{8}$$

The value of the filter capacitor can be calculated by the following expression,

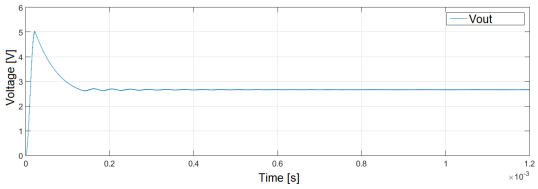
$$C_o = \frac{V_i DT}{\Delta V_o (1-D) R_o} \tag{9}$$

The values calculated from the above analysis can be observed in table III.

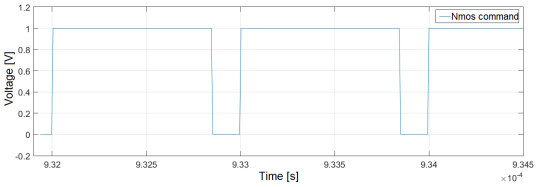
TABLE III: Specifications for the boost converter topology.

Components	Values
Inductor (L)	150 μH
Filter Capacitor (C_f)	8.2 nF
Switching frequency (f_s)	1 MHz
Duty cycle (D)	85 %
Load resistance (R_L)	10 kΩ

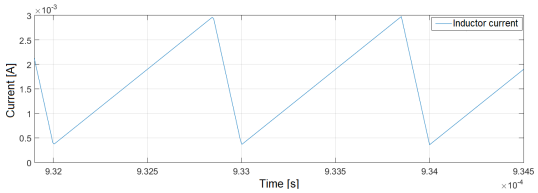
1) Simulated results: The simulated waveforms for this topology are shown in figure 12.



(a) Output voltage.



(b) NMOS transistor command.



(c) Inductor current.

Fig. 12: Waveforms obtained by simulation.

It can be seen that an output voltage of 2,67 V has been obtained. Similar to the first topology, it is possible to observe that when the NMOS transistor is ON, the value of the inductor current increases. When the NMOS transistor cuts-off, the current in the inductor decreases flowing to the load. It is also possible verify that the converter are in CCM, once the current is always $i_L > 0$.

2) Experimental results: The output voltage obtained experimentally can be seen in figure 13. It is possible to verify that the achieved voltage is 2,4 V. This value is very close to the value obtained by simulation, with a small difference of 270mV.

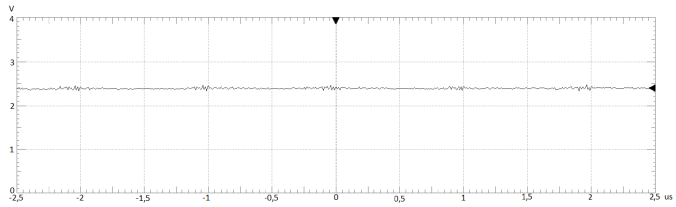


Fig. 13: Output Voltage.

The change in output voltage with respect to duty cycle is shown in figure 14. Similar to the previous topology, it is possible to observe that with the increase of the duty cycle, the output voltage also increase, which was expected. A decrease in the value of the output voltage is observed for a high value of duty cycle, in this case 95 %. This is directly related to the existence of losses in the switching of the active elements of the circuit.

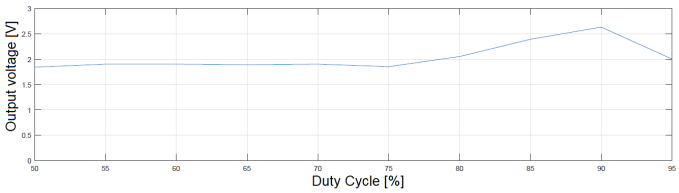


Fig. 14: Output Voltage vs Duty Cycle.

Figure 15 shows the variation of the output voltage versus the increase of the switching frequency, where is it possible to observe that the output voltage decreases with the increase of the switching frequency. This fact is related with the difficulty of the transistor to switch to such high frequencies due to the intrinsic capacities.

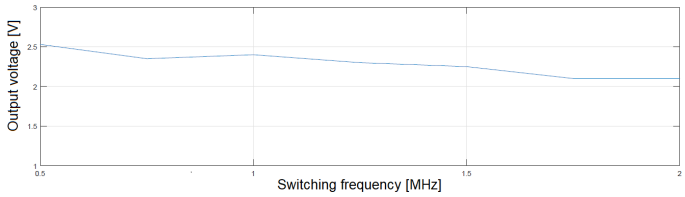


Fig. 15: Output Voltage vs Switching frequency.

Trough figure 16 it is possible to verify that this circuit guarantees a minimum voltage of 1,2 V for the entire input voltage range and 2,4 V for a range of input voltages from 0,5 V to 1 V.

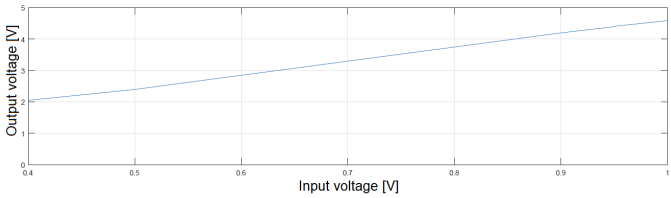


Fig. 16: Output voltage vs Input voltage.

C. Multilevel boost converter

Figure 17 depicts the third proposed topology, the multilevel boost converter. This converter combines the boost converter and a switched charge-pump type circuit. This circuit is composed by one inductor, one transistor, 2N-1 diodes and 2N-1 capacitors, where N represents the number of levels.

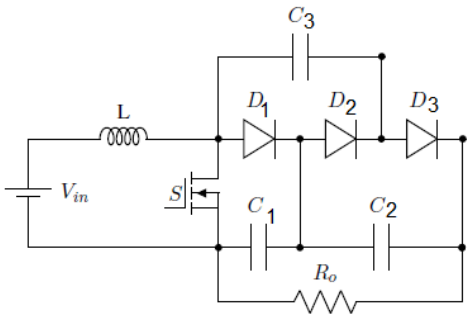


Fig. 17: Multilevel boost converter.

Based on [11], this circuit comprises two stages of operation. During the first stage, the switch is ON and the inductor is connected to V_{in}. If the voltage across the capacitor C_3 is smaller than C_1 then the capacitor C_3 clamps C_1's voltage trough the D_2 and the switch S. During the second stage, when the switch turns OFF, the inductor current turns ON the diode D_1 charging C_1. When D_1 is OFF, the voltage across the capacitor C_3 and the voltage V_{in} plus the voltage across the inductor clamps the voltage across C_2 and C_1 trough diode D_3.

The equation that shows the voltage gain of the circuit is almost identical to the boost converter, with the difference that the number of levels used is multiplied to this gain.

$$V_o = N \times V_C = \frac{N \times Vin}{1 - D} \tag{10}$$

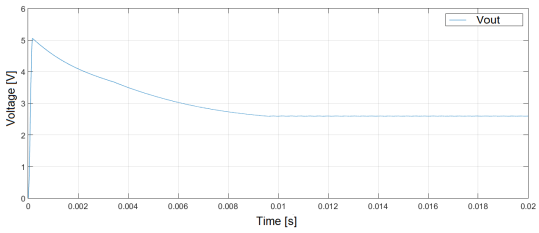
The output voltage can also be expressed as a function of the number os levels and the voltage to the terminals of each capacitor. This is only possible if all the capacitors have the same value.

The values calculated for this topology are summarized in table IV.

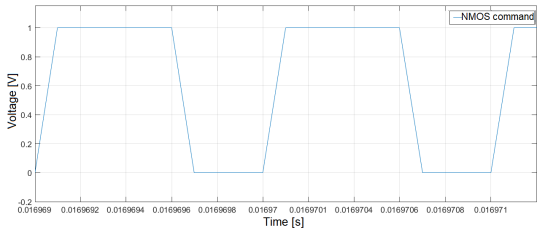
TABLE IV: Specifications for the multilevel boost topology.

Components	Values
Inductor (L)	150 μH
Capacitors (C_1, C_2 and C_3)	1 μF
Switching frequency (f_s)	1 MHz
Duty cycle (D)	70 %
Load resistance (R_L)	10 kΩ

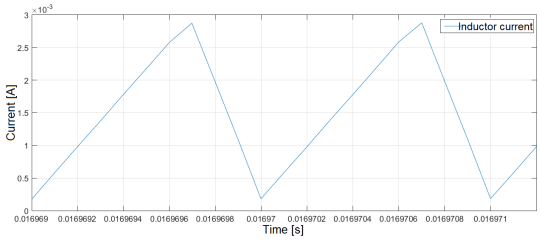
1) Simulated results: The simulated waveforms are shown in figure 18. It has been observed that the value obtained for the output voltage in steady state is 2,66 V. It is possible to observe that when the NMOS transistor is ON, the value of the inductor current increases, charged by the voltage source. When the NMOS transistor cuts-off, the current value decreases, with the discharge of the stored energy in the inductor. Similar to the previous converters it is also possible to verify that the converter is in CCM.



(a) Output voltage.



(b) NMOS transistor command.



(c) Inductor current.

Fig. 18: Waveforms obtained by simulation.

2) Experimental results: The output voltage obtained experimentally can be seen in figure 19. From the experimental results, it has been observed that the converter can reach an output voltage of 2,1 V. It is observed that there is a 0,55 V difference from simulation. This difference is due to the non-idealities of the components of the circuit, namely the voltage drop across each diode.

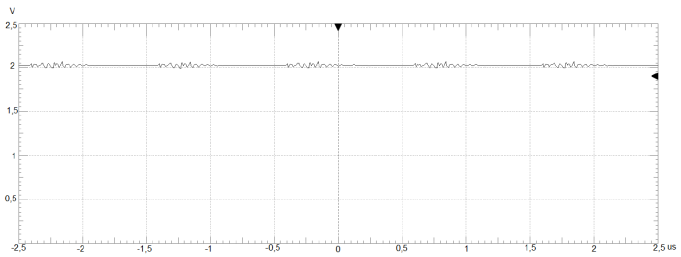


Fig. 19: Output Voltage.

The change in output voltage with the respect to duty cycle is shown in figure 20. It is observed that the output voltage increases as the duty cycle increases, until a maximum of 90 %. Once again, the decrease above 90 % is related to excessive switching losses in the active elements of the circuit.

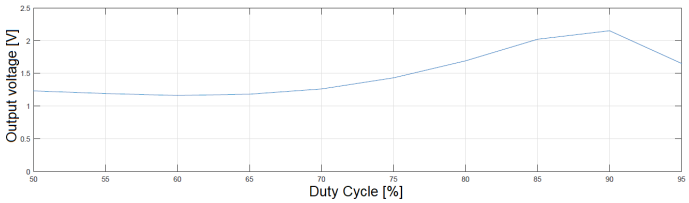


Fig. 20: Output Voltage vs Duty Cycle.

Figure 21 shows the change in the output voltage with respect to the switching frequency. Similar to the previous circuits, it is possible to observe that the output voltage decreases with the increase of switching frequency, once again related with the difficulty of the transistor to switch to such high frequencies.

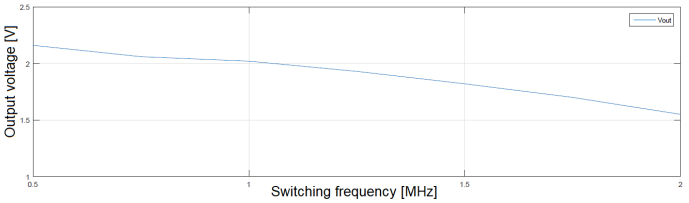


Fig. 21: Output Voltage vs Switching frequency.

Trough figure 22 it is possible to verify that the circuit guarantees a minimum voltage of 1,2 V for the entire input voltage range and 2,4 V from an input voltage above 0,6 V.

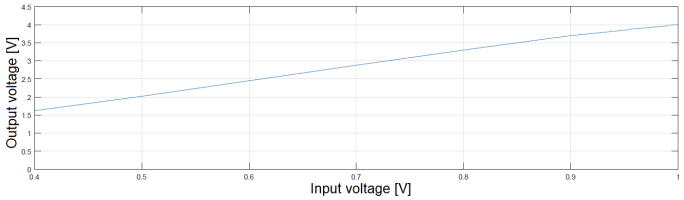
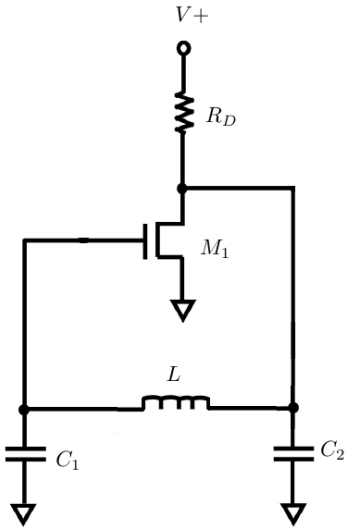


Fig. 22: Output voltage vs Input voltage.

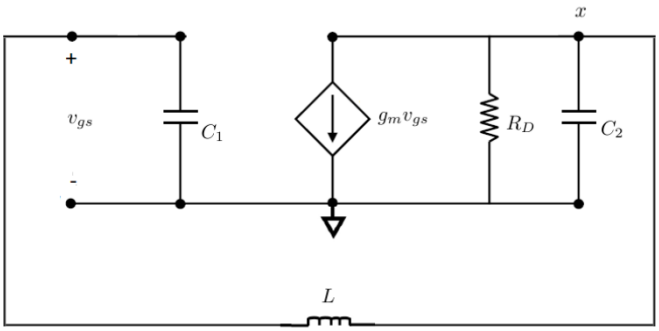
D. LC Colpitts Oscillator

The implementation of an internal oscillator allows the realization of one of the main objectives of this work: to create

a completely autonomous converter system, which does not depend on an external oscillator to drive the switches. An LC Colpitts oscillator was studied and designed, which can be seen in figure 23(a). To determinate the oscillation frequency for the Colpitts oscillator, the transistor was replaced by the equivalent circuit, as shown in figure 23(b).



(a) LC Colpitts Oscillator.



(b) Equivalent circuit of the Colpitts oscillator.

Fig. 23: LC Colpitts oscillator and the equivalent circuit.

From the analysis of the circuit, a characteristic equation of the circuit in figure 23(b) is given by,

$$sC_1v_{gs} + g_m v_{gs} + (\frac{1}{R_D} + sC_2)(1 + s^2LC_1)v_{gs} = 0 \quad (11)$$

Assuming the oscillations have begun, $V_{gs} \neq 0$, can be eliminated, and the equation can be rearranged in the form,

$$s^3LC_1C_2 + s^2(\frac{LC_1}{R_D}) + s(C_1 + C_2) + (g_m + \frac{1}{R_D}) = 0 \quad (12)$$

Substituting $s = j\omega$ and rearranging the real and imaginary terms lead to,

$$(g_m + \frac{1}{R_D} - \frac{\omega^2 LC_1}{R_D}) + j[\omega(C_2 + C_1) - \omega^3 LC_1C_2] = 0 \quad (13)$$

To maintain oscillation both real and imaginary terms of (13) must become zero. The oscillation frequency can then be derived from the imaginary part of (13),

$$f_0 = \frac{1}{2\pi\sqrt{L(\frac{C_1C_2}{C_1+C_2})}} \quad (14)$$

and the amplifier condition to sustain oscillation is derived from equating the real part to zero, at the oscillation frequency (14),

$$\frac{C_1}{C_2} = g_m R_D \quad (15)$$

Initially, the loop gain must be made greater than unity, so the following inequality must be satisfied,

$$g_m R_D > \frac{C_1}{C_2} \quad (16)$$

The value of the components are summarized in table V, for an oscillation frequency of 1 MHz.

TABLE V: Specifications for the Colpitts Oscillator.

Components	Values
Inductor (L)	470 μH
Capacitor (C_1)	10 pF
Capacitor (C_2)	47 pF
Resistor (R_D)	1,2 kΩ

1) Simulation results: For the simulation of the circuit the value of the components mentioned in table V were used, supplied at 0,5 V. The simulated waveform is shown in figure 24.

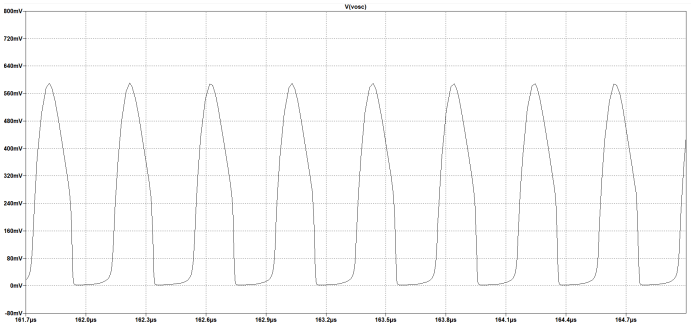


Fig. 24: Waveform of the simulated results.

It can be seen from the analysis of figure 24 that a waveform with a duty cycle of approximately 53 % and an oscillation frequency of 2,48 MHz was obtained.

2) Experimental results: Once the circuit functionality was verified, it was evaluated through the experimental implementation using a test PCB.

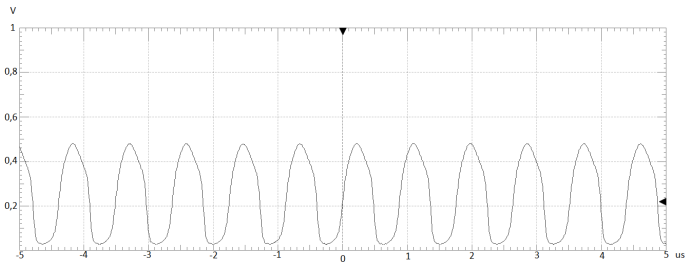


Fig. 25: Waveform of the experimental results.

The waveform obtained can be seen in figure 25, which contain a duty cycle of 53 % and an oscillation frequency of 1,2 MHz.

The difference in the value of the oscillation frequency obtained experimentally is essentially due to the MOSFET parasitic capacities, which were not contemplated in calculations and simulation.

Observing the circuit represented in figure 23(a), it can be seen that the parasitic input and output capacitances of the MOSFET are in parallel with capacitors C_1 and C_2. This addition of the parasitic capacitances of the transistor leads to the significant change in the oscillation frequency.

Although the duty cycle is very low (53 %), an oscillator for a very low supply voltage was implemented. The low number of components is also a determining factor that contributes to the objective of this work, where the resultant implantation area is critical.

V. Experimental Implementation and Results Analysis

This section shows the experimental results obtained for the three prototypes, externally supplied by a DC voltage source and by the OPV, to validate the operation of the complete conversion system.

A. Experimental tests using an external voltage source

The conversion circuits were tested considering a range of input voltages between 0,2 V and 1 V with a fixed duty cycle of 53 % and a switching frequency of 1,14 MHz.

1) Boost converter with switched capacitors at the output: The PCB resulting from the first topology is shown in figure 26. The prototype under analysis has an area of 2,28 cm^2. Through the analysis of figure 27 it can be seen that the minimum desired voltage of 1,2 V can be reached at the output with 0,65 V at the input, in case of a 10 kΩ load. In the case where the load is higher, 100 kΩ, it was possible to reach a voltage of 2,4 V with an input voltage of 0,75 V. In open circuit, an output voltage of 1,2 V is reached for an input of 0,45 V and 2,4 V for 0,65 V at the input.

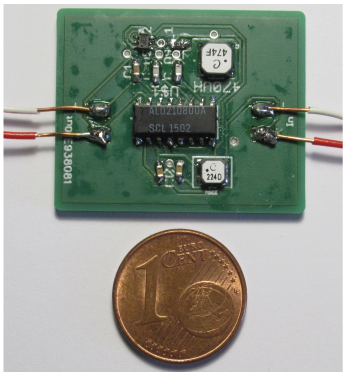


Fig. 26: PCB of the Boost converter with switched capacitors at the output.

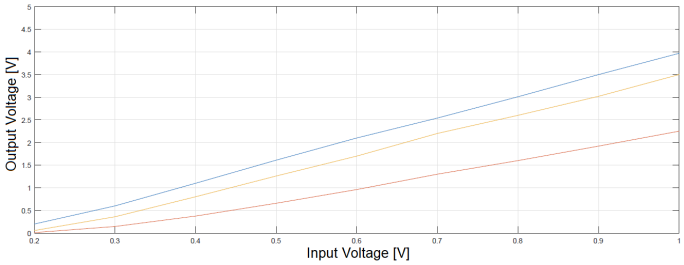


Fig. 27: Output voltage for a range of input voltages between 0,2 V and 1 V with a load of 10 kΩ (red), 100 kΩ (yellow) and without load (blue).

2) Boost converter: The PCB resulting from the second topology is shown in figure 30. The circuit under analysis has an area of 2,15 cm^2. The analysis of figure 29 shows that it is possible to reach the desired minimum output voltage of 1,2 V with an input voltage of 0,65 V, which are values similar to those obtained with the previous topology, for the case of a 10 kΩ load. In the case where the load is higher, 100 kΩ, is possible to reach an output voltage of 2,4 V with an input voltage of 0,6 V. For the case with no load, an output voltage of 2,4 V can be obtained for 0,45 V at the input.

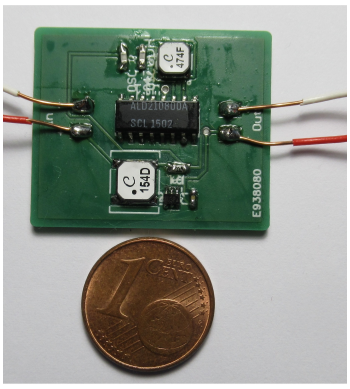


Fig. 28: PCB of the Boost converter.

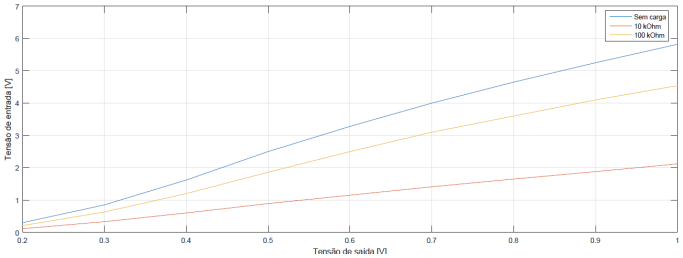


Fig. 29: Output voltage for a range of input voltages between 0,2 V and 1 V with a load of 10 kΩ (red), 100 kΩ (yellow) and without load (blue).

3) Multilevel Boost converter: The PCB resulting from the multilevel boost topology is shown in figure 32. The circuit under analysis has an area of 2,17 cm^2.

Figure 31 shows a similar performance relative to the previous converters. It is emphasized that it is possible to achieve the same output voltages with lower input voltages. The minimum output voltage of 1,2 V with an input voltage of 0,65 V can be reach with a load of 10 kΩ and it is possible to obtain 1,2 V at the output with an input voltage of 0,35 V with a load of 100 kΩ.

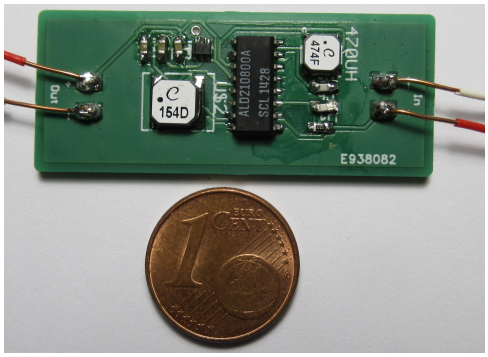


Fig. 30: PCB of the Multilevel converter.

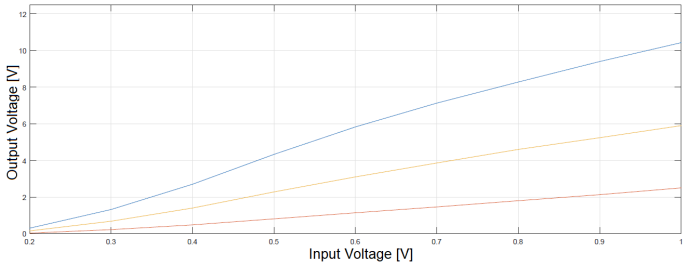
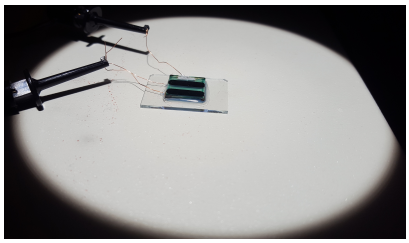


Fig. 31: Output voltage for a range of input voltages between 0,2 V and 1 V with a load of 10 kΩ (red), 100 kΩ (yellow) and without load (blue).

B. Experimental tests powered by the Organic Photovoltaic Cell

To perform the tests of the circuits with the OPV as the power supply the experimental setup-up can be observed in figure 32(a). The OPV under irradiation can also be observed in figure 32(b).

(a) Solar Simulator.



(b) OPV under test.

Fig. 32: Solar simulator and OPV.

In figure 33 it is possible to observe the waveform generated by the Coplitts oscillator that is part of the conversion system. The duty cycle of the waveform is approximately 53 % and the switching frequency is 1,2 MHz. The signal amplitude is the same as the input voltage, which in this case is provided by the OPV, 0,63 V.

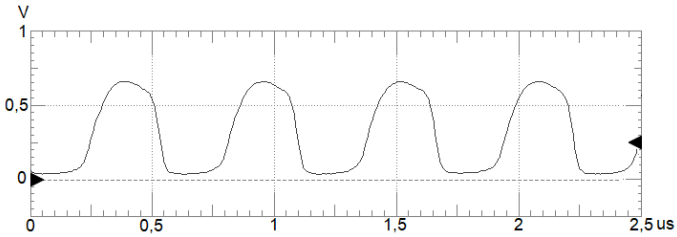
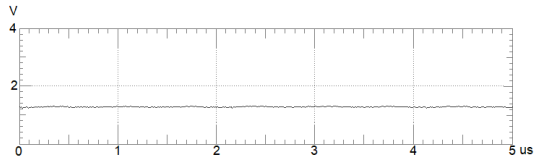
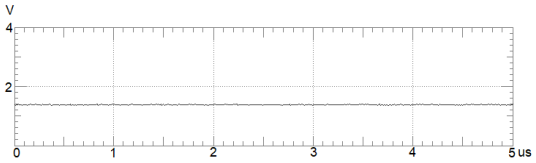


Fig. 33: Waveform generated by the Colpitts oscillator.

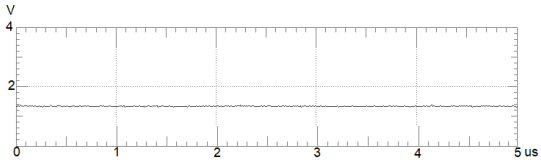
The time diagrams of the output voltage of the three conversion systems can be seen in figures 34(a), 34(b) and 34(c). These graphs were obtained with an input voltage of 0,63 V supplied by the OPV, with a load of 10 kΩ at the output.



(a) Boost converter with switched capacitors at the output



(b) Boost converter.



(c) Multilevel boost converter.

Fig. 34: Temporal diagrams of the output voltage of the three conversion systems.

It can be concluded from figure 34 that the circuits have a similar behavior with respect to the value of the output voltage. In both cases the required minimum output voltage of 1,2 V was reached.

1) Comparative analysis of the three conversion topologies: The results obtained for the three circuits are represented in table VI. These results allow a comparative analysis between the designed conversion systems.

TABLE VI: Experimental results.

Topology	Parameters							
	V_{in} [V]	V_{out} [V] Load [kΩ]			Switching frequency [MHz]	Duty cycle [%]	Area [cm^2]	Component cout
		10	100	Without load				
(1)	0,65	1,295	1,93	2,87	1,2	53 %	2,28	10
(2)		1,396	2,7	4,2			2,15	8
(3)		1,356	3,43	7,394			2,17	10

The analysis of table VI shows that all circuits reach the required minimum voltage of 1,2 V with a load of 10 kΩ. This value can be increased if a higher load is used. In relation to the duty cycle and the switching frequency, both circuits have the same values, reaching a switching frequency of 1,2 MHz and a duty cycle of 53 %. The areas of the three prototypes are slightly larger than 2 cm^2, with a minimum component count of 10.

VI. Conclusions

Three prototypes of a discrete solution for an OPV step-up voltage conversion system, resorting only to COTS low profile SMC, were designed and tested. The designed prototypes include a step-up DC-DC conversion topology, togheter with a Colpitts oscillator to drive the MOSFET switches. The design of the converters allowed to achieve the objectives proposed in this work, since it is possible to reach the required minimum standard voltage of 1,2 V for a load above 10 kΩ. The main constraint of the designed systems was the reduced duty cycle of the oscillator (< 53 %), which limited the DC-DC conversion gain.

It is important to note that a Colpitts oscillator has been achieved for very low values of supply voltage, operating at voltages in the order of 300 mV. The low component count (<10) and the required prototyping area slightly below 2,3 cm^2 must also be emphasized.

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