Integrated Eddy Current based Non-destructive Testing System for High-end Applications

A Capacitively Coupled Chopper Instrumentation Amplifier

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***Abstract*—This work focuses an Eddy Current (EC) Non-Destructive Testing (NDT) system that uses Magneto-Resistive (MR) sensors to inspect metallic test subjects. Low-frequency magnetic signals are used for higher penetration depths, resulting in low-frequency signals that are processed by an Application Specific Integrated Circuit (ASIC). The ASIC has a pre-amplifier that presents a very significant flicker noise, that impairs measurements. The pre-amplifier is the focus of this work and is the target of improvements, such as the implementation of Chopper Stabilization to reduce flicker noise.**

The pre-amplifier is configured in a Capacitively Coupled Chopper Amplifier topology and due to chopper modulators, the input DC components are up-modulated and pass through the input capacitors of the amplifier capacitive feedback. These DC components cause the saturation of the amplifier. A DC Servo Loop (DSL) is added to cancel input DC by means of negative feedback.

The pre-amplifier was designed in AMS 0.35 μm CMOS technology and has a simulated gain of 20 dB, presenting an Input-Referred Noise (IRN) of 6 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 100 Hz and noise floor of 4 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The pre-amplifier also presents an attenuation of 60 dB of DC signals, allowing the removal of DC components up to 200 mV.

***Index Terms*—Non-destructive Testing, Flicker Noise, Chopper Stabilization, DC Suppression**

I. Introduction

NOWADAYS, society is aided, in the process of creating new products and services, by all kind of electronic devices. The increasing autonomy and processing power of these devices has allowed the development of testing techniques that rely on measuring physical attributes of the manufactured goods without compromising their integrity, that is NDT. NDT provides a way to diagnose defects on the test subjects without compromising its characteristics. This evaluation of the condition of an object can be done via X-ray, ultrasounds, ECs and other means [1], [2], [3]. EC NDT is used to assess the condition of conductive materials, by inducing electric currents on them, generated by magnetic fields. The presence of defects will, consequently, modify the magnetic field that is picked up and used to characterize the test subject. The conventional EC NDT probes usually implement one or more sensing coils [3], while other probes rely on sensors, which may help in reducing chip area, but their reduced number usually result in low resolutions.

This work is inserted in the project described in [4] and focus an EC NDT system, in which an array of MR sensors is used. The number of sensors in the array can be scaled to allow increased resolution and inspection speed. The sensors present variations in resistance with the applied magnetic field, which are picked up and processed by an ASIC, that amplifies the signal and filters out the unwanted components. Higher penetration depths require lower frequencies, which lead to increased flicker (or low-frequency) noise. Also, the sensors are biased by a DC signal that, when amplified, saturates the output of the pre-amplifier.

In this work, solutions to these two problems are addressed by studying flicker noise reduction techniques, such as Chopper Stabilization, DC cancellation solutions, namely the DSL, to produce an improved fully-differential pre-amplifier for the NDT system, with the specifications presented on TABLE I.

TABLE I: Circuit Specifications

Technology	AMS 0.35 μm CMOS
Power Supply [V]	3.3
Open Loop Gain [dB]	70
Close Loop Gain [dB]	20
Bandwidth [MHz]	10
Phase Margin [°]	60
IRN @ 100Hz [$\mathrm{nV}/\sqrt{\mathrm{Hz}}$]	<20
DC Attenuation [dB]	40

A. Outline

This document is organized in five sections. This section makes an introduction to the context of the work and proposed objectives. Section II describes in more detail the EC NDT system and makes a theoretical review on flicker noise reduction techniques and DC cancellation. Section III makes a technical overview of this system, describing the sensor biasing and reading, as well as the considerations regarding the amplifier in focus. It also describes the designing process of the circuits proposed. Section IV presents the circuit simulation results obtained and a comment on them. In Section V, conclusions are drawn.

II. Background

This section presents the background of the work. It briefly describes the EC NDT system, in terms of functioning and building blocks, presents models for the noise of the used amplifier topology and introduces Chopper Stabilization to deal with flicker noise.

A. Eddy-current Non-destructive Testing System

An EC NDT is an efficient metallic body inspection method that uses a coil conducting a current, which generates a primary magnetic field with frequency f_1, according to Ampère's Law [5], with a magnitude B given by

$$B = \mu n I \tag{1}$$

where n is the number of turns of the coil, μ is the magnetic permeability and I the current that travels through the coil. As a consequence, electric currents appear [6], which will induce a secondary magnetic field, again according to Ampère's Law. In the presence of defects on the conductive material, the magnetic permeability μ is changed, altering the characteristics of the secondary magnetic field. If picked up by a device, using a sensing coil or, in this case an array of MR sensors, these changes on the secondary magnetic field may indicate flaws on the material. Fig. 1 illustrates the process described.

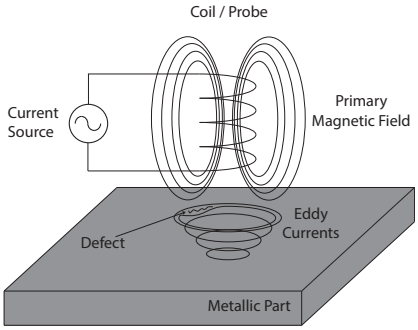

Fig. 1: Eddy current NDT illustration.

The MR sensors are biased by a current of frequency f_2 and they present a variation in their characteristic resistance with the magnetic field applied, producing an electric signal $y(t)$ that carries the information regarding that variation. When operating in their linear region, the total sensor resistance, which is a function of the sensed magnetic field, is given by

$$R_H(t) = R_0 + \Delta R(H(f_1)) \tag{2}$$

where R_0 is the nominal resistance and $\Delta R(H(f_1))$ is the resistance variation as a function of the sensed magnetic field created by the ECs. Given the sensors biasing current as

$$i(t) = I_0 + I_m sin(2\pi f_2 t), \tag{3}$$

their output signal $y(t)$ can be found by multiplying $R_H(t)$ by $i(t)$, that is

$$\begin{aligned} y(t) = {} & R_0 I_0 + R_0 I_m \sin(2\pi f_2 t) + R_m(f_b) I_0 \sin(2\pi f_1 t) + \\ & + \frac{R_m(f_b) I_m}{2} \sin(2\pi (f_1 - f_2) t) \\ & + \frac{R_m(f_b) I_m}{2} \sin(2\pi (f_1 + f_2)) \end{aligned} \tag{4}$$

The output signal presents two components, R_m and I_m, that are the resistance and current variation produced by the MR sensors, respectively, which hold useful information regarding the presence of defects and are present at frequencies $f_1 - f_2$ and $f_1 + f_2$. f_1 represents the frequency of the primary magnetic field, as referred, and is set according to the desired penetration depth. f_2 is the frequency of the sensor biasing current and is set in such a way that $f_1 - f_2$ must be within the pre-amplifier bandwidth, so that the information regarding defects can be preserved and the signals amplified. For this work, the biasing current is a DC current, that is $f_2 = 0$ Hz.

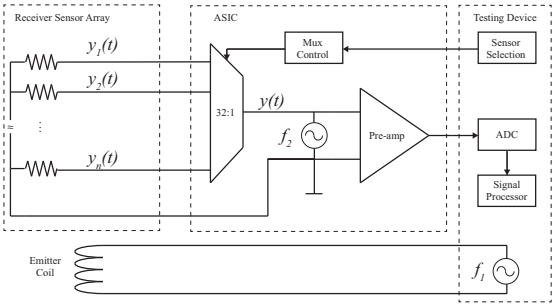

Fig. 2: Top-level diagram of the system.

The signals produced are processed by an ASIC, with an internal structure shown in Fig. 2. The MR sensors are selected by a multiplexer and their signals are amplified by a pre-amplifier present in the ASIC. The ASIC is also connected to a test device, which controls the sensor multiplexing, drives the emitter coil and samples signals for digital processing.

The pre-amplifier of the ASIC introduces significant amounts of flicker (or low-frequency) noise that impair readings as, to achieve high penetration depths, low-frequency magnetic signals must be used.

B. Noise modeling and Chopper Stabilization

The noise present in the amplifier is associated to the Metal-Oxide-Semiconductor (MOS) transistors. The transistors present two main types of noise, thermal (or white) noise and flicker (or low-frequency) noise. Thermal noise is caused by voltage fluctuations, originated by the random motion of electrons in a conductor. This type of noise is proportional to the absolute temperature [7], since temperature elevations cause an increase in kinetic energy of electrons, leading to an even more erratic motion, increasing the voltage fluctuations, thus increasing thermal noise. In MOS transistors, the most significant source of thermal noise is the channel. The thermal noise can be modeled as a current source connected between drain and source or as a voltage source connected to the gate and is given by

$$\overline{I_{n,thermal}{}^2} = \frac{2}{3} g_m (4 k_B T) \tag{5}$$

and

$$\overline{V_{n,thermal}{}^2} = \frac{2}{3} g_m (4 k_B T) r_o^2 \tag{6}$$

where $\overline{I_{n,thermal}{}^2}$ is the thermal noise current, $\overline{V_{n,thermal}{}^2}$ is the thermal noise voltage, k_B is the Boltzmann constant, T is the temperature in Kelvin, g_m and r_o are the transconductance and output impedance of the transistor, respectively. Flicker noise occurs due the to trapping of charges in the interface between the silicon substrate and the gate oxide. When these charges are released, they add a contribution to the drain

current in the form of noise. This phenomenon happens more often at low frequencies, therefore being also called $1/f$ noise [7]. The flicker noise current $\overline{I_{n,flicker}{}^2}$ and flicker noise voltage $\overline{V_{n,flicker}{}^2}$ are respectively given by

$$\overline{I_{n,flicker}{}^2} = \frac{K}{C_{OX}WL}\frac{1}{f}g_m^2 \tag{7}$$

and

$$\overline{V_{n,flicker}{}^2} = \frac{K}{C_{OX}WL}\frac{1}{f} \tag{8}$$

where K is the flicker noise parameter, that depends on the process and the type of transistor, C_{OX} is the capacitance per unit area of the gate oxide, W and L are the width and length of the channel, respectively. These noise models can be applied

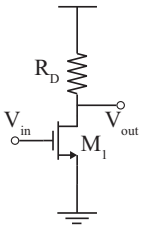

Fig. 3: A CS stage.

to describe the noise of circuits, such as a Common-Source (CS) stage (Fig. 3). The noise of the CS stage is found by summing all the noise contributions and is given by

$$\overline{I_{n,out}{}^2} = \frac{2}{3}g_m(4k_BT) + \frac{K}{C_{OX}WL}\frac{1}{f}g_m^2 + \frac{4k_BT}{R_D}, \tag{9}$$

where R_D is the drain resistor. Consequently, the total output noise voltage $\overline{V_{n,out}{}^2}$ is found by multiplying the output noise current $\overline{I_{n,out}{}^2}$ by R_D^2. As the output noise depends on the gain of the circuit, a normalization to noise is appropriate for better comparison between different circuits. For this reason the concept of Input-Referred Noise (IRN) is introduced. In order to be independent of the gain of the circuit, the IRN is found by taking the output noise voltage and divide it by the gain, which in this case is given by

$$\begin{aligned}\overline{V_{n,in}^2} &= \frac{\overline{V_{n,out}{}^2}}{A_v^2} \\ &= \frac{2}{3g_m}(4k_BT) + \frac{K}{C_{OX}WL}\frac{1}{f} + \frac{4k_BT}{g_m^2R_D}\end{aligned} \tag{10}$$

The noise of the CS stage (10) can be used to describe the noise of more complex circuits such as the differential pair, which has twice the IRN of the CS stage, and a folded cascode amplifier (Fig. 4). The IRN of this last circuit (considering only thermal noise) is given by

$$\begin{aligned}\overline{V_{n,i}^2} &= \frac{16k_BT}{3g_{m1,2}}\left(1 + \frac{g_{m5,6}}{g_{m1,2}} + \frac{g_{m11,12}}{g_{m1,2}}\right) \\ &= \frac{16k_BT}{3I_{D3}}V_{OD1,2}\left(1 + \frac{C-1}{A} + \frac{C}{B}\right)\end{aligned} \tag{11}$$

where A, B and C are, respectively, given by

$$A = \frac{V_{OD5,6}}{V_{OD1,2}} \qquad B = \frac{V_{OD11,12}}{V_{OD1,2}} \qquad C = \frac{2I_{D11}}{I_{D3}}. \tag{12}$$

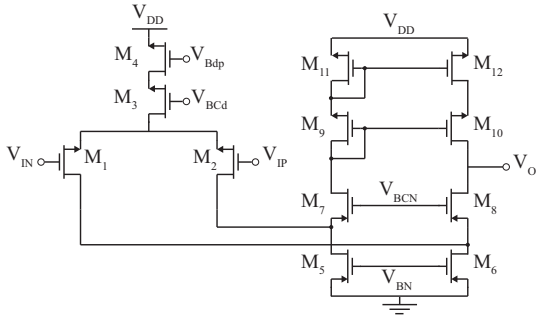

Fig. 4: Folded Cascode OTA.

$V_{ODx,y}$ and I_{Dx} are the overdrive voltage and drain current of the transistors indicated by x and y, respectively. As can be noticed, the thermal noise can be reduced by increasing A and B and reducing C, that is, by making sure that $V_{OD1,2}$ is higher than the remaining and by increasing the amplifier tail current.

As for flicker noise, it can be mitigated using specific techniques like Chopper Stabilization. Chopper Stabilization is a flicker noise reduction technique that uses modulation to shift the spectrum of the signal to high frequencies, where the flicker noise contribution is negligible, and then, after amplification, the signal is demodulated back to its baseband, while flicker is up-modulated. Fig. 5 shows a diagram describing the general Chopper Stabilization process.

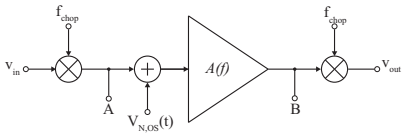

Fig. 5: Diagram of chopper stabilization.

Fig. 6 shows the spectra of the signals along the signal path of the chopper circuit (Fig. 5). Suppose the signal V_{in}, with a spectrum represented on Fig. 6(a), is modulated by a square wave carrier of unitary amplitude. The resulting signal, V_A, has a spectrum composed by replicas of the spectrum of the input signal V_{in}, centered on odd multiples of the carrier frequency f_{chop} (Fig. 6(b)), since the carrier only has odd harmonics. The modulated signal is then exposed to noise and amplified, before it is demodulated, resulting in signal V_B, with a spectrum represented in Fig. (6(c)). Demodulation is accomplished by using the same carrier wave, as before. This time, the flicker noise component is shifted to the odd harmonics of the carrier and the spectrum of the signal returns to its baseband (Fig. 6(d)). The resulting signal can be, afterwards, low-pass filtered in order to eliminate the unwanted quantities present at the odd multiples of the chopper frequency f_{chop}, if necessary.

As referred, for Chopper Stabilization to work, the input and output signals of the amplifier must be modulated in amplitude. This is accomplished by chopper modulators that use a square wave, of frequency f_{chop} and unitary amplitude, as a carrier, which is shaped by the input signal. The modulator output signal is then the multiplication of the input signal

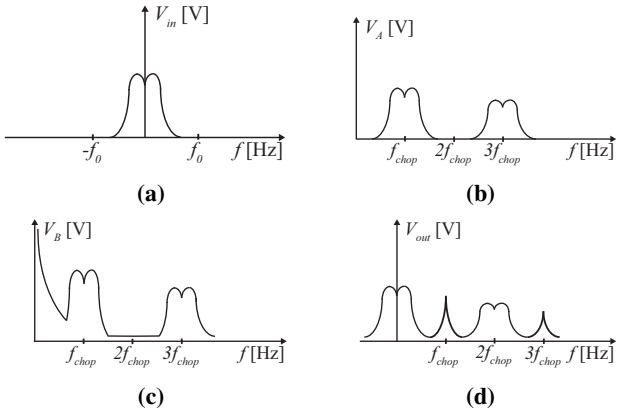

Fig. 6: Spectra of signals at several stages of chopper stabilization process: (a) input signal; (b) signal after the first modulation; (c) signal after amplification; (d) output signal.

by the carrier, which can be seen as a periodical inversion of the input signal, with frequency f_{chop}. Internally, chopper modulators are simple circuits composed by two pairs of switches, triggered by opposite clock phases (Fig. 7(a)). They also have two input and two output terminals that allow differential signals to be switched, creating the referred periodical inversion of the input signal, to achieve its modulation.

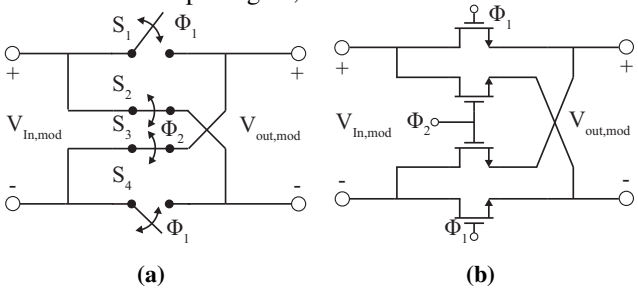

Fig. 7: Representation of a chopper modulator: (a) ideal switches; (b) switches implemented as NMOS transistors.

Consider the input, $V_{in,mod}$, and the output, $V_{out,mod}$ signals to be differential ones, that is $V_{in,mod} = V_{in,mod+} - V_{in,mod-}$ and $V_{out,mod} = V_{out,mod+} - V_{out,mod-}$. During phase ϕ_1, switches S_1 and S_4 are closed and the remaining are opened, making $V_{in,mod+} = V_{out,mod+}$ and $V_{in,mod-} = V_{out,mod-}$, therefore, $V_{out,mod} = V_{in,mod}$. On the next phase, ϕ_2, switches S_2 and S_3 are now closed, while S_1 and S_4 are opened, making $V_{in,mod+} = V_{out,mod-}$ and $V_{in,mod-} = V_{out,mod+}$, leading to $V_{out,mod} = -V_{in,mod}$, that is the desired periodic input signal inversion. The switches used to modulate the signals are usually simple MOS transistors, as seen in Fig. 7(b), however the usage of single transistors often lead to some problems, like charge injection [8], which is a phenomenon that occurs at the interruption of the channel of the MOS transistor as it enters cut-off region. As the channel is made up moving charges, upon entering cut-off region, the channel is interrupted and these charges are split, flowing to the drain and source terminals. The charge splitting is not uniform, as it depends on the impedance at each one of these terminals. Furthermore, the amount of charge injected is proportional to the parasitic capacitances of the transistor, that depend on its area, meaning that larger transistors will have more charges injected [8]. In this particular application, charge injection may lead to residual offsets, as charges injected into high impedance nodes, such as the inputs of an amplifier, originate periodical voltage spikes and, thus unwanted spectral components that are demodulated to the signal baseband, increasing the offset and the IRN.

It is stated in [9] that the injected charges, due to chopper action, causes transient current spikes with an average value I of

$$I = 2f_{chop}(WLC_{OX}V_{OD} + C_{OL}V_{CLK}) \tag{13}$$

where, f_{chop} is the chopping frequency, C_{OX}, C_{OL} and V_{CLK} are, respectively, the gate oxide capacitance per unit of area, the overlapping capacitance and the amplitude of the clock signal. This current, if not compensated, can have a value up to tens of pA, which is greater than the gate leakage current of a MOS transistor [9]. Thus the current associated with chopper action, when injected into high impedance nodes, such as the inputs of the amplifier, leads to high noise voltage levels. From the simulations performed in [9], it is found that of all noise sources, the contribution associated with charge injection is dominant and proportional to the chopper frequency and transistor area, as shown by (13). If chopper is disabled, this noise contribution disappears and the total IRN is significantly lower. To overcome this problem, the current associated to chopper action should be compensated by the presence of dummy switches.

The usage of single MOS transistors as switches also lead to reduced signal input swing as both NMOS and PMOS transistors are not capable of being "ON" during all the voltage range. This can result in signal distortion if the signal amplitude is close to the supply voltage.

To reduce the effects of charge injection, shorted half-sized dummy transistors are added to the drain and source of the main transistor and triggered with a clock phase opposite to the one of the main switch (Fig. 8). When the main switch turns off and interrupts its channel, the charges that compose it leave the transistor through the drain and source. At the same time, the dummy switches are switching on, thus they are attracting the charges injected by the main transistor to compose their channel. This way, the amount of charges injected into the surrounding circuits is reduced. To increase signal input swing

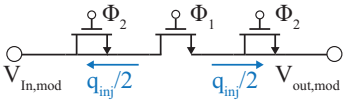

Fig. 8: Compensation of one transistor of a modulator with dummy transistors.

Transmission Gates (TGs) can be used. The TG is a form of switch composed by a PMOS transistor and a NMOS transistor in parallel, triggered by opposite clock phases, as shown in Fig. 9(a). This configuration provides both bidirectional current flow and an almost constant "ON" resistance across wide ranges of input voltages [10]. The "ON" resistance is defined

as the source-to-drain resistance of the transistor, when it works as a turned on switch. It is an important parameter as high "ON" resistances cause significant voltage drops that may lead to significant signal losses, if the switch is place on the signal path.

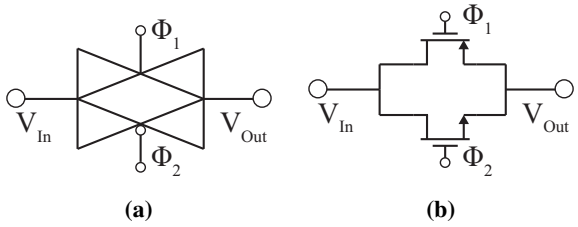

Fig. 9: Transmission Gate: (a) circuit; (b) symbol.

III. System Overview

As seen in the previous section, the system of this work presents an ASIC that is used for the analog processing of signals that characterize the test subject. The pre-amplifier of the ASIC suffers from increased flicker noise and has a significant DC component that can saturate it. In this section, the ASIC is revisited, focusing its pre-amplifier. The amplifier is converted into a fully-differential amplifier and the implementation of Chopper Stabilization is covered. Then, the cancellation of input DC signals is discussed.

A. The ASIC

The circuit of the ASIC is shown in Fig. 10. As seen, it is composed by an array of MR sensors and a pre-amplifier. The sensors are biased by a current source composed by an amplifier, a CS stage and a current mirror.

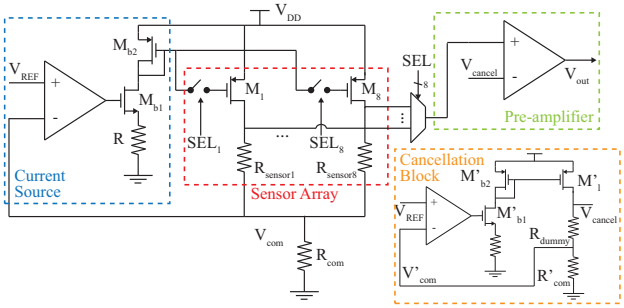

Fig. 10: Full circuit schematic.

A reference voltage is applied to the amplifier of the current source, producing an output current I_{out} that is made independent from the sensor resistance by using the CS stage. This output current is mirrored to the selected sensor and as a value given by

$$I_{Out} = \frac{G.\frac{g_{mb1}}{1+g_{mb1}R}.k}{1+G.\frac{g_{mb1}}{1+g_{mb1}R}.k+R_{com}}.V_{REF} \approx \frac{V_{REF}}{R_{com}}, \quad (14)$$

where R_{com} is an external resistor used to adjust I_{out}. In this work I_{out} is a DC current that bias the sensors and originate large DC voltage components that, if amplified, will lead to the saturation of the pre-amplifier. To reduce such effect, the ASIC uses a cancellation block, which is a copy of the current source connected to a dummy sensor. The cancellation block produces a DC component equal to the biasing signal of the sensors to apply it to the amplifier. As both components are equal, their are rejected due to the amplifier high common-mode rejection ratio (CMRR). However, due to process mismatch, both components may not be exactly equal, resulting in residual DC offsets that are addressed by the DC cancellation technique discussed ahead.

B. Capacitively Coupled Chopper Instrumentation Amplifier

To implement the pre-amplifier block of the ASIC, a Capacitively Coupled Chopper Instrumentation Amplifier was chosen (Fig. 11). This topology is proposed in [11] and [12], and includes a fully-differential amplifier with its feedback paths within the chopper path.

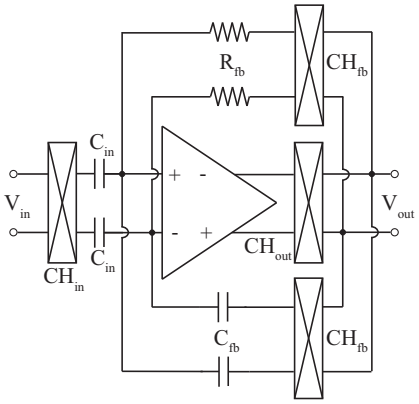

Fig. 11: Top-level diagram of the proposed CCCIA.

The CCCIA makes use of the amplifier inside a capacitive feedback loop, which has some advantages when compared to a resistive feedback network, such as the fact that integrated capacitors have superior process accuracy than resistors, which result in reduced gain variations due to mismatch.

In this configuration two paths for each feedback are used: one resistive path and another capacitive. The resistive feedback is here employed to ensure that the CM output voltage is fed into the amplifier inputs to accomplish their correct bias. To do this, a very large feedback resistor must be used to be able to not allow any current through it that can cause a voltage drop. If any significant current is present, the voltage drop across the resistor is significantly large and the CM voltage at the inputs of the amplifier is no longer equal to the one at its outputs.

The pass-band gain of the CCCIA is established by the ratio between the input C_{in} and feedback C_{fb} capacitors, for a very large DC gain.

$$G \approx \frac{C_{in}}{C_{fb}}. \quad (15)$$

In this work, to set the gain to 20 dB, C_{in} was chosen to be 10 pF as C_{fb} was chosen to be 1 pF.

The CCCIA makes use of two additional chopper modulators in both feedback paths to up-modulate the output signal

and feed it back into the amplifier inputs, besides the usual two input and output modulators. Considering Fig. 12, these two additional modulations allow the matching of the signal components frequency in the amplifier input node V_a (note that in each node, a representation of the signal component is present, however the components in black are not present at those nodes, being there just to make a frequency comparison). As the input signal, with frequency f, is modulated by the input chopper CH_{in}, its signal components are shifted from their baseband to the chopper frequency f_{chop}, resulting in an amplifier input signal V_a in that same frequency (highlighted in green). After amplification, the signal is demodulated by CH_{out}, resulting in V_{out} with the same f frequency as the input.

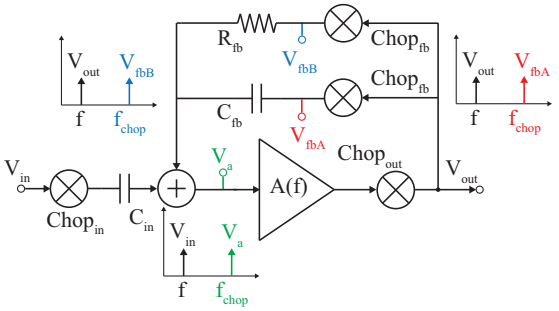

Fig. 12: Signal components along the feedback paths.

To be able to apply feedback, one can not simply connect the output and input nodes as the signal components of interest are at different frequency bands. If such connection is done, the node V_a would have a component in f_{chop} and in f, thus the signal feedback is not achieved. Therefore, to be able to correctly apply feedback, V_{out} must be modulated to f_{chop}, using the modulators CH_{fb}. Then the up-modulated signal can be fed into the feedback resistor R_{fb} and into the feedback capacitor C_{fb} to accomplish the DC feedback (in blue) and the signal feedback (in red), respectively, as all three components are at the same frequency band in the input node V_a.

A very important aspect is that due to action of the input chopper, DC signals are no longer blocked, since they are modulated to the chopper frequency. This presents a major problem, since the DC signals coming from the sensors will saturate the amplifier and the CCCIA will not be able to function. To overcome this problem, a DC suppression method, presented in [11] and in [12], is applied to the CCCIA: the DSL.

C. DC Servo Loop

The DSL is a DC suppression technique, that creates an high-pass characteristic, enabling the cancellation of sensor DC biasing signals, which can be up to 1 V. The basic principle behind this technique is to take the DC component of the output voltage of the CCCIA and apply it to the amplifier input node by means of a negative feedback.

In Fig. 13, the DSL was added as a new feedback path. It is composed by an integrator, a chopper modulator and a feedback capacitor, here called high-pass capacitor C_{hp}.

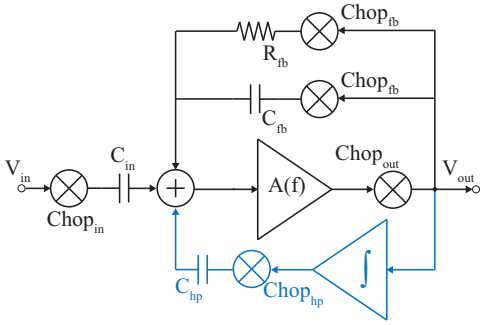

Fig. 13: Inclusion of the DSL.

To take the DC component from the output signal, a fully-differential inverting (or Miller) integrator is implemented to create low-pass filter with a very narrow bandwidth, to allow only the DC component to be amplified and reject other frequencies. The integrator makes use of input resistors R_{int} and a feedback capacitors C_{int}, that define the integrator unity-gain frequency as

$$f_{0,int} = \frac{1}{2\pi C_{int} R_{int}}, \tag{16}$$

which needs to be sufficiently small to allow enough attenuation of the signal component, while amplifying only the DC component. This filtered DC component V_{hp}, which is the output signal of the integrator, is then up-modulated to the chopper frequency f_{chop}, in order to match the up-modulated sensor DC biasing signal present at the amplifier inputs. The up-modulated DC component V_{hp} is fed to the amplifier input node through C_{hp}, achieving a negative feedback configuration that cancels out the sensor DC biasing signal and places a low-frequency high-pass pole in the circuit transfer function. The high-pass pole frequency f_{hp} is given by

$$f_{hp} = \frac{C_{hp}}{C_{fb}} f_{0,int}. \tag{17}$$

and, once more, needs to be very small, so that the CCCIA only rejects DC signals and amplifies signals originated by the sensors. To decrease f_{hp} the capacitor ratio C_{hp}/C_{fb} and/or $f_{0,int}$ can be decreased. To unity-gain frequency of the integrator $f_{0,int}$ as much as possible, large C_{int} and R_{int} must be chosen, as described by (16). For example, if the capacitor ratio of (17) is set to 1, then the high-pass pole frequency is equal to the unity-gain frequency of the integrator. Since the pole must be placed in a region typically below 1 Hz, $C_{int} \times R_{int}$ must be set to at least $1/2\pi$ s, which requires a GΩ resistor for a typical 10 pF capacitor.

To reduce f_{hp} by changing the ratio C_{hp}/C_{fb}, C_{hp} needs to be smaller than C_{fb}. However, the additional feedback path formed by the DSL, shown in Figure 13, establishes a relation between the DC sensor biasing signal $V_{in,DC}$ and the output of the integrator V_{hp}, given by

$$\frac{V_{hp}}{V_{in,DC}} = \frac{C_{in}}{C_{hp}}. \tag{18}$$

This means that by reducing C_{hp}, the maximum sensor DC biasing signal $V_{in,DC}$ that can be attenuated is also reduced,

for the same V_{hp}. Noting that V_{hp} is limited by the maximum and minimum output voltages of the amplifier that composes the integrator, the maximum input DC voltage that can be attenuated is given by $(C_{hp}/C_{in})V_{hp}$, thus for a maximum V_{hp} of 1 V, to attenuate 1 V, C_{in} and C_{hp} must be equal.

To ease the requirement of having to attenuate the input DC voltage $V_{in,DC}$ by 1 V, the previously referred cancellation block is used, while the DSL is used to target the residual offset originated due to mismatch between the cancellation block and the sensors.

D. Pseudo-resistor

As described before, the CCCIA needs very large resistors, in the order of GΩ, to employ the DC feedback and to set the unity-gain frequency of the DSL integrator to a very low value. The usage of integrated resistors of the technology is not possible, since that would mean huge die areas. To overcome this problem, these resistors are replaced by pseudo-resistors. A pseudo-resistor is usually composed by one or more diode-connected MOS transistors in series in near cut-off or sub-threshold region, as shown in Fig. 14. This simple architecture adds small noise and parasitics to the circuit, being able to achieve resistance values in the order of GΩ [13]. However, pseudo-resistors, like the one in Fig. 14, present a variation in resistance for large voltage swings and are sensitive to process mismatch.

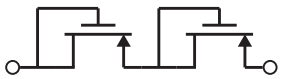

Fig. 14: A pseudo-resistor.

Also, these pseudo-resistors have a fixed resistance value, determined by the dimensions of the transistors used and the voltages applied, not being able to be change after fabrication. In [14] and [13], a tunable pseudo-resistor is proposed, in which the gate voltage V_G of the transistors is changed using a voltage source, in order to change the "ON" and "OFF" state of the transistor, therefore controlling its resistance.

IV. Results

In this section simulated results are presented to evaluate the behavior of the final circuit. To start, the CCCIA gain and IRN were simulated without the DSL. As can be seen from Figure 15, the CCCIA without the DSL achieves a low-pass characteristic with 20 dB at its pass-band and a cut-off frequency of about 7 MHz. The gain specification is met, however the cut-off frequency is 3 MHz bellow the specification of 10 MHz. Also, without DSL, the input DC components are also amplified with a 20 dB gain, which will saturate the amplifier, as they can be up to 1 V. As for the IRN, with this configuration an almost constant value of 4 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ is achieved, even at very low frequencies, except for the spike present at 10 kHz, which represents the modulated flicker noise component. However, this spike presents no problems for the circuit, since with chopper turned on, only signals up to 5 kHz will be used and this modulated flicker noise can be filtered out. With higher frequencies, the chopper modulators are turned off, as it would not be advantageous to use them, because of the very low noise floor.

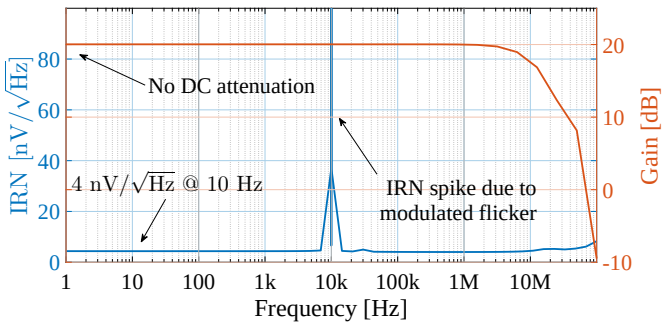

Fig. 15: Gain and IRN of the CCCIA without the DSL.

With the DSL included in the CCCIA, the gain and IRN are once more simulated. The DSL is able to place an high-pass pole in a frequency about 16 mHz and achieves an attenuation of 60 dB for input DC signals up to 200 mV, as seen in Fig. 16. Fig. 17 shows a transient simulation of the output signal

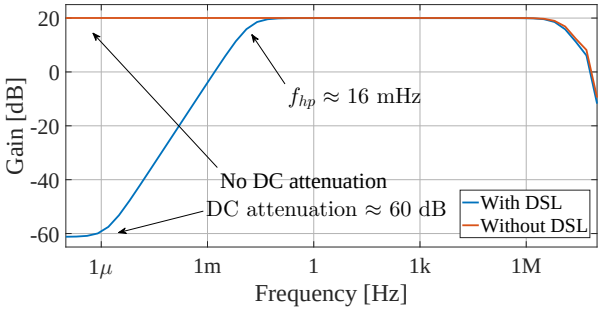

Fig. 16: Gain of the CCCIA with the DSL.

V_{out}, with and without the DSL, for an input signal with a DC component of 200 mV and 100 mV, respectively, and a signal amplitude of 100 mV and 10 mV, also respectively. As can be seen, the DSL allows an almost total cancellation of DC components up to 200 mV, which are attenuated 60 dB (Figure 16). Without the DSL, 100 mV DC components were injected at the inputs and were amplified by 10 times, as expected, which resulted in differential offset of 1 V.

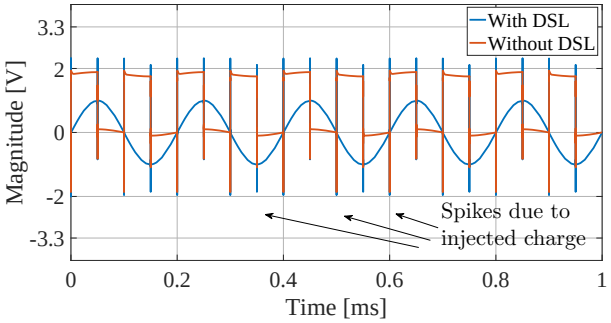

Fig. 17: Transient response the output V_{out} of the CCCIA.

As for the noise analysis, the DSL increases significantly the IRN to 43 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, about 10 times the IRN of the CCCIA without it, at 1 Hz (Figure 18). However, at 10 Hz the IRN is increased about 3 times and the noise floor is kept at the same level. This happens because the amplifier used in the integrator is a copy of the one used as main amplifier in the CCCIA thus, it has a noise contribution in the same order as the main amplifier. Nonetheless, it was found that this contribution can be mitigated by reducing the high-pass capacitor C_{hp}, with the cost of reducing the maximum sensor DC signal level that can be attenuated, which is given by (18).

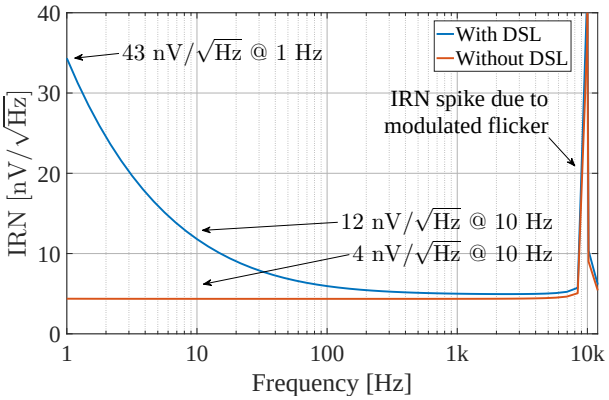

Fig. 18: IRN analysis of the CCCIA with the DSL.

As all chopper modulators are driven by the same clock, their switches can be grouped in two groups, where in Group 1 are the switches that are turned on by the first clock phase ϕ_1 and the on Group 2, the ones that are turned on by the second clock phase ϕ_2. This way, two states are defined, where State 1 corresponds to the moment when switches of Group 1 are turned on and when switches of Group 2 are turned off, and State 2 corresponds to the moment when switches of Group 1 are turned off and when switches of Group 2 are turned on. Simulations were performed in both states to evaluate the stability of the circuit, where both of them present similar stability performance. Stability summary indicates a phase margin of 87.5 ° for each state. However, the behavior of each separate state may not reflect the final behavior of the CCCIA, where modulators are constantly switching from one state to another. Still, the fact that the CCCIA presented no gain overshoot and each state has phase margin of 87.5 ° are positive indicators of the stability of the circuit.

A. Monte Carlo Simulations

To be able to predict the behavior of the system in multiple conditions, 500 Monte Carlo runs were performed, in which the band-pass gain, DC attenuation and IRN were evaluated. To perform yield calculation, the metrics just referred were used, having as specifications 20 dB, 40 dB and 10 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ (at 100 Hz), respectively.

Figure 19 shows the result of the 500 runs for the gain of the CCCIA, in which, for sub-hertz frequencies, the DC components have an average attenuation of 60 dB, however in some cases the attenuation is lower, but never below 40 dB. As for the pass-band gain, it has an average of 20 dB, with the exception of some cases where the signal is attenuated more than 40 dB, which indicates that in these cases the circuit does not work.

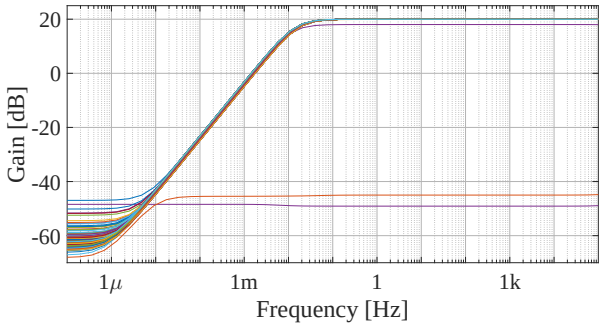

Fig. 19: Monte Carlo simulations: CCCIA gain.

As for the noise performance shown in Figure 20, for all the tested cases, the circuit presents an IRN below 20 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 10 Hz and about 6 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 100 Hz, with the exception of just one case, which achieves 65 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, thus not meeting the specification. At 1Hz, in all tested cases with the exception of one, the IRN is below 40 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$.

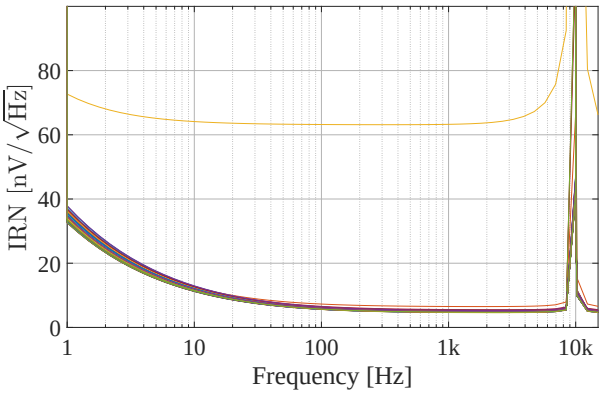

Fig. 20: Monte Carlo simulations: IRN of the CCCIA.

In these Monte Carlo runs, PSS analysis were made to allow the execution of the PAC and PNOISE analysis. As the PSS analysis uses iterative methods to converge to a solution for the periodic operating point, in some cases tested in Monte Carlo, it did not converge to a solution. This resulted in a failed test, as the simulator could not evaluate the gain and IRN of the circuit, which contributed negatively to the yield calculation, resulting in a value of 71%, which does not really represent the ratio between cases where the specifications were not met and cases that the specifications were met. However, a PSS analysis that could not converge to a solution does not necessarily means that the circuit does not work, it only means that that case could not be evaluated. For this reason, the yield was manually calculated by discarding the cases where the PSS did not converge and take only into account the cases that could be evaluated (362 cases) and and the cases that not met the specifications (5 cases), leading to a yield of 98.6%.

B. Specification and Obtained Results Comparison

To finish, in Table II, the simulated results are compared to the specifications. As can be seen, the simulated open-loop and close-loop achieve specifications. However, the bandwidth does not meet the specification, being just half the wanted value. The phase margin was found by performing stability simulations for two states of the circuit, as explained, achieving a value of 87.5 °. However this phase margin may not reflect the actual stability of the circuit, with the modulators constantly switching.

The CCCIA has a IRN, at 100 Hz, of 6 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, while its specification has a value of 20 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. It also presents a DC attenuation of 60 dB, 20 dB above the specification.

TABLE II: Circuit specifications and results.

Parameter	Specification	Simulated
Open Loop Gain [dB]	60	58
Close Loop Gain [dB]	20	19.9
Bandwidth [MHz]	10	5
Phase Margin [°]	60	50
IRN @ 100Hz [$\mathrm{nV}/\sqrt{\mathrm{Hz}}$]	<20	6
DC Attenuation [dB]	40	60

V. Conclusions

The present work addresses an EC NDT system that uses MR sensors. This system also makes use of an ASIC that multiplexes and bias the sensors, and amplifies the signals they produce. The work addresses two problems that the ASIC present: large flicker noise when using low signal frequencies, which are required to achieve higher penetration depths, and large sensor DC biasing signals that saturate the pre-amplifier.

To mitigate flicker noise, Chopper Stabilization was chosen to be implemented, as it is a fully-analog technique that modulates the signal to an higher frequency, before being exposed to noise and offsets originated by the amplifier of the ASIC. This way, the spectral components of signal and noise are not overlapped and, after being amplified, the signals are demodulated, returning to their baseband, as noise and offsets are up-modulated, thus being removed.

The pre-amplifier was implemented as a CCCIA. This topology builds the capacitive feedback within the chopper path, thus the input modulator is placed before the input capacitor, which avoids having the noise current of the modulators injected in the high impedance input node of the amplifier. With the placement of the input modulator before the input capacitor, sensor DC biasing signals are up-modulated and are not block by the input capacitors. This leads to the amplification of DC components, which are significantly large and will saturate the amplifier. To solve the problem, an additional feedback path is implemented, the DSL. The DSL is composed by a Miller integrator that isolates and amplifies the output DC voltage by having a very narrow pass-band. This narrow pass-band is achieved by reducing the integrator unity-gain frequency as much as can be, by implementing GΩ input pseudo-resistors, composed by PMOS transistors in a near cut-off region. This way, the integrator only allows DC signals to be amplified, up-modulated and subtracted from the main amplifier input by means of a negative feedback. This feedback makes use of high-pass capacitors that establish a relation between the integrator output voltage and the maximum sensor DC biasing signal that can be attenuated, as well as a relation between the frequency of the system high-pass pole and the unity-gain frequency of the integrator.

The CCCIA targets the amplification of signals with a gain of 20 dB and the attenuation of DC signals up to a maximum of 200 mV. Since the sensors are biased by a 1 V DC signal, the DSL alone is not capable of blocking all this component, therefore, the previously developed cancellation block is used. This cancellation block implements a copy of the sensor biasing circuitry, as well as a dummy sensor, to provide an equal DC biasing voltage as a cancellation signal. The sensors DC biasing voltage and the cancellation signal are applied to the amplifier and, since they are equal, they are seen by the amplifier as a CM voltage, thus being rejected. DC components originated from mismatch between the sensors and cancellation circuit are targeted by the DSL, to allow a complete DC signal canceling.

By simulating the implemented circuit, it was found that the CCCIA presents a pass-band gain of 20 dB, as expected. Its bandwidth is about 5 MHz and its IRN is about 6 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 100 Hz, 12 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 10 Hz and 43 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 1 Hz. Input DC signals up to 200 mV are found to be attenuated by 60 dB. These results are proved by Monte Carlo simulations, where an yield of 98.6% was obtained, when discarding the cases where the PSS analysis did not converge. Regarding stability, it was evaluated for the two states of the circuit, defined by the on and/or off state of the chopper switches. In both states, a phase margin of 87.5 ° was obtained, but gives no guarantees that with chopper switching the circuit does not become unstable. However, this phase margin and the fact that there is no gain overshoot are good indicators of the stability of the circuit. This way, it can be said that the gain and DC attenuation specifications are met, while the requirement of having a bandwidth of 10 MHz was not achieved. However, the IRN obtained at 100 Hz was almost 4 times less than the specification.

References

[1] L. Rosado, "New Eddy Current Probes and Digital Signal Processing Algorithms for Friction Stir Welding Testing," PhD Thesis, Universidade de Lisboa, Instituto Superior Técnico, 2014.

[2] P. E. Mix, *Introduction To Nondestructive Testing: A Training Guide*, 2nd ed. New Jersey, USA: John Wiley & Sons, 2005.

[3] A. Sophian, G. Y. Tian, D. Taylor, and J. Rudlin, "Electromagnetic and eddy current NDT: A review," *Insight: Non-Destructive Testing and Condition Monitoring*, vol. 43, no. 5, pp. 302–306, 2001.

[4] D. M. Caetano, M. Piedade, and J. Graça, "A CMOS ASIC for Precise Reading of a Magnetoresistive Sensor Array for NDT," in *11th European Conference on Non-Destructive Testing*. Prague: IEEE, 2014, pp. 1–10.

[5] R. A. Serway and J. W. Jewett Jr., *Physiscs for Scientists and Engineers with Modern Physics*, 9th ed. Brooks/Cole, 2014.

[6] E. Kriezis, T. Tsiboukis, S. Panas, and J. Tegopoulos, "Eddy currents: theory and applications," *Proceedings of the IEEE*, vol. 80, no. October, pp. 1559–1589, 1992.

[7] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. New York, NY, USA: McGRAW-HILL, 2001.

[8] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of Op-Amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, 1996.

[9] J. Xu, Q. Fan, J. H. Huijsing, C. Van Hoof, R. F. Yazicioglu, and K. A. A. Makinwa, "Measurement and analysis of current noise in chopper amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 7, pp. 1575–1584, 2013.

[10] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, sixth edit ed. Oxford: Oxford University Press, 2009.

[11] Q. Fan, F. Sebastiano, J. H. Huijsing, and K. a. a. Makinwa, "A 1.8 uW 60 nV/Hz Capacitively-Coupled Chopper Instrumentation Amplifier in 65 nm CMOS for Wireless Sensor Nodes," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 7, pp. 1534–1543, 2011.

[12] C. Y. Wu and C. S. Ho, "An 8-channel chopper-stabilized analog front-end amplifier for EEG acquisition in 65-nm CMOS," *2015 IEEE Asian Solid-State Circuits Conference, A-SSCC 2015 - Proceedings*, pp. 0–3, 2016.

[13] H. Kassiri, K. Abdelhalim, and R. Genov, "Low-distortion super-GOhm subthreshold-MOS resistors for CMOS neural amplifiers," *2013 IEEE Biomedical Circuits and Systems Conference, BioCAS 2013*, pp. 270–273, 2013.

[14] J. Silva, D. Oliveira, D. Caetano, and J. Fernandes, "Variable Bandwidth Chopper Amplifier for Eddy-current Non-destructive Testing," in *21st International Workshop on Electromagnetic Nondestructive Evaluation*, Lisbon, 2016, pp. 2–3.