Very low power consumption SAR ADC for wireless sensor networks

(Master Thesis Extended Abstract)

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Abstract **— This study aims to design analog-to-digital converter based on successive approximations (SAR ADC), with very low power consumption, in an advanced CMOS technology (*28* nm), following the industrial methodologies IC. This project was conducted in partnership with Synopsys, operating at a supply voltage of *0.5* V ± *10%* with a resolution of *12* bits and *500* kS/s sampling frequency.**

Keywords— Analog-to-Digital Converter (ADC), Successive-Approximation Register (SAR), low power consumption, Integrated Circuit (IC).

I. Introduction

Nowadays, there is a demand for analog-to-digital converters (ADCs) with low power consumption, namely for wireless sensor networks. Since is difficult and expensive to develop new types of battery, electronic circuits need to consume less. Over the past decade, the research projects show that the SAR topology is suitable for this situation. Thus, the main goal of this work is to develop an Asynchronous SAR ADC with 12 bit resolution. It aims to operate at 500 kS/s sampling frequency, with a supply voltage of 0.5 V ± 10% and a differential full-scale input range of 1 V. The design ought to cover 16 PVT corners, with temperature range from -40 to 125 ºC, and a SNR above 65 dB.

The present paper is organized as follows: Section II: The typical SAR topology and the asynchronous one (that is used) are depict. It also lists the noise and time specifications. Section III: Features the comparator, according to its topology, time and noise specifications. Section IV: Describes the Sampling DAC employed, accordingly to its topology and the sizing of its capacitors and switches. It also mentions the employed clock-boost. Section V: Summarizes the state machine with a delay cell that mimics the DAC switchings. Section VI: Addresses the required calibrations for the converter. Section VII: Lists the conclusions and future work.

II. ADC Arquitecture

The SAR ADC operates through a binary search algorithm, estimating a digital word that represents, as closer as possible, its input signal voltage. The word is created by testing each bit individually, so that in each step the selected bit origins a reference voltage (produced by the internal DAC) which will be compared with the stored input signal voltage. This process is repeated N times (ADC resolution) until the last bit conversion.

The traditional converter operates in a synchronous way, where each bit conversion takes the same amount of time, regarding the slowest bit conversion. Whether an asynchronous one has a variable time for each bit conversion, since it only uses the necessary time so that the comparator can make a decision. This way, the asynchronous converter is generally faster converting a signal. It should also have a lower power consumption, since it would allow the blocks to be disabled sooner. Hence we selected the asynchronous way, but its sizing is made the same way as a synchronous.

The synchronous operation requires a high-frequency clock signal which based on the converter's resolution (N) limits the sampling frequency (f_S) as

$$f_S[Hz] = \frac{f_{CLK}}{N+1}, \qquad (1)$$

where f_{CLK} is the required clock signal frequency and N is the number of clocks necessary for every bit conversion, plus one clock for sampling. The maximum clock frequency (f_{CLKmax}) must ensure that all bits are converted, so its estimation must consider the time of the slowest bit conversion for every bit conversion. Therefore the f_{CLKmax} is determined based on the worst (slowest) comparison time per bit ($t_{COMPworst}$), the DAC settling time (t_{DAC}) and the sampling time (t_S), yielding

$$f_{CLKmax}[Hz] = \frac{1}{N(t_{COMPworst} + t_{DAC}) + t_S}. \qquad (2)$$

Since, at extremely low supply voltage, the transistors of the comparator and sampling DAC operate at sub-threshold region, the switches ON-resistance is high, originating a large $t_{COMPworst}$, t_{DAC} and t_S.

The SAR ADC described in this work is composed by five main blocks, as depicted in Fig. 1. At first, the differential input signal is sampled by the Sampling DAC (controlled by a synchronous external clock), and afterwards the stored signal will be successively processed in an asynchronous way. The comparator decides, based on the differential output voltage of the DAC, returning q (and its inverse value) to the SAR block (which stores the bit decision in a register) and to the delay block, which generates an internal (asynchronous) clock. This internal clock ensures, for every bit conversion cycle, a constant time for settling the voltages of the DAC capacitors and a variable time for each comparator bit decision. After all bits are converted, the final word is synchronously delivered

I present my sincere gratitude to my mentor Dr Pedro Figueiredo.

to the output, the sampling phase is restarted and the cycle repeats.

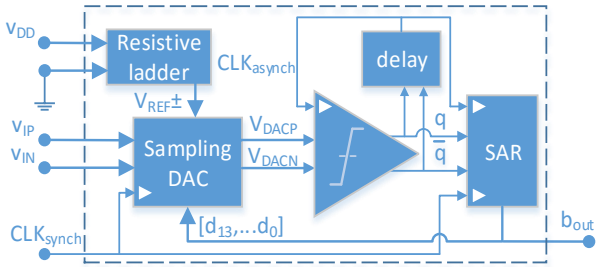

Fig. 1. Implemented SAR DAC block diagram.

This ADC was sized regarding as top guidelines, the time and the noise constraints. We attributed most of the clock period for conversion and the remaining for sampling. In turn, the noise restriction was used to limit the noise that each block was allowed to produce. Thus, limiting the value of the noise capacitor of the comparator and the unit capacitor of the DAC.

A. Time constraints

The time operations use $f_S = 500\ kHz$ as guideline, which makes a clock period of 2 µs. Then, missing 10% of the clock period to input signal sampling (t_{samp}), the remaining 90% are used for conversion (t_{conv}), resulting in

$$\begin{matrix} t_{samp} = 0.1T_{CLK} = 200\text{ ns} \\ t_{conv} = 0.9T_{CLK} = 1800\text{ ns} \end{matrix}. \qquad (3)$$

In turn, stipulating that each word conversion takes 12 decisions (given the resolution) plus 2 more due to redundancy, makes 128 ns for every bit conversion. Since that time comprises the settling time of the DAC (t_{DAC}) and the time for the comparator to decide (t_{comp}), we attributed

$$\begin{cases} t_{DAC} = 0.55t_{bit} = 70\text{ ns} \\ t_{comp} = 0.45t_{bit} = 58\text{ ns} \end{cases}. \qquad (4)$$

B. Noise constraints

Besides the quantization noise present in ideal ADCs, real ADCs also have noise due to internal components and external factors. Yet, the dominant contribution corresponds to thermal noise, which is given by kT/C. The noise produced comes from the three typical blocks, meaning from sampling ($\overline{v_{n,samp}^2}$), quantization ($\overline{v_{n,Q}^2}$) and the comparator ($\overline{v_{n,comp}^2}$). We can distribute the noise using the SNR expression, as

$$SNR = 10\log_{10}\left(\frac{P_{signal}}{\overline{v_{n,Q}^2} + \overline{v_{n,samp}^2} + \overline{v_{n,comp}^2}}\right). \qquad (5)$$

In turn, we can relax the comparator and sampling noise by selecting a 12 bit resolution, obtaining $\overline{v_{n,Q}^2} = (70.5\ \mu V)^2$. Then, using the specified SNR and assuming that the comparator noise is the same as the sampling noise, results in $\overline{v_{n,samp}^2} + \overline{v_{n,comp}^2} = (186\ \mu V)^2$.

Ergo, $\overline{v_{n,samp}^2} = \overline{v_{n,comp}^2} \simeq (131.5\ \mu V)^2$. Consequently, knowing the sampling noise it is possible to determine the overall sampling capacitance using

$$C_{samp} = \frac{8}{3}\frac{kT}{\overline{v_{n,samp}^2}} \simeq 688\text{ fF}. \qquad (6)$$

III. Comparator

A dynamic comparators only consumes energy during the decision phase, being more power efficient than a high gain operational amplifier. Therefore, a dynamic comparator is used, based on [21], where part of its circuit is illustrated in Fig. 2. It consists of a differential pair – M_{1P} and M_{1N} – (that charge C_F making an integrator) and a pair of back to back inverters – M_{4P}, M_{6P}, M_{7P} and M_{4N}, M_{6N}, M_{7N} – (or cross coupled inverters). Moreover, the integrator was sized to place the transistors of the differential pair in the sub-threshold region (namely in the weak inversion region); combined with a sufficient current supply that obey with the temporal goals.

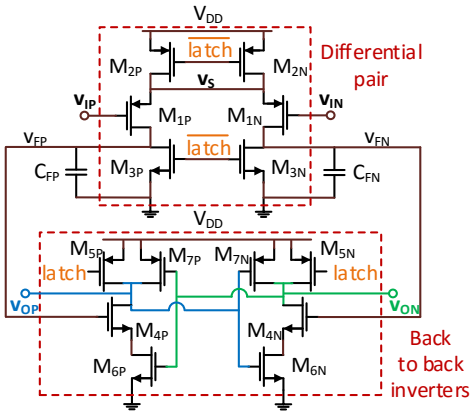

Fig. 2. Part of the dynamic comparator schematic.

The comparator circuitry is designed firstly ensuring the noise restriction and secondly the time, which comprises the phases of integration and regeneration, denoted in Fig. 3. To do so, a theoretical model is required to instruct a first approach and then simulate the circuit. Hence, the study from [18], regarding the comparator modeling and transient behavior at the regeneration phase, and [22], [23], regarding the transconductance model for the MOSFET in the weak inversion region, are combined.

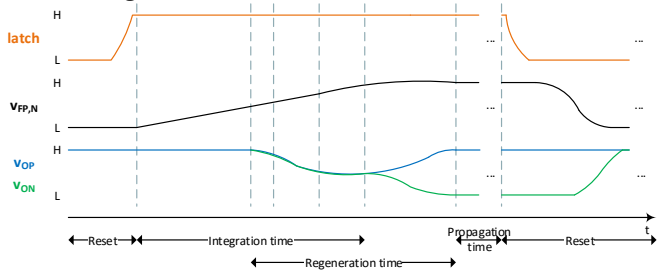

Fig. 3. Integration and regeneration phases.

A. Theoretical first approach

The integrator switches (M_{1P}/M_{1N} and M_{2P}/M_{2N}) were designed to be in the sub-threshold region (preferably in the

weak inversion), where in a slow rate operation the current consumption is best leveraged. Then, the (noise) capacitors (C_F) are sized in order to comply with the comparator noise restriction. Hence, assuming, that the comparator output noise is mainly given by the noise produced from the comparator integration nodes, as stated in [18], yields

$$\sigma^2\big(v_o(t)\big) \approx \sigma_{int}^2(t) = \frac{4kT\gamma g_m}{{C_F}^2}t. \qquad (7)$$

In turn, as illustrated in Fig. 4, the comparator input referred noise –$\sigma_{ni}^2(t)$ – is quantified by

$$\sigma_{ni}^2(t) = \frac{\sigma^2\big(v_o(t)\big)}{G^2(t)} \approx \frac{4kT\gamma}{g_m t}, \qquad (8)$$

where $G(t)$ is the integration voltage gain that neglecting g_{DS1} is given by

$$G(t) = \frac{v_{F\,diff}(t)}{v_d} = \frac{g_{m1}}{C_F}t, \qquad (9)$$

and in the end of the integration is

$$G(t_{int}) = 2g_{m1}\frac{\Delta V_F}{I_{SS}} = \frac{g_{m1}}{I_D}\Delta V_F. \qquad (10)$$

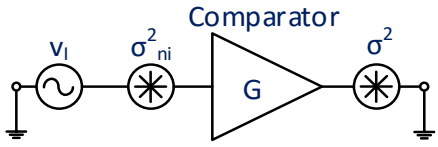

Fig. 4. Comparator output and input referred noise model.

Furthermore, one can relate the transistors size through its current, which is given, in the weak inversion region, as [22]

$$I_D = \frac{W}{L}I_M exp\left(\frac{V_{GS}-V_M}{n\phi_t}\right)\left[1-exp\left(\frac{-V_{DS}}{\phi_t}\right)\right], \qquad (11)$$

where I_M and V_M are the current and voltage for the representative point that ends the weak inversion. Moreover, knowing the transconductance in this region as

$$g_m = \frac{I_D}{n\phi_t} \Leftrightarrow I_D = g_m n\phi_t, \qquad (12)$$

where n is a transistor intrinsic parameter and ϕ_t is the thermal voltage,

$$\phi_t[mV] = 25.9 \times (T/300), \qquad (13)$$

if we substitute the equation (10) and (12) in (8), we get the comparator input referred noise at the integration time as

$$\sigma_{ni}^2(t_{int}) \approx \frac{4kT\gamma}{C_F}\frac{I_D}{g_m\Delta V_F} = \frac{4kT\gamma}{C_F}\frac{n\phi_t}{\Delta V_F}. \qquad (14)$$

This way, we can determine a guideline value to size C_F, using the noise restriction as the input referred noise, meaning $\sigma_R^2 = \sigma_{ni}^2 = (131.5\ \mu V)^2$, and $T = 398°K$ (125°C), $n = 1.6$, $\Delta V_F = 300$ mV and $\gamma = 1$, through (14) we obtain the theoretical value as

$$C_F = \frac{4kT\gamma}{\sigma_{ni}^2(t_{int})}\frac{n\phi_t}{\Delta V_F} \approx 230\text{fF}. \qquad (15)$$

B. Time restrictions

Once stablished the necessary current supply, the size of the differential pair is adjusted by simulation to comply with the integration time restriction, taking in consideration the relation of W/L from equation (11). Likewise, the transistors of the back to back inverters are adjusted with the remaining time for the regeneration phase.

However during the complete ADC sizing, was required to increase the comparator input common mode voltage, what consequently delayed the comparator response, causing the slowest corner to fail the time constraint. So, instead of resizing the comparator, we aggregated an extra capacitor to the differential pair (as depicted in Fig. 5) that supplies more current and, thus, accelerating the integration phase.

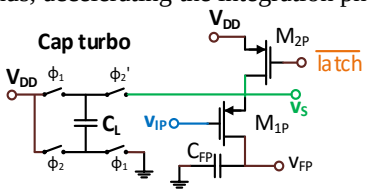

Fig. 5. Comparator turbo capacitor that speeds up the integration stage.

This solution is proven for the worst case as illustrated by Fig. 6, when the turbo is disabled, and by Fig. 7, when it is enabled.

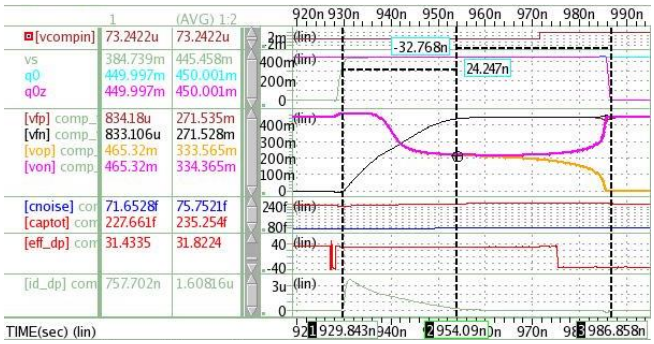

Fig. 6. Transient simulation of comparator operation in corner 14 (slowest), having 73uV at input, with turbo OFF.

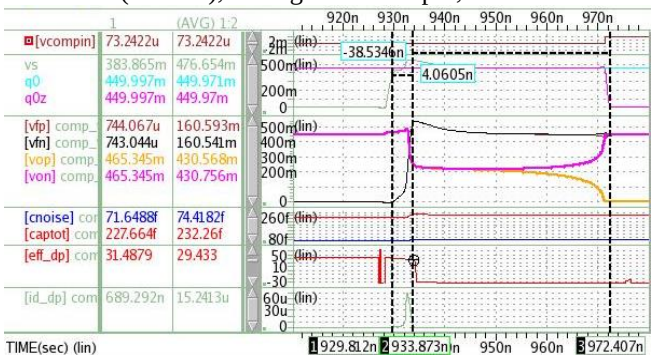

Fig. 7. Transient simulation of comparator operation in corner 14 (slowest), having 73uV at input, with turbo ON.

C. Noise restriction

Besides complying the operating times of the comparator with the time restriction, the **noise restriction** must be confirmed. So, a transient noise simulation is performed for all corners, where it is possible to obtain the standard deviation value and, consequently, the estimated comparator output noise. This is done through a stochastic process by triggering the comparator 500 times with a maximum noise frequency of 15 GHz, at a fixed input signal of 1 mV, whose standard deviation value (i.e. the output referred noise) is given by [18]

$$\sigma^2\big(X(t)\big) = E(X(t)^2) - E\big(X(t)\big)^2, \qquad (16)$$

where $X(t)$ is a Gaussian distributed stochastic process and $E(X(t))$ is its expected value, which is equivalent to the relation between the differential output voltage root mean square (RMS) and its average (AVG) values as

$$\sigma(X(t)) = \sqrt{RMS^2 - AVG^2}. \quad (17)$$

In turn, we can express the comparator input referred noise as determined by [18] [24]

$$\sigma_{ni}(t) = \sigma(X(t))/G_{eff}(t), \quad (18)$$

where $G_{eff}(t)$ is the effective gain of the regeneration nodes at a given sampling instant (as illustrated in Fig. 8). Then, applying these concepts for the same selected corner as before, yields Table I and Table II, respectively without and with turbo, which confirm that the produced noise is below the noise constraint ($\boldsymbol{\sigma_R}$), within a sufficient margin.

Table I - Comparison of the produced input referred noise between main corners, with turbo OFF.

Input referred noise from main corners with turbo OFF				
File_tr	0	5	7	14
V	0,5	0,45	max	Min
T	50	max	max	Min
Corner	Typ	**Noisy**	Faster	Slowest
RMS [mV]	50.4	50,96	50.84	51,04
AVG [mV]	−50.2	−50.57	−50.52	−50,97
σ [mV]	4	6.3	5.7	2.8
$Geff$	50.1	50.2	50.8	50.2
σ_{ni} [µV]	79.3	**126**	111	56.1
σ_R [µV]	**131,5**			
Margin: $\sigma_R - \sigma_{ni}$ [µV]	52,2	**5,5**	20,5	75,4

Table II - Comparison of the produced input referred noise between main corners, with turbo ON.

Input referred noise from main corners with turbo ON				
File_tr	0	5	7	14
V	0,5	0,45	max	Min
T	50	max	max	Min
Corner	Typ	**Fast**	**Faster**	Slowest
RMS [mV]	51,37	50,8	51,6	50,1
AVG [mV]	−51.22	−50,41	−51,18	−50,07
σ [mV]	3,87	6,27	6,52	2,05
$Geff$	50,45	50,07	50,88	50,2
σ_{ni} [µV]	76,8	**125**	**128**	41
σ_R [µV]	**131,5**			
Margin: $\sigma_R - \sigma_{ni}$ [µV]	54,7	**6,5**	**3,5**	90,5

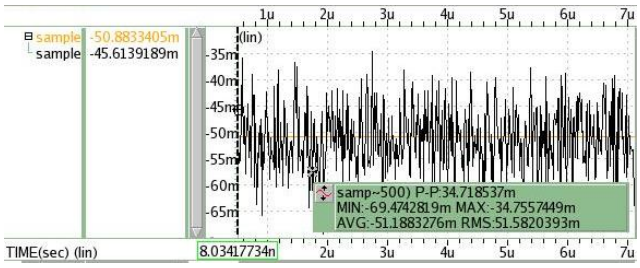

Fig. 8. Transient noise simulation of the comparator in corner 5, having turbo ON, with and without noise for a fixed input voltage of 1 mV, acquiring 500 samples with a noise frequency of 15 GHz and static gain of 50.

D. Kickback noise

The kickback effect or noise [25] is any disturbance coming from an internal stage that causes a re-action to the previous stage. The kickback might not be a critical issue for general signals; however, when we are dealing with a small signal, in the comparator input, it makes the difference between a right and bad decision. The Fig. 9 shows half of the differential pair, where we can state that this type of disturbance propagates to the input terminal, mainly from the current flowing in the capacitances (C_{GS} and C_{GD}) inherent to the transistor. It can also be originated by charge variations at the gate of M_{1P}, when it changes the operating region (cut-off, triode and saturation). Note that these currents exist because v_S and v_{FP} vary.

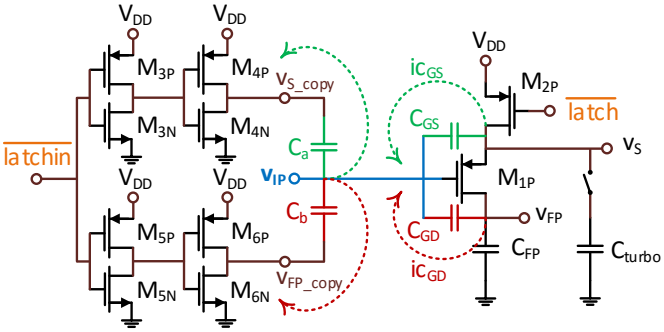

Fig. 9 - Half of the comparator differential pair with parasitic and counter-kickback mechanism.

Having the M_{1P} transconductance constant, during the integration stage, the solution employed to minimize this effect goes through the reproduction of the reverse behavior caused by the parasitic capacitances. Hence, we add two capacitors to the input node, both with a similar value of the MOS parasitic capacitance and on the opposite terminal plate it is applied a signal that tries to replicate an inverted phase of the respective node (namely v_{S_copy} and v_{FP_copy}). The Fig. 10 and Fig. 11 illustrates the result of the kickback effect, during the LSB decision (st_0), without and with the counter-kickback (CK) solution, while the comparator turbo mode is OFF and ON respectively. We can observe that the DAC differential output voltage - v_{DAC} (or the comparator input voltage), during the comparator integration phase (depicted by the rise of v_{fp}), have a more steady behavior with this solution than without it.

Although, the simulation without turbo has a more clear impact of the effect reduction than the one with turbo, the important is to ensure that v_{DAC} has less deviation until the regeneration phase begins. In both cases, the node common voltage,

$$v_{CM} = \frac{v_{CM\ DACP} + v_{CM\ DACN}}{2}, \qquad (19)$$

maintains its behavior, but without turbo v_{DAC} reduces its oscillation (in comparison with the case without the counter-kickback solution) approximately 4 times. In turn, with turbo we have v_{DAC} almost flat during most of the integration stage.

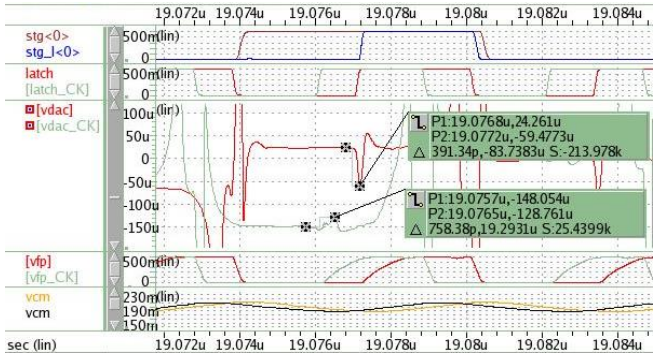

Fig. 10. Comparator input without and with counter-kickback (CK) effect, in typical corner, having turbo OFF.

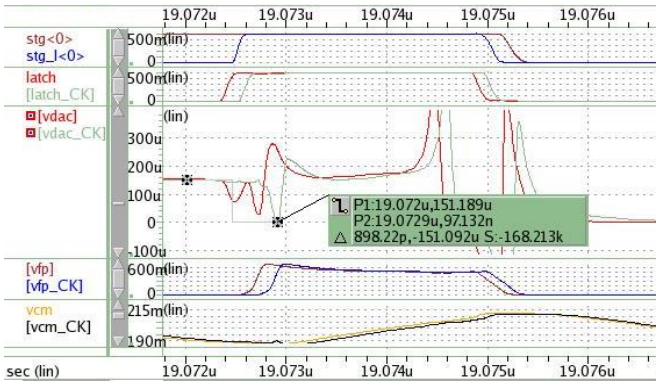

Fig. 11. Comparator input without and with counter kickback (CK) effect, in typical corner, having turbo ON.

IV. Sampling DAC

The sampling DAC was made with two capacitive arrays, having one array illustrated in Fig. 12. Instead of a typical array, this one uses pseudo-binary scaled due to use of redundancy. The redundancy allows a recover of eventual wrong bit decision, which is only possible when the comparator takes more than one decision over a range of voltages, where the search algorithm has already passed.

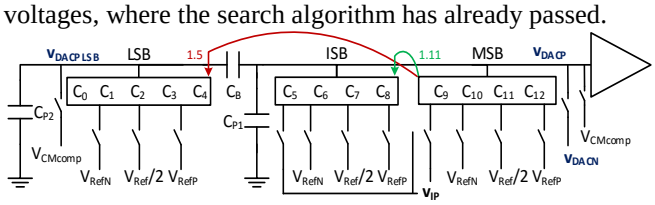

Fig. 12. One branch of the Sampling DAC block.

As stated before, this ADC is conceived to have a 12-bit resolution, for that it demands 12 decisions. However, 2 more decision are added to make redundancy, and rectify wrong MSB decisions, when determining the inferior decision [26]. For that to happen, we use 12 capacitors plus 1 (for digital calibration), employing an array split in 3 groups – MSB, ISB and LSB, as shown in Fig. 12, our redundancy is created by multiplying the capacitors of the last two groups with scale factors.

Attached to each capacitor, there is a block of switches that need to ensure a minimum error for sampling as for conversion. Thus, the switches need to have a small ON resistance, such as it allows to commute the capacitor bottom plate to a selected reference voltage within the required settling times. It should also be small to minimize the voltage drop at its terminal (preventing different reference voltages). There is a mutual dependency between the capacitors and their respective switches to ensure this settling. So, we first sized the capacitors, accordingly to its noise constraint, and then, we size the switches to meet the times with minimal error.

In order to facilitate these commutations and reduce the power consumption, every capacitor in the DAC array are placed to a mid-scale value ($V_{REF}/2$), when the sampling ends. For that to happen each capacitor is split in half and each one is put at different reference voltages. Thus, after sampling, the positive reference voltage (V_{REFP}) is applied directly to one half of C_{unit} (C_a) and the negative reference (V_{REFN}) to the other half (C_b), i.e.

$$\begin{cases} C_a + C_b = C_{unit} \Leftrightarrow C_a = C_b = C_{unit}/2 \\ (V_{REFP} - V_{REFN})\, C_a/(C_a + C_b) = V_{REF}/2 \end{cases}. \qquad (20)$$

A. Sampling DAC Capacitors

The first step to size these capacitors is to determine the unit capacitor (C_{unit}), which is defined by the ratio of the total sampling capacitance (C_{Samp}), from (6), and their binary weighted sum. Thus, choosing the contribution of ISB and MSB group capacitors for sampling (stated in Table I), the binary weighted sum is given by 256.65, which results in

$$C_{unit} = \frac{C_{Samp}}{256.65} \simeq 2.7\ \text{fF}. \qquad (21)$$

Secondly, using a bridge capacitor in the middle of the capacitor array, they were sized accordingly to their group. This bridge capacitor solves size discrepancies, allowing the LSB capacitors to be larger, being less affect by parasitic capacitors, as well as the MSB to be smaller. In a third place, our redundancy is created by multiplying the capacitors of the last two groups with scale factors. The capacitors of the MSB group are binary weighted scaled, since they have a multiplicative factor of 1. However to create redundancy, the capacitors of the ISB group have a multiplicative factor of 1.11 and LSB have a factor of 1.5. While the ISB have multiplicative factor in their capacitance value, the LSB simply increased and their scale factor is produced by adjusting the size of the bridge capacitor.

Table III - Index and binary weight of the Sampling DAC capacitors

Group	C bit index	C bit weight
MSB	$C_9, C_{10}, C_{11}, C_{12}$	$16C + 32C + 64C + 128C$
ISB	C_5, C_6, C_7, C_8	$1.11C + 2.22C + 4.44C + 8.88C$
LSB	C_0, C_1, C_2, C_3, C_4	$0.25C + 0.5C + C + 2C + 4C$
Samp	C_5 to C_{12}	256.65C

B. Sampling DAC Switches

After sizing the switches for the MSB capacitor, respecting the time constraints, the following switches were scaled binary. However due to leakage current their topology had to be customize as depicted in Fig. 13. In addition, every capacitor have their top plate connected to a shared node (V_{DACP}) that is linked to other two switches, the comparator biasing switch (CM) and the one that short-circuits the comparator input (SC).

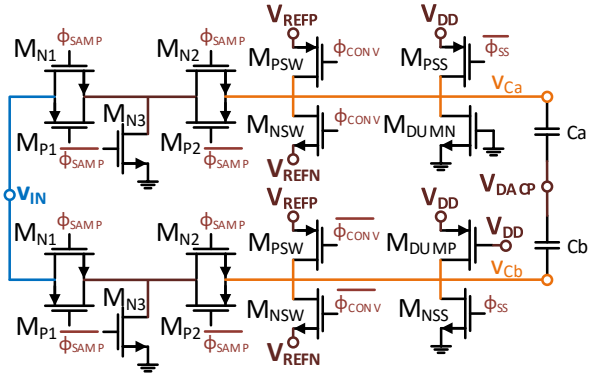

Fig. 13. Sampling DAC switches block for one bit-capacitor (split in C_a and C_b) from side V_{DACP} of the array.

Here, instead of using just one NMOS as a sampling switch, there are five in a T-scheme. Both M_{N1} and M_{N2} correspond to the sampling switch, whether M_{N3} creates a path for current leakage that is caused by the input signal during the conversion phase. Moreover, the PMOS added in parallel are used to help the sampling connectivity for larger input signals, since their inner resistance behaves inversely to the NMOS.

Now, we illustrate in Fig. 14 the Sampling DAC switches during sampling, focusing just one of the capacitors in that situation. Now, the operating transistors behave as resistors, namely the sampling (M_{N1}, M_{N2}) and biasing switches of the DAC, and the ones that are cut-OFF behave as current sources, namely the rest of the switches (M_{N3}, M_{PSW}, M_{NSW}, M_{DUMP}, M_{DUMN}, M_{PSS} and M_{NSS}), due to their continuous leakage current.

Likewise, we represent in Fig. 15 the situation during the conversion phase, where, now, only the reference switches (M_{PSW}, M_{NSW}) behave as resistors and the rest as current sources. The M_{N3} will drain the leakage interference from the input signal and the M_{DUMP}/M_{DUMN} will try to counter-balance the leakage from the reference switch that is not selected.

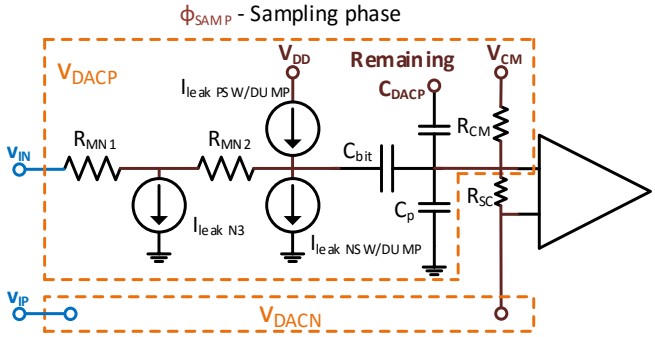

Fig. 14. Sampling DAC switches during sampling phase.

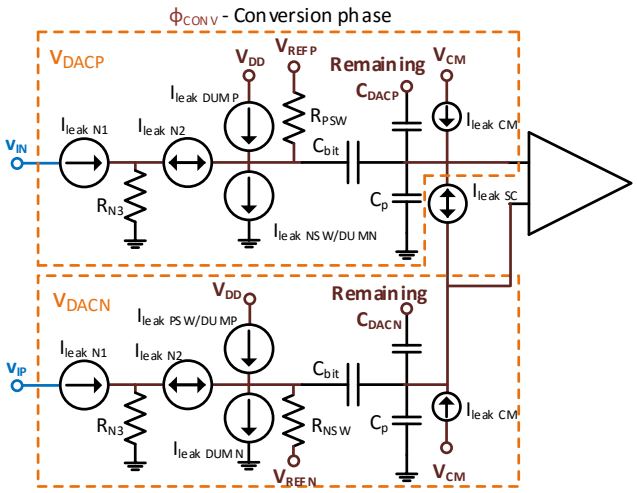

Fig. 15. Sampling DAC switches during conversion phase.

In addition, the switches used during sampling required a better biasing voltage to ensure smaller resistance and quicker settling times. For that matter we employed the clock-boost illustrated in Fig. 16, which basically combines the sampling input voltage with a percentage of the circuit voltage supply.

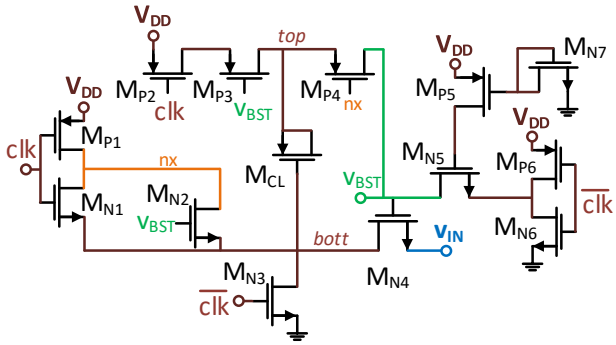

Fig. 16. Clock-boost circuit schematic.

V. State Machine

Although the ADC has an asynchronous behavior, it is only resultant of the different time of each bit conversion. In fact after each bit decision the comparator is disabled for a fixed time (that allows the voltage of the capacitors to stabilize). The state machine (illustrated in Fig. 17) assures this fixed time

thanks to a custom delay cell, which mimics the behavior of the DAC switching references (depicted in Fig. 18).

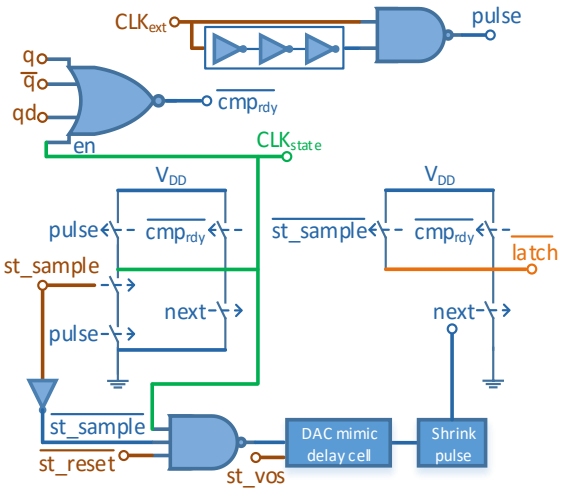

Fig. 17. Delay block logic circuit representation.

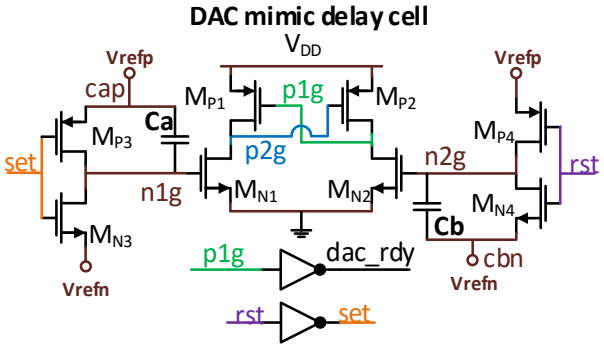

Fig. 18. Delay cell that mimics the DAC switchings.

This state machine is centralized in a delay block that, depending on the comparator outcome, creates the control signals of the comparator ($\overline{latch}$) and the ring counter (CLK_{state}). It produces a total of 17 consecutive states of the per period, as shown in Fig. 19.

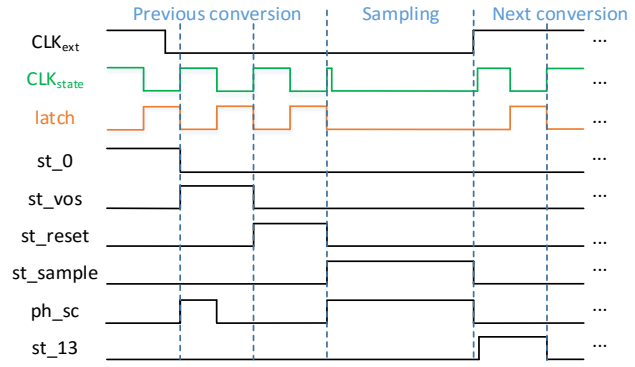

Fig. 19. ADC sequence example of sampling and conversion states for a slow conversion case.

VI. Calibrations

About the non-linearity issues we can state that their origin is mainly from the sampling DAC block, due to capacitors mismatches. However, it can be mitigated by a digital calibration. On the other hand, the comparator might insert an offset voltage, which can cause wrong bit decisions. Although those possible errors could be recovered by redundancy, the digital calibration that we intended to use requires a comparator with low offset voltage.

The static non-idealities of linear circuits are decomposed in offset, gain errors and non-linear errors, so ADCs are inherently non-linear, but they can be modeled as a linear system, by highlighting the sources of those errors in the circuit. Thus, the Fig. 20 pinpoints the gain errors (G_{Esh}, G_{Edac}) in the ADC, which estimated through a digital calibration (of the sampling DAC) can fix the output digital word (i.e. the ADC transfer function, regardless of the DAC).

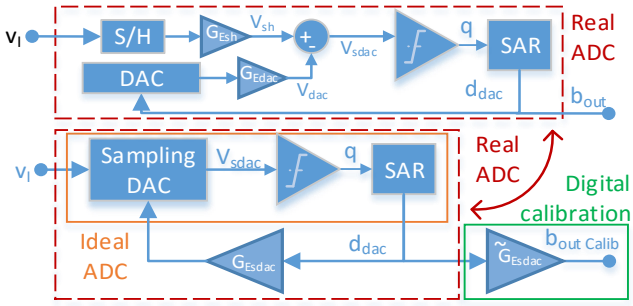

Fig. 20. Sources of non-linearity and gain errors solved with digital calibration.

Likewise, the Fig. 21 pinpoints the offset error in the ADC, which can be referred just as one source at the ADC inputs, however, since the sampling DAC is treated with a digital calibration, the real impact of this error falls upon the comparator decision, hence the ADC only requires an offset voltage calibration for the comparator.

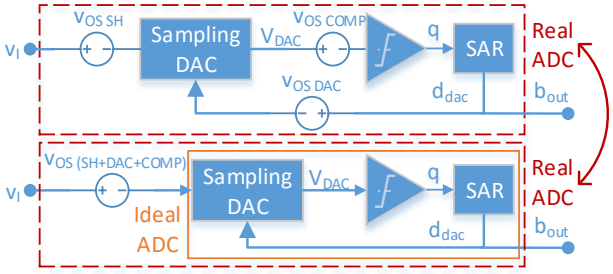

Fig. 21. Offset voltage source.

VII. Conclusions and Future Work

The challenge of this project was to create a functional SAR ADC with transistors supplied at 0.5 V, though their nominal voltage were 0.9 V. Briefly, it turns difficult to obtain low ON-resistance switches and to contain the significance of leakage current. Thus, it results in slow switchings and increased difficulty to contain the charge in the nodes.

A. Achievements

The comparator was aimed to operate at a maximum sample rate of 500 kS/s, based on 16 corners plus the typical one. However, corner 2 had to be discard, since it implies a scenario that requires around 4 times larger sizes of the transistors than the second slowest corner (14). Even so, this case was only

ensured by using a turbo mode that adds an extra capacitor to integration node of the comparator. This provides a higher voltage than the supply, accelerating the integration phase and, thus, the overall conversion time. Although, this method brings the advantage of internally producing a voltage higher than the supply (without requiring other external voltage), at the expense of more occupied area. It requires a greater complexity in its control circuit as well as in the adjustment of the counter-kickback effect.

The sampling DAC required a custom topology for its block of switches, in order to mitigate and balance the leakage current, when those switches are OFF. In addition, clock-boosts are employed to drive the gates of the transistors used for sampling.

The last efforts in this work were fixed in an attempt to solve the offset calibration with an analog calibration. Unfortunately the explored topology was successful due to leakage current. Revising the state of art works, they suggest a re-sizing of the comparator with transistors with bigger dimension. Since the transistors become less susceptible to offsets at the cost of increasing their consumption. However, as seen in this project, enlarging the transistors sizes is not enough to solve this matter. Hence it leads to believe that, to maintain the explored topology, we should use transistors with less leakage current, such FinFets. Or else apply another topology more complex.

Revising the primary goal of this project, it was not complied. Since top simulations have not been acquired, which allow the ADC characterization, the designed converter cannot be proved to be operational. Nor a proper solution for the comparator offset calibration was found. Nonetheless, we can point out the difficulties faced, between corners, to size each block of the ADC, with some suggestion for topologies to deal with the significant leakage current.

B. Future Work

- Improve the comparator turbo mechanism.
- Simulate and re-size the blocks with non-ideal reference voltages;
- Optimize the delay chains, instead of using simple chains of inverters with higher length values and re-adjust the DAC delay cell;
- Optimize the circuit that generates the driving phases of the switches, namely the short-circuit pulse before the offset calibration state;
- Improve the comparator counter kickback voltage mechanism by creating a more complex logic that mimics better the integration voltage node, and also adjusting in two operating modes for using turbo ON and OFF;
- Explore a better (and functional) calibration topology for the comparator offset voltage.
- Design and simulate the respective layouts of every block.

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