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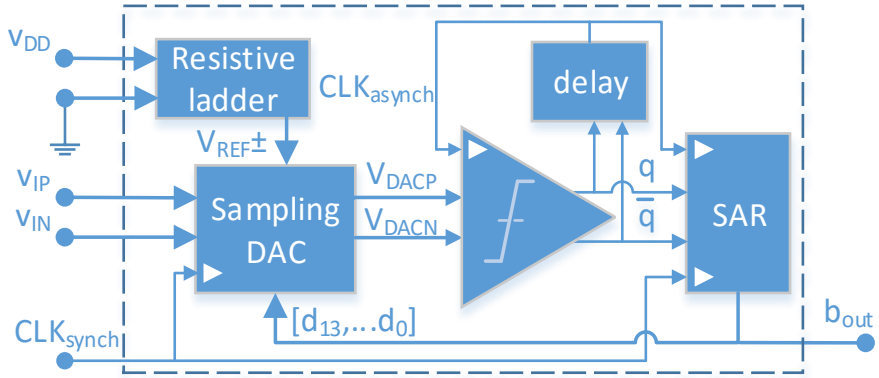

Very low power consumption SAR ADC for wireless sensor networks

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Thesis to obtain the Master of Science Degree in

Electronics Engineering

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I would like to dedicate this work to my family and the Portuguese social services that allowed me to persecute this extension of my education. I also give a special dedication to those who already departed, namely my grandfather and father, Manuel and Rui de Pádua, and a firefighter friend, Bernardo Figueiredo.

Abstract

Nowadays, there are more and more autonomous wireless sensor networks, for many different applications and, as its title suggests, each one of these devices must be independent and supply itself. Although the majority of these devices require a long lasting battery life, it is possible to employ energy harvesting devices, which transform the energy present on its environment into electrical energy. This way, there is a demand for better topologies featuring low power consumption circuits. This work focuses on one module of these sensors – the analog-to-digital converter (ADC) – which translates the (physical) analog signals to the digital domain, where they will be processed.

This study aims to design a SAR ADC (analog-to-digital converter based on successive approximations) with an extremely low power consumption, in an advanced CMOS technology (28 nm), following the industrial methodologies IC. This project was conducted in partnership with Synopsys, operating at a supply voltage of $0.5\,\mathrm{V} \pm 10\%$, with a resolution of 12 bits and 500 kS/s sampling frequency.

Keywords:

Analog-to-Digital Converter (ADC), Successive-Approximation Register (SAR), low power consumption, Integrated Circuit (IC).

Resumo

Atualmente, há cada vez mais e mais redes de sensores autónomos sem fios, para diversas aplicações, e, como o título sugere, cada um destes dispostivos deve ser independente e capaz de se auto-abastecer. Embora a maioria destes dispositivos requeiram baterias de longa duração é possível aplicar dispositivos de colheita (harvesting), que transformam a energia presente no ambiente, onde se inserem, em energia elétrica. Desta forma, existe uma procura por melhores topologias para circuitos de consumo de baixa potência. Este trabalho foca-se num módulo destes sensores – um conversor analógico-digital (ADC) – que traduz sinais (físicos) analógicos para o domínio digital, onde serão processados.

Este trabalho visa projectar um SAR ADC (conversor analógico-digital baseado em aproximações sucessivas) com um consumo de potência extremamente reduzida, numa tecnologia avançada CMOS (28 nm), seguindo as metodologias industriais de IC. Este projecto foi realizado em parceria com a empresa Synopsys, operarando a uma tensão de alimentação de $0.5\ \mathrm{V} \pm 10\%$, com uma resolução de 12 bits e 500 kS/s de frequência de amostragem.

Palavras-chave:

Conversor Analógico-Digital (ADC), Registo de Aproximações Sucessivas (SAR), Consumo de baixa potência, Circuitos integrados (IC).

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Acronyms

ADC	Analog-to-Digital Converter
CB	Clock-Boost
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Converter
DNL	Differential Non-Linearity
ECG	Electrocardiographic
ENOB	Effective Number of Bits
FoM	Figure of Merit
IC	Integrated Circuit
ISSCC	International Solid-State Circuits Conference
INL	Integral Non-Linearity
KCL	Kirchhoff Current Law
LSB	Least Significant Bit
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MSB	Most Significant Bit
OPAMP	Operational Amplifier
PG	Power Gating
PVT	Process-Voltage-Temperature
S/H	Sample-and-Hold
SAR	Successive-Approximation Register
SNDR/SINAD	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion
TSMC	Taiwan Semiconductor Manufacturing Company, Ltd
$\mathbf{V_{FS}}$	Full-Scale input range
VLSI	Very Large Scale Integration Circuit
WSN	Wireless Sensor Network

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1. Introduction

1.1. Motivation

Society has enlarged its number of communication points, there are more and more autonomous wireless sensor networks (WSN), and hence both the consumer and the industry share a need that rises the demand for superior energy lasting devices. Since it is hard and expensive to develop new types of batteries, electronic circuits must consume less. These devices are commonly named sensor node circuits, and should operate at extremely low power and be as small as possible to reduce the manufacturing cost of chips. The trend to make these sensors more independent, as illustrated in Figure 1-1, is to combine them with energy harvesting circuits, which supply themselves by transforming some energy from the surrounding environment into electrical energy.

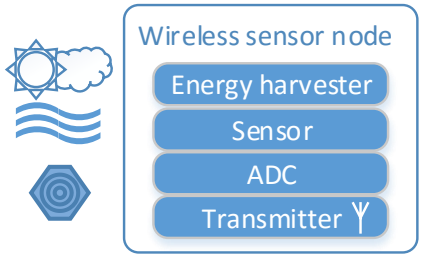

Figure 1-1 - Simplified wireless sensor node.

This work focuses on one module of these sensors, namely in the development of an analog-digital converter (ADC). This module translates analog signals (e.g. sound, temperature, light intensity, humidity) to the digital domain, where processing is easier. Therefore, there are several applications for WSN, where ADCs are employed, essentially for health care, environmental and industrial monitoring. An example of this are the implantable healthcare microelectronic systems that convert the human body physical signals, such as electrocardiographic (ECG), into digital signals, and whose usual location is difficult to re-supply (e.g. near the heart). Industrial and environmental disasters can be avoid, such as a forest fire by placing sensors nodes, in a selected region, to measure temperature, humidity and gases which are produced by fire in the vegetation. Likewise, they can be used for monitoring temperature and water level in tanks of nuclear power plants, as to control the air/water pollution (or waste) of any factory, etc. Thus, whether it is for a need of health, safety or comfort, there is a demand for ADCs.

Over the years, the evolution of transistor scaling technology allows the creation of circuits that occupy a smaller area, which is aligned with the interests of reducing manufacturing cost of chips (Integrated Circuits – IC). However, the diversification of topologies does not follow this evolution, so the usual practice of the industry is to migrate their products, namely ADCs, for more advanced technologies. Meanwhile, when one intends to obtain lower power consumption, a direct way of doing so goes by cutting the supply (even below the transistors nominal voltage value) and adapting the ADC specifications (resolution, sampling frequency and bandwidth), as well as making the necessary adjustments to the topology.

Between the different architectures of ADCs the most common known are the Flash, the SAR (Successive-Approximation Register) and the Pipeline. Depending on the specifications and regarding the area, SNR (Signal-to-Noise Ratio) and FoM (Figure of Merit), the most efficient might be the SAR topology. It only requires one dynamic comparator and follows a recursive algorithm (consuming less resources). Therefore this study aims to design a SAR ADC with extremely low consumption, in advanced CMOS technology (28 nm) from Taiwan Semiconductor Manufacturing Company, Ltd (TSMC), following the industrial methodologies IC. This project is conducted in partnership with Synopsys, having access to their exclusive software tools in its facilities, operating at a supply voltage of $0.5\ \mathrm{V} \pm 10\%$, with a resolution of 12 bits and 500 kS/s sampling frequency.

1.2. Goals

The main goal of this work is to develop an Asynchronous SAR ADC with 12 bit resolution, 500 kS/s sampling frequency and 0.5 V ± 10% supply voltage, which should be able to convert analog signals with a differential full-scale input range of 1 V. The design process ought to cover 16 PVT (process, voltage, temperature) corners, whose temperature range from -40 to 125 ºC, and ensure a noise relation SNR above 65 dB, regarding the thermal noise. Having non-linearities of INL/DNL below 1 LSB and an effective number of bits (ENOB) above 10.

1.3. Document structure overview

This report is divided in 5 sections, by first identifying the operational field and goals of this project. Chapter 2 presents some basic concepts and metrics applied to ADCs, which are performed to measure and characterize them. It also features an explanation and distinction between Nyquist rate and oversampling ADCs.

Chapter 3 explains the reasons and characterizes the chosen architecture, SAR ADC, as well as providing some works of state of the art works in low power implementations, where their common and differ points are emphasized.

Chapter 4 features the design steps for the proposed ADC, specifying the noise and time constraints and, then, explaining in a more thorough way the dynamic comparator and the sampling DAC blocks. Showing the theoretical model approach and followed by the practical implementation, mainly stressing the way of dimensioning while dealing with the leakage current. Moreover, it also explains the coordination of the state-machine mechanism and the suggested calibrations for the two main blocks.

Finally, in chapter 5, the conclusions for this work are disclosed, as well as some suggestion for future work.

2. General ADC architectures

This chapter defines the metrics and concepts used to characterize and understand ADCs, and compares Nyquist rate and oversampling ADC arquitectures.

2.1. Metrics and concepts

The purpose of an analog-to-digital converter (ADC) is to capture analog signals (continuous in time and amplitude) and translate them into the digital domain (discrete signal in time and amplitude), whereas the digital-to-analog converter (DAC) performs the inverse translation. Hence, at first the input signal is sampled at a certain rate (f_S – **sampling rate**), becoming a time discrete signal; then it is quantized (becoming discrete in amplitude). Then, encoding is performed, to the discrete in time and in amplitude signal as a binary number with a certain number of bits (N – **resolution**). To understand the ADCs characterization is necessary to define some concepts and parameters used to evaluate its performance, namely its static and dynamic behavior.

The characterization of an ADC regarding its static performance is given by the parameters that characterize the deviation of the actual transfer function from the ideal one (measuring the offset). The ADC can distinguish 2^N input voltage regions, meaning that its output ranges from 0 to $2^N - 1$, when the input voltages goes from V_{MIN} to V_{MAX}. To obtain this, the **full-scale input range** (V_{FS}) of the ADC is

$$V_{FS} = V_{MAX} - V_{MIN}. \tag{2.1}$$

For the quantization process it is necessary to properly define the code transition levels, the quantization step, error and noise. The difference between two code transition levels is called **quantization step** (Δ),

$$\Delta = \frac{V_{FS}}{2^N} = V_{LSB}\,. \tag{2.2}$$

The **code transition levels** are the values of input voltage that translate the transitions of the output code. The input voltage value that produces a transition between the codes $n - 1$ and n is

$$V_T[n] = V_{MIN} + \, n \times \Delta\,, \tag{2.3}$$

where the digital code (n) and output bits (b_i), are related by

$$n = \sum_{i=0}^{N-1} 2^i b_i\,. \tag{2.4}$$

Some loss of information is inherently to the quantization, originating a **quantization error**, illustrated in Figure 2-1 similar to a sawtooth wave, with peak-to-peak amplitude of one quantization level and uniform distribution, which can be regarded as noise (**quantization noise**), whose power is given by

$$\overline{v_{n,Q}^2} = \frac{\Delta^2}{12}. \tag{2.5}$$

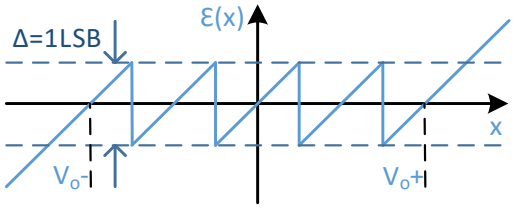

Figure 2-1 - Quantization error.

The Figure 2-2 illustrates the gain error, which is the difference between the ideal and actual slope transfer functions, and the offset error, which is the constant difference between the ideal and real voltages for every transition level (i.e. a shift to the right of the ideal transfer function). Both of these errors are usually denominated linear static errors because they do not produce distortion.

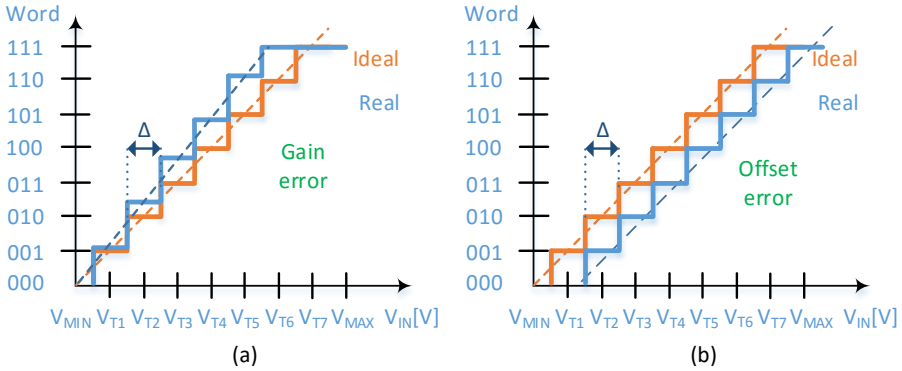

Figure 2-2 - Examples of ADC's Gain error (a) and Offset error (b).

Static non-linearity is characterized by the **Differential Non-Linearity** (DNL) and the **Integral Non-Linearity** (INL) as presented in Figure 2-3. The DNL measures the difference between the ideal and actual code widths for every transition level, being zero when these transition are equally spaced, and so every code width equals the quantization step [1], [2], being express as

$$DNL[n] = \frac{V_T[n+1] - V_T[n]}{\Delta} - 1\,, \tag{2.6}$$

where $n = 1 \ldots (2^N - 2)$. In turn, the INL measures the deviation between the real and the ideal of transfer function,

$$INL[n] = \frac{V_T[n] - V_{ideal}[n]}{\Delta} = \frac{V_T[n] - V_{ideal}[1]}{\Delta} - (n-1), \tag{2.7}$$

where $n = 1 \ldots (2^N - 1)$.

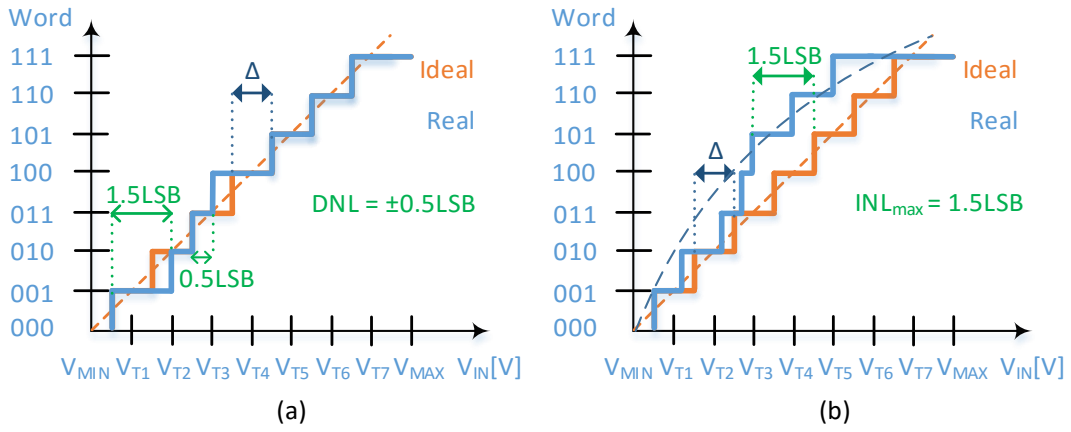

Figure 2-3 - Examples of ADC's DNL (a), INL (b) measures.

Besides these errors and non-linearities, an ADC can be classified regarding its monotonicity, which is a way to verify if the output signal behaves proportionally with the input signal, i.e. if the input signal increases then the output will also increase and vice-versa. As seen in (2.6), the ADC is monotonic if the DNL is higher than -1.

Whereas static imperfections (such as gain and offset), which are quantified in a direct way, real converters have additional noise sources and distortion processes that cause imperfections in the ADC dynamic behavior, degrading their performance [3]. The characterization of dynamic performance of the converter relies in usual parameters applied for linear circuits and these are measured through a Fast Fourier Transform (FFT) at the output sequence. The ratio of the signal power (P_{signal}) and noise power (P_{noise}), whose origin comes from every type of noise (ex: thermal, flicker), quantization error, etc, is denominated as **Signal-to-Noise Ratio** (SNR), given by

$$SNR[dB] = 10\log_{10}\frac{P_{signal}}{P_{noise}}. \tag{2.8}$$

In turn, considering only the quantization error, the maximum value of the SNR achieved by an ideal ADC is

$$SNR_{max}[dB] = 1.76 + 6.02 \times N, \tag{2.9}$$

where N is the ADC resolution.

The non-linearity of a circuit produces the occurrence of spectral components in multiple frequencies of the input signal, which is measured by the **Total Harmonic Distortion** (THD). This measure relates the power of the harmonic content in the digital output of the converter ($P_{i,f1}$) with the power at the fundamental frequency (P_{f1}), as

$$THD[dB] = 10\log_{10}\frac{\sum_{i=2}^{k+1} P_{i,f1}}{P_{f1}}, \tag{2.10}$$

where k is the number of harmonics taken in account, P_{f1} is the power of the fundamental frequency and $P_{i,f1}$ is the power of harmonic i. It is also possible to define the **Signal-to-Noise and Distortion Ratio** (SNDR, also known as SINAD),

$$SNDR[dB] = -10\log_{10}\left(10^{-SNR/10} + 10^{THD/10}\right). \quad (2.11)$$

The parameter that allows an easy evaluation of the real and dynamic performance of the converter is the **Effective Number of Bits** ($ENOB$) expressed by

$$ENOB[bits] = \frac{SNDR - 1.76}{6.02}. \quad (2.12)$$

As shown in (2.12), the higher the noise and distortion, the lower the $ENOB$ will be, in other hand the performance of the converter is better for higher ENOBs (being at most the same value as N bits).

A typical parameter of comparison between converter implementations is the **Figure of Merit** (FoM) that is a numerical quantity based on one or more characteristics of a system or device, representing a measure of efficiency. This parameter is often used as a benchmark tool to convince consumers to choose a particular brand, and among the existing figures we can point the $Walden\ FoM$ [4], which relate the ADC power consumption ($P_{Consumption}$), the sampling rate (f_S) and the $ENOB$, as

$$FoM[\text{fJ}/c.s.] = \frac{P_{Consumption}}{f_S \times 2^{ENOB}}. \quad (2.13)$$

This shows the usual trend of the ADCs that for each one bit increase, the power consumption should double, in order to maintain the same FoM value. The same can be said if the sampling rate has also been doubled.

2.2. Oversampling vs Nyquist rate converters

The ADCs can be separated into two categories depending on the sampling rate and on how their output is generated [5], [6]. To help visualize the operating frequency of both categories, Figure 2-4 illustrates their respective spectrum and when there is undesired spectrum overlap – aliasing. The first category of the converters are called **NR (Nyquist rate) ADC**, which in theory can sample signals with a bandwidth until $f_S/2$.

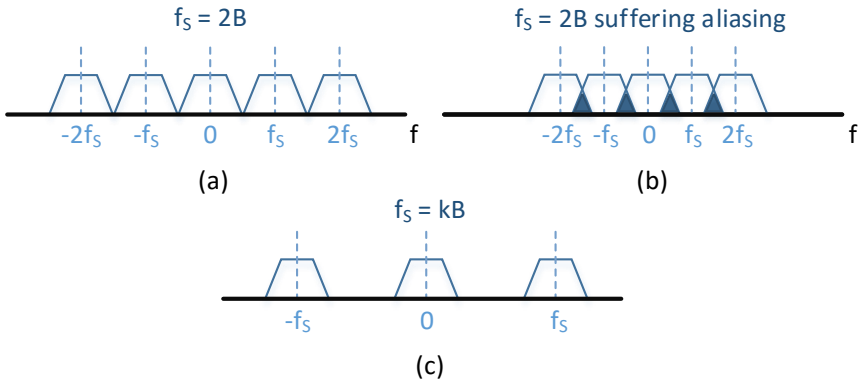

Figure 2-4 - Frequency domain for (a) Nyquist rate converters, (b) the aliasing that occurs and (c) an oversampling converter, where *B* is the signal bandwidth and *k* a multiple constant.

Although in practice they require anti-aliasing filters, what leads to a sampling rate of

$$f_S \geq 1.5 \times f_N = 1.5 \times (2B), \tag{2.14}$$

where f_N is the Nyquist rate and B is the bandwidth of the signal. These ADCs generate a series of output values with a direct (one-to-one) correspondence to a single input value. Likewise, a NR DAC would generate a series of analog output levels, where each level is a result of a single N-bit input word.

The second category is called **OSR (oversampling rate) ADC**, because this type samples the signal at a rate much higher than the signal bandwidth, typically 10 to 512 times the Nyquist rate, generating an output based on a mean of the input samples. In Figure 2-5 we can see the typical blocks from the referred converters, outlining the difference between the analog and the digital ones. The Nyquist rate ADC appear to have more blocks than the oversampling ADC, because this one relax the requirements placed on the analog circuitry at the expense of more complicated digital circuitry [7]. However, both converters have their input signals sampled, quantized and encoded, and they might need an anti-aliasing filter, without requiring a strict Sample-and-Hold (S/H) block.

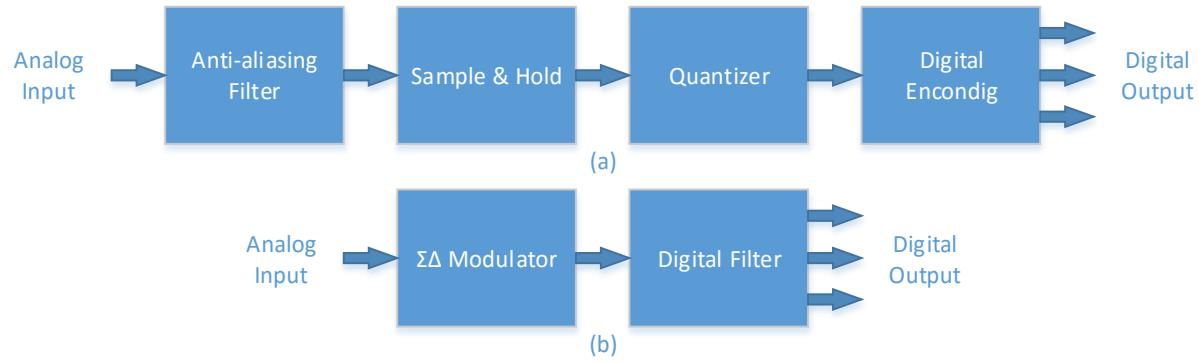

Figure 2-5 - Typical block diagram: Nyquist Rate ADC (a) and oversampling ADC (b).

The oversampling ADCs perform their quantization with a modulator and the encoding with a digital filter. Usually a sigma-delta modulator is used since its output is a pulse-density modulated signal that represents the average of the input signal. Constructing these pulses in real time, it leaves off any need to hold the input value and perform the conversion. A conventional N-bit oversampling ADC fixes a certain bandwidth and reduces its noise by using high sampling rates and, constantly, filtering the frequencies above that band ($f_S/2$). To exemplify this ADC, the first order sigma-delta converter is explained, while the Nyquist rate ADC will be more detailed in the next section.

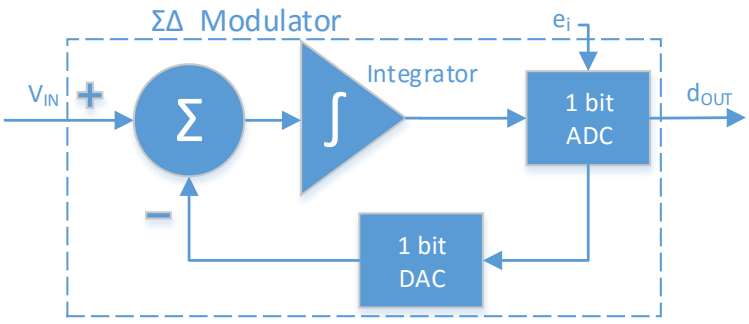

Figure 2-6 - Typical block diagram: first order sigma-delta modulator.

The first order sigma-delta modulator, presented in Figure 2-6, works in each cycle with only 1 bit through an integration process. At first, the internal signal produced form the DAC, which adds (shaped) white noise to the input signal (also known as dither), is subtracted to the input signal (v_{IN}). Secondly, the residue (resulting signal) is integrated, in a given period of time, and applied to a 1-bit ADC (often made by one clocked comparator), which produce a bit stream – d_{OUT}. In turn, as seen in Figure 2-5, d_{OUT} is applied to the digital filter (low passing filter) that performs a mean value of the input.

In a cyclic way, thanks to a large amount of samples, the modulator shapes the noise along the spectrum, where, as shown in Figure 2-7, a large amount of quantization noise is put out of the desired bandwidth. Then, using a sampling rate (f_S) far higher than the Nyquist rate (f_0), the digital filter chops the desired bandwidth from the rest of the spectrum. The core die size of this converter will not change with resolution, although its component matching requirements double with every bit. It addition, its complexity increases as high order digital filters are demanded.

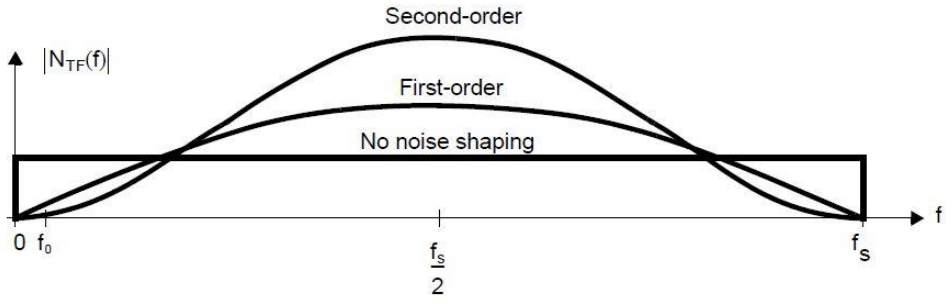

Figure 2-7 - Some different noise-shaping transfer functions [8], where f_0 is the Nyquist rate.

The choice between converters always rely in a tradeoff between consumption, resolution, conversion rate and technology node, where it is easy to deduce that the higher the resolution and the sampling rate then the higher the power consumption needs to be. Oversampling converters are popular for high-resolution medium-to-low-speed applications such as high-quality digital audio and baseband signal processing in some wireless systems [6]. They improve resolution, reduce noise and help avoiding aliasing and phase distortion by relaxing the anti-aliasing filter, compensating with its digital filter. This tradeoff became desirable with the advent of deep submicron CMOS technologies as complicated high-speed digital circuitry became more easily realized in less area. However, the realization of high-resolution analog circuitry was aggravated by the low power-supply voltages and poor transistor output impedance caused by short-channel effects [6]. Although there is no fine line that distinguishes what is the best converter, for this work the oversampling converter was not considered.

2.3. Nyquist rate ADC architectures

The Nyquist rate ADC category is illustrated through its most common topologies, presenting their typical characteristics [1]. This allows a distinction of one topology over another, leaving the SAR converter to be explained more ahead. As depicted in Figure 2-8, the **full-flash ADC** has four blocks, one S/H block, one resistive ladder, one set of comparators and one encoder logic block. At first, the input signal is captured in the S/H block. Secondly, the resulting signal is compared simultaneously with reference voltages that through the encoder logic will originate a matching digital word. This converter

can perform a parallel conversion for every bit, allowing high speed conversion, but it has low/medium accuracy and a high power consumption, due to its number of reference components and comparators, given by 2^{N-1}. It employs a thermometer code (since it resembles a mercurial thermometer) implemented with a reference ladder (typically by resistors) for comparisons of voltage or current. While the resolution increase (limited by component matching), its conversion time almost does not change, however its die size and power consumption vary exponentially.

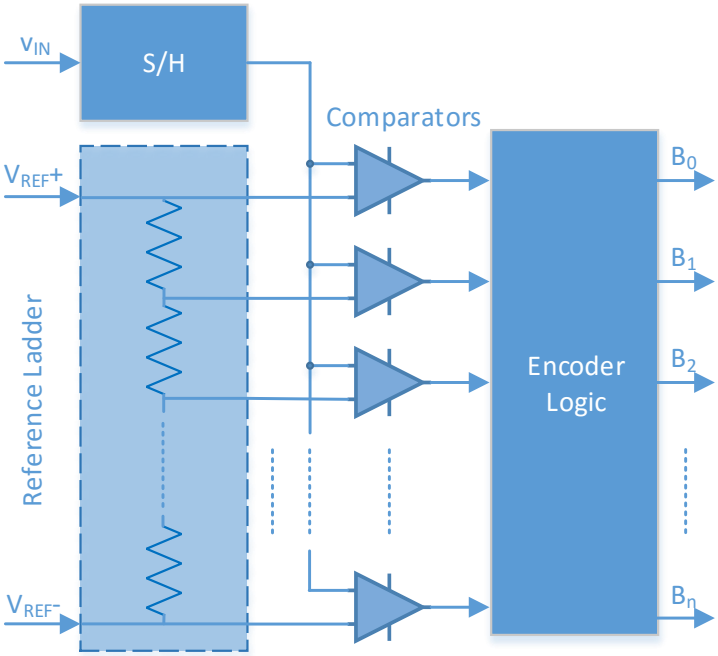

Figure 2-8 - Typical block diagram: Flash ADC.

In Figure 2-9 is shown the **dual slope** (or Integrating) **ADC**, which is known as voltage to time converter and makes its conversion in two steps. Its integrator block is composed by a single amplifier with an RC loop, where, at first, integrates the input signal (v_{IN}) during a fixed time (T_1). Then, at a second step, integrates a reference voltage (V_{REF} – with an opposite signal to v_{IN}) until the previous integrated voltage reaches zero, what takes a variable time (T_2).

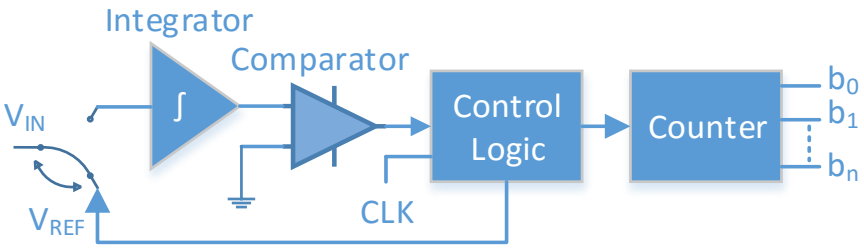

Figure 2-9 - Typical block diagram: Dual slope or Integrating ADC.

As illustrated in Figure 2-10, in a first step, v_{IN} is used to create a ramp during T_1 (with a variable slope), charging the integrator capacitance to its maximum voltage value. Then, in a second phase,

another ramp (with a fixed slope) is made by discharging the previous capacitor, while counting a set of internal clock pulses (2^N clock cycles), produced by the control logic. This way, the time of the second step is directly proportional to v_{IN} with a relation given by

$$T_2 = -T_1 \left(\frac{v_{IN}}{V_{REF}}\right). \tag{2.15}$$

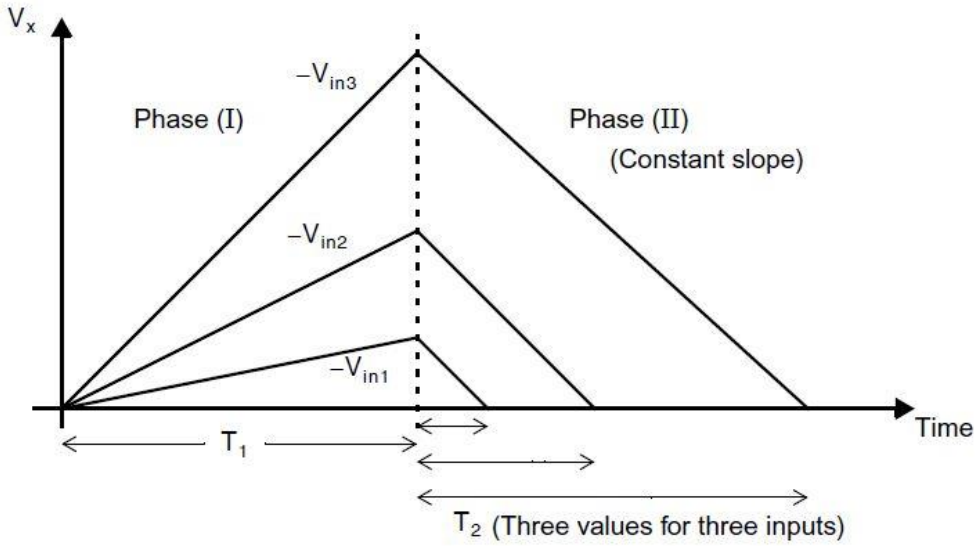

Figure 2-10 - Integrating (Dual Slope) ADC conversion [9].

The core die size of this converter will not change with the increase of each bit of resolution, but its conversion time doubles. Although, it has slow conversion rate and course accuracy, it has high linearity, low power consumption, good noise performance to monitor DC signals. It is regularly chosen for voltmeters or multimeter devices.

The **pipeline ADC** performs an iterative search of a digital code that accurately reflects the analog input signal. However, rather than perform the iterations with a single analog circuit, pipelined converters have a separate analog stage dedicated to performing each iteration [6]. As it can be seen in Figure 2-11, the input signal is sampled and held, the MSBs are converted and released to the output, and then its correspondent voltage is subtracted to the original input signal, originating a residue. This residue is applied to the respective residue amplifier (because of its small amplitude), which enlarges the voltage scale of the next conversion. This process is repeated in every stage until the last bit conversion is reached. Note that the depicted figure is very generic, the number of bits converted in each stage can theoretically be very different, however in practical cases each stage operate with the same number of bits (1 or 2 bits).

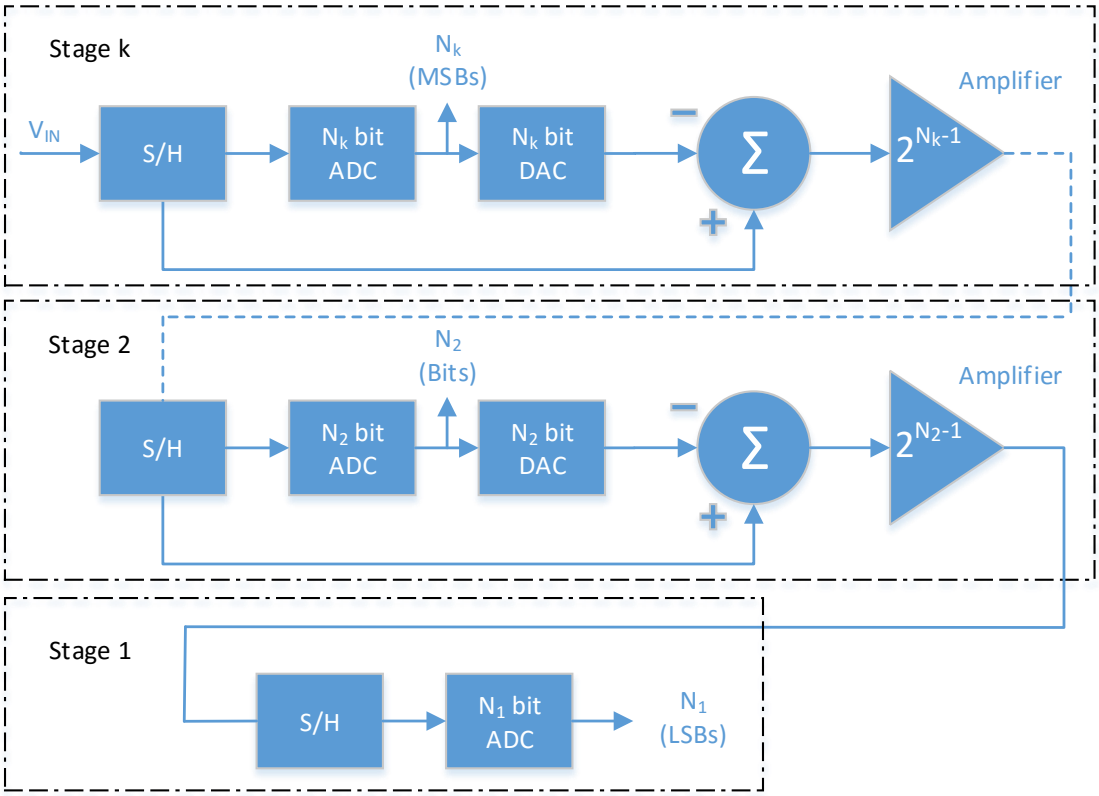

Figure 2-11 - Typical block diagram: Pipeline ADC of k stages.

This converter is generally chosen for high speed, with a wide selection of sampling frequency and resolution. While increasing resolution, its conversion time and its core die size increase linearly, due to the increased number of stages, which consequently also increases its latency (the sum of the delays of every stage), power consumption, settling errors and noise.

In short, besides the previously presented, there are more converters, as well as hybrids, and among them are the denominated algorithmic converters, which are based on comparisons, as the pipeline and the SAR ADC (ADC based on successive-approximation). This last converter follows a recursive algorithm that allows using less components than the pipeline, what tends to occupy less area and, consume less energy. Moreover, it also enables a wide selection of resolution for an acceptable range of sampling rate.

3. SAR ADC Topology

The ADC is one of the most important circuits in sensor nodes, so a solution to reduce the sensor power consumption is to fabricate the ADC with a SAR topology, since is suited for low voltage and low power operation. The data in Figure 3-1 support this idea, where we can see that, in the past decade, the ADCs research projects (presented at conferences) have chosen more and more this topology. Hence, the performance of the SAR ADC improved as depicted by the evolution of its FoM, even obtaining the best results in the last seven years between the converters presented.

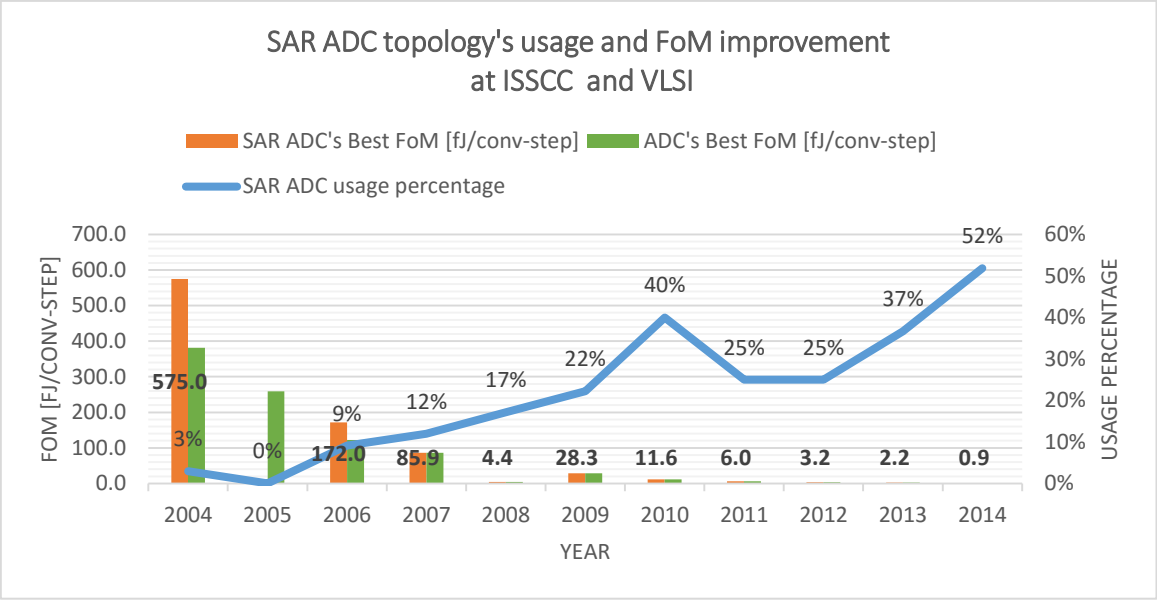

Figure 3-1 - SAR ADC topology's usage and FoM improvement at ISSCC and VLSI, along the last decade, from Prof. Boris Murmann's survey [9].

Reinforcing the idea, Figure 3-2 presents the same database filtered for a group of SARs with a SNR between 60 and 70 dB, which shows that, around the SNR we want, the SAR also has the best FoM.

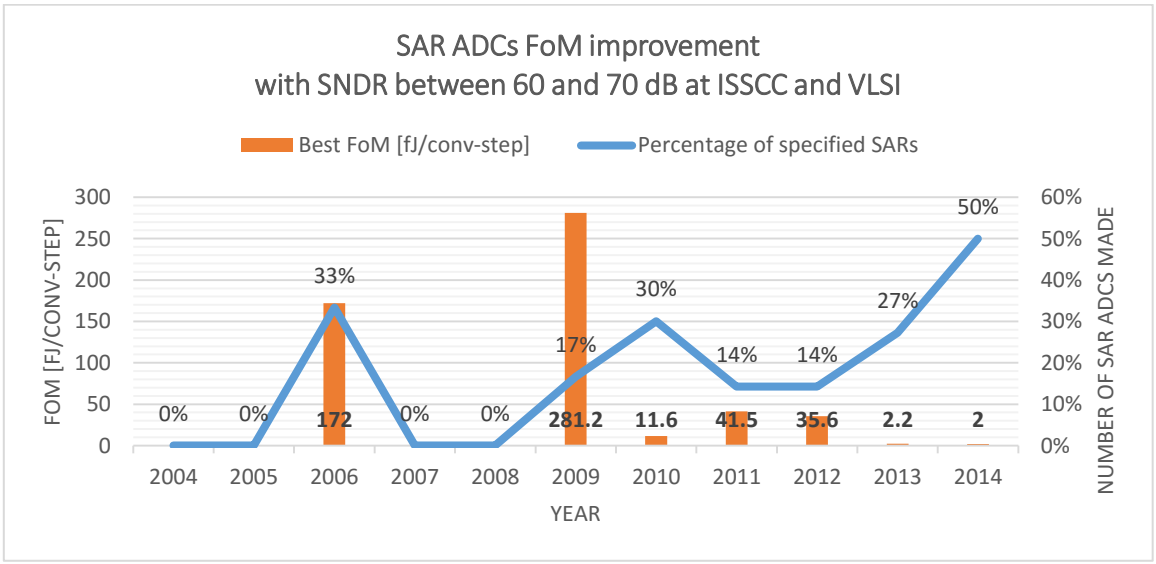

Figure 3-2 - Evolution of SAR ADCs FoM performance with a SNR between 60 and 70 dB at ISSCC and VLSI, along the last decade, from Prof. Boris Murmann's survey [9].

Moreover, a few distinctions can be made between the previously mentioned topologies, namely the sigma-delta and the pipeline. The sigma-delta, as an OSR ADC, has its topology dependent of the sampling rate, operating for a fixed bandwidth, i.e. the sampling rate limits the components selection and inhibits superior bandwidths. Whereas the SAR ADC, as a NR ADC, has the sampling rate only as a system specification, thus, even with a reduced performance, the converter can operate at rates outside of the bandwidth for which it was designed. Typically, the sigma-delta takes more time to give a response, once it performs a mean of the input samples, while the SAR has a direct correspondence to each input sample (allowing a quicker response). Moreover, the SAR ADC are more relaxed than the sigma-delta converters, without dealing with complexed high order filters (which might be conditionally stable), nor noise modulation.

Comparing to the pipeline topology, the SAR topology has less blocks, which limits the introduction of noise, as only having one S/H block, and it also reduces the existence of latency from several stages (even that it might be tolerated for slow applications) [10]. Typically, the SAR has better linearity, because it just depends of capacitors matching, and it is less susceptible to sparkle codes (random offset in the output signal in comparison with the expected Gaussian noise distribution) [11]. Therefore, once the final goal is to implement a device for a wide range of applications, following the trend of the past decade, the SAR topology is often more flexible, less expensive in area and components, while achieving top performances.

3.1. General characterization

The SAR ADC operates through a binary search algorithm, which determines a digital word that represents a voltage, as closer as possible, of the input voltage signal. Its output word is created by testing each code bit individually. This converter is typically constituted by three blocks, as illustrated in Figure 3-3, one sampling DAC block, quantization block and one SAR (Successive-Approximation Register and control logic) block. The DAC could be made by an array of resistors or current sources scheme, however through a binary-weighted capacitors scheme there is no static power consumption and, this way, is possible to combine it with the S/H block in the same physical block. At a first step, the S/H block is made when the input signal is stored in the capacitors and then, in a second step, the DAC block is made when the binary-weighted capacitors are switched to the reference voltages.

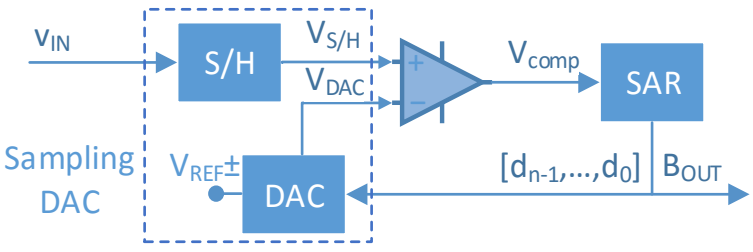

Figure 3-3 - Typical block diagram: SAR ADC.

In every clock cycle, the comparator block compares the input signal with the voltage generated by the DAC and, then, the tested bit is stored “1” if the DAC voltage is below the input signal and “0”

otherwise. The procedure repeats, updating (returning) the respective digital word after tested bit, until the last cycle (whose number equals the number of bits of the converter).

The synchronous operation of the traditional SAR requires a high-frequency clock signal which based on the converter's resolution (N) limits the sampling frequency (f_S) as

$$f_S[Hz] = \frac{f_{CLK}}{N+1}, \tag{3.1}$$

where f_{CLK} is the required clock signal frequency and N is the number of clocks required for every bit conversion, plus one clock for sampling. The maximum clock frequency (f_{CLKmax}) must ensure that all bits are converted, so its estimation must consider the time of the slowest bit conversion for every bit conversion. Therefore the f_{CLKmax} is determined based on the worst (slowest) comparison time per bit ($t_{COMPworst}$), the DAC settling time (t_{DAC}) and the sampling time (t_S), resulting in

$$f_{CLKmax}[Hz] = \frac{1}{N(t_{COMPworst} + t_{DAC}) + t_S}. \tag{3.2}$$

Since, at extremely low supply voltage, the transistors of the comparator and sampling DAC operate at sub-threshold region, the switches ON-resistance is high, originating a large $t_{COMPworst}$, t_{DAC} and t_S.

Let us consider a small example of a conversion process of a 4 bit synchronous SAR ADC that has at its input (v_{IN}) 4.532V and at its single reference voltage (V_{REF}) 5V. Knowing the quantization step (Δ) and v_{IN}, the correspondent code of ADC conversion is given by

$$Code = integer\left(\frac{v_{IN}}{\Delta}\right). \tag{3.3}$$

For this case, the rounding to integer is considered only for a higher value if its decimal part is above 5. When bit b_n changes, the output voltage of the DAC experiences a step,

$$Step[V] = 2^{n-1} \times \Delta, \tag{3.4}$$

where n is the number of the bit in test. After that happens, the output voltage of the DAC can be written as

$$V_{DAC}[V] = \Delta \sum_{k=1}^{n} b_{n-k} \times 2^{n-k}. \tag{3.5}$$

The results of this search process are presented in Table 1, where the bits are tested from the MSB to the LSB, having the tested word converted in a step voltage. This sequence of steps is also illustrated in Figure 3-4, where the code value matches with the ADC's final word.

Table 1- Example of a 4 bit SAR ADC conversion with $v_{IN} = 4.532\text{V}$ and $V_{REF} = 5\text{V}$.

Step Word	Step Voltage [V]
1000	$2^3 \times \Delta = 2.5$
1100	$(2^3 + 2^2) \times \Delta = 3.75$
1110	$(2^3 + 2^2 + 2^1) \times \Delta = 4.375$
1111	$(2^3 + 2^2 + 2^1 + 2^0) \times \Delta = 4.6875$
Final Word	V_{DAC} [V]
1110	4.375
Parameter	Result
Δ	$\frac{5}{2^4} = 0.3125V$
Code	$int\left(\frac{4.532}{0.3125}\right) = 14$
Error	$\varepsilon = \lvert v_{IN} - V_{DAC} \rvert = 0.157V$

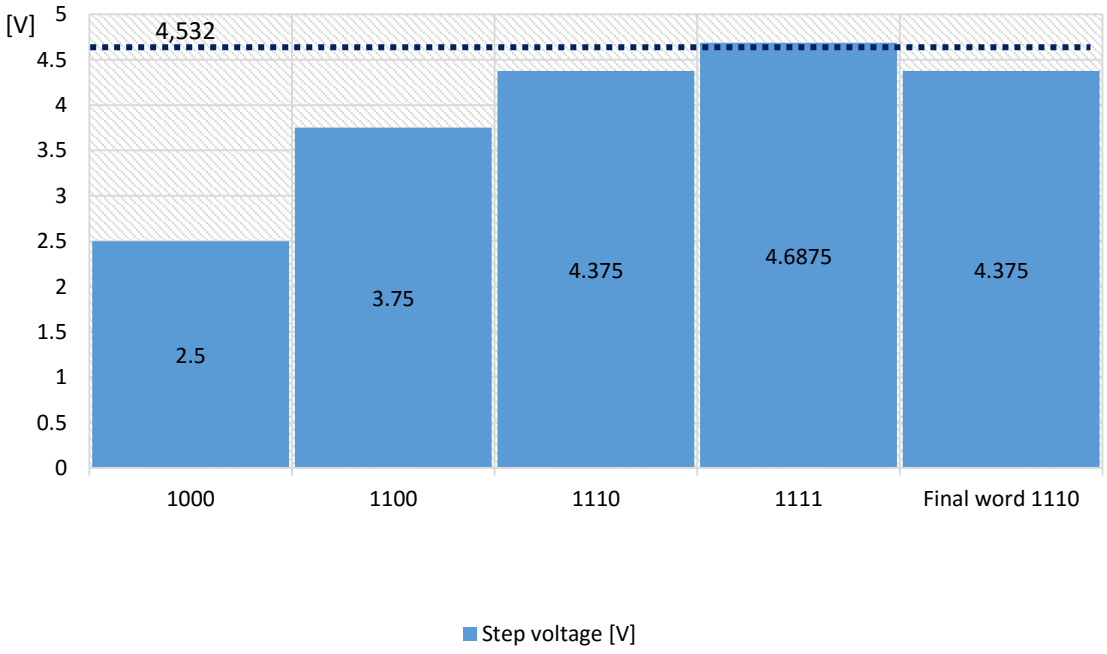

Figure 3-4 – Chart of each step of a 4 bit SAR ADC conversion with $v_{IN} = 4.532\text{ V}$ and $V_{REF} = 5\text{ V}$.

3.2. Typical topology improvements

The SAR ADC is typically composed by the blocks presented in Figure 3-3, but considering its input, output, common links and performance some arrangements or optimization can be done. Regarding the input of the circuit, a fully differential input architecture is often chosen due to its advantage on rejection of the common mode disturbances and better SNR. Considering the clock (CLK) operation, the converter can be synchronous or asynchronous, although the sampling phase always occurs in a synchronous way, the conversion phase can be asynchronous.

The traditional converters (synchronous), as shown in the previous section through the equations (3.1) and (3.2), require a high-frequency clock based on the converter resolution, which limits the sampling frequency and guarantees the same time of every bit conversion. On the other hand, as illustrated in Figure 3-5, the asynchronous converters use just the necessary time for each bit conversion, allowing the overall time conversion to be shorter than the synchronous ones. A converter to be asynchronous requires two clock signals, one external with sample-rate frequency and another internal with a variable frequency. The external clock, besides stipulating the sampling intervals, initiates the conversion process and the internal clock, based on the comparator decision, dictates the start and ending of each bit state, hence the time to convert each bit. In other words, it only needs the rising edge of the external clock to wake the process and the rest operates asynchronously. This type of converter allows a power saving mechanism (sleep mode), turning off the unnecessary blocks when the successive approximation is finished. Therefore, the proposed converter will be a differential and asynchronous SAR ADC.

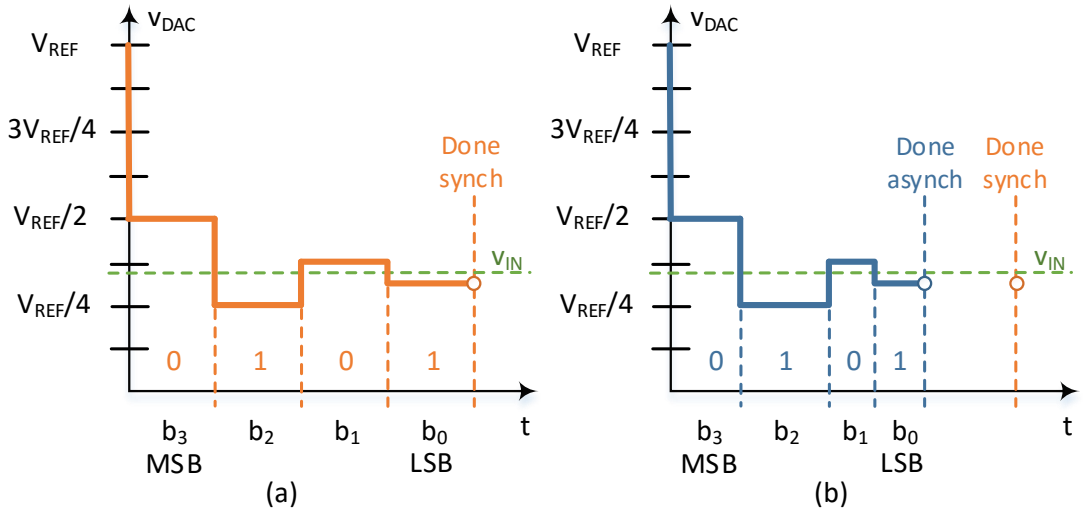

Figure 3-5 - Comparison between a synchronous (a) and an asynchronous (b) 4-bit SAR ADC conversion.

As explained in 2.1 (the metrics sub-section), the converters suffer from non-linearity due to imperfections in the analog blocks, therefore is crucial to design carefully the sampling ADC and the comparator blocks to obtain low DNL/INL and high SNR. For this work, the decision block uses a latched comparator circuit over a linear operational amplifier (OPAMP), because the OPAMP requires a really high gain to ensure that small signals are detected and a decision is reached for every signal. For

example, to detect an input signal with $100\mu V$ of amplitude, in a scale of $\pm 1V$, it would require a gain around 10000. On the other hand, even if it takes a long time to decide, the latched will always reach a decision, due to the internal positive feedback.

Moreover, our sampling DAC block applies the bottom plate sampling technique, as illustrated in the Figure 3-6, where the top plate of each capacitor in the array is connected to the node of the DAC output (negative) voltage (v_{ON}) and the bottom plate can be attached to the input voltage (v_{IP}) or a reference voltage (V_{REFP} and V_{REFN}). When a transistor is switched on, it always accumulates some charge internally and, when it is switched off, this charge is released to its terminal nodes, this is called charge injection. Therefore, the bottom plate technique isolates v_{ON} from v_{IP}, mitigating the charge injection from the sampling switches, thus, reducing the signal distortion at the input of the comparator. Whereas the top plate sampling technique, which is seen in Figure 3-8 from the next section 3.3, has the sampling switches directly attached at the comparator input. This way the first conversion (for the MSB) can be performed directly by the comparator without a physical MSB capacitor, thus reducing the number of capacitors, however every charge injection distortion is dependent of the input signal, which increases the complexity of the digital calibration associated.

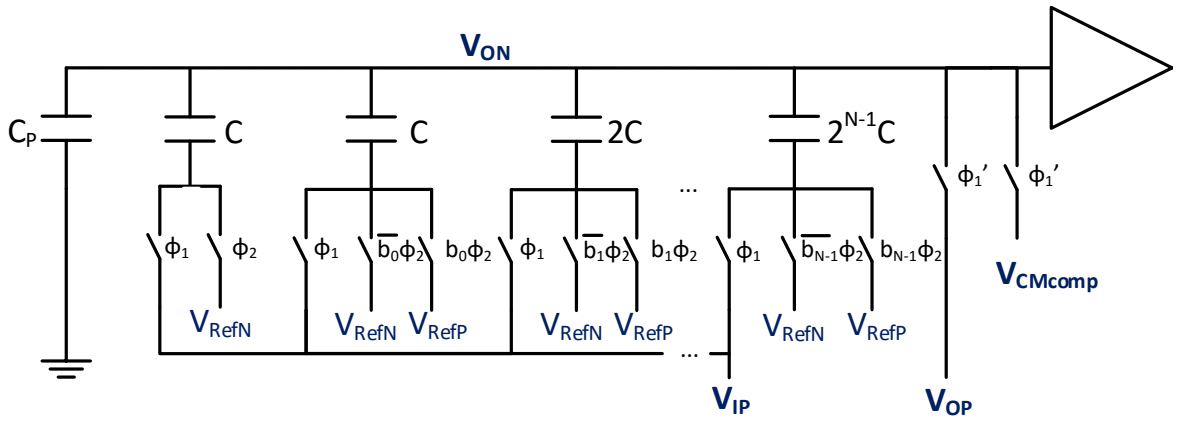

Figure 3-6 – A branch of a typical sampling DAC architecture.

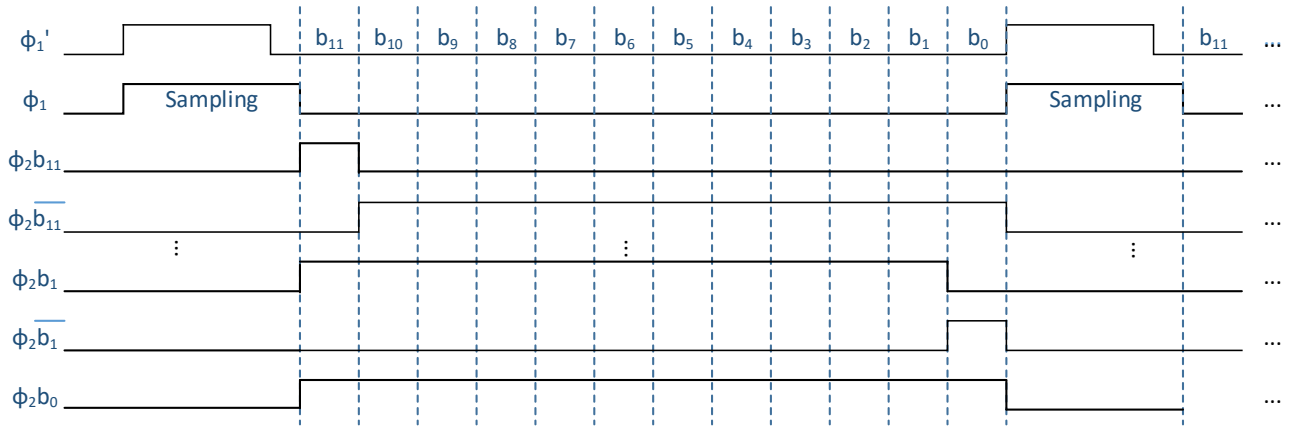

Figure 3-7 - Timing diagram of the phases from the circuit in Figure 3-6.

In Figure 3-7 we can see the sequence of the phases that control the DAC switches from MSB to LSB bit decisions. At first, during the sampling phase (ϕ_1), the bottom plate capacitor of all capacitors

are connected to the input signal (v_{IP}) and comparator biasing voltage (V_{CMcomp}), storing the sampling charge over all the capacitors. Then, after the sampling is made (the switches controlled by ϕ_1 are opened), the comparator will start making bit decisions (conversion stage - ϕ_2), controlled by the SAR control unit. These decisions correspond to the commuting the respective bit capacitor to the selected reference voltage (activating the respective bit switch). This will force the stored charge to be redistributed between the capacitors, whose equations are presented further ahead (section 4.4 Sampling DAC).

3.3. State of the art

Before starting any project, one must investigate what similar projects have been made in the field, in order to learn and use them as reference for comparison with our case. What type of topology, technique or method should be explored as well as the values expected to obtain. In this section, seven papers are mentioned to represent different versions of SAR ADCs, with supply voltages below $1\ \mathrm{V}$, as indicated in Table 2. After the presentation of a summary of each work, an overview is made of the common and different points between them.

Table 2 - Comparison of state of the art of SAR ADC, organized by voltage supply.

Reference	[12]	[13]	[14]	[15]	[16]	[17]	[18]
Principle / Method	Background self-calibration of comparator offset	Boosted self power gating	Tri-level comparator	Data-driven noise reduction	Noise reduction and linearity enhancements	Capacitive-swapping technique	Ladder-based reconfigurable time-domain comparator
Technology / Area	130nm / 0.0377mm^2	40nm	40nm / 0.0112mm^2	65nm / 0.076mm^2	65nm / 0.18mm^2	110nm / 0.092mm^2	180nm
Supply [V]	0.35 – 0.6	0.4 – 0.7	0.5	0.6	0.8	0.9	0.9
f_S [Sps]	200k – 3M	0.1k – 4M	1.1M	40k	32k – 128k	1M	200k
Power [W]	84.7n – 3.44µ	0.56n – 7.3µ	1.2µ	72n – 97n	0.31µ – 1.37µ	16.5µ	1.07µ
Resolution	8 bit	9 bit	9 bit	10 - 12 bit	12 – 14 bit	12 bit	12 bit
ENOB	6.4 – 6.5 bit	7.4 – 8.2 bit	7.5 bit	9.4 – 10.1	8.8 –11.1 bit	10.9 bit	11.5 bit
FOM [fJ/c.s.]	5 – 12.5	5.2	6.3	2.2 – 2.7	4.4 – 23.2	8.5	1.8
Date	Jul 2014	Nov 2012	April 2012	Dec 2013	2014	Nov 2012	2014

Similarly, all the analyzed papers are SAR ADCs that obey to an asynchronous operation with differential input, hence possessing two capacitor banks. The switched capacitor array (from the sampling DAC) have each capacitor with one plate connected to the common node and the other connected to a negative or positive reference voltage in each conversion step. These reference connections can be a limitation, because the DAC settling time is given by the time the capacitors take to reach these references, so in order to have a quick settling time, the reference voltage source should have a low-impedance node, which might require a buffer circuitry (if they are not the same as the supply voltages).

As explained in the previous section, the charge distribution of the switched capacitor array (from the sampling DAC) follows the principle of charge conservation, regardless of its implementation, however there are some distribution techniques denominated accordingly to its implementation. The **charge-redistribution technique** (CR) consists in an implementation where all the capacitors are used to sample the input signal, as in Figure 3-6. Whereas the **charge-sharing technique** (CS) is the implementation where only one (or some) capacitor (MSB) is used to sample, while the input signal is being sampled, the comparator is in reset mode and the rest of the DAC capacitors have both plates connected to fixed reference voltages (GND and V_{DD}). This technique is exemplified by Figure 3-8, after the sampling is done (reset $= 0$), the switches S_p and S_n open and the voltage is held in V_p and V_n, at the respective sides, while the DAC capacitors hold V_{DD}. Then, the successive-approximation controller starts operating by initially sending a request to the comparison trigger, which will consequently activate the comparator. Depending on the comparison result ($+1$ or -1), the controller adds or removes charge from the S/H, by closing the corresponding switches in the DAC [12], and so on until the LSB comparison.

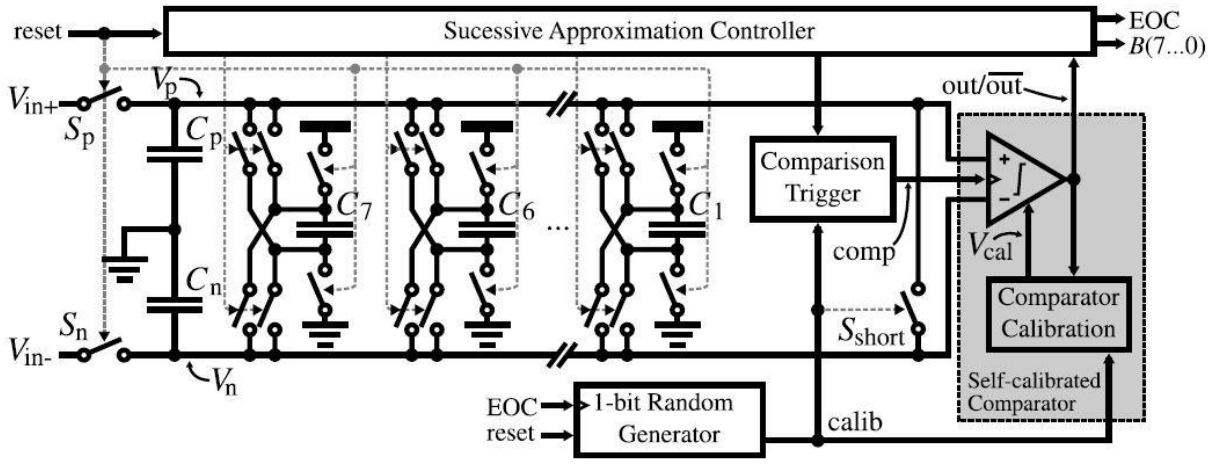

Figure 3-8 – 8 bit SAR ADC, with background self-calibration of comparator offset, topology diagram [12].

In [12] an ADC that uses a CS technique is proposed, in order to solve the limitation of the DAC settling time derived from applying the CR technique, and a background **calibration** technique to cancel out the comparator mismatch and improve ADC linearity, continuously nullifying the comparator offset. Moreover, while in the CR ADC the comparator offset is translated into offset in the ADC transfer curve,

in CS topologies it leads to ADC non-linearity. To reduce the comparator offset voltage, larger transistors could be used, leading to higher power consumption for the same speed of operation.

This converter guarantees the operation under low voltages with only regular threshold voltage (V_{TH}) transistors by employing a voltage-booster (VB), which doubles the gate voltage for all the switches in the S/H, the DAC and the comparator calibration blocks. It also employed a custom controller that is very energy-efficient, but uses the parasitic capacitances to store the digital values used during the conversion. However, at lower supply voltages, the controller operation is excessively slow, so the bits stored on the parasitics are lost due to the leakage from the controller transistors.

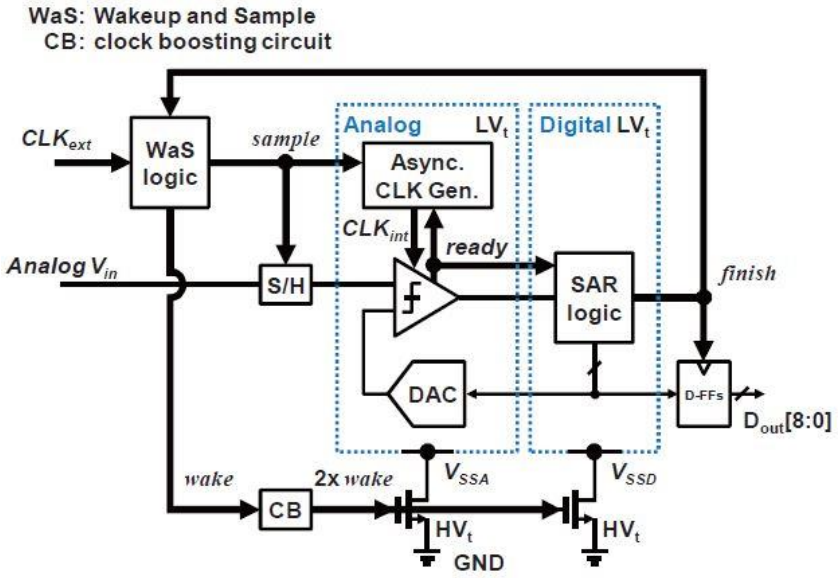

Figure 3-9 - Full Asynchronous Nano-Watt SAR ADC with 98% Leakage Power Reduction [13].

The work in [13] studies the sub-threshold leak of the advanced CMOS process that increases with process scaling and becomes power dominant in power at low frequency. In order to solve this leakage, this converter uses a **boosted self power gating** (PG) technique, which also resorts to VBs, as clock boosting (CB) in the gates of transistors that are inserted between local (V_{SSA}, V_{SSD}) or global (GND) grounds. As shown in Figure 3-9Figure 3-10, this asynchronous ADC applies bootstrapping mechanism for both analog and digital blocks, it also consists of a Wake up and Sample (WaS) logic, bootstrapped S/H circuit, asynchronous clock generator, comparator, DAC, SAR logic, clock boosting circuit, power gating switches and output registers – D-flip flops (D-FFs). The blocks inside the PG domain are designed with low V_{TH}, which run nine times at each conversion (since it is a 9 bit DAC). Whilst, the outside blocks of the PG domains run only once a conversion, having less influence on the total conversion speed, therefore these blocks, namely the ground references (V_{SSA}, V_{SSD}, GND), are mainly designed using high V_{TH} MOSFETs to reduce leakage power.

In [14] the power consumption is reduced through the use of a Tri-Level comparator and a reconfigurable DAC architecture, with a possibility to operate at single supply voltage. It also employs a stochastic calibration (i.e. through a pattern in random sequences) for the metastable region of the comparator, improving the ADC resolution, without increasing the internal DAC resolution. Any comparator decide according to its input signal, whether it is positive or negative, which corresponds to

1 and 0 respectively (considering a negative feedback), however for a very small signal the comparator might become unable to reach a decision in the available amount of time – **metastability** [19].

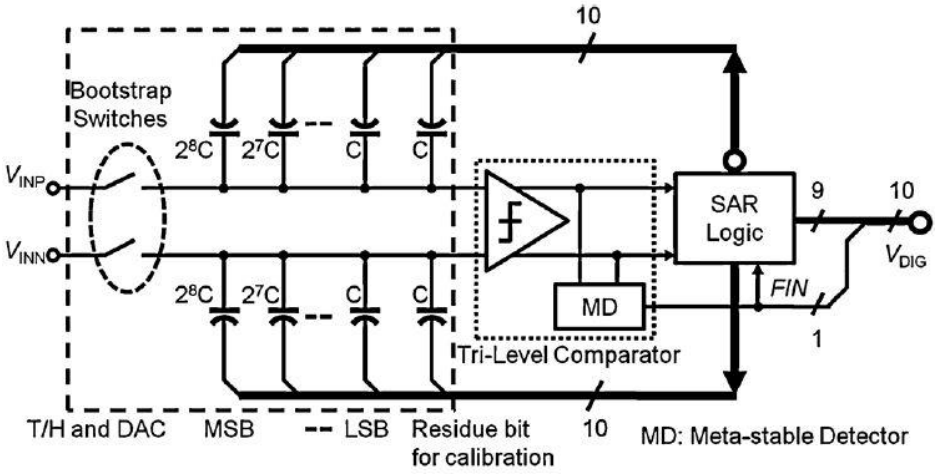

Figure 3-10 - SAR-ADC With Tri-Level Comparator [14].

The **Tri-level comparator** aims to relax the comparator speed requirement and decrease the resolution of internal DAC by 1-bit, in turn decreasing the total capacitance from the DAC. Similar to others, performs a CR technique and solves the capacitor mismatch through a reconfigurable capacitor array and a calibration procedure, as in [12] and [13]. This quantization block consists of a single comparator and a metastable detector (MD), as shown in Figure 3-10, which is used to reduce the decision time (enables a bit skipping option) and detect three types of input levels (positive, negative or too small).

The work in [15] enhances the comparator noise performance by the **Data-Driven Noise-Reduction** (DDNR) method. It selectively reduces noise effect, in critical cases, through a digital **majority voting** (MV), which is based on the comparator output probability to be 1 or 0, depending on the relation of the input amplitude (v_{IN}) and the input noise (σ_{noise}). This noise probability is calculated from the Cumulative Distribution Function (CDF) assuming a Gaussian distribution of the input noise.

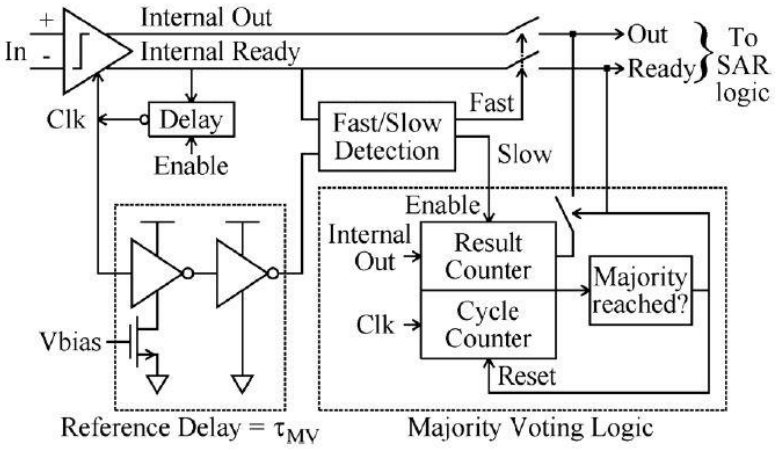

Figure 3-11- Circuit implementation of the Data-Driven Noise-Reduction method [15].

The critical case can be determined whether v_{IN} is smaller than a certain threshold voltage (V_{MV}) or the conversion time takes longer than a certain threshold time (τ_{MV}). Hence, as seen in Figure 3-11, when a slow conversion is detected, the MV logic is activated, which resorts to a counter that counts the number of comparator cycles and a second counter that counts the test results. Thus, when the conversion takes too long and the same decision is repeated several times (3 to 5 samples) the MV logic allows to foresee the comparator result.

In addition, the implemented DAC applies a CR technique over two arrays of 12 bit, where the 8 LSBs are binary-encoded, whereas the 4 MSBs are thermometer-encoded. The thermometer encoding reduces the probability of large DNL errors and the switching activity (energy), while the binary-scaled array saves more power.

The work in [16] is an improvement of the previous work, introducing a hybrid oversampled SAR ADC, it also employs a DDNR method, but combines techniques of oversampling, chopping and dithering, having in view to increase both SNR and linearity in a power-efficient way. **Chopping** is employed because it suppresses DC offset, flicker $\left({}^{1}/_{f}\right)$ noise and also modulates distortion components. Its implementation has the sampling rate (f_S) divided by a factor of two, and uses two clock-boosts to drive the NMOS sampling switches that also implement the input chopping. Therefore, by chopping at half the sampling rate and using oversampling, the dominant even-order distortions are moved out of the signal bandwidth, which arise from mismatch in the ADC four MSBs thermometer-encoded that are used to save switching energy.

The binary part of the DAC also suffers distortion that is reduced through **dithering**, which randomize this effect, and combined with oversampling puts the spurious tones outside the critical baseband. Note that spurious are the output components at frequencies that are not harmonically related with the oscillating frequency.

The work [17], as [12], [13], and [14], employs a digital calibration, but presents a capacitor rotation, for mismatch compensation of its capacitor array, through the **capacitor swapping technique**. This technique removes the middle-code transition error from the DAC, making its averaged error null, to improve linearity, without needing large capacitor size for good capacitor matching. Moreover, an **on-the-fly programmable dynamic comparator** is adopted in the design, instead of a low noise comparator, with a continuous pre-amplifier and latch for low noise. It applies monotonic switching techniques to reduce the total input capacitance by a factor of two with a digital redundancy, which provides additional reference settling error tolerance for achieving speedup ADC operation at low power consumption.

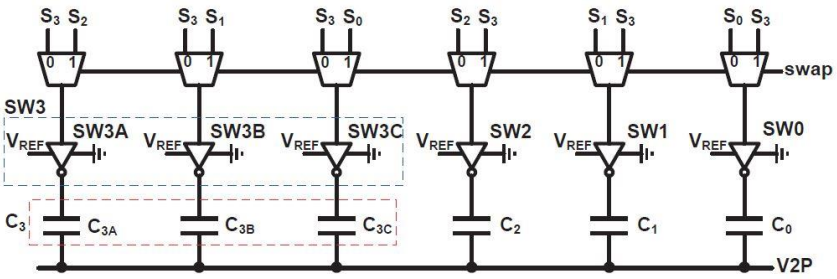

Figure 3-12 - 3 bit Capacitor swapping DAC [17].

The capacitor swapping technique is performed to exchange DAC capacitors for consecutive sub-conversions, either in regular or random fashions, to represent the DAC feedback, which is illustrated by an example of 3 bit C-DAC, in Figure 3-12. The C-DAC possesses 4 capacitors ($C_3 = 4C$, $C_2 = 2C$, $C_1 = C_0 = C$), however the MSB capacitor (C_3) is divided in 3 LSB capacitors (C_{3a}, C_{3b}, C_{3c}), whose values equalize the other capacitors (i.e. $C_{3a} = C_2$, $C_{3b} = C_1$ and $C_{3c} = C_0$). The same happens for the MSB switch, which is divided in 3 smaller switches. Although, the number of switches and capacitors increases, the total switch size and capacitance remain the same as those of the original binary C-DAC.

The work [18] introduces a **ladder-based reconfigurable time domain** (RTD) comparator for noise reduction, which automatically adjusts its power consumption according to the input, combined with a custom synchronous clock distribution circuit and two bootstrapped switches (BS). Its DAC employs a switching strategy that reuses its last capacitor, plus a bridge capacitor (explained in a further section) to reduce the array. It uses a custom clock circuitry to avoid unnecessary dynamic power consumption of registers, through the addition of control signals of previous and present clock to their input.

The proposed comparator uses a high differential ladder-based voltage-controlled delay cells (LVCDC), which allows to convert voltage difference into time delay difference, fully using the transition time to produce higher voltage-to-time (V/T) gain. It has noise reduction by cascading multi-delay stages and increasing the W/L ratio of the input transistors, which also increases V/T gain. Since the cell is a current-starved delay, as the comparator input becomes smaller, the transistors operate in sub-threshold region. Moreover, the number of delay stages are adjusted by employing control logic gates and a work-mode switching unit (WMSU), after the first delay stage to reconfigure the work mode of the comparator. For a large enough input difference, a power-saving mode enables to skip stages, while for a small difference, all the stages amplify the difference, improving its distinction (normal mode).

In sum, these works usually have in common:

- A **top plate sampling** in the capacitive DAC, which samples the input signal directly in the comparator input, this way the first conversion (for the MSB) can be performed without switching any reference voltage to the MSB capacitor, being calibrated later any error related to this conversion.
- A **limited sampling rate**, because while the number of stacked transistors increases, V_{GS} of input transistor decreases, thus the capacitance speed to charge or discharge becomes slower.
- A **digital calibration** that solves mismatching and redundancy issues in the capacitor array, which allows a recover of eventual wrong bit decision (during the conversion). For this redundancy to happen, the comparator has to make another decision for a range of voltages for which it has already been triggered, that is, over a range of voltages where the search algorithm has already passed.

On other hand, all of these works are often distinguished by their way to handle:

- The **sampling principle** or technique for charge distribution in the sampling DAC, between Capacitive-Sharing, Capacitive Redistribution or Capacitive-Swapping.
- The **non-linearity, distortion and offsets** are treated employing background calibration, custom designed small size inter-digital capacitors and hybrid topologies.
- **Conversion speed** through techniques as MV, applying comparator circuitry, clock distribution circuitry or delay cells.
- **Dominant power consumption and overall noise**, which relies on the comparator, where are applied topologies as DDNR comparator, tri-comparator, programmable dynamic comparator and RTD comparator.
- **Leakage current** (in sub-threshold region), essentially employing transistors with different threshold voltages and **boosted mechanisms**, for biasing the switches (that operate at a low frequency-rate). Since the bootstrapping circuit has a large dimension, the number of switches is limited to maintain the ADC area with a reduced size.

4. SAR ADC design

The ADC described in this work is composed by five main blocks, as depicted in Figure 4-1. At first, the differential input signal is sampled by the Sampling DAC (controlled by a synchronous external clock), and afterwards the stored signal will be successively processed in an asynchronous way. The comparator decides, based on the differential output voltage of the DAC, returning q (and its inverse value) to the SAR block (which stores the bit decision in a register) and to the delay block, which generates an internal (asynchronous) clock. This internal clock ensures, for every bit conversion cycle, a constant time for settling the voltages of the DAC capacitors and a variable time for each comparator bit decision. After all bits are converted, the final word is synchronously delivered to the output, the sampling phase is restarted and the cycle repeats.

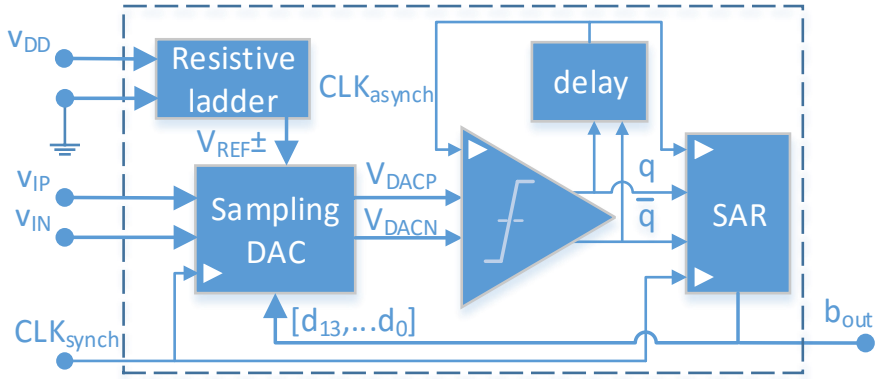

Figure 4-1 - Implemented SAR DAC block diagram.

The requirements to properly size an ADC, to attain the desirable performance, is made regarding the sampling frequency and SNR, which define the time and noise constraints, respectively. In turn, one must start splitting the times and determining the noise level that each analog block can bear. What, consequently, leads to set several tradeoffs between the demands of electrical schemes and sizes of the diverse elements of the circuits.

4.1. Time constraints

In this work, $f_S = 500\ k\text{Hz}$ so the sampling clock period is

$$T_{CLK} = \frac{1}{500 \times 10^3} = 2\ \mu\text{s}. \tag{4.1}$$

Hence, attributing 10% of the clock period to input signal sampling (t_{samp}) and the remaining 90% of the clock period for the conversion (t_{conv}), we have

$$\begin{cases} t_{samp} = 0.1T_{CLK} = 200\ \text{ns} \\ t_{conv} = 0.9T_{CLK} = 1800\ \text{ns} \end{cases}. \tag{4.2}$$

Then, stipulating that each word conversion takes 12 decisions (given the ADC resolution) plus 2 more due to redundancy and, for simplification, that the time for every bit conversion is the same, the time per bit is

$$t_{bit} = \frac{t_{conv}}{N+2} = \frac{1800}{14} \approx 128 \text{ ns}. \tag{4.3}$$

The redundancy allows a recover of eventual wrong bit decision, which is only possible when the comparator takes more than one decision over a range of voltages, where the search algorithm has already passed. In turn, since every bit decision comprises the settling time of the DAC (t_{DAC}) and the time for the comparator to decide (t_{comp}). A slightly more time was attributed for settling than for the comparator decisions, leading to

$$\begin{cases} t_{DAC} = 0.55 t_{bit} = 70 \text{ ns} \\ t_{comp} = 0.45 t_{bit} = 58 \text{ ns} \end{cases}. \tag{4.4}$$

Note that these values have just an indicative purpose for sizing, because, as said in sub-section 3.2, the conversions are asynchronous, i.e. the comparator decision time varies accordingly to its input signal

4.2. Noise constraints

Besides the quantization noise present in ideal ADCs, real ADCs also have noise due to internal components and external factors, whose dominant contribution corresponds to thermal noise, the output noise power in a simple RC circuit is

$$\overline{v_n^2} = \frac{kT}{C}, \tag{4.5}$$

as demonstrated in [20], where k is the Boltzmann constant (1.381×10^{-23} JK^{-1}), T is the temperature in Kelvin (typically 323 °K $\equiv 50$ ℃) and C is the capacitance.

In turn, from (4.5) considering the parasitic capacitance (C_p) and the sampling capacitance (C_{samp}) present in the array of the sampling DAC (in Figure 3-6), assuming $C_p = {C_{samp}}/{3}$, while the charge is stored, as demonstrated in [21], the total noise power generated during sampling is given by

$$\overline{v_{n,samp}^2} = 2\frac{kT}{C_{samp}}\left(1 + \frac{C_p}{C_{samp}}\right) = 2\frac{kT}{C_{samp}}\left(\frac{4}{3}\right) = \frac{8}{3}\frac{kT}{C_{samp}}, \tag{4.6}$$

where the multiplying factor of 2 accounts the fact the circuit differential input is present. Following the sampling circuitry, the parasitic capacitance causes a gain factor

$$G_{DAC} = {C_{samp}}\Big/{C_{samp} + C_p} = {3}/{4}. \tag{4.7}$$

Thus, the noise power correspondent to the comparator block can be obtained, referring the output noise of the comparator to ADC input through this gain factor, as

$$\overline{v_{n,comp}^2} = \frac{v_{comp}^2}{G_{DAC}^2}. \tag{4.8}$$

Once the main causes of noise in the ADC were identified, now it is necessary to limit the restrictions for each block. Meaning that we need to define the total thermal noise power generated by the S/H and the comparator blocks. Therefore, applying the specification of this work of a $SNR = 65\ \text{dB}$ in the equations (2.8), (2.5), (4.6), (4.8) plus P_{noise}, as the sum of every block noise, we obtain

$$\begin{aligned} & SNR[dB] = 10\log_{10}\left(P_{signal}/\overline{v_{n,Q}^2} + \overline{v_{n,samp}^2} + \overline{v_{n,comp}^2}\right) \\ & \Leftrightarrow 10^{SNR/10}P_{noise} = P_{signal} \\ & \Leftrightarrow \overline{v_{n,samp}^2} + \overline{v_{n,comp}^2} = \frac{P_{signal}}{10^{SNR/10}} - \overline{v_{n,Q}^2}, \end{aligned} \tag{4.9}$$

where $\overline{v_{n,Q}^2}$ is the power noise from quantization. Moreover, substituting the specification in (2.9), the $SNR = 65\ \text{dB}$ is equivalent to $N = 10{,}5$, so, considering a margin of error, the minimum resolution to choose would be $N = 11$. Nevertheless, we can increase the margin of error, further increasing the resolution. However, looking at the Table 3, we can see that it gets to a point where it is no longer compensatory.

Table 3 - Achieved noise regarding 11, 12 or 13 bits.

Parameters for $SNR = 65\ dB$	**Resolution**		
	$N = 11$	$N = 12$	$N = 13$
V_{Ref}	$V_{DD} = 0.5\ \text{V}$		
$P_{signal} = \left(\frac{V_{FS}}{2}\right)^2/2$	$\frac{(0.5)^2}{2} = 0.125\ \text{V}^2$		
$\Delta = \frac{V_{FS}}{2^N}$	$\frac{1}{2^{11}} = 488\ \mu\text{V}$	$\frac{1}{2^{12}} = 244\ \mu\text{V}$	$\frac{1}{2^{13}} = 122\ \mu\text{V}$
$\overline{v_{n,Q}^2} = \Delta^2/12$	$(141\ \mu\text{V})^2$	$(70.5\ \mu\text{V})^2$	$(35.2\ \mu\text{V})^2$
$\overline{v_{n,samp}^2} + \overline{v_{n,comp}^2}$	$(138.4\ \mu\text{V})^2$	$(186\ \mu\text{V})^2$	$(195.7\ \mu\text{V})^2$

Alternatively, using $N = 12$, the accuracy would increase, since its quantization step would be (twice) smaller than $N = 11$, relaxing the value of the ENOB. In turn, using $N = 13$, the quantization is now four times smaller than $N = 11$, however the improvement in the overall noise costs 2 more decision

(consequently in time). Hence, selecting $N = 12$, adds just 1 more decision, gives a sufficient margin of error for this converter.

Assuming that the comparator noise is the same as the sampling noise, for 12 bits, the respective values are

$$\overline{v_{n,samp}^2} + \overline{v_{n,comp}^2} = (186\ \mu\text{V})^2, \tag{4.10}$$

$$\Longrightarrow \overline{v_{n,samp}^2} = \overline{v_{n,comp}^2} \simeq (131.5\ \mu\text{V})^2. \tag{4.11}$$

Consequently, knowing the sampling noise it is possible to determine the overall sampling capacitance using (4.6),

$$C_{samp} = \frac{8}{3}\frac{kT}{\overline{v_{n,samp}^2}} = \frac{8}{3}\frac{(1.381 \times 10^{-23})(323)}{(131.5\ \times 10^{-6})^2} \simeq 688\ \text{fF}. \tag{4.12}$$

Now that the top specifications were gathered, the circuit topologies of each analog block shall be introduced, first through a theoretical analysis, to understand better the main points that each bit decision must be based on, followed up by the suited simulations to meet these specifications.

4.3. Comparator block

The comparator block, as mentioned before, is a crucial block in the development of ADCs, particularly of the SAR ADC, being important to guarantee that it is able to decide whether the result of the sampling DAC block output is positive or negative, in a fast and accurate way. The comparator could be made through a high gain operational amplifier (in an open loop), that is, pulling the output to low or high. However, it is harder to ensure high gain than to use dynamic comparators (also known as clocked comparators), which have regenerative feedback that will cause the output to latch at one of two levels.

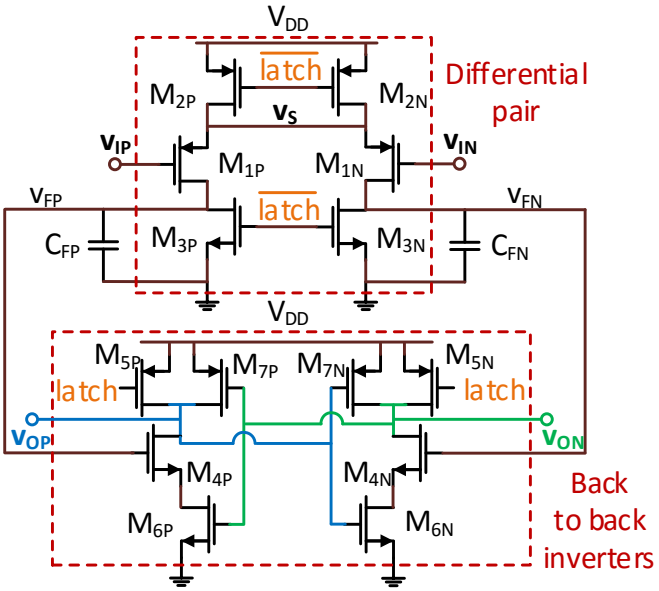

Figure 4-2 - Part of the dynamic comparator schematic [22].

In addition, the dynamic comparators only consumes energy during the decision phase, being more power efficient. Therefore, a dynamic comparator circuit is used, based on [22], where part of its schematic is illustrated in Figure 4-2. It consists of a differential pair – M_{1P} and M_{1N} – and a pair of back to back inverters – M_{4P}, M_{6P}, M_{7P} and M_{4N}, M_{6N}, M_{7N} – (or cross coupled inverters).

In Figure 4-3, we can observe the comparator states that happen for each bit conversion, where the conversion mode comprises the states of integration, regeneration and propagation delay (due to internal blocks). First, the reset mode occurs when the latch control signal is low (i.e. $latch = 0$ or $\overline{latch} = 1$). In this mode, M_{2P}, M_{2N} are cut off, meaning that the differential pair (M_{1P}, M_{1N}) has no current to drive, independently of the input signal (v_{IP}, v_{IN}). On the hand, both M_{3P}, M_{3N} are driving, meaning that the integration nodes (v_{FP}, v_{FN}) are pulled to GND (discharging the capacitors – C_{FP} and C_{FN}). Likewise, M_{5P}, M_{5N} are also driving, what pulls output node (v_{OP}, v_{ON}) to V_{DD}.

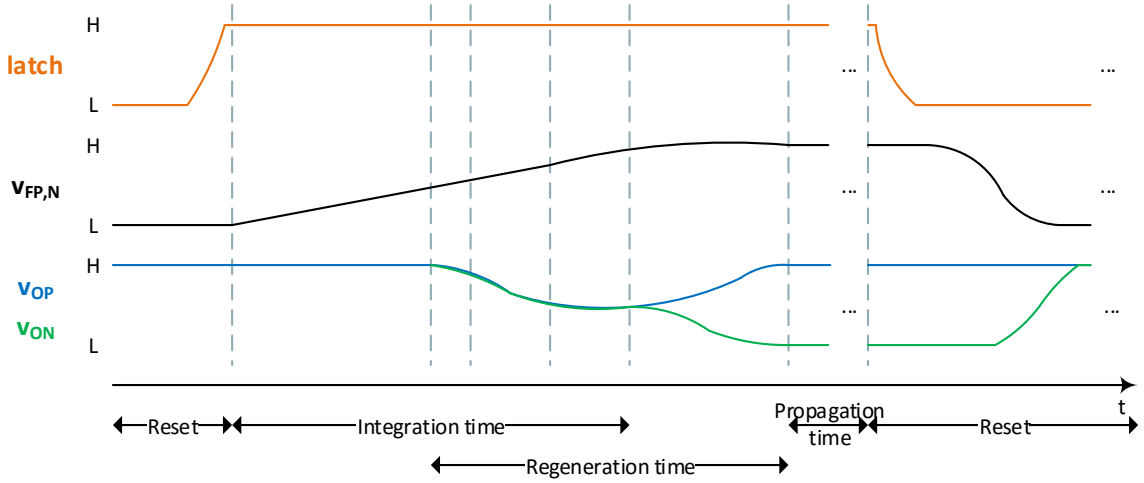

Figure 4-3 - Time diagram of the comparator operation regarding a positive input signal.

Secondly, the conversion mode starts when the $latch$ is high (i.e. $latch = 1$ or $\overline{latch} = 0$), what consequently turn M_{2P}, M_{2N} and allows M_{1P}, M_{1N} to have current to drive. Now, since M_{3P}, M_{3N} are cut off, that current (controlled by the input signal) will charge the capacitors C_{FP}, C_{FN}. Thus, the nodes v_{FP}, v_{FN} will also vary, dictating the start of the integration phase, which in turn ends when the capacitors are fully charged. On the other hand, the regeneration phase begins when v_{FP}, v_{FN} reach a voltage value that turn M_{4P}, M_{4N}, and it ends when v_{OP} or v_{ON} return back to V_{DD}. That said, the purpose of the pair of back to back inverters is to pull up v_{OP} or v_{ON} and pull down the other (maintaining its voltage until the next reset), dictated by which transistor M_{4P} or M_{4N} conducts more.

For instance, as illustrated in Figure 4-3, when the comparator input signal is positive ($v_{IP} > v_{IN}$), since M_{1P} and M_{1N} are PMOS, M_{1N} will start to conduct more, allowing current to flow through the node v_{FN}, eventually turning M_{4N}, which pulls v_{ON} down. This way, even though the same happens to v_{OP}, after a while both nodes reach a threshold voltage, but v_{ON} will continue to decrease (first) to GND, whereas v_{OP} will start to be pulled up to V_{DD}.

4.3.1. Analysis of the comparator sub-blocks

The first step to analyze any circuit is to choose an approximate model for large and small signals, where for the differential pair block the large signals model allows obtaining the integration time. Whereas, for small signals it allows to obtain its voltage gain, revealing the most influence parameters for its implementation. The model for large signals is represented as an equivalent circuit composed by a current source charging a capacitor, where the current source is composed of transistors M_{2P}, M_{2N} and M_{1P}, M_{1N}. This way, as illustrated in Figure 4-4, the current supply assumed to be equally split by the two branches, allows to analyze only one of them.

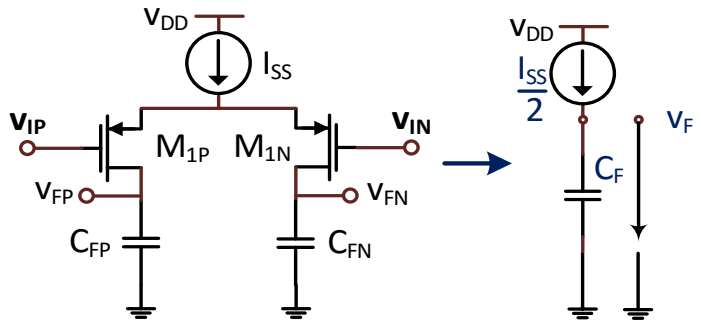

Figure 4-4 – Sub-block: differential pair equivalent circuit for large signals.

Analyzing the large signal equivalent model, yields

$$\frac{I_{SS}}{2} = C_F \frac{dv_F(t)}{dt} \tag{4.13}$$

$$\Leftrightarrow v_F(t) = \frac{I_{SS}}{2C_F} t, \tag{4.14}$$

where I_{SS} is the tail current of the differential pair, I_D is the transistor M_1 drain current, C_F the noise capacitor, $v_F(t)$ are the respective capacitor voltage. Moreover, stipulating that the integration phase ends when initiates the regeneration phase happens for ΔV_F, the amount of voltage that turn the transistors M_{4P} or M_{4N}, it is possible to determinate the integration time as

$$V_C(t_{int}) = \Delta V_F, \tag{4.15}$$

$$\Leftrightarrow t_{int} = \frac{2C_F}{I_{SS}} \Delta V_F = \frac{C_F}{I_D} \Delta V_F. \tag{4.16}$$

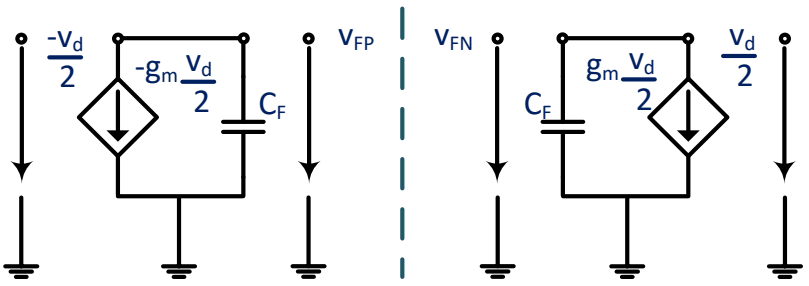

Figure 4-5 - Differential pair equivalent circuit for small signals, neglecting g_{DS}.

In turn, applying the bisection theorem, the small signals model is represented, as illustrated in Figure 4-5, by the incremental model of the transistors M_1 charging capacitor C_F, where its intrinsic

conductance (g_{DS1}) is ignored, with half of a differential voltage (v_d) applied at the input terminal of each side. This way, analyzing both sides of the comparator, their respective output voltages are

$$\begin{cases} v_{FP}(t) = g_{m1}\frac{v_d}{2C_F}t \\ v_{FN}(t) = -g_{m1}\frac{v_d}{2C_F}t \end{cases}. \tag{4.17}$$

where g_m is the transistor transconductance. Therefore, the differential output voltage of the differential pair is

$$v_{F\,diff}(t) = v_{FP}(t) - v_{FN}(t) = g_{m1}\frac{v_d}{C_F}t, \tag{4.18}$$

thus, the integrator gain (neglecting g_{DS1}) is

$$G(t) = \frac{v_{F\,diff}(t)}{v_d} = \frac{g_{m1}}{C_F}t, \tag{4.19}$$

which is linear and always increases with time, (though as it is shown next it will saturate). Nevertheless, substituting the (4.16) in (4.19), the gain at the end of the integration phase is

$$G(t_{int}) = 2g_{m1}\frac{\Delta V_F}{I_{SS}} = \frac{g_{m1}}{I_D}\Delta V_F. \tag{4.20}$$

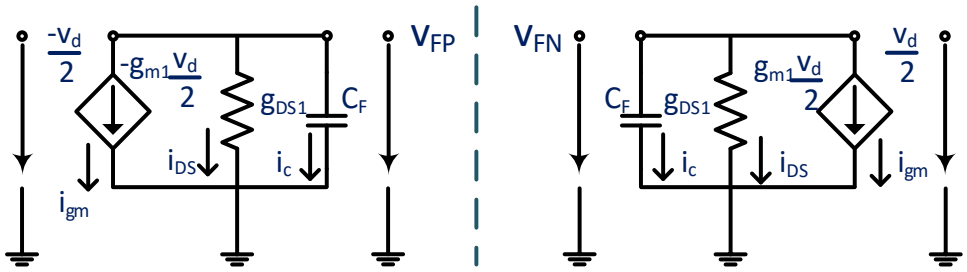

Figure 4-6 - Differential pair equivalent circuit for small signals, with g_{DS}.

Now, considering the incremental model with g_{DS1}, we can determine the value that $v_{F\,diff}(t)$ will saturate. Again, applying the KCL to the circuit represented in Figure 4-6, for both sides, yields

$$i_C + i_{g_{DS}} + i_{g_m} = 0, \tag{4.21}$$

which results in a first order differential equation for each side

$$\begin{cases} C_F\frac{dV_{FP}}{dt} + v_{FP}g_{DS1} - g_{m1}\frac{v_d}{2} = 0 \\ C_F\frac{dV_{FN}}{dt} + v_{FN}g_{DS1} + g_{m1}\frac{v_d}{2} = 0 \end{cases}. \tag{4.22}$$

Consequently, knowing that

$$v_{F\,diff}(t) = v_{FP}(t) - v_{FN}(t), \tag{4.23}$$

$$\Leftrightarrow v_{FP}(t) = v_{F\,diff}(t) + v_{FN}, \tag{4.24}$$

then, equalizing both equations of (4.22) in order to $\frac{dV_{FN}}{dt}$ and substituting (4.24) results in

$$\Rightarrow \frac{\Delta v_{F\,diff}(t)}{\Delta t} = -\frac{g_{DS1}}{C_F} v_{F\,diff}(t) + \frac{g_{m1}}{C_F} v_d, \tag{4.25}$$

$$\Leftrightarrow \frac{\Delta v_{F\,diff}(t)}{\Delta t} = - \left. v_{F\,diff}(t) - \frac{g_{m1}}{g_{DS1}} v_d \right/ \frac{C_F}{g_{DS1}}, \tag{4.26}$$

$$\Leftrightarrow \int \frac{\Delta v_{F\,diff}(t)}{\Delta t} \frac{1}{v_{F\,diff}(t) - \frac{g_{m1}}{g_{DS1}} v_d} dt = \int -\frac{1}{\frac{C_F}{g_{DS1}}} dt, \tag{4.27}$$

$$\Leftrightarrow \ln\left(v_{F\,diff}(t) - \frac{g_{m1}}{g_{DS1}} v_d\right) = -\frac{t}{\frac{C_F}{g_{DS}}} + D, \tag{4.28}$$

$$\Leftrightarrow \begin{cases} v_{F\,diff}(t) = e^{-\frac{t}{\tau_{int}} + D} + \frac{g_{m1}}{g_{ds1}} v_d \\ \tau_{int} = \frac{C_F}{g_{ds1}} \end{cases}, \tag{4.29}$$

where D is the integration mathematical constant and τ_{int} the time constant of the integration period. Then, assuming that $v_{F\,diff}(t)$ has the initial value null,

$$v_{F\,diff}(0) = 0 \Leftrightarrow e^D = -\frac{g_{m1}}{g_{DS1}} v_d. \tag{4.30}$$

Finally, the integrator function is expressed as

$$v_{F\,diff}(t) = A_i v_d \left(1 - e^{-t/\tau_{int}}\right), \tag{4.31}$$

$$\Leftrightarrow v_{F\,diff}(t) = \frac{g_{m1}}{g_{DS1}} v_d \left(1 - e^{-g_{DS1}\, t/C_F}\right), \tag{4.32}$$

where A_i is the intrinsic voltage gain of the transistor $M_{1P,N}$, (g_{m1}/g_{DS1}).

Looking to the back to back inverters block, depicted in Figure 4-7, its analysis is not as straightforward as the differential pair block, since its input voltage is constantly varying. In the beginning of the integration phase $M_{4P,N}$ is disabled (Figure 4-7-a). After a while, when the $M_{4P,N}$ starts driving and $M_{6P,N}$ is not saturated, behaving as a resistor, both make a common source amplifier with source degeneration (Figure 4-7-b). In that case, the $M_{7P,N}$ are disabled and the output voltage ($v_{O\,diff}$) is affected accordingly to the input integration nodes ($v_{F\,diff}$). Thirdly (Figure 4-7-c), when the output voltage nodes drop enough and the integrator nodes continue to rise, the $M_{7P,N}$ is turned (having a sufficient v_{SG}) and $M_{6P,N}$ saturates (because its v_{DS} becomes too great). Now, the $M_{6P,N}$ and $M_{7P,N}$ behave as a back to back inverters and the regeneration takes place. Moreover, if $M_{4P,N}$ is saturated, it behaves has a cascode and, thus, the effect of the integration nodes cease to matter. Therefore, accordingly to [22], the differential output voltage can be expressed as

$$v_{O\,diff}(t) = A_y v_d e^{t/\tau_{reg}}, \tag{4.33}$$

where A_y is the gain of the previous block combined with the amplifier gain, v_d is the input differential voltage. τ_{reg} is the time constant of the regeneration period [19],

$$\tau_{reg} = \frac{C_d+2C_c}{G_m-G_{DS}}, \tag{4.34}$$

where C_d is the sum of the parasitic capacitances from any component connected only at one of the output terminals; C_c is the sum of the parasitic capacitances from any component connected between both the output terminals. G_m is the sum of the transconductances of each inverter ($M_{6P,N}$ and $M_{7P,N}$), G_{DS} is the sum of the intrinsic conductances of every transistor ($M_{4P,N}$, $M_{6P,N}$ and $M_{7P,N}$).

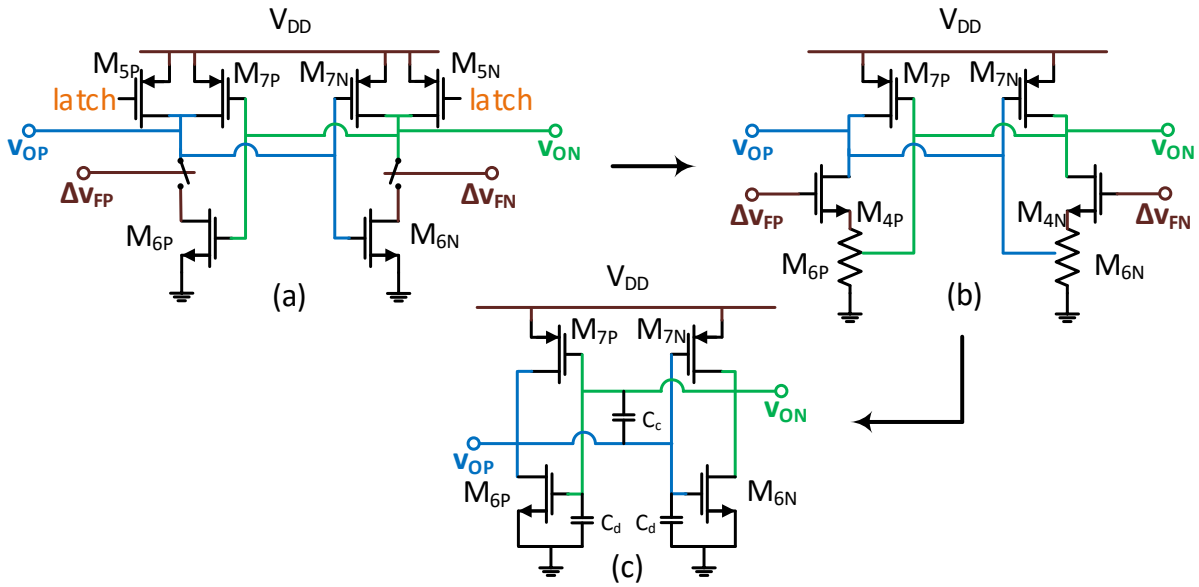

Figure 4-7 - Sub-block: back to back inverters when (a) $M_{4P,N}$ is disabled, (b) $M_{4P,N}$ and $M_{6P,N}$ are turned making a common source with degeneration amplifier and (c) $M_{6P,N}$ is saturated and $M_{7P,N}$ is turned.

4.3.2. Comparator sizing

The comparator circuitry is designed considering the previously mentioned time and noise constraints as main aspects, first ensuring the noise restriction and secondly the time. To do so, a theoretical model is required to instruct a first approach and then simulate the circuit. Hence, the study from [19], regarding the comparator modeling and transient behavior at the regeneration phase, and [23], [24], regarding the transconductance model for the MOSFET in the weak inversion region, are combined.

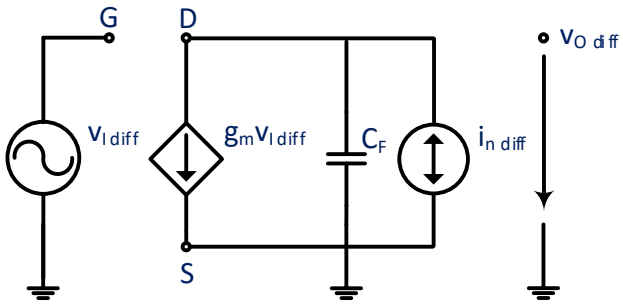

Figure 4-8 - Equivalent incremental model of the differential pair with a noise output current source.

At first, assuming that the major noise contribution is from the integrator, composed by M_1 and C_F (presented in Figure 4-2), it is possible to simplify the circuit through the incremental model of the differential pair regarding its output noise (neglecting g_{DS}), as shown in Figure 4-8. Hence applying the KCL to the circuit yields

$$g_m v_{I_{diff}} + C_F \frac{dv_{O_{diff}}}{dt} + i_{n_{diff}} = 0, \tag{4.35}$$

where $v_{O_{diff}}$ is the output differential voltage, $i_{n_{diff}}$ is differential random noise current and C_F is the noise capacitance. Let us assume $v_{I_{diff}} = 0$ to quantify the last noise, which allows simplifying (4.35) to

$$\frac{dv_{O_{diff}}}{dt} + \frac{i_{n_{diff}}}{C_F} = 0. \tag{4.36}$$

Accordingly to [19] the noise current can be expressed as

$$\frac{i_{n_{diff}}}{\xi(t)} = \sqrt{4kT\gamma G_m}, \tag{4.37}$$

where $\xi(t)$ is the Gaussian distributed white noise random variable, k is the Boltzmann constant, T is the temperature, γ is a coefficient dependent of the channel length of the technology node, and G_m the overall transconductance. This allows the equation (4.36) to be re-written as

$$\frac{dv_{O_{diff}}}{dt} = \frac{\sqrt{4kT\gamma g_m}}{C_F}\xi(t). \tag{4.38}$$

yielding the noise produced form comparator integration nodes (during the integration stage) as [19]

$$\sigma_{int}^2(t) = \frac{4kT\gamma g_m}{{C_F}^2} t. \tag{4.39}$$

Consequently, the comparator output noise is expressed by

$$\sigma^2\big(V_o(t)\big) = \sigma_0^2 + \sigma_{int}^2(t), \tag{4.40}$$

where σ_0^2 is the comparator initial noise as

$$\sigma_0^2 = \frac{kT}{C_F}. \tag{4.41}$$

As illustrated in Figure 4-9, the comparator input referred noise –$\sigma_{ni}^2(t)$ – is quantified by

$$\sigma_{ni}^2(t) = \frac{\sigma^2\big(V_o(t)\big)}{G^2(t)} = \frac{\sigma_0^2}{\left(\frac{g_m}{C_F} t\right)^2} + \frac{4kT\gamma}{g_m t} \approx \frac{4kT\gamma}{g_m t}, \tag{4.42}$$

where $G(t)$ is the integration voltage gain, mentioned in (4.20), and the initial condition (σ_0^2) can be ignored, since it depends quadratically of the time and rapidly loses its significance.

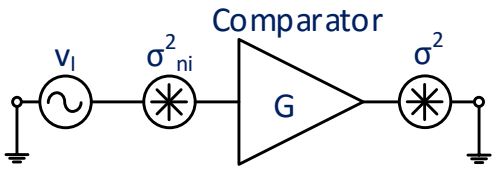

Figure 4-9 - Comparator output and input referred noise circuit model.

In spite of using low voltage supplies (e.g. below $1\ V$) turns the device more susceptible to noise, it also places the transistors in the weak inversion region (whose current depends exponentially of v_{GS} [23]). In this region, the transistor is placed at its best efficiency performance (though always limited by the output resistive load [25]) which can be seen as

$$Eff = \frac{g_m}{I_D}. \tag{4.43}$$

Furthermore, one can relate the transistors size through its current, which is given, in this region, as [23]

$$I_D = I_{DS} = \frac{W}{L} I_M exp\left(\frac{V_{GS}-V_M}{n\phi_t}\right)\left[1 - exp\left(\frac{-V_{DS}}{\phi_t}\right)\right], \tag{4.44}$$

where I_M and V_M are the current and voltage for the representative point that ends the weak inversion.

Hence, knowing the transconductance in the weak inversion region as

$$g_m = \frac{I_D}{n\phi_t} \Leftrightarrow I_D = g_m n\phi_t, \tag{4.45}$$

where n is a transistor intrinsic parameter and ϕ_t is the thermal voltage,

$$\phi_t[mV] = 25.9 \times (\mathrm{T}[K]/300), \tag{4.46}$$

where T is the temperature in Kelvin, if we substitute the equations (4.20) and (4.45) in (4.42) we get the comparator input referred noise at the integration time as

$$\sigma_{ni}^2(t_{int}) \approx \frac{4kT\gamma}{C_F}\frac{I_D}{g_m \Delta V_F} = \frac{4kT\gamma}{C_F}\frac{n\phi_t}{\Delta V_F}. \tag{4.47}$$

Now, using the comparator noise restriction, from equation (4.11), as the input referred noise, meaning $\sigma_R^2 = \sigma_{ni}^2 = (131.5\ \mu\mathrm{V})^2$, and $T = 398\ \mathrm{K}\ (125℃)$, $n = 1.6$, $\Delta V_F = 300\ \mathrm{mV}$ and $\gamma = 1$, through (4.47) we obtain the theoretical value for C_F (noise capacitance) as

$$C_F = \frac{4kT\gamma}{\sigma_{ni}^2(t_{int})}\frac{n\phi_t}{\Delta V_F} \approx 230\mathrm{fF}. \tag{4.48}$$

Note that the parameters used in (4.48) take in consideration the behavior of this circuit through several transient simulations for different scenarios, namely 16 corners and the typical one, as listed in Table 4. The typical corner simulates a standard process, where every device is supplied with VDD at a temperature of $50℃$. The corners 1 to 4 simulate a slow-slow (SS) process variation, where both carriers (p^+) and electrons (n^-) are less doped, decreasing the mobilities, supplying the devices with $VDD \pm 10\%$ at a minimum or maximum temperature. The corners 5 to 8 simulate a fast-fast (FF) process variation, where both carriers and electrons are more doped, increasing the mobilities, within the same supply and temperature conditions as the slow corners. The corners 9 to 12 simulate a fast-slow (FS) process variation, where the carriers are more doped and electrons are less doped, decreasing the mobilities, within the same supply and temperature conditions as the corners before. The corners 13 to 16 simulate a slow-fast (SF) process variation, similar to the fast-slow ones but with the carriers and electrons inversely doped.

Table 4 - Voltage and temperature of the typical and 16 PVT Corners, for slow, fast and crossed PMOS/NMOS mobilities.

Type	Corner	Voltage [V]	Temperature [°C]
Typical		0.5	50
SS, FF, SF, FS	1,5,9,13	0.45	125
	2,6,10,14	0.45	-40
	3,7,11,15	0.55	125
	4,8,12,16	0.55	-40

Since these corners provide distinct scenarios, the capacitance value will not be the same for every corner, though it should not vary greatly. So, before sizing the transistors to comply with the time and the noise restriction, it is necessary to select the slowest and noisiest corners. The Figure 4-10 shows a simulation of one the comparator integration nodes, at a frequency of $7\ \mathrm{MHz}$, where it can be identified the longest case scenarios. Namely, the slowest corner 2, with minimum supply voltage ($0.45\mathrm{V}$) and minimum temperature ($-40℃$), the second slowest corner 14, with maximum supply voltage ($0.55\mathrm{V}$) and minimum temperature ($-40℃$), plus the third slowest corner 4, with maximum supply voltage ($0.55\mathrm{V}$) and minimum temperature ($-40℃$). In spite of corner 2 be the proper choice to attend the time constraint, it had to be put aside, because it would demand far larger transistors (area) just to ensure a single case. Ergo the transistors of the integration block and regeneration block of the comparator are sized accordingly to the second slowest corner of the list – corner 14, which demanded an integrator with almost four times bigger dimensions than the required for corner 4. Now, we will first discuss the time constraints (speed), and only later the noise restrictions will be addressed.

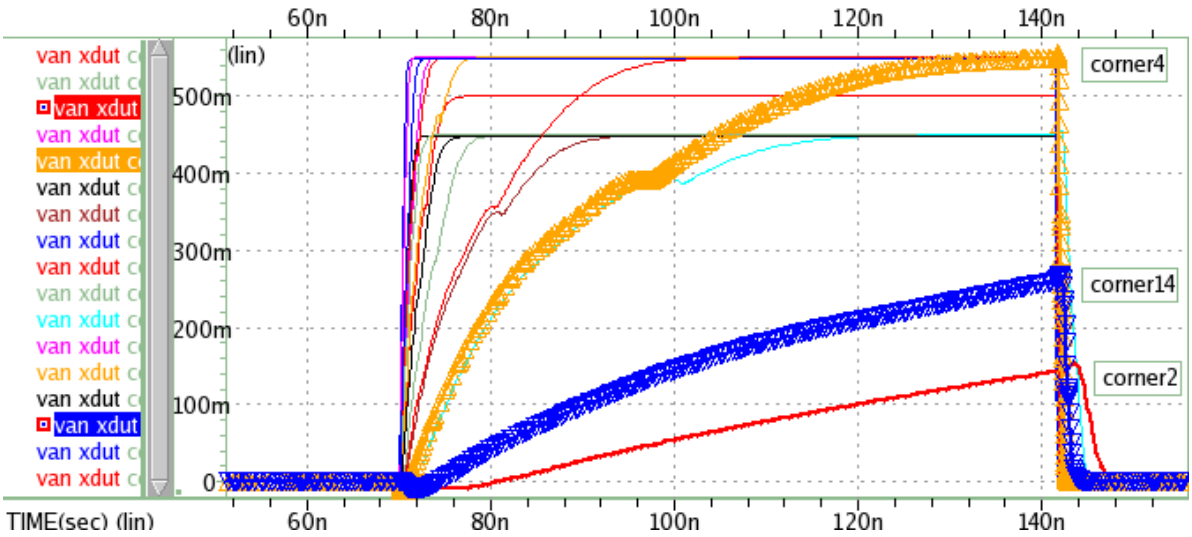

Figure 4-10 – Comparison of one integration node of the comparator in the typical and 16 corners at 7 MHz.

While sizing a transistor, relating the previous equations, one must consider that increasing its length (L) decreases its transconductance (g_m), enlarges its output resistance (r_{DS}) and also its associated capacitance (C_{bg}, C_{gs}, C_{gd}, C_{ds}). Consequently, it increases the integration time, but helps reducing its current leakage. On the other hand, increasing its width (W), the current allowed to pass increases, obtaining a decreased slew rate and r_{DS}, however its capacitance increases, since the area between the metal layer of the terminals and the substrate enlarges. In addition, for a fixed V_{GS}, the g_m is proportional to the ratio W/L, and, for a fixed r_{DS}, the NMOS has around 2 to 3 times more mobility, thus larger g_m, than the PMOS. Nevertheless, there are different corners that alter the oxide doping which influences their mobility and, likewise, their resistive relation. Regarding the integrator capacitance, it could be made (as conventionally) by two metal layers, which create a parallel-plate structure, or through a transistor implementation, whether by P or NMOS. The second procedure is often more area efficient, since a MOSFET as a capacitor can have the same value of an equivalent metal capacitor in a smaller space. Moreover, the C_F, which is charge during the integration phase, is made by a shorted PMOS instead of a NMOS, because while the capacitance value of the NMOS increases with its v_{GS}, the PMOS value decreases with its v_{GS}, being more area efficiency in this phase.

Furthermore, the previous theoretical calculation considers that the regeneration period begins when the integration as almost ended, whereas the processes occur in parallel (as shown in Figure 4-3), which makes the parameter ΔV_F (assumed to be constant) to differ with the integration rate, and, likewise, with the size of C_F. Hence, the sizing follows a convention, that makes a virtual time distinction, as shown in Figure 4-11, where the new integration period begins when M_1 starts conducting, evidenced by the node v_S, and ends when the output nodes (regeneration nodes) start diverging between them of a value of 3mV, where at the same instance we obtain ΔV_F. Subsequently, it starts the new regeneration time and ends when the output voltages $V_{OP,N}$ reach their respective voltage reference (with a deviation of 1mV). In turn, the decision time of the comparator only finishes after some inverters, as its output bit signal (q or $\bar{q}$) toggles and, likewise, the control signal of the state machine ($\overline{cmp\_rdy}$) returns a pulse.

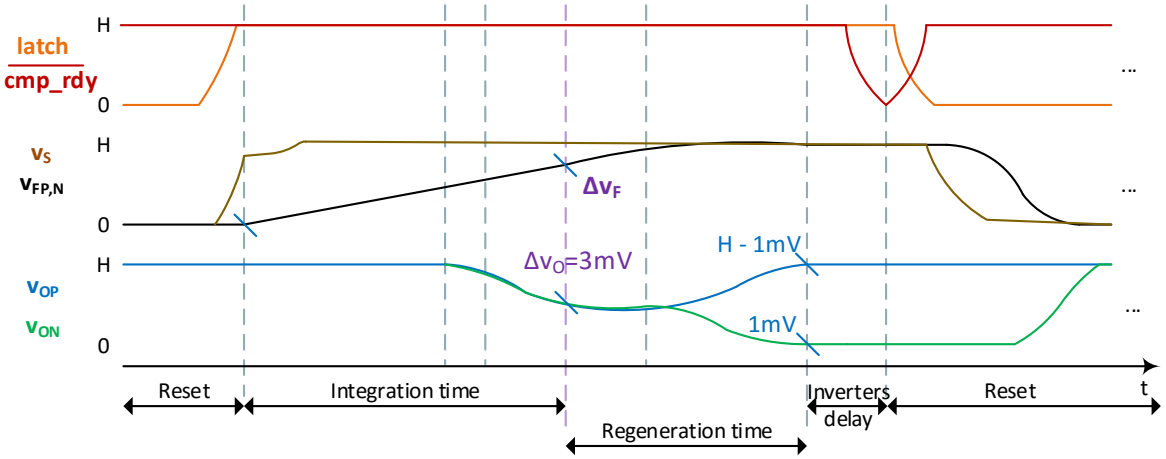

Figure 4-11 - Time diagram of the comparator operation convention regarding a positive input signal.

Although, the final values used for the transistors sizes (present in Table 5), do fulfill the **time restrictions** for corner 14, when the complete ADC is later simulated was seen that the common mode bias voltage (v_{CMcomp}) used at the time (around 130 mV) was not enough. In that situation, when the comparator differential voltage (v_{ID}) was around V_{DD}, one of the PMOS (comparator single ended inputs) had a negative voltage at its gate, which would wear or even disrupt that transistor. Therefore, to guarantee only positive input voltages, the v_{CMcomp} must increase to around 190 mV, which consequently slows down the device. In order to solve that, instead of resizing the comparator block, an extra capacitive circuitry is added (as presented in Figure 4-12) to accelerate the integration. In a similar way, it resembles a voltage doubler, since it consists of a capacitor that, while $latch$ is low (ϕ_1), is pre-charged to VDD, and, when $latch$ is high (ϕ_2), its top plate voltage reaches $2V_{DD}$. In turn, after M_1 starts conducting (ϕ_2'), the capacitor charge is passed to v_S (the mutual node of M_1 and M_2 of Figure 4-2). In order to have the charge injection in a profitable way, the switches size (obtained by simulation) have to be large enough to charge the capacitor (C_L) and minimize the voltage discrepancy between its top plate voltage and v_S.

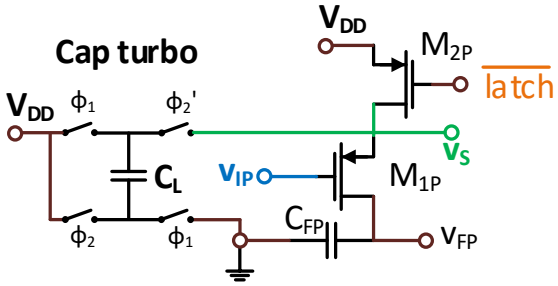

Figure 4-12 - Turbo capacitor that speeds up the integration stage, placed in one half of the Comparator differential pair.

In short, simulating with HSPICE, based on the previously explained assumptions, the dimensions of the components used in the implementation of the comparator are listed in Table 5, where the noise capacitor (C_F) is in fact composed by the Cap_noise and the parasitic capacitances in the node connected to the gate of transistor M_4.

Table 5 - Main components sizes in the comparator block.

Main comparator elements					
Transistor	**W [µm]**	**Fingers**	**W_{total} [µm]**	**L [nm]**	**Ratio W/L**
Cap_noise	2	40	80	250	320.0
M_1	0.44	80	35.2	30	1173.3
M_2	0.44	40	17.6	30	586.7
M_3	0.4	5	2	30	66.7
M_4	2.4	64	153.6	30	5120.0
M_5	1.5	64	96	30	3200.0
M_6	2.4	64	153.6	30	5120.0
M_7	0.6	64	38.4	30	1280.0
ϕ_1	2	16	32	30	3200.0
ϕ_2	2	128	256	30	8533.0
C_L	Cap turbo [pF]	5.5			

Hence, whether the turbo mechanism is turned OFF or ON, Table 6 presents the values of times, average capacitance, efficiency and average current of the selected main corners, namely the typical (Figure 4-13 and Figure 4-14), the noisiest, the fastest and slowest (Figure 4-17 and Figure 4-18) corners. Where we can verify, as supposed, that a faster corner consumes more current and, consequently, the transistors of the differential pair decrease their performance, by leaving the weak inversion region (where E_{ff} is around 20 or higher [25]) to the moderate (or even strong) inversion region. Likewise, we can state that in the slowest corner the differential pair is deeply in the weak inversion region.

Table 6 - Comparison of times, average noise capacitance, efficiency and average current between typical, noisiest, faster and slowest corners, with turbo OFF or ON.

Comparator data from main corners								
Corner	Typical		5		7		14	
Turbo	OFF	ON	OFF	ON	OFF	ON	OFF	ON
Observation	Standard		**Fast and Noisiest**	Fast	Faster	**Faster and noisiest**	**Slowest**	
V [mV]	500		**450**		**550**		**450**	
T [°C]	50		**120**		**120**		**−40**	
t_{integ} [ns]	1.14	0.23	**0.36**	0.15	0.16	**0.08**	24.25	**4.06**
$t_{regen+inv}$ [ns]	0.96	1.61	**0.37**	0.5	0.17	**0.23**	32.77	**38.53**
$t_{decision}$ [ns]	2.1	1.84	**0.73**	0.65	0.33	**0.31**	57.02	**42.59**
Cap_{noise}_av [fF]	74	75	**75**	77	73	**77**	76	**74**
C_F_av [fF]	234	237	**240**	247	239	**252**	235	**232**
E_{ff} (g_m/i_D)	19	14	**14**	10	12	**8**	32	**29**
$i_{D\_av\_period}$ [uA]	1.3	7.7	**1.3**	4.4	1.3	**5**	0.7	**5.2**

Moreover, evaluating the turbo, when enabled, in the slowest corner, it allows a reduction of around 20% of the comparator time decision at a cost of around 10 times the average current consumption (regarding when its disabled). Note that even though the regenerative time increases, the integration time decreases mores, reducing the overall decision time.

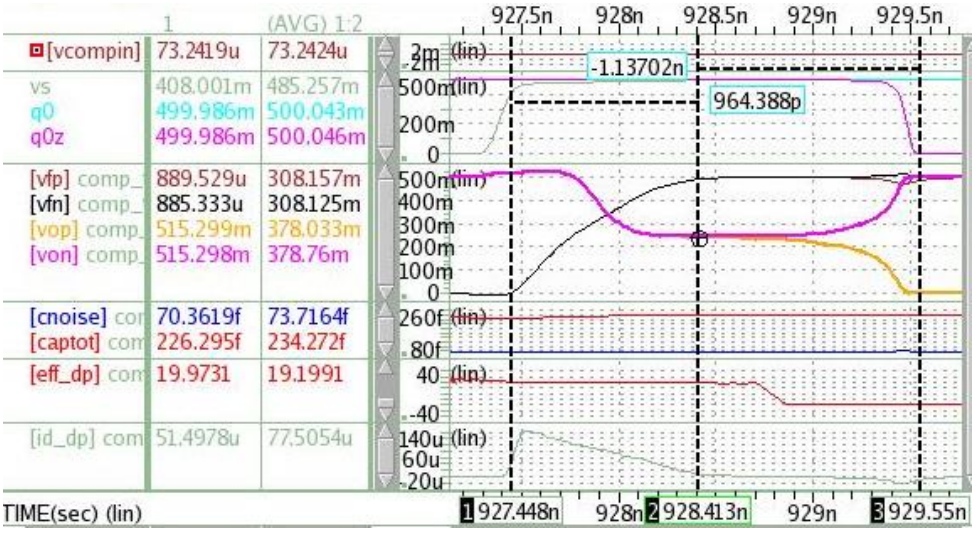

Figure 4-13 – Transient simulation of comparator operation in typical corner, having 73uV at input, with turbo OFF.

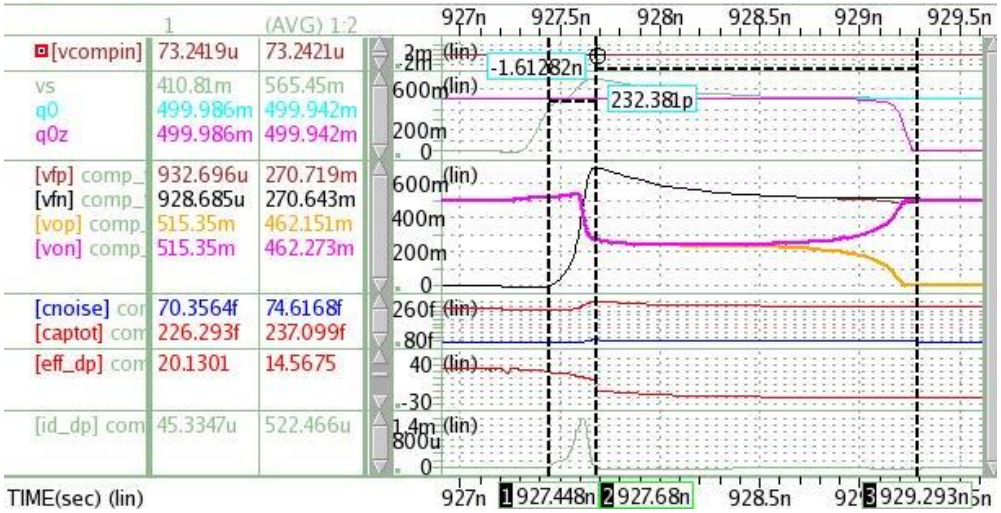

Figure 4-14 – Transient simulation of comparator operation in typical corner, having 73uV at input, with turbo ON.

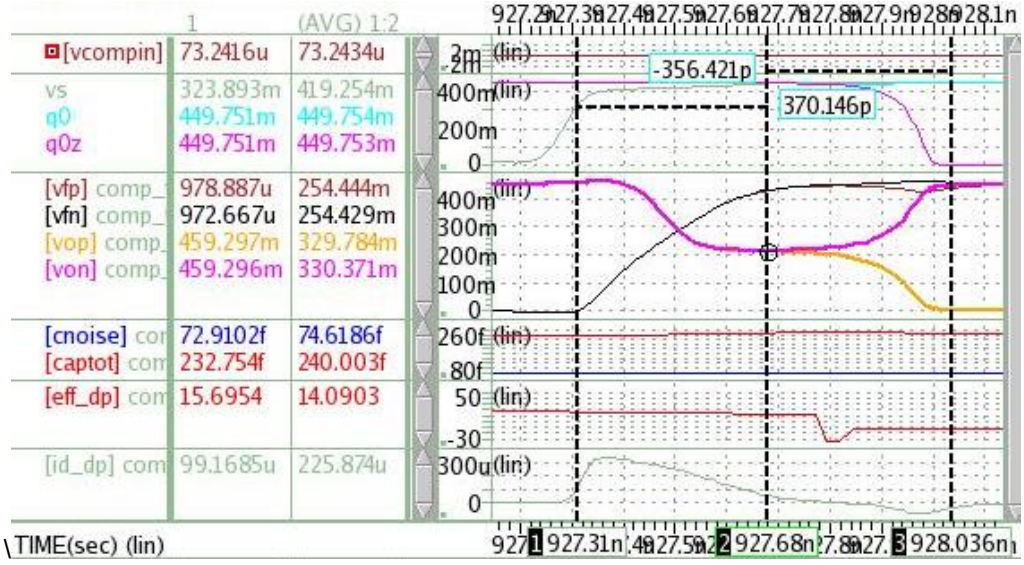

Figure 4-15 – Transient simulation of comparator operation in corner 5, having 73uV at input, with turbo OFF.

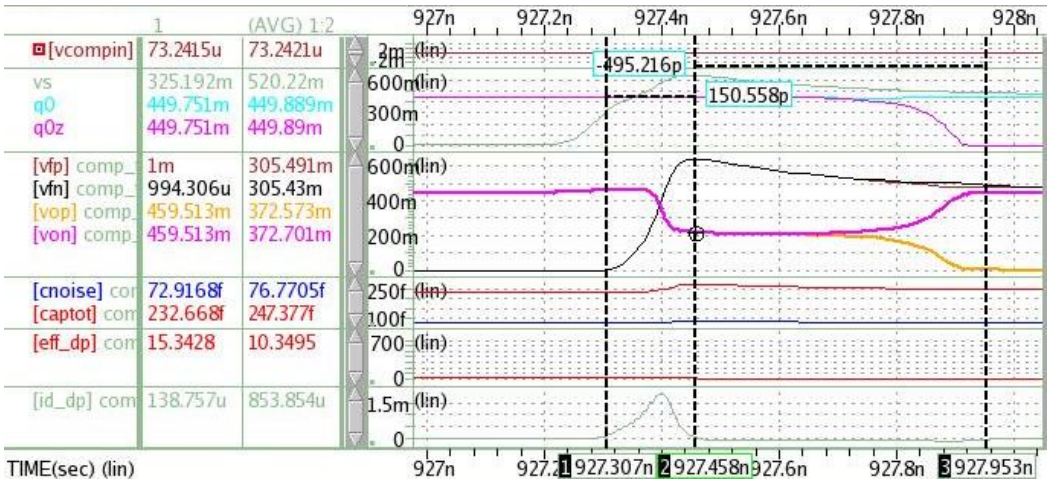

Figure 4-16 – Transient simulation of comparator operation in corner 5, having 73uV at input, with turbo ON.

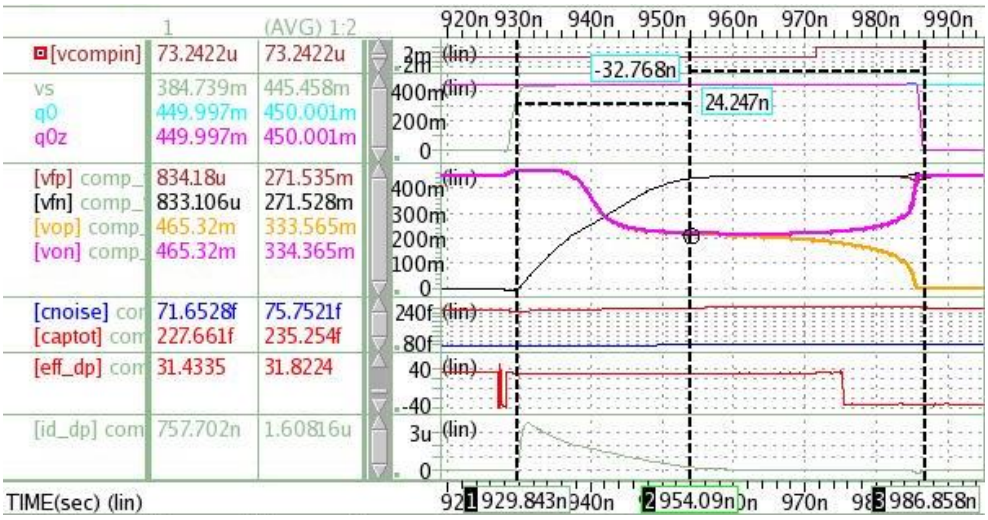

Figure 4-17 – Transient simulation of comparator operation in corner 14 (slowest), having 73uV at input, with turbo OFF.

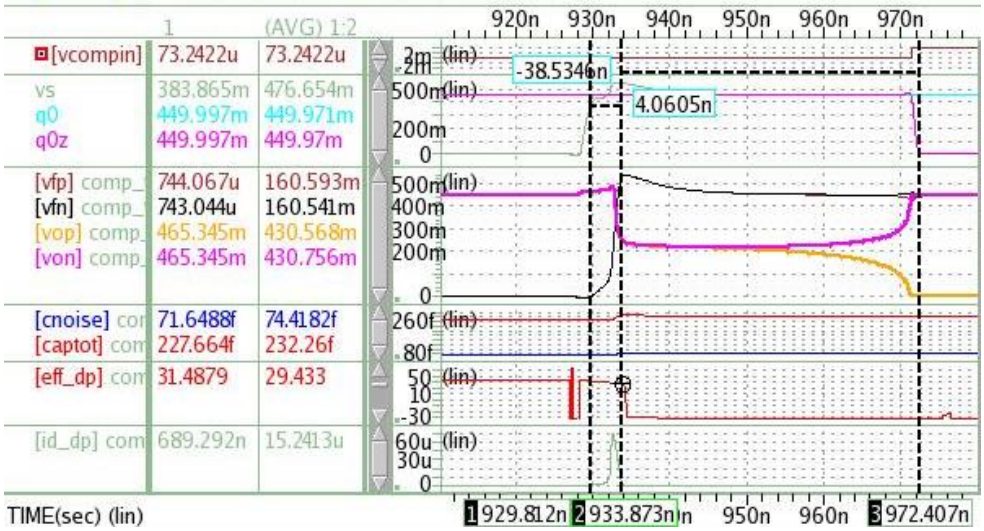

Figure 4-18 – Transient simulation of comparator operation in corner 14 (slowest), having 73uV at input, with turbo ON.

As shown the comparator operating times comply with the time restriction, and the **noise restriction** must be confirmed, so a transient noise simulation is performed for all corners, where it is possible to obtain the standard deviation value and, consequently, the estimated comparator output noise. This is done through a stochastic process by triggering the comparator 500 times with a maximum noise frequency of $15\ \mathrm{GHz}$, at a fixed input signal of $1\ \mathrm{mV}$, whose standard deviation value (i.e. the output referred noise) is given by [19]

$$\sigma^2\big(X(t)\big) = E(X(t)^2) - E\big(X(t)\big)^2, \tag{4.49}$$

where $X(t)$ is a Gaussian distributed stochastic process and $E\big(X(t)\big)$ is its expected value, which is equivalent to the relation between the differential output voltage root mean square (RMS) and its average (AVG) values as

$$\sigma\big(X(t)\big) = \sqrt{RMS^2 - AVG^2}. \tag{4.50}$$

In turn, we can express the comparator input referred noise as determined by [19] [25]

$$\sigma_{ni}(t) = {\sigma\big(X(t)\big)}\Big/{G_{eff}(t)}, \tag{4.51}$$

where $G_{eff}(t)$ is the effective gain of the regeneration nodes at a given sampling instant. Then, applying these concepts for the same selected corner as before, yields Table 7 and Table 8, respectively without and with turbo, which confirm that the produced noise is below the noise constraint ($\boldsymbol{\sigma_R}$), within a sufficient margin. Moreover, as an example of this procedure, Figure 4-19 illustrates the case for the fast noise corner 5. It also complies with the theoretical equation (4.47), using the simulation parameters from corner 5 with turbo disabled (Figure 4-16)

$$\begin{cases} C_F \approx 230\ \mathrm{fF} \\ \Delta V_F \approx 400\ \mathrm{mV}' \end{cases} \tag{4.52}$$

generates an input referred noise of

$$\sigma_{ni}^2 \approx (126\mu V)^2. \tag{4.53}$$

Table 7 - Comparison of the produced input referred noise between main corners, with turbo OFF.

Input referred noise from main corners with turbo OFF				
File_tr	0	5	7	14
V	0.5	0.45	max	Min
T	50	max	max	Min
Corner	Typ	**Worst noise**	Faster	Slowest
$\boldsymbol{RMS}$ [mV]	50.4	50.96	50.84	51.04
$\boldsymbol{AVG}$ [mV]	−50.25	−50.57	−50.52	−50.97
$\boldsymbol{\sigma}$ [mV]	4	6.3	5.7	2.8
$\boldsymbol{Geff}$	50.1	50.2	50.8	50.2
$\boldsymbol{\sigma_{ni}}$ [µV]	79.3	**126**	111	56.1
$\boldsymbol{\sigma_R}$ [µV]	**131.5**			
Margin: $\boldsymbol{\sigma_R - \sigma_{ni}}$ [µV]	52.2	**5.5**	20.5	75.4

Table 8 - Comparison of the produced input referred noise between main corners, with turbo ON.

Input referred noise from main corners with turbo ON				
File_tr	0	5	7	14
V	0,5	0,45	max	Min
T	50	max	max	Min
Corner	Typ	**Fast**	**Faster – worst noise**	Slowest
$\boldsymbol{RMS}$ [mV]	51.37	50.8	51.6	50.1
$\boldsymbol{AVG}$ [mV]	−51.22	−50.41	−51.18	−50.07
$\boldsymbol{\sigma}$ [mV]	3.87	6.27	6.52	2.05
$\boldsymbol{Geff}$	50.45	50.07	50.88	50.2
$\boldsymbol{\sigma_{ni}}$ [µV]	76.8	**125**	**128**	41
$\boldsymbol{\sigma_R}$ [µV]	**131.5**			
Margin: $\boldsymbol{\sigma_R - \sigma_{ni}}$ [µV]	54.7	**6.5**	**3.5**	90.5

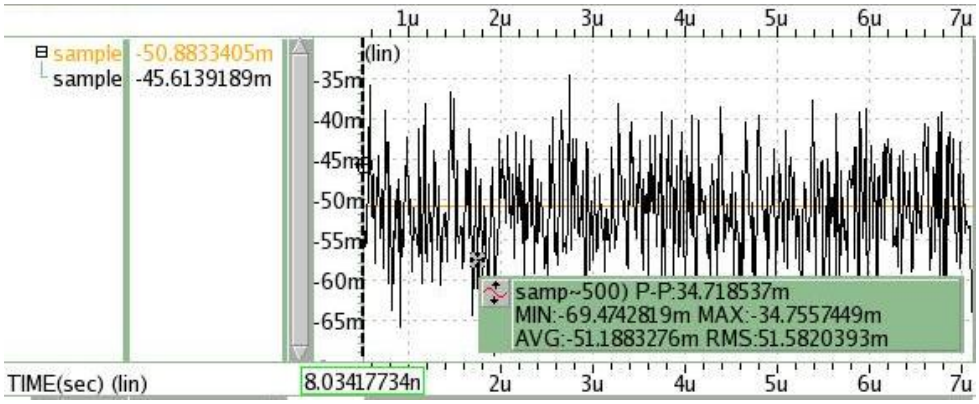

Figure 4-19 – Transient noise simulation of the comparator in corner 5, having turbo ON, with and without noise for a fixed input voltage of 1 mV, acquiring 500 samples with a noise frequency of 15 GHz and static gain of 50.

After making the comparator block satisfy its main restriction, having a sufficient margin for the noise and time restriction, in their both worst cases, we can now move on to the sampling block, which must be sized within the complete circuit of the converter. Although, as in any system every action is followed by a reaction, the error associated with the sampled signal also has a contribution from the comparator, so its effect shall be explained first.

4.3.3. Kickback Noise

Once a latched comparator has a positive feedback mechanism to regenerate the analog input signal into a full-scale digital level, its regenerative nodes need to vary within a large voltage excursion, and this voltage deviation can disturb the input voltage nodes, known as kickback effect or noise [26]. This is just a particular example, because any disturbance coming from an internal stage causes a re-action to the previous stage. The kickback might not be a critical issue for general signals; however, when we are dealing with a small signal, in the comparator input, it makes the difference between a right and bad decision. The Figure 4-20 shows half of the differential pair, where we can state that this type of disturbance propagates to the input terminal, mainly from the current flowing in the capacitances (C_{GS} and C_{GD}) inherent to the transistor. It can also be originated by charge variations at the gate of M_{1P},

when it changes the operating region (cut-off, triode and saturation). Note that these currents exist because v_S and v_{FP} vary.

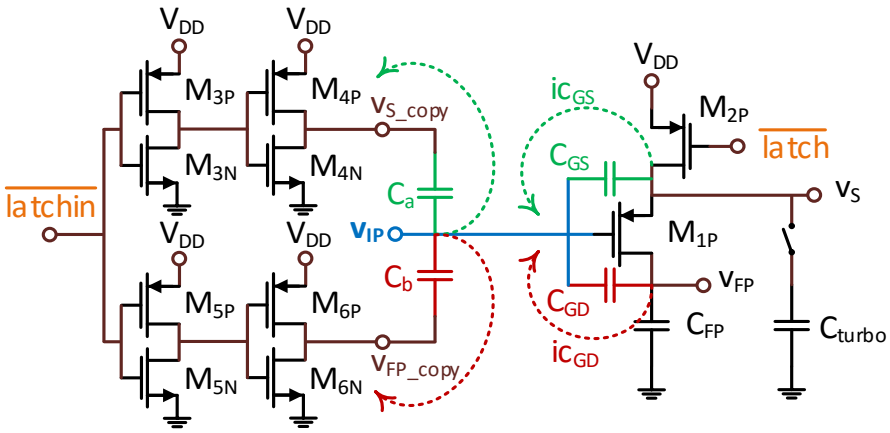

Figure 4-20 - Half of the comparator differential pair with parasitic and counter-kickback mechanism.

Having the M_{1P} transconductance constant, during the integration stage, the solution employed to minimize this effect goes through the reproduction of the reverse behavior caused by the parasitic capacitances. Hence, we add two capacitors to the input node, both with a similar value of the MOS parasitic capacitance and on the opposite terminal plate it is applied a signal that tries to replicate an inverted phase of the respective node, namely v_{S_copy} and v_{FP_copy}.

The inverted signals, as ideally denoted in Figure 4-21, are made by adjusting the signal that precedes and originates the signal $latch$. For that to happen, we use custom inverters to produce a similar slope for the rising edge of the copied signal, when the comparator input is near zero. Meaning that ideally the falling edge of v_{S_copy} should have the same rate as v_S rising edge, and likewise for v_{FP_copy} and v_{FP}, whilst v_{FP_copy} does not satisfy this idea because each corner has different integration rates.

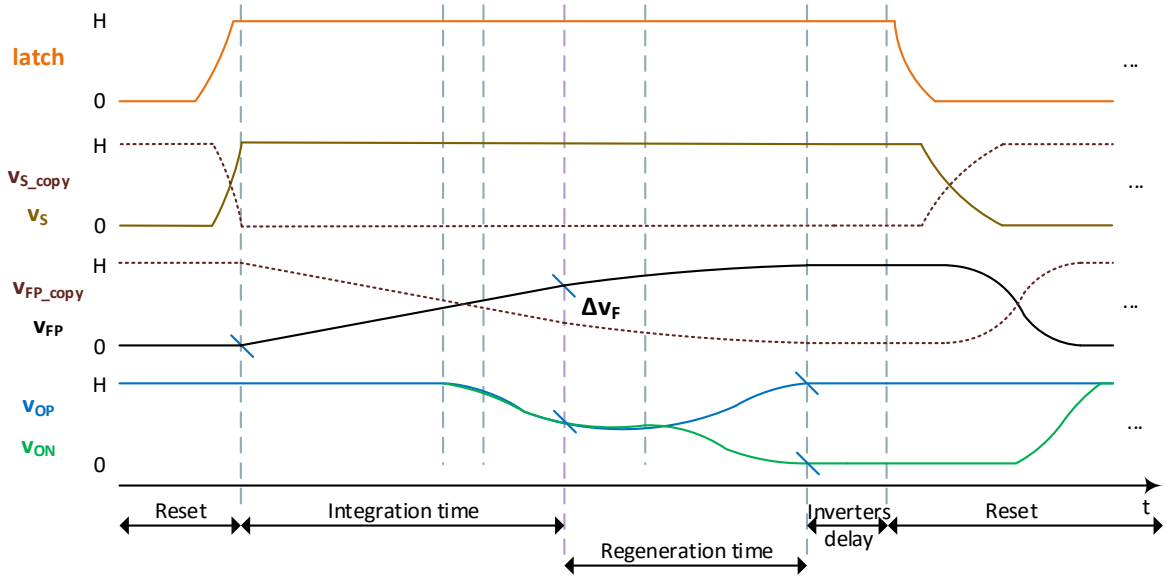

Figure 4-21 - Kickback effect and counter kickback phases (vs_copy and va_copy), in typical corner.

Consequently, Figure 4-22 and Figure 4-23 illustrates the result of the kickback effect, during the LSB decision (st_0), without and with the counter-kickback (CK) solution, while the comparator turbo mode is OFF and ON respectively. We can observe that the DAC differential output voltage - v_{DAC} (or the comparator input voltage), during the comparator integration phase (depicted by the rise of v_{fp}), has a more steady behavior with this solution than without it. Although, the simulation without turbo has a more clear impact of the effect reduction than the one with turbo, the important is to ensure that v_{DAC} has less deviation until the regeneration phase begins. In both cases, the node common voltage,

$$v_{CM} = \frac{v_{CM\ DACP} + v_{CM\ DACN}}{2}, \tag{4.54}$$

maintains its behavior, but without turbo v_{DAC} reduces its oscillation (in comparison with the case without the counter-kickback solution) approximately 4 times. In turn, with turbo we have v_{DAC} almost flat during most of the integration stage.

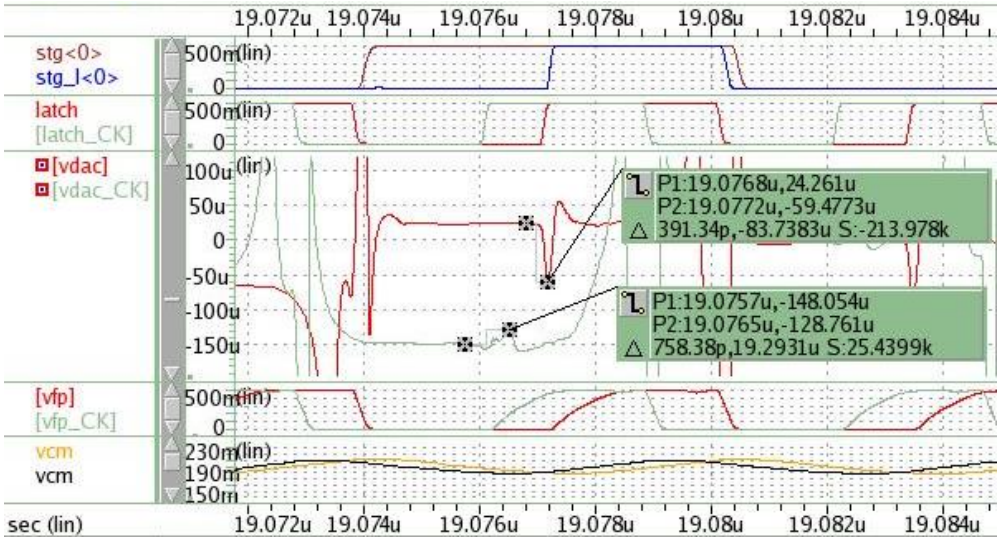

Figure 4-22 - Comparator input without and with counter-kickback (CK) effect, in typical corner, having turbo OFF.

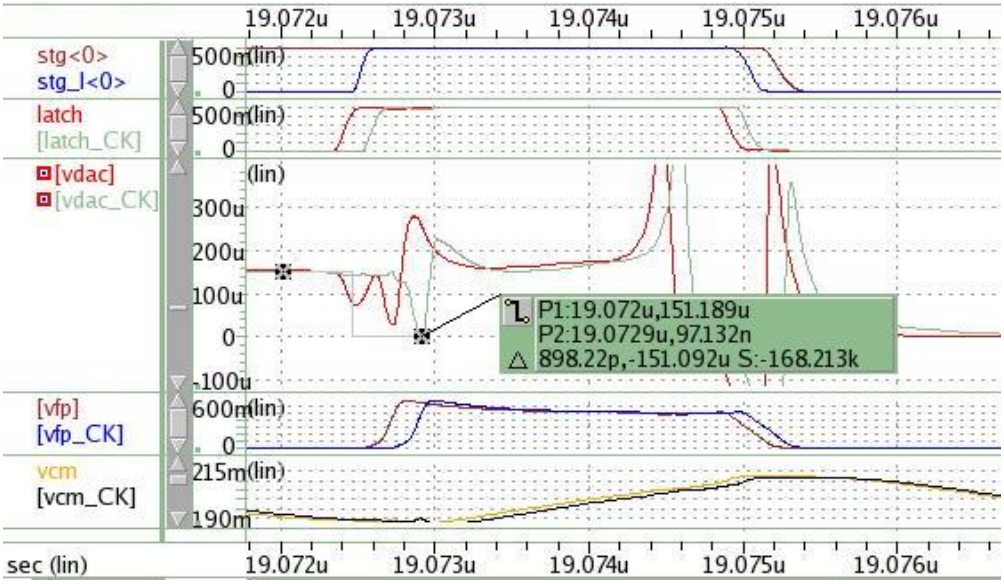

Figure 4-23 - Comparator input without and with counter kickback (CK) effect, in typical corner, having turbo ON.

4.4. Sampling DAC block

As referred in section 3.2 and depicted in Figure 3-6, after the sampling phase there is the conversion phase, where the sampled charge will be redistributed between capacitors. When the comparator decides a bit, its respective switches are activated to commute the respective capacitors to the selected reference voltage. This way, forcing a charge flowing in the array that directly causes voltages variations in the output node (v_{ON}). Thus, through the charge conservation principle, it is possible to determine the final value of v_{ON}, and afterwards the DAC differential output voltage (v_{OD}). So, let us assume Q_1 is the sampling charge and Q_2 is the charge when the conversion starts.

$$\begin{aligned} Q_1 &= \left(V_{CMcomp} - v_{IP}\right)\left(\sum_{k=0}^{N-1} 2^k + 1\right)C + V_{CMcomp}C_p \\ \Leftrightarrow Q_1 &= \left(V_{CMcomp} - v_{IP}\right)2^N C + V_{CMcomp}C_p \end{aligned} \tag{4.55}$$

$$\begin{aligned} Q_2 = {} & 2^{N-1}C\left(v_{ON} - b_{N-1}V_{REFP} - \overline{b_{N-1}}V_{REFN}\right) \\ & +2^{N-2}C\left(v_{ON} - b_{N-2}V_{REFP} - \overline{b_{N-2}}V_{REFN}\right) + \cdots + \\ & +C\left(v_{ON} - b_0 V_{REFP} - \overline{b_0}V_{REFN}\right) + C(v_{ON} - V_{REFN}) + C_p v_{ON} \\ \Leftrightarrow Q_2 = {} & \left(2^N C + C_p\right)v_{ON} \\ & -C(2^{N-1}b_{N-1} + 2^{N-2}b_{N-2} + \cdots + 2b_1 + b_0)V_{REFP} \\ & -C\left(2^{N-1}\overline{b_{N-1}} + 2^{N-2}\overline{b_{N-2}} + \cdots + 2\overline{b_1} + \overline{b_0} + 1\right)V_{REFN} \end{aligned} \tag{4.56}$$

Knowing that $V_{REF} = V_{REFP} - V_{REFN} \Leftrightarrow V_{REFP} = V_{REF} + V_{REFN}$ and applying the Boolean Complementary law $\left(b_i + \overline{b_i}\right) = 1$ in (4.56), then

$$\begin{aligned} \Leftrightarrow Q_2 = {} & \left(2^N C + C_p\right)v_{ON} \\ & -C(2^{N-1}b_{N-1} + 2^{N-2}b_{N-2} + \cdots + 2b_1 + b_0)V_{REF} \\ & -C\begin{bmatrix} 2^{N-1}\left(b_{N-1} + \overline{b_{N-1}}\right) + 2^{N-2}\left(b_{N-2} + \overline{b_{N-2}}\right) + \cdots + \\ +2\left(b_1 + \overline{b_1}\right) + b_0 + \overline{b_0} + 1 \end{bmatrix} V_{REFN} \end{aligned} \tag{4.57}$$

$$\begin{aligned} \Leftrightarrow Q_{2=} & \left(2^N C + C_p\right)v_{ON} - 2^N C V_{REFN} \\ & -C(2^{N-1}b_{N-1} + 2^{N-2}b_{N-2} + \cdots + 2b_1 + b_0)V_{REF}. \end{aligned} \tag{4.58}$$

Now, applying the charge conservative principle in the node v_{on}, the output voltage of the conventional binary-weighted capacitor array is

$$Q_1 = Q_2 \tag{4.59}$$

$$\Leftrightarrow \left(V_{CMcomp} - v_{IP}\right)2^N C + V_{CMcomp}C_p \tag{4.60}$$

$$= \left(2^N C + C_p\right) v_{ON} - 2^N C V_{REFN}$$

$$-C(2^{N-1} b_{N-1} + 2^{N-2} b_{N-2} + \cdots + 2b_1 + b_0) V_{REF}.$$

$$\Leftrightarrow v_{ON} = \frac{1}{2^N C + C_p}\left[2^N C (V_{REFN} - v_{IP}) + V_{CMcomp}\left(2^N C + C_p\right) + C(2^{N-1} b_{N-1} + \cdots + b_0) V_{REF}\right]$$

$$\Leftrightarrow v_{ON} = \frac{1}{1 + {C_p}/{2^N C}}\left[V_{REFN} - v_{IP} + (2^{N-1} b_{N-1} + \cdots + b_0)\frac{V_{Ref}}{2^N}\right] + V_{CMcomp}$$

$$\Leftrightarrow v_{ON} = \frac{1}{1 + {C_p}/{2^N C}}\left[V_{REFN} - v_{IP} + \frac{V_{Ref}}{2^N}\sum_{k=0}^{N-1} 2^k b_k\right] + V_{CMcomp}. \tag{4.61}$$

Having a differential input, there are two identical capacitive arrays that generate v_{ON} and v_{OP}, corresponding to each sampling line voltage, where the array relatively to v_{op} has its digital bits swapped by their complementary values and the input signal voltage is v_{IN} instead of v_{IP}, resulting in

$$\begin{cases} v_{ON} = \dfrac{1}{1 + {C_p}/{2^N C}}\left[V_{REFN} - v_{IP} + \dfrac{V_{REF}}{2^N}\displaystyle\sum_{k=0}^{N-1} 2^k b_k\right] + V_{CMcomp} \\ v_{OP} = \dfrac{1}{1 + {C_p}/{2^N C}}\left[V_{REFP} - v_{IN} - \dfrac{V_{REF}}{2^N}\displaystyle\sum_{k=0}^{N-1} 2^k b_k\right] + V_{CMcomp}. \end{cases} \tag{4.62}$$

Defining $G_{DAC} = \frac{1}{1 + {C_p}/{2^N C}}$ yields the differential output voltage as

$$\begin{cases} v_{OD} = v_{OP} - v_{ON} \\ v_{ID} = v_{IP} - v_{IN} \end{cases}, \tag{4.63}$$

$$\Leftrightarrow v_{OD} = G_{DAC}\left[v_{ID} - V_{REF}\left(\frac{2}{2^N}\sum_{k=0}^{N-1} 2^k b_k - 1\right)\right]. \tag{4.64}$$

As it can be seen, the C_p only introduces an attenuation ($G_{DAC} < 1$), not affecting the linearity, the DAC output is not distorted by this factor and once the comparator only verifies if its input is positive or negative, then G_{DAC} will be ignored in the following expressions. In turn, having the S/H and DAC blocks merged in the sampling DAC, its output voltage (v_{OD}) is given by the difference between the sampled signal $v_{S/H}$ and the digital code analog representation as its input, i.e.

$$v_{OD} = v_{S/H} - v_{DAC} \Leftrightarrow v_{OD} = v_{ID} + V_{REF}\left(1 - \frac{2}{2^N}\sum_{k=0}^{N-1} 2^k b_k\right), \tag{4.65}$$

$$\begin{cases} v_{S/H} = v_{ID} \\ v_{DAC} = V_{REF}\left(\frac{2}{2^N}\sum_{k=0}^{N-1} 2^k b_k - 1\right). \end{cases} \quad (4.66)$$

Consequently, the easiest way to verify the correct operation of the array, following the previous equations, it is to check when its output voltage is null, which implies

$$v_{OD} = 0 \Leftrightarrow v_{ID} = V_{REF}\left(\frac{2}{2^N}\sum_{k=0}^{N-1} 2^k b_k - 1\right). \quad (4.67)$$

For the lowest digital code possible to address the sampling DAC (every bit at 0), the necessary input voltage (v_{ID}) that makes the comparator decision threshold is $v_{ID} = -V_{Ref}$. In opposite, for the highest digital code possible to address (every bit at 1), the respective input is $v_{ID} = V_{REF}$. This helps to clarify how the reference voltage defines the converter full-scale input range, as stated in the metrics section. Moreover, considering $V_{REF} = V_{DD} = 0.5$ V and $V_{FS} = 2V_{DD}$, the reference voltages for every bit decision are determined by

$$\begin{cases} V_{REFP} = \frac{V_{DD}}{2} + \frac{V_{FS}}{4} = V_{DD} = 0.5 \text{ V} \\ V_{REFN} = \frac{V_{DD}}{2} - \frac{V_{FS}}{4} = 0 \text{ V}. \end{cases} \quad (4.68)$$

This way, these references are the same as the supply voltages (V_{DD} and GND), which are inherently of low impedance, this way the capacitors are easily charged and also creates a larger quantization step than more limited voltages, allowing the maximum wide of FS, which reduces the noise effect (thus improving the SNR).

Another practice employed that saves time and power consumption (during conversion) is accomplished by connecting every capacitor in the DAC array to a mid-scale value ($V_{REF}/2$) right before the conversion. Whereas it requires more switches to provide a mid-scale reference, only half of the power is required to switch a capacitor to the selected reference, instead of using the entire voltage excursion from the negative to the positive reference. In addition, this creates a differential voltage that allows the MSB decision to be taken without switching any capacitor, only switching the MSB capacitors afterwards, and the same happens to the LSB. Rather than using more complex circuitry to provide this voltage supply, the C_{unit} is split in half and each one is put at different reference voltages. Thus, after sampling, the positive reference voltage (V_{REFP}) is applied directly to one half of C_{unit} (C_a) and the negative reference (V_{REFN}) to the other half (C_b), i.e.

$$\begin{cases} C_a + C_b = C_{unit} \Leftrightarrow C_a = C_b = C_{unit}/2 \\ V_{REF}/2 = (V_{REFP} - V_{REFN})\, C_a/(C_a + C_b) = V_{DD}/2 \end{cases}. \quad (4.69)$$

4.4.1. Bridge capacitor array

While the device resolution is improved, the number of capacitors would increase linearly, in the sampling DAC array, and so it would increase their size, for its respective binary weight, as shown in Figure 3-6. However, their size does not need to follow this trend when a split capacitor is employed in

the array, also known as bridge capacitor, still maintaining the DAC output of (4.64). In addition, the higher the size difference between the bigger and the smaller capacitors, the higher would be the problems due to mismatch from fabrication (namely their symmetry and error in its overall capacitance). Consequently, besides the cost of silicon area for big capacitors, the major issue regarding parasitics would be in the smaller ones, which could be the same size or smaller than the parasitics themselves, degrading their contribution.

Following a 12-bit sampling DAC array, in binary weighted linear scaling, would correspond to a MSB capacitor of $2^{12-1}C = 2048C$, admitting a LSB of unitary value C, hence there is a significant margin of values between the bigger and the smaller capacitors, causing a great discrepancy in their size. So, knowing that the binary weighted array is scaled up by a factor of 2, the output voltage variation of the DAC between two capacitors can be expressed as

$$\frac{\Delta v_{ON}|_i}{\Delta v_{ON}|_j} = \frac{C_i}{C_j} = 2^{i-j}, \tag{4.70}$$

where $i > j \; \forall \, i,j \in \mathbb{N} \wedge i \subset [0; N-1]$. Thus, as illustrated in Figure 4-24, employing a bridge capacitor (C_B) in the middle of the array, the MSB capacitor would only have to be $2^{(12/2)-1}C = 32C$, having the LSB as a unit capacitor. This way, not only the MSB capacitor uses less area, but it also allows the LSB to not have a size too small. It decreases the size discrepancy and improves capacitor mismatch. In addition, the LSB could be fabricated with a size smaller the unit size (maintaining the binary relation), however if its size is too small its significance could be overcome by the parasitic capacitance (i.e. $C_p > C_{LSB}$).

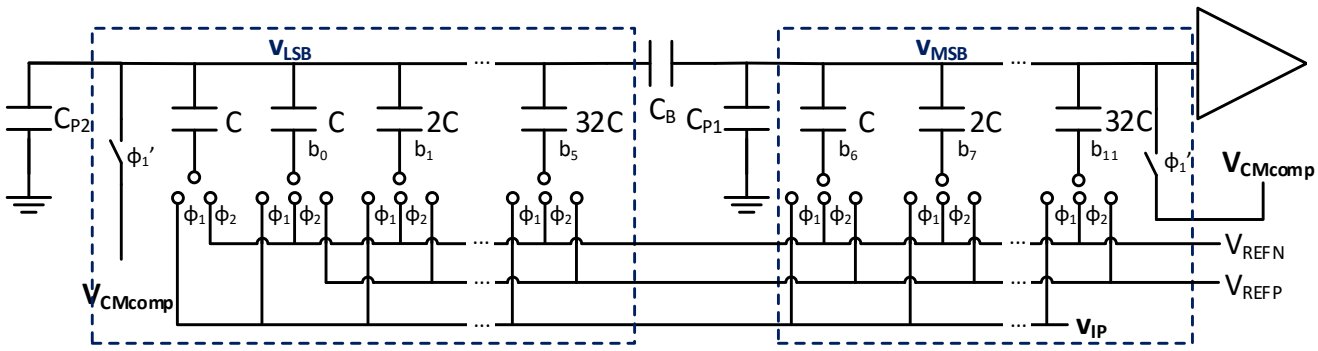

Figure 4-24- Example of a 12-bit split capacitive array.

An option to determine this bridge capacitor can be done through (4.70), relating the ratio of voltage variations correspondent of 1 bit from the MSB capacitors group and 1 bit from the LSB capacitors group. So, for instance, let us consider bit 7 and bit 2 in the next calculations, whose equivalent circuits are represented in Figure 4-25, assuming $v_{IP} = V_{CMcomp} = 0\,\text{V}$, and the reference voltages as stipulated in (4.68).

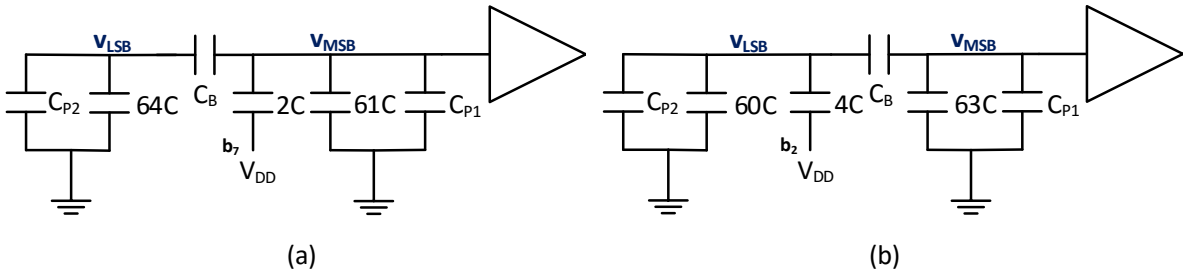

Figure 4-25 - Equivalent circuits of the sampling DAC for the selection of bit 7 (a) and for bit 2 (b).

Thus, the associated output voltage variation of bit 7 – $\Delta v_{MSB}[b_7]$, where $b_7 = 1$ and the remaining bits are 0, is given, as a capacitive divider, by

$$\Delta v_{MSB}[b_7] = \left({}^{2C}\Big/ {}_{2C + 61C + C_{P1} + \frac{C_B \times 64C}{C_B + 64C}} \right) V_{DD}. \tag{4.71}$$

In turn, the associated intermediate voltage variation of bit 2 – $\Delta v_{LSB}[b_2]$, where $b_2 = 1$ and the remaining bits are 0, is given, as a capacitive divider, by

$$\Delta v_{LSB}[b_2] = \left({}^{4C}\Big/ {}_{4C + 60C + C_{P2} + \frac{C_B(63C + C_{P1})}{C_B + 63C + C_{P1}}} \right) V_{DD}, \tag{4.72}$$

which allows to obtain its respective output voltage variation – $\Delta v_{MSB}[b_2]$ – as

$$\Delta v_{MSB}[b_2] = \left({}^{C_B}\Big/ {}_{C_B + 63C + C_{P1}} \right) \Delta v_{LSB}[b_2] \tag{4.73}$$

$$= \frac{C_B}{C_B + 63C + C_{P1}} \left({}^{4C}\Big/ {}_{4C + 60C + C_{P2} + \frac{C_B \times 63C}{C_B + 63C}} \right) V_{DD}. \tag{4.74}$$

Therefore, the bridge capacitor is given by the ratio of (4.71) and (4.74), regarding (4.70), plus admitting $C_{P2} = 0$, yield

$$\frac{\Delta v_{ON}|_7}{\Delta v_{ON}|_2} = \frac{\Delta v_{MSB}[b_7]}{\Delta v_{MSB}[b_2]} \Leftrightarrow 2^{7-2} = \frac{C_B + 64C}{2C_B} \tag{4.75}$$

$$\Leftrightarrow C_B = \frac{64C}{63}, \tag{4.76}$$

which shows that C_{P1} does not affect this ratio. Now, admitting $C_{P2} \neq 0$, the same expressions yield

$$\frac{\Delta v_{ON}|_7}{\Delta v_{ON}|_2} = \frac{\Delta v_{MSB}[b_7]}{\Delta v_{MSB}[b_2]} \Leftrightarrow 2^{7-2} = \frac{C_B + 64C + C_{P2}}{2C_B} \tag{4.77}$$

$$\Leftrightarrow C_B = \frac{64C + C_{P2}}{63}, \tag{4.78}$$

which shows that, on the other hand, C_{P2} has an influence in this ratio, and thus in the linearity of the DAC array. As mentioned before, although this technique is better than the conventional one (for size discrepancy), due to this disadvantage in linearity, the DAC array shall require a digital calibration.

When we use redundancy, the previous method could also be used, but another method is used to facilitate the calculation. The determination of C_B can also be simplified by the charge fluctuation of

sampling exactly zero (forcing it with a DC voltage source) and just switching the largest capacitor attached at the v_{LSB} node, as depicted in Figure 4-26.

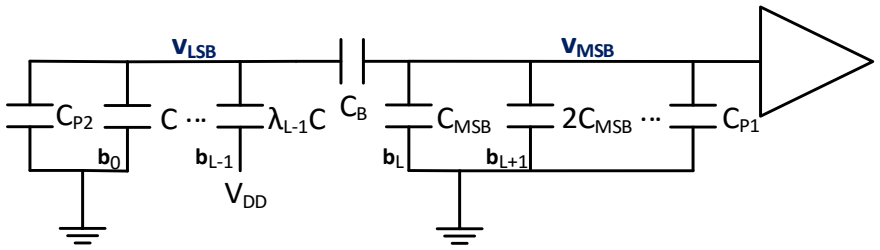

Figure 4-26 - Equivalent circuits of the sampling DAC for the selection of the biggest capacitor in the LSBs.

At first, we sample zero input value, having Q_1 as its charge (i.e. $v_{IP} = V_{CM} = V_{test} = 0$ V), forcing no voltage variation in the v_{MSB} node nor in the v_{LSB} node. Secondly, the bit of the biggest capacitor in the v_{LSB} side is set to 1, making Q_2 as the charge right after the conversion. This way we get

$$\begin{cases} Q_1 = 0 \\ Q_2 = \left(C_P + C_B + \sum_{i=0}^{L-1} \lambda_i C\right) v_{LSB} - \lambda_{L-1} C V_{DD}, \end{cases} \tag{4.79}$$

$$\Longrightarrow v_{LSB} = {\lambda_{L-1} C V_{DD}} \Big/ {C_P + C_B + \sum_{i=0}^{L-1} \lambda_i C}, \tag{4.80}$$

where λ_i is the capacitor weight coefficient and L is the smallest capacitor attached to v_{MSB} node. Plus knowing that the amount of charge that flows through C_B into V_{test} is

$$\Delta q = C_B v_{LSB}, \tag{4.81}$$

we want that the transition of the $\lambda_{L-1}C$, the biggest capacitor attached to v_{LSB} node, causes a charge flow equal to

$$\Delta q = \propto (C_{MSB}/2) V_{DD}, \tag{4.82}$$

where $\propto$ is the redundancy factor. Hence, relating the equations (4.81) and (4.82), we have

$$C_B \, {\lambda_{L-1} C V_{DD}} \Big/ {C_P + C_B + \sum_{i=0}^{L-1} \lambda_i C} = \propto (C_{MSB}/2) V_{DD}, \tag{4.83}$$

$$\Leftrightarrow C_B(\lambda_{L-1} C - \propto C_{MSB}) = \propto (C_{MSB}/2) \left(C_P + \sum_{i=0}^{L-1} \lambda_i C\right), \tag{4.84}$$

$$\Leftrightarrow C_B = \left(C_P + \sum_{i=0}^{L-1} \lambda_i C\right) \Big/ \left(\frac{\lambda_{L-1} C}{\propto (C_{MSB}/2)} - 1\right), \tag{4.85}$$

meaning that C_B is given by the ratio of

$$(The\ sum\ of\ every\ cap\ in\ v_{LSB}\ node, except\ C_B) \Big/ \left(\frac{Biggest\ cap\ in\ v_{LSB}\ node}{Smallest\ cap\ in\ v_{MSB}\ node(\propto/2)} - 1\right) \tag{4.86}$$

4.4.2. Sampling DAC sizing

As detailed in this section, the sampling DAC consists mainly by three sub-blocks, one block for the capacitive array, one for their switches and another for their respective logic, which is controlled by

the converter state machine. The sizing of the capacitive array and the respective switches are made through an iterative process, starting by binary scaling both capacitors and switches, regarding their bit weight. Similarly, both of them can be made through a unit block (with unit sizes) that are replicated as many times necessary to achieve the desired size, or through a custom schematic block for each bit weight, depending on the layout. Even though using more instances or transistors with multiple fingers gamble with parasitic effects. At first will be denoted the employed topologies for those blocks and then explained their trade-offs decisions.

4.4.2.1. Sampling DAC capacitors

As stated before, this ADC is conceived to have a 12-bit resolution, for that it demands 12 decisions. However, 2 more decisions are added to make redundancy, and rectify wrong MSB decisions, when determining the inferior decision [27]. Since each decision would imply a capacitor, so 14 decisions would imply 14 capacitors, in each branch of the Sampling DAC, but in fact is not necessary. Instead, we use 12 plus 1 (for digital calibration, explained later), employing an array split in 3 groups – MSB, ISB and LSB, as shown in Figure 4-27, our redundancy is created by multiplying the capacitors of the last two groups with scale factors. These factors increase the voltage levels (or steps) of the DAC transfer function, allowing the voltage decision window to enlarge. This way, the SAR algorithm can repeat its search, within a voltage range for which the comparator already had been triggered. In addition, a bridge capacitor (C_B) is used between the ISB and LSB group capacitors, for the reasons explained before.

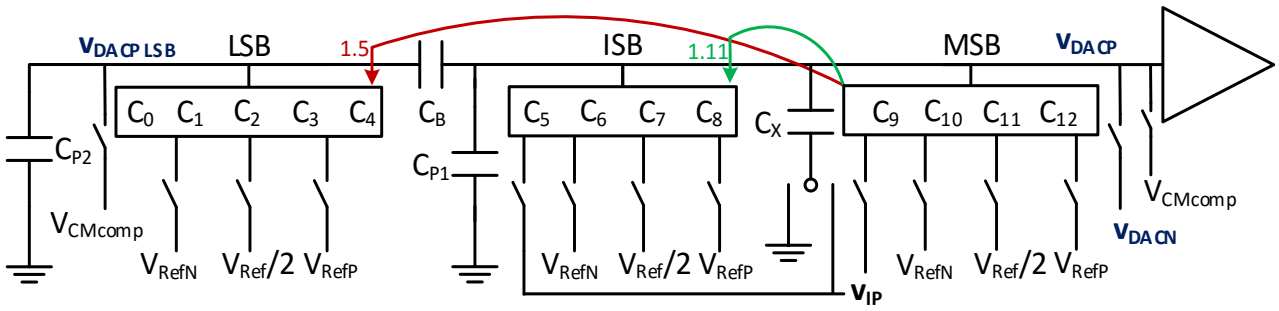

Figure 4-27 - One branch of the Sampling DAC block.

As shown in section 3.3, the input signal does not need to be sampled in every capacitor (nor just one), allowing a reduction of the number of commutations during sampling (ergo on consumption). Once the LSB group has a larger overall capacitance, it would increase the overall capacitance seen by the input of the Sampling DAC. In our case, we use the capacitors from the MSB and ISB group to sample, leaving the LSB group only for conversion and (mismatch) calibration purposes. If the input signal was sampled within a smaller capacitance than the one used for conversion, it would affect the DAC voltage scale, causing a gain error (i.e. attenuation) in the ADC transfer function. In order to fix that, we could add another capacitor (C_X) just during sampling, with the same size as the smallest one of the sampling group as substitution of the non-used load (LSB group). However, since we apply redundancy in the ISB group, we increase its capacitance value and there is no need for an extra capacitance. Moreover, eventual errors can also be fixed by the digital calibration.

The first step to size these capacitors is to determine the unit capacitor (C_{unit}), which is defined by the ratio of the total sampling capacitance (C_S), from (4.12), and their binary weighted sum. Thus, choosing the contribution of the ISB and MSB group capacitors for sampling, the binary weighted sum is given by 256.65, which results in the C_{unit} stated in **Error! Reference source not found.**.

Secondly, the redundancy is applied, while the MSB group capacitors are binary scaled, the ISB group capacitors have a scaling factor of 1.11 (though they are binary scaled between them). This makes the last capacitor of the MSB group (C_9) to be $2/1.11$ larger than the first one of the ISB group (C_8). In turn, the LSB group is also scaled the same way as the ISB group, but the C_B size has to be such that performs a scaling factor of 1.5 between the C_9 and the first one of the LSB group (C_4). Making C_9 to be $2/1.5$ larger than C_4 .Even though, the size of C_B is adjusted by simulation, we can determine its contribution as shown in section 4.4.1, replacing the parameters in equation (4.85), as

$$C_B = \frac{C_P + 0.25C + 0.5C + C + 2C + 4C}{\frac{4C}{(1.5/2) \times 1.11C} - 1} = \frac{C_P + 7.75C}{3.8}. \tag{4.87}$$

Table 9 - Sampling DAC capacitors units, regarding their architecture and binary weight.

Capacitor group	C bit index	C bit weight and size
MSB	$C_9, C_{10}, C_{11}, C_{12}$	$C''' + 2C''' + 4C''' + 8C'''$
		$16C + 32C + 64C + 128C$
ISB	C_5, C_6, C_7, C_8	$C'' + C'' + 2C'' + 4C'' + 8C''$
		$1.11C + 2.22C + 4.44C + 8.88C$
LSB	C_0, C_1, C_2, C_3, C_4	$C' + 2C' + 4C' + 8C' + 16C'$
		$0.25C + 0.5C + C + 2C + 4C$
Sampling	$\boldsymbol{C_5}$ to $\boldsymbol{C_{12}}$	$\boldsymbol{256.65C}$
$\boldsymbol{C_{unit}}$	$C = \frac{C_S}{256.65} = \frac{688}{256.65} \approx 2.7$ fF	
$\boldsymbol{C'''}$	$16C$	
$\boldsymbol{C''}$	$1.11C$	
$\boldsymbol{C'}$	$0.25C$	

4.4.2.2. Sampling DAC switches

After toggling a switch, there is always a period time for which its output voltage transits to the same input voltage, taking longer as bigger the capacitive load in the output node and the switch ON-resistance. Hence, having sized the capacitors, we now require switches that commute within the stipulated settling time. However, due to the supply conditions of this work this was not just a straightforward task. When transistors operate with a voltage supply inferior to the nominal one (0.5 V instead of 0.9 V), their V_{GS} decreases, whilst their V_T does not decrease, but, in fact, it stays almost the same. So, for a sizing guideline, we can use the expression for the channel resistance (r_{DS}) of the MOS transistor, in the triode region (with a linear behavior), given by [22]

$$r_{DS} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (v_{GS} - V_T)}, \tag{4.88}$$

where $\mu_n C_{ox}$ and V_T are factors dependent of the used technology, W/L is the ratio of the MOS sizes (width and length, respectively). One can state that a small v_{GS} results in a large r_{DS}. Although, in reality for $V_{DD} < V_N$, we have far bigger resistances when the switch is suppose to be ON, which increases the

switching settling time. Plus, since the resistance will never be infinite, the transistor will always drive some current (i_{DS}). So when a switch is OFF, its driving current is denominated i_{OFF} or leakage current (i_{leak}) and, likewise as V_T, independent of v_{GS}(or V_{DD}), its value is the same.

In short, lower supply voltages generate two setbacks, bigger ON-resistances and increased significance of leakage current, which, respectively, results in slower switchings and greater difficulty to contain the charge in the nodes. In order to reduce the leakage current impact, several attempts have been put into practice. One can manipulate the transistors sizes, whether through: **A)** increasing the resistance by using a minimal (or small) W, while increasing just its L; or **B)** by maintaining the resistance value, increasing both W and L, maintaining its W/L ratio, (since it places the internal terminals further apart); or **C)** employing small or minimal W and L sizes combined with clock-boosts (CBs). Alternatively, we can use escape routes transistors to isolate the leakage current impact, or even place dummy transistors to counter balance it in different branches.

The switches group of the sampling DAC are separated as their functionality, for sampling phase or for conversion phase. In a first step, a sampling circuit is often composed of a capacitive load charged by one simple switch, as depicted in Figure 4-28 (a), which is a parallel pair of a NMOS complemented with a PMOS. As shown in Figure 4-28 (b), the r_{DS} of the NMOS increases with v_{IN}, but on the other hand the PMOS behaves inversely. Thus, when both switches are used, we can ensure that the sampling capacitor will always be charged, regardless of v_{IN}. In a second step, conversion circuitry is composed of the capacitive load linked to the references switches, namely one PMOS for the positive reference and another NMOS for the negative one. Moreover, another similar pair of switches is used to perform a mid-scale voltage.

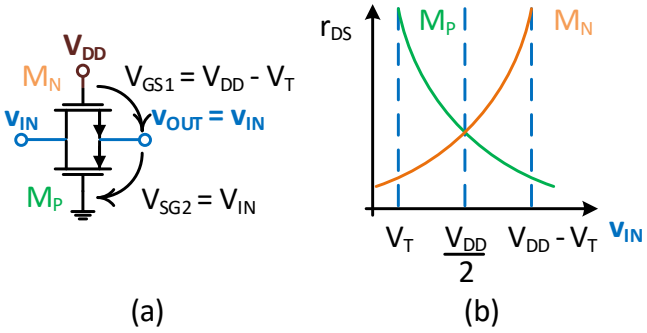

Figure 4-28 – Sampling switches, showing their (a) voltages and (b) inner resistance as the input voltage varies.

For ease of explanation, let us represent the sampling DAC as a simple RC circuit during sampling as depicted in Figure 4-29, where the sampling switch (M_N) is ON – behaves as a resistor (R_S) – and the references switches (M_{PSW} and M_{NSW}) are OFF– behave as a leakage current source (I_{leak}) while charging a capacitor. We know that v_{IN} would be sampled with an associated error (ε_{samp}), which is given by the amount of voltage drop in R_S and the leakage currents, that is

$$\varepsilon_{samp} \equiv R_S(I_{leakP} - I_{leakN}). \tag{4.89}$$

Hence, if we have $V_{DD} < V_N$, the I_{leak} would maintain, but R_{ON} would increase and, so, would the ε_{samp}. This way, respecting equation (4.88), to decrease R_{ON}, one need to increase the W.

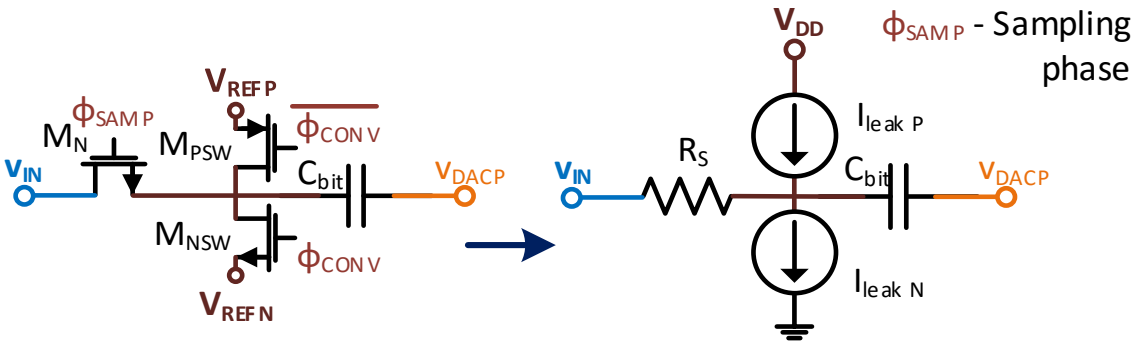

Figure 4-29 - Simple Sampling DAC switches during sampling phase.

In turn, let us see the same way the sampling DAC during the conversion phase, when for instance one bit is already decided, as depicted in Figure 4-30, where now the sampling switches are OFF, the selected reference switch is ON (e.g. putting the respective capacitor at the positive reference voltage) and the other reference switch if OFF. Here, the leakage current is so significant that destroys the bit conversion phase, and after trying the above mentioned hypotheses, we chose to create the sampling switches in T-format. This way, the previous pair is split in two, creating an intermediate node, which connected to another transistor allows an escape route for the leakage current, generated from the first pair associated to v_{IN}. Besides that when one branch of the DAC has a positive reference switch ON and the negative one OFF, the complementary action happens in the other (branch) side. Thus, the leakage current, present from those switches (PMOS or NMOS), is different in both sides, causing an asymmetry reflected in a differential DAC output voltage (v_{DAC}), which is even aggravated as v_{IN} increases. Hence, to counter-balance this asymmetry, another dummy pair of switches are added, with the same sizes as the reference ones (being turned OFF the whole time).

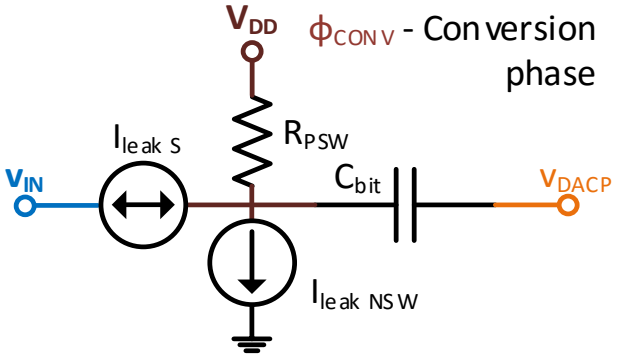

Figure 4-30 - Simple Sampling DAC switches during conversion phase.

Therefore, each capacitor in the array has its bottom plate linked to a group of switches as illustrated in Figure 4-31, which is composed by the pair of sampling switches, two reference switches for conversion, two switches for the middle-scale voltage, and two dummy switches. The sampling switches are now made by two consecutive pairs of both NMOS and PMOS – $N_1/\ P_1$ and N_2/P_2, plus having an intermediate escape route NMOS - N_3. For the conversion switches is required a PMOS (P_{SW}) that connects the capacitor to the positive reference (V_{REFP}) and a NMOS (N_{SW}) to the negative reference (V_{REFN}), and likewise, to perform the mid-scale voltage are used two secondary switches – P_{SS} and N_{SS}.

Moreover, two dummy loads – DUM_P and DUM_N – are added to mitigate the unbalanced leakage current between P_{SW} and N_{SW}.

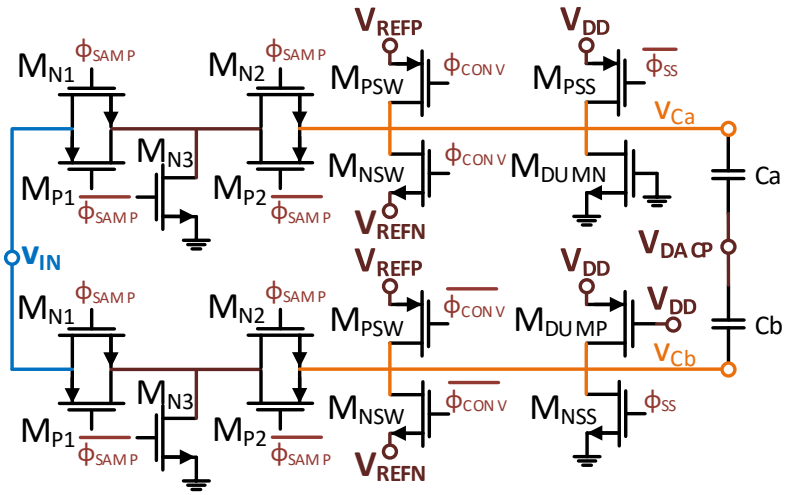

Figure 4-31 – Sampling DAC switches block for one bit-capacitor (split in C_a and C_b) from side V_{DACP} of the array.

In addition, as shown in Figure 4-27, every capacitor have their top plate connected to a shared node that is linked to other two switches, the comparator biasing switch (CM) and the one that short-circuits the comparator input (SC). Now, similarly as before, we illustrate in Figure 4-32 the Sampling DAC switches during sampling, focusing just one of the capacitors in that situation. Now, the operating transistors behave as resistors, namely the sampling (M_{N1}, M_{N2}) and biasing switches of the DAC, and the ones that are cut-OFF behave as current sources, namely the rest of the switches (M_{N3}, M_{PSW}, M_{NSW}, M_{DUMP}, M_{DUMN}, M_{PSS} and M_{NSS}), due to their continuous leakage current.

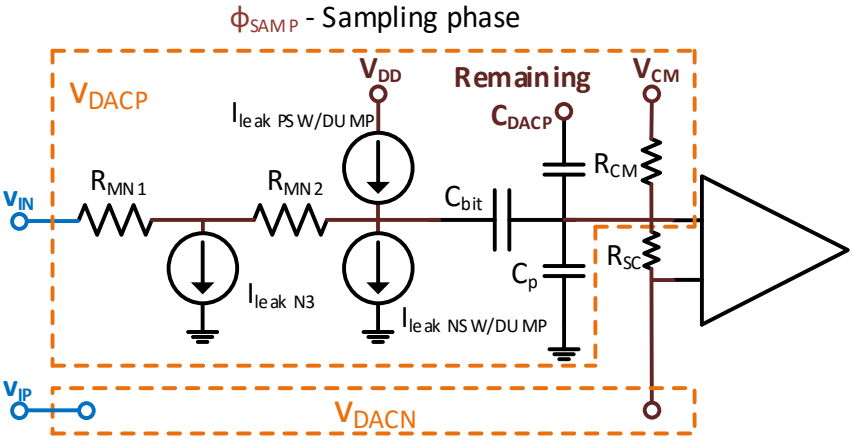

Figure 4-32 - Sampling DAC switches during sampling phase.

Likewise, we represent in Figure 4-33 the situation during the conversion phase, where, now, only the reference switches (M_{PSW}, M_{NSW}) behave as resistors and the rest as current sources. The M_{N3} will drain the leakage interference from the input signal and the M_{DUMP}/M_{DUMN} will try to counter-balance the leakage from the reference switch that is not selected.

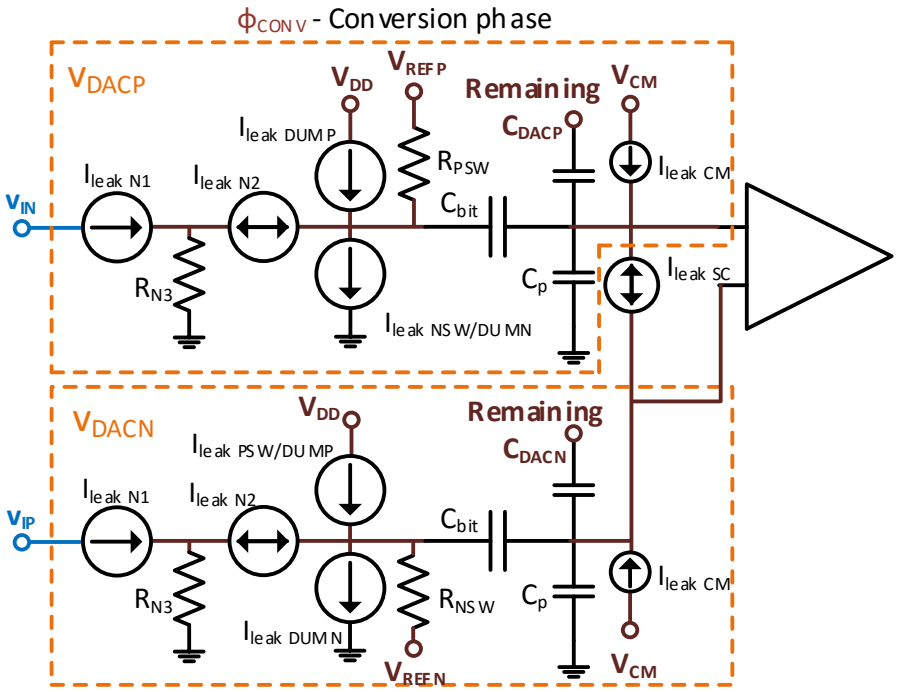

Figure 4-33 - Sampling DAC switches during conversion phase.

Presented the employed topology, let us remember the primary concern while sizing these switches, which regardless of its application, is to obtain a proper ON-resistance that must satisfy the settling time, for every corner. The case of the sampling and secondary switches is more relaxed than of the reference ones, because the last ones have a titter time window to settle the capacitors voltage to the proper reference voltage. In other words, the period that the capacitor bottom voltage takes from V_{REFN} to V_{REFP} (or vice-versa) has to be inferior than the time the comparator control signal – latch – is reset (low). Then, on the other hand, we need to reduce the leakage impact preferably with a big OFF-resistance. Although we designed the conversion switches by option B), the sampling switches required the option C), so, before continuing the switches restrictions, the CB will be explained first, in a simple and a thorough way. Nonetheless, even after testing those options above, both switches of biasing (R_{CM}) and short-circuit (R_{SC}) of the comparator will also continue to leak, thus, unbalancing the charge from the DAC branches. So to mitigate it the we use a mix of the option B) and C), where both their W and L sizes were increased (or adjusted) to have a big OFF-resistance, and to ensure a small ON-resistance (not degrading the sampling) they require a clock-boost.

4.4.2.2.1. Clock-boost

When we want a switch correctly turned ON, the transistor needs a small ON-resistance, if that is not the case then the voltage applied at its gate terminal has to increase. As seen in the section of the state of the art, [12], [13], [16], the solution is to apply clock-boosts (CBs), which in the case of a NMOS forces a higher v_{GS} to reduce its r_{DS}; specially helping when the sampling signal is great. In this project, the critical switches that require CBs at their gates are the ones used for sampling, namely M_{N1}, M_{N2} (that combined are R_S) and R_{VCM}, R_{SC}. Hence, these switches should have a v_{GS} around or superior to $80\%V_{DD}$, obtaining a good efficiency, seen as

$$Eff_{R_S} = {V_{GS\,[R_S]}}/{V_{DD}} \times 100. \tag{4.90}$$

Figure 4-34 illustrates the basic operation of a CB. At first, while the ADC is not sampling, the capacitor C_L is pre-charged at V_{DD} (ϕ_1), having the top plate-terminal (top) connected to V_{DD} and the bottom plate ($bott$) to GND. Then, when the sampling is activated (ϕ_2), the capacitor bottom plate is switched to the input sampling voltage. Thus, obeying the charge conservation principle, the top voltage is increased, making $v_{BST} \approx v_{DD} + v_{IN}$. Nevertheless, the performance of this circuit is dependent of its input signal and capacitive effects of the switches. In order to understand better its designing choices, we can state those dependencies through its charge distribution in both phases depicted in Figure 4-34.

$$Q^I_{top} + Q^I_{v_{BST}} = Q^{II}_{v_{BST}}, \tag{4.91}$$

$$\Leftrightarrow C_L V_{DD} - [C_{GS} v_{IN}(0) + C_3 v_{OUT}(0)] = (C_L + C_{GS} + C_{GD} + C_P) v_{BST} - (C_L + C_{GS}) v_{IN}(t) - C_{GD} v_{OUT}(t) \tag{4.92}$$

$$\text{Assuming} \begin{cases} v_{OUT}(t) = v_{IN}(t) \\ C_T = C_L + C_{GS} + C_{GD} + C_P \\ \beta = {C_L}/{C_T} \end{cases},$$

$$\Leftrightarrow v_{BST} = {C_L[V_{DD} - v_{IN}(t)] + C_{GS}[v_{IN}(t) - v_{IN}(0)] + C_{GD}\big(v_{OUT}(t) - v_{OUT}(0)\big)}/{C_T}$$

$$= {(C_L + C_{GS} + C_{GD}) v_{IN}(t) + C_L V_{DD} - [C_{GS} v_{IN}(0) + C_{GD} v_{OUT}(0)]}/{C_T} \tag{4.93}$$

$$= \beta V_{DD} - [C_{GS} v_{IN}(0) + C_{GD} v_{OUT}(0)] + v_{IN}(t)\left[1 - \frac{C_P}{C_T}\right]. \tag{4.94}$$

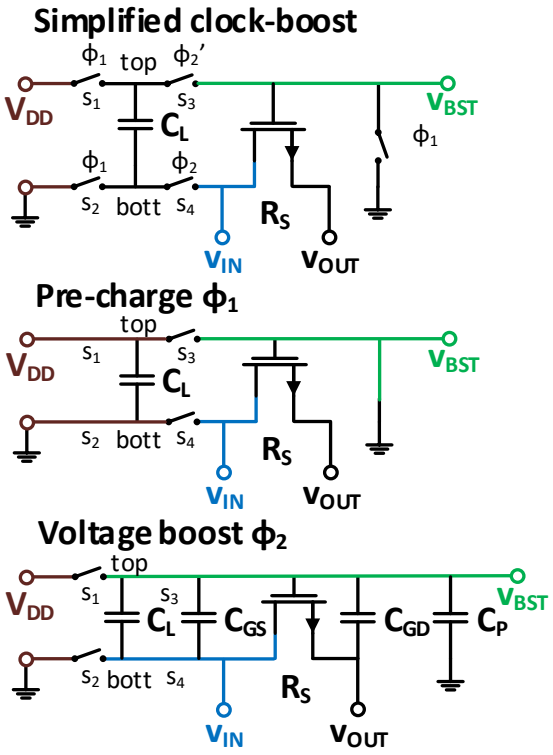

Figure 4-34 - Simplified clock-boost circuit applied to the sampling switch during its operating phases.

Now, observing the complete circuit in Figure 4-35, we can see that s_2 and s_4 are simply NMOS (M_{N3} and M_{N4}, respectively), s_3 is a PMOS (M_{P4}) and s_1 is made by two PMOS. One controlled by its clock signal (M_{P2}) and other by v_{BST} (M_{P3}), due to current leakage in the top plate node of C_L to V_{DD} supply. Plus, s_3 requires a particular gate signal (nx) to be generated by M_{N1}, depending on the clk, and M_{N2}, controlled by v_{BST}, which ensures that nx is v_{IN} even for values near V_{DD}.

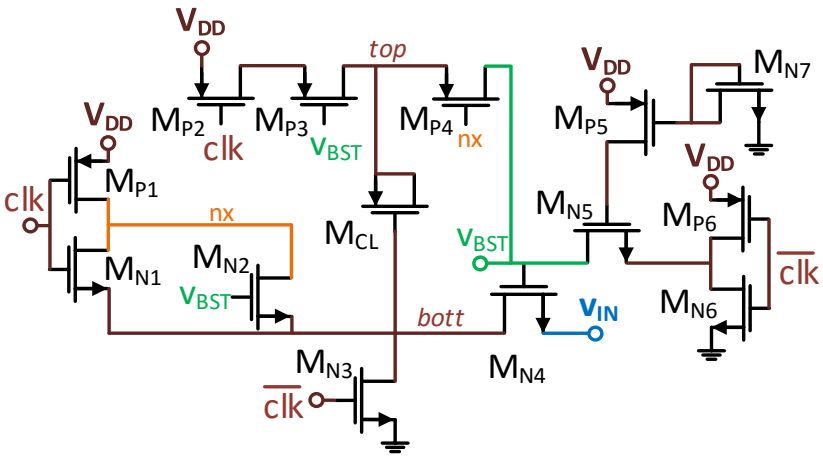

Figure 4-35 - Clock-boost circuit schematic.

During the pre-charge phase ($clk = 0$), M_{P2}, M_{P3} and M_{N3} are conducting, which sets V_{DD} at the top node and GND at the $bott$ node, thus charging C_L, while M_{P4}, M_{N4} are cut-off; since M_{P1} is driving nx to V_{DD} and M_{N5}, M_{P6} are driving v_{BST} to GND. Then, in the voltage-boost phase ($clk = 1$), M_{P2}, M_{P3} and M_{N3} are cut-off, while M_{P6} disables M_{N5} (nullifying its v_{GS}) and M_{N1} is driving nx to $bott$, which enables M_{P4}, increasing v_{BST} (with the top voltage). In turn, M_{N4} starts driving the $bott$ node with v_{IN}, which increases the top node voltage (at most to $2V_{DD}$, when $v_{IN} = V_{DD}$) and, likewise, rising v_{BST}. Note, as mentioned before, when v_{IN} gets near V_{DD}, it drives the V_{GS} of M_{N1} to cut-off, but even so M_{N2} is operational. Moreover, to avoid electrostatic discharges, M_{N7} is placed in diode configuration ensuring the M_{P5} is always conducting and M_{N5} has always V_{DD} at its gate.

In addition, the size of C_L is adjusted by simulation to provide a sufficient v_{BST}, however its value is also dependent of the capacitive input load placed by the switches that the CB is driving. That said, since the DAC sampling switches are oversized, due to leakage current, consequently, it demands a larger C_L to compensate that factor. Moreover, during the sizing of the sampling DAC switches, as the differential input signal was greater, the single-ended input signal between branches was further apart. It produced a greater the sampling error, because the resistive behavior of the sampling switches is different, since it varies with its v_{DS}. Therefore to mitigate difference of the resistances between branches, thus, the sampling error, the CB had to used at its maximum capability, by fixing its v_{IN} at V_{DD}.

4.4.2.2.2. Sampling restrictions

While storing the input signal, the bottom plate voltage of the sampling capacitors must converge to the input voltage within $t_{samp} = 200\ \text{ns}$ (from section 4.1), with the lowest possible error (ε_{samp}), or else the conversion will have a misleading sampled value. Theoretically, the worst-case for this scenario, as depict in Figure 4-36, happens when the previously sampled signal value is at the extreme of the

full-scale (of the input range) and, then, the new sample value is at the opposite extreme, i.e. $v_{IN} = \pm V_{FS}/4 = \pm V_{DD}/2$.

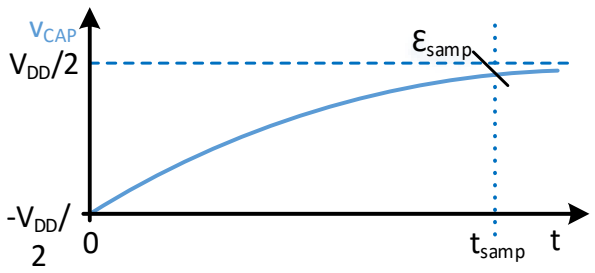

Figure 4-36- Theoretical worst sampling case.

Therefore, considering an RC circuit, the capacitors voltage (v_{CAP}) is given by

$$v_{CAP}(t) = -\frac{V_{FS}}{4} + \frac{V_{FS}}{2}\left(1 - e^{-t/\tau}\right), \tag{4.95}$$

and, when the sampling time finishes, we want v_{CAP} to settle with an error of a fourth of the quantization step $\left(\varepsilon_{samp} = \Delta/4 = 61\ \text{uV}\right)$, as

$$v_{CAP}\left(t_{samp}\right) = \frac{V_{FS}}{4} - \varepsilon_{samp}. \tag{4.96}$$

So, relating (4.95), (4.96) and $t_{samp} = 200\ \text{ns}$, we obtain the time constant, as

$$-\frac{V_{FS}}{4} + \frac{V_{FS}}{2}\left(1 - e^{-t_{samp}/\tau}\right) = \frac{V_{FS}}{4} - \frac{\Delta}{4} \Leftrightarrow \tau = 22.2\ \text{ns}, \tag{4.97}$$

in turn, we can obtain the total resistance value of sampling, for the slowest case, given by

$$\begin{cases} \tau = RC_s \Leftrightarrow R = 32\ \text{k}\Omega \\ R = R_S + R_{CM} \end{cases}. \tag{4.98}$$

Once the total resistance (R) attached to one branch of the sampling DAC comes from the combination of the internal resistances of the switches used for sampling (R_S) and for the comparator (common mode) biasing (R_{CM}), we have to arrange a tradeoff between them. Since all of these switches require a boosted phase at their gates and its r_{DS} is given by equation (4.90), we could determine a suggestive value for the W/L ratio. However, there are significant discrepancy of the CB efficiency between the resistance of both branches of the DAC, which are aggravated while simulating the PVT corners, as illustrated by Figure 4-37, Figure 4-38 and Figure 4-39, respectively the typical, the fastest (corner 7) and the slowest (corner 14) cases. Hence, these transistors size are adjusted by simulation to better fit the slowest case timeline and ensure the smallest ε_{samp} for every corner, as presented later in Table 10.

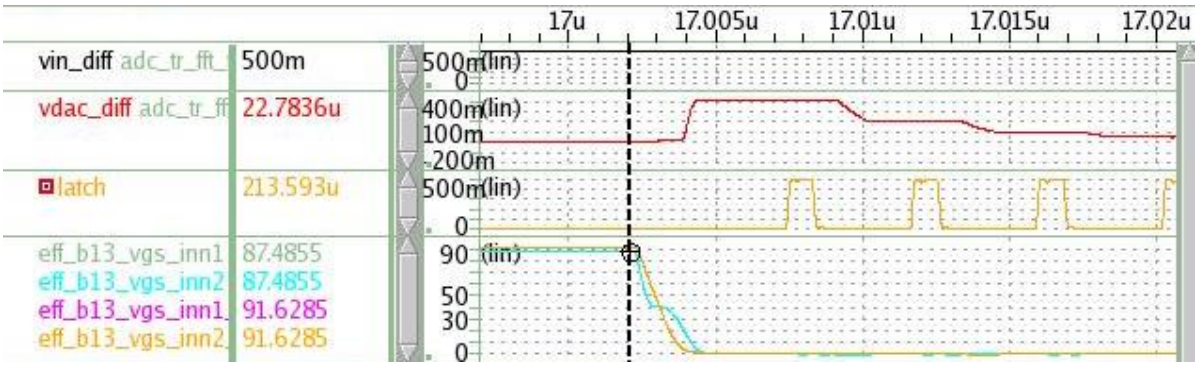

Figure 4-37 - Efficiency discrepancy between the sampling switches of both DAC branches in the typical corner.

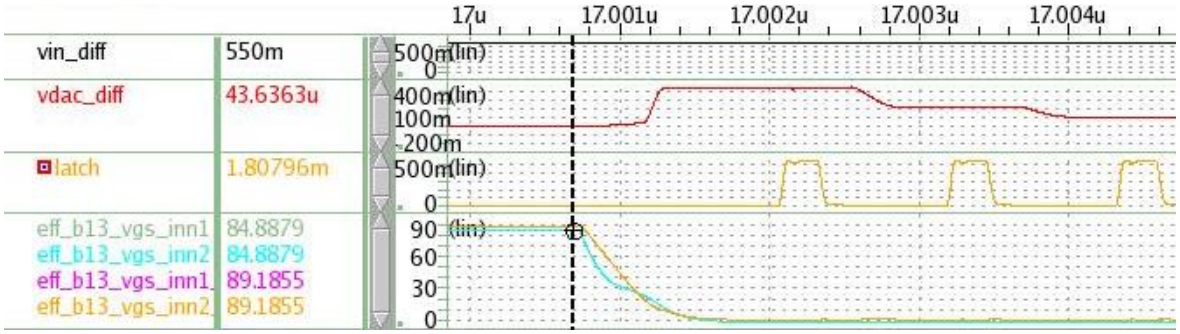

Figure 4-38 - Efficiency discrepancy between the sampling switches of both DAC branches in the fastest corner.

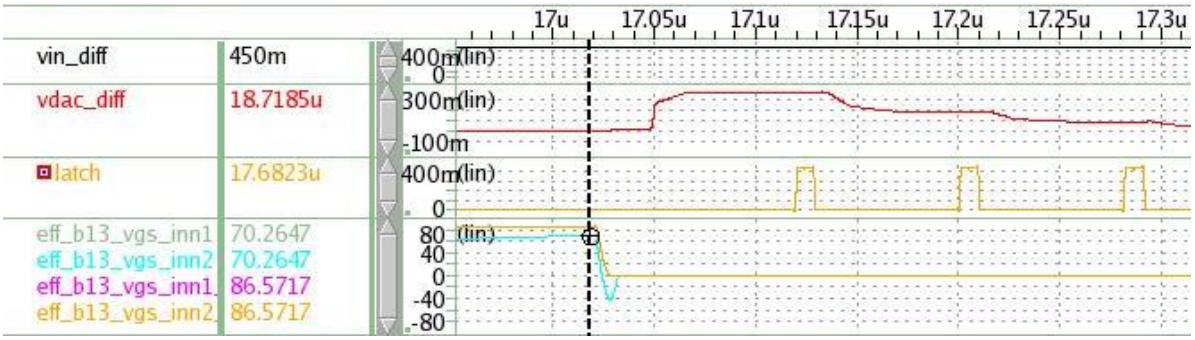

Figure 4-39 - Efficiency discrepancy between the sampling switches of both DAC branches in the slowest corner.

4.4.2.2.3. Conversion restrictions

Secondly, the conversion begins where after each bit decision of the comparator, the respective capacitor bottom voltage needs to stabilize to the desired reference voltage, within $t_{DAC} = 70\ \text{ns}$ (from section 4.1), if not it may lead to a wrong decision of the next bit. Therefore, the M_{PSW} and M_{NSW} ought to have a similar ON-resistance small enough to ensure a settling time ($t_{settling}$) inferior than t_{DAC}, thus similar rise and fall times for switching, in the typical corner. We must verify if these switching times do satisfy every corner, but, in a straightforward view, the ones that would require a particular attention would be the corner 10 (FS– where the NMOS are slower than PMOS) for the M_{NSW}, and, likewise, the corner 14 (SF) for M_{PSW}. However, this dimensioning is not straightforward because they affect the entire operation of the converter, since their mutually dependent of the t_{DAC}, which, produced by a custom delay cell (explained in the next section), is responsible for the synchronous clock (CLK_{state}) signal of

the state machine. So, after first adjusting the delay cell that originates the CLK_{state} that provides the stipulated t_{DAC} for the slowest corner, we can finally adjust these switches by simulation.

Whether it is important that the voltage of the capacitors settle before triggering the comparator, what is crucial is that its result ensures that v_{DAC} settles to a supposed value with a minimal error. Hence, instead of looking at the bottom plate voltage of every capacitor and using the one that required more time to settle, in every corner, we can make the sizing just by looking at v_{DAC}. Nonetheless, there is always a voltage drop in the reference switch that generates an associated error (ε_{ref}), that directly causes a gain error in the DAC transfer function. This way, since an offset error in v_{DAC} is also caused by the combination of the ε_{samp} and ε_{ref}, it also facilitates the determination of their impact.

Knowing that before the first MSB decision occurs, the DAC capacitors are put at mid-scale voltage ($V_{DD}/2$), the v_{DAC} will always evolve from zero, which makes easier the comparator take a right decision. This way, the M_{PSS} and M_{NSS} have a more relaxed settling time than the reference ones, thus, they do not require such a small ON-resistance, meaning they can have smaller dimensions. Therefore, the critical case to size M_{PSW} and M_{NSW} happens, before the second MSB decision takes place, when the first MSB (or the 13th bit) capacitor is settling to the selected reference voltage. Thus, an easy way to see the offset error produced in v_{DAC} is to sample a value that should result in $v_{DAC} = 0$, as exemplified in Figure 4-40. If we sample a fourth scale input voltage ($V_{DD}/2$), after the 13th bit comparator decision, v_{DAC} should transit from its maximum value (ΔV_0) cross zero and stabilize to ε_{13}.

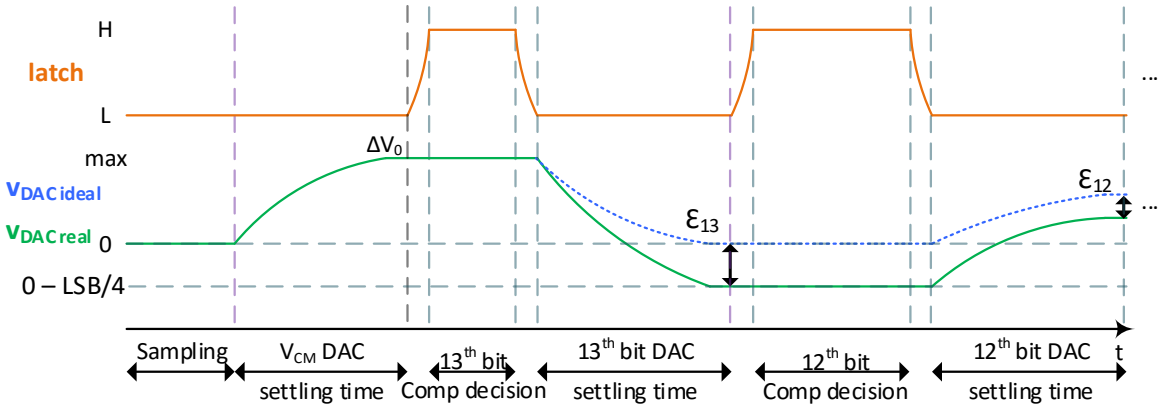

Figure 4-40 - Offset error of the differential DAC output voltage having a fourth scale input voltage.

Note that given a binary scaling of the capacitive array, the offset error will also scale regarding each bit (e.g. $\varepsilon_{13} = 2\varepsilon_{12}$), hence if we ensure that the greater contribution of the offset error is small enough, then the overall error in v_{DAC} (ε_{DAC}) would be insignificant to the produced digital word. Thus, if we stipulate $\varepsilon_{13} \approx \Delta/4$, the ε_{DAC} should be inferior to Δ. Then, reminding that when half of the 13th bit capacitor is (dis)charged is, in fact, the result of C_a or C_b ranging from zero to V_{DD}, in each DAC branch (indexed by concatenating P or N), the Figure 4-41, Figure 4-42 and Figure 4-43 illustrate, respectively, this worst case scenario for the typical, fastest (7) and slowest (14) corners. In these figures, we can also see the discrepancy between a reference switch ON/OFF-resistance as well as its associated ε_{ref}.

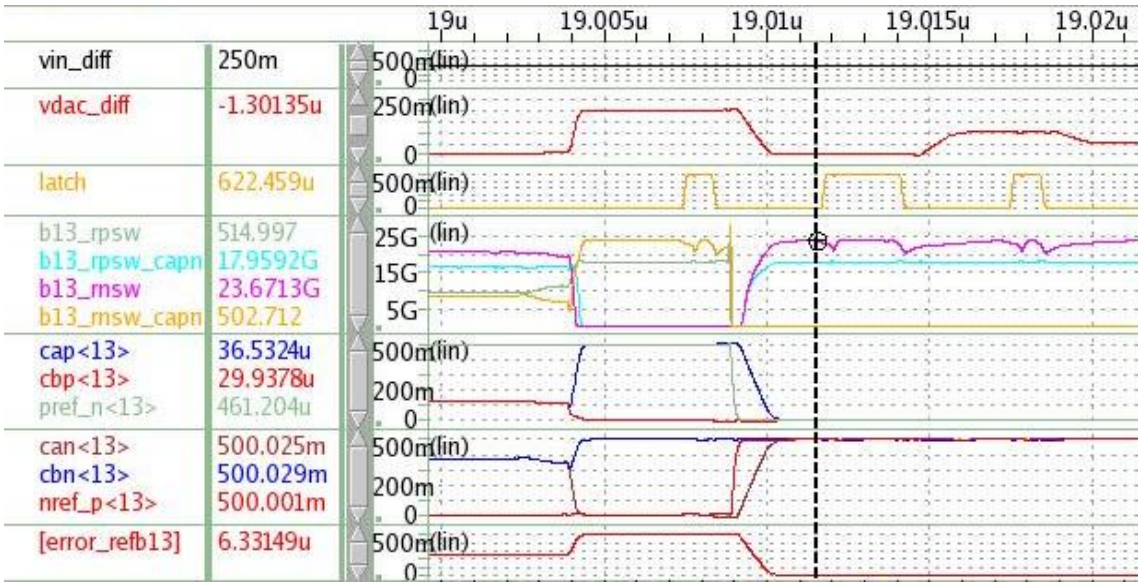

Figure 4-41 – Settling of the bottom plate voltage of the 13th bit capacitors, in the typical corner.

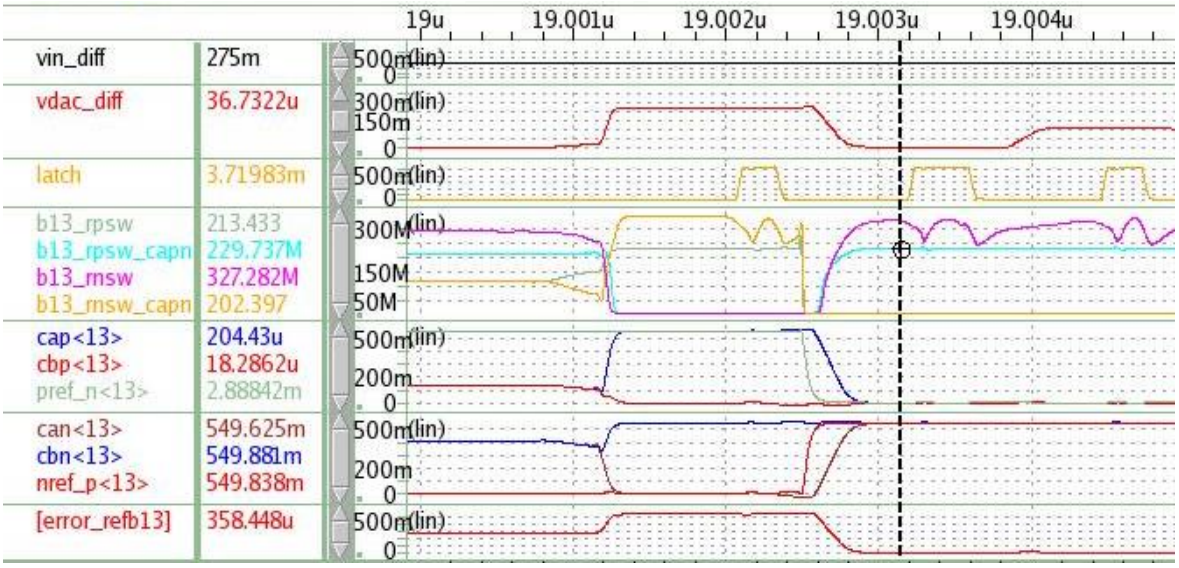

Figure 4-42 – Settling of the bottom plate voltage of the 13th bit capacitors, in the fastest corner.

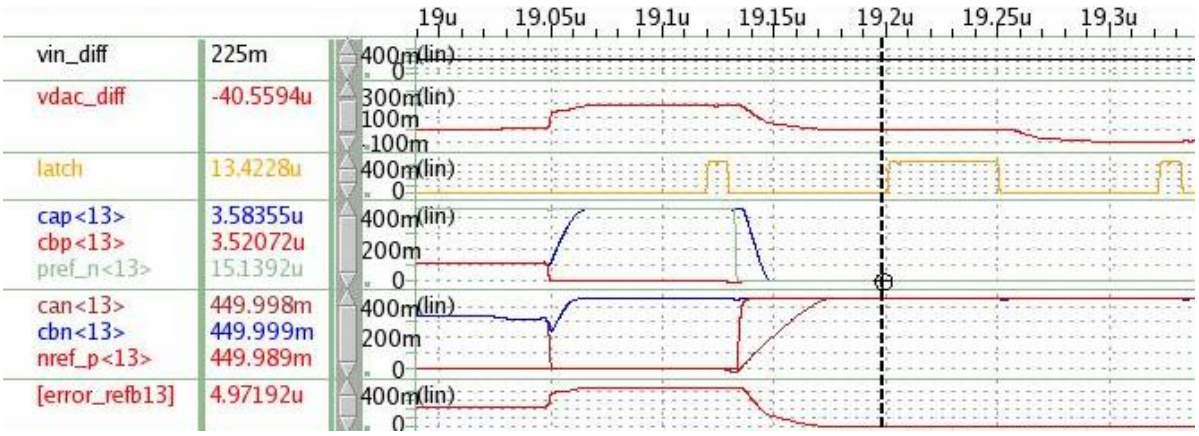

Figure 4-43 - Settling of the bottom plate voltage of the 13th bit capacitors, in the slowest corner.

In conclusion, the DAC switches are scaled by their number of fingers (based on the same unit W/L ratio), starting the MSB block with 32 fingers (as presented in Table 10) and decreasing the following blocks by half until 1 finger (respectively bit 8), maintaining this size for the rest of the inferior capacitors. Note that since the capacitors are split in two, the mentioned switches attached to their bottom plate have to be duplicated.

Table 10 - DAC switches block for the MSB capacitor,
plus the shared switches for biasing and short-circuit the comparator.

Main transistors dimensions for MSB Capacitor						
Used for	**Transistor**	**W [µm]**	**Fingers**	**Wtotal [µm]**	**L [nm]**	**Ratio W/L**
Sampling	N_1	0.25	32	8	30	266.7
	N_2				80	100.0
	N_3		1	0.25	30	8.3
	P_1		32	8		266.7
	P_2				40	200.0
Sampling and calibration	SC	2	1	2	200	10
	CM	0.5	3	1.5	180	8.3
Conversion	P_{SW}	0.5	32	16	160	100.0
	DUM_P					
	N_{SW}	0.48		15.36	180	85.3
	DUM_N					
	P_{SS}	0.25		8	80	100.0
	P_{SS}				120	66.7

4.4.2.3. DAC mimic delay cell

Instead of using just a chain of inverters (NOT logic gates) to create a delay cell, a more efficient and dynamic way is to create a cell that replicates, in a simplified model, the number of gates or switchings of the circuitry we are dimensioning. In this case, we adapted the cell from paper [28] to provide the necessary settling time for the DAC capacitors (to switch properly) is given, as presented in Figure 4-44 and whose operational signals behave as illustrated in Figure 4-45.

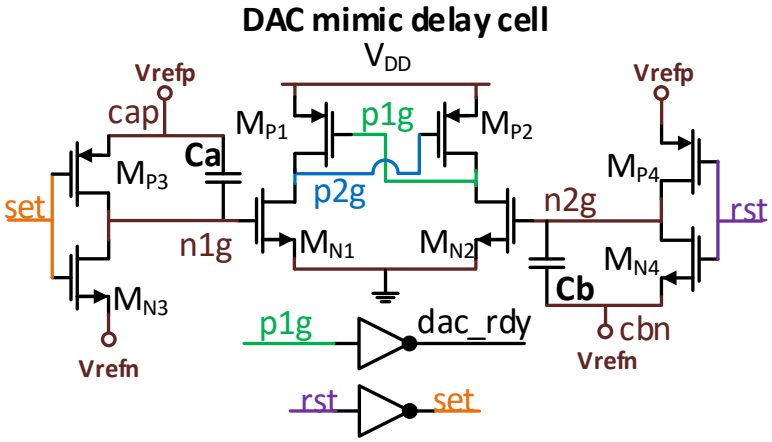

Figure 4-44 - Delay cell that mimics the DAC switchings.

At first, the interior switches of the latch (M_{P1}/M_{N1} and M_{P2}/M_{N2}) are sized with the minimal dimensions of the technology and, then, adjusted by simulation, so that the PMOS have more strength than the NMOS, ensuring that the output signal (dac_rdy) does toggle when enabled. Secondly, the capacitors (C_a/C_b) and switches (M_{P3}/M_{N3} and M_{P4}/M_{N4}) that (dis)charge to replicate the DAC switches, are sized with the same dimensions as the LSB DAC switches to provide a similar time constant. Then, those capacitors are manipulated by simulation until the required t_{DAC} is performed. The signals of reset (rst) and dac_rdy are defined to be set at a high level.

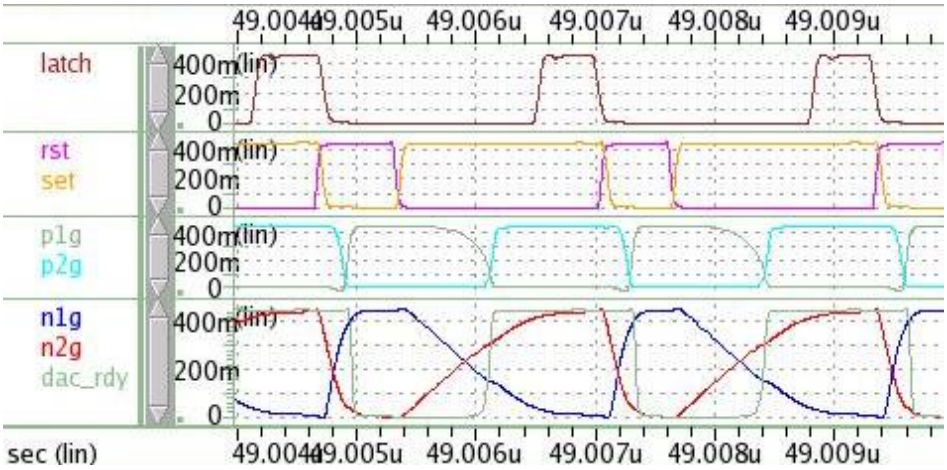

Figure 4-45 – The operational signals behavior from the DAC mimic delay cell.

Observing the operational signals of this delay cell along the converter CLK_{state} in Figure 4-45, the cell is disabled, when rst is high (set is low), both C_a and C_b are short-circuited (M_{P3} and M_{N4} are ON) making the node $n1g$ go high and $n2g$ to low, which respectively make the nodes $p2g$ to go low and $p1g$ to go high, thus setting the signal dac_rdy to low. Then, cell is enabled, when rst is low (set is high), C_a starts to discharge, slowly decreasing $n1g$ and, likewise, C_b starts to charge (M_{N3} and M_{P4} are ON), slowly increasing $n2g$, which respectively pulls down the nodes $p1g$, thus, making $p2g$ to go high, finalizing with dac_rdy to high.

In addition, another option is created to increase the delay produced (intended to be triggered in the offset calibration state) by enabling the signal $extrac$, which aggregates an extra capacitance (C_{aex}/C_{bex}), with the triple of the previous size (plus switches with same size), as illustrated in Figure 4-46. In turn, if the signal $extrac$ was set to high, then C_a would be combined with C_{aex} and C_b with C_{bex}, originating a slower phase of charge and discharge of those capacitances.

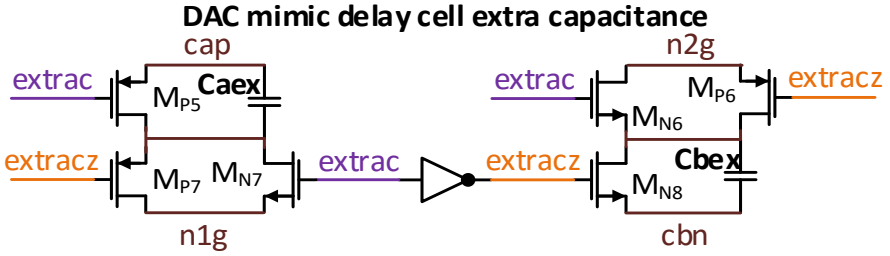

Figure 4-46 – Extra capacitance to enable a longer option of the DAC mimic delay cell.

4.5. Delay block - State Machine

This converter requires a state machine as a core block to coordinate every other, ensuring that a continuous sample and conversion is done, while storing the resultant bits. For that to happen, as illustrated in Figure 4-47, when the initial conditions are set and the ADC reset bit is low, it starts sampling at the negative edge of the (synchronous) external clock (CLK_{ext}). In turn, at the positive edge (of CLK_{ext}), it starts the sequential conversion of each bit through an asynchronous internal clock (CLK_{state}). Consequently, finishing the conversion, if the reset is still disabled, it will repeat the process, resuming the sampling within the available time and so on.

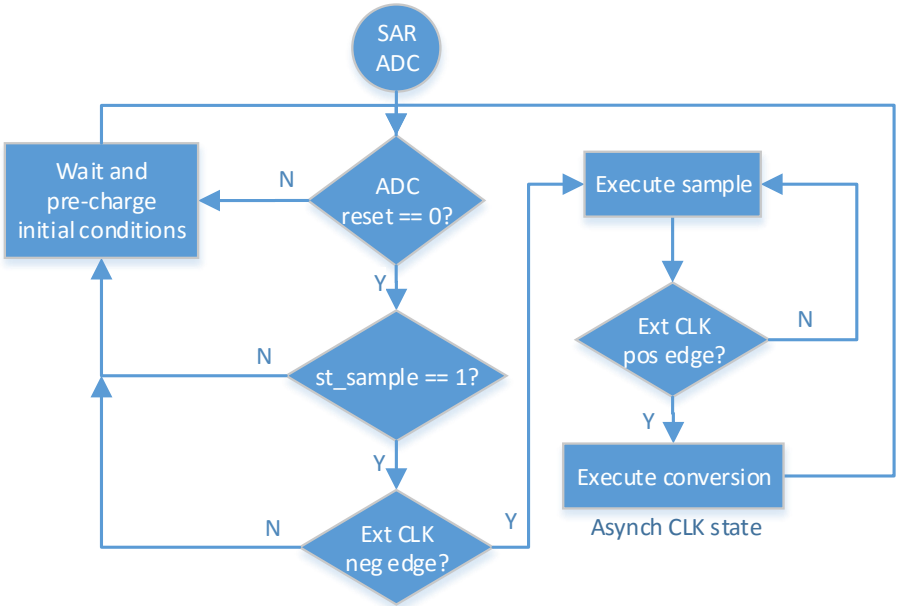

Figure 4-47 - General SAR ADC flowchart.

After every sample state, as depicted in Figure 4-48, there is a sequence of states for conversion, making a total of 17 states per period. While the sampling is performed during st_sample, the conversion is composed by states st_13 to st_0, correspondent to each decision bit (by the comparator), followed by st_vos used for the calibration of the comparator voltage offset, and st_reset, to grant the same starting point for sampling capacitors, that ends the conversion and the cycle repeats. Note that, although the signals latch and CLK_{state} are similar, the first is used just to (dis)enable the comparator, whereas the second is responsible to initiate the conversion, controlling the registers and, thus, begin the sequential states. Alongside with these signals, both SC and CM switches require a special phase of control (ph_sc), because both are used during st_sample and, also, during st_vos. Independently of the calibration topology, to acquire an estimate of the voltage offset produced by the comparator, we need to replicate the situation (during st_vos) as if we sampled zero ($v_{DAC} = 0$) at its input and take a decision (thus, obtaining the direct voltage offset). Hence, only after taking several samples (e.g. at least 100) can we extrapolate an estimate that mitigates this voltage error. Moreover, since the value of v_{DAC} of the last conversion varies with v_{IN} and the switches behave differently between corners, this st_vos requires a particular longer settling time (thus, a longer t_{DAC}), which is given by enabling the longer option of DAC mimic delay cell (also depicted in in Figure 4-49).

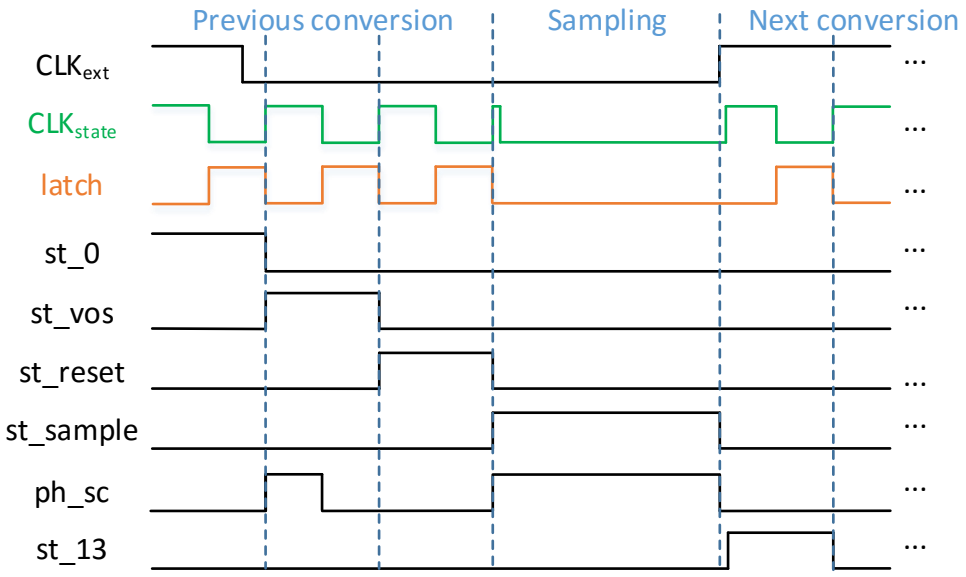

Figure 4-48 - ADC sequence example of sampling and conversion states for a slow conversion case.

In order to create these signals, the delay block contains the simplified sequential logic circuit shown in Figure 4-49, where (at the top) we can see the circuit that generates the start $pulse$ of the CLK_{state}, at every positive edge of the CLK_{ext}, as a result of delaying the CLK_{ext} and chopping it. While sampling ($st\_sample = 1$), when the $pulse$ is high, CLK_{state} is pulled down and $\overline{latch}$ is pulled up, then when the sampling is over ($st\_sample = 0$), when the $pulse$ is high, the CLK_{state} is pulled up. Consequently, it toggles st_13 to high and, having the other states low (i.e. $\overline{st\_reset} = \overline{cmp_{rdy}} = 1$), also activates the DAC mimic delay cell (at the bottom), which will create the signal $next$ that toggles $\overline{latch}$ to low, begging the first bit decision, and it also feedbacks CLK_{state} (maintaining it low).

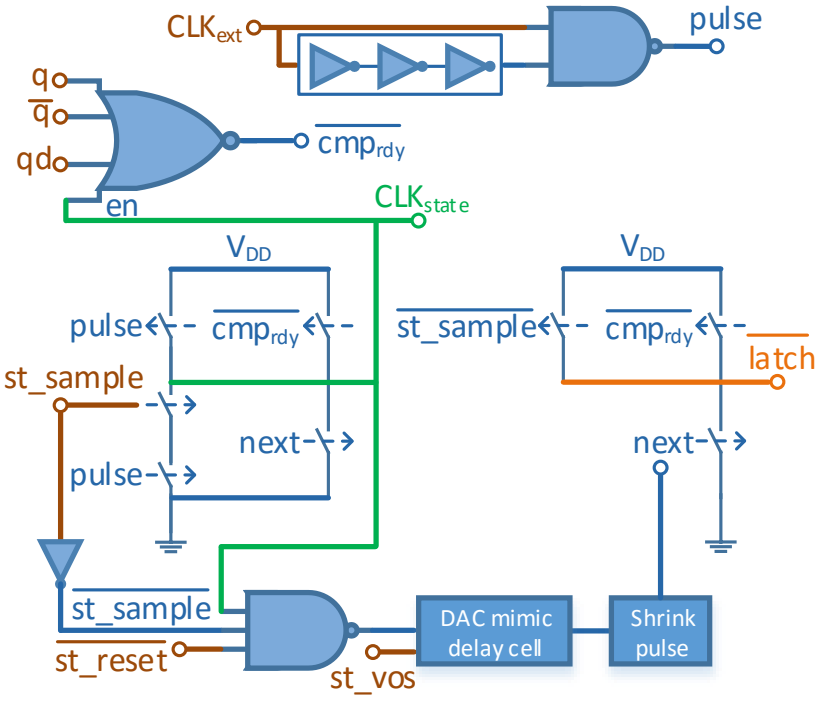

Figure 4-49 - Delay block logic circuit representation.

When the comparator decides (e.g. $q = 1$), $\overline{cmp_{rdy}}$ goes low which pulls both CLK_{state} and $\overline{latch}$ back up, hence st_13 goes low, st_12 to high and another $next$ is generated, repeating the process until the last state ($\overline{st\_reset} = 0$). Finalizing st_reset generates a quick decision ($qd = 1$) of the comparator which toggles $\overline{cmp_{rdy}}$ and resets both CLK_{state} and $\overline{latch}$ back up. Then, in the following sample (meaning another start $pulse = 1$ plus $st_{sample} = 1$), the CLK_{state} goes low and the cycle repeats itself.

In turn, to create the conversion states, the SAR mechanism is employed through a chain of registers (flip-flops D) in serie, known as ring counter like in Figure 4-50, controlled by CLK_{state}, while each converted bit is stored in a secondary set of similar registers. These registers have at the input the previous state, this way (while $reset = 0$) at each rising edge a logical 1 travels between them, unlocking the succeeding register state, and so on. Note that, while the ADC reset is ON ($reset = 1$), every register output is put at low, expect the register for st_sample that is put at high. Hence, at an initial condition, when the ADC is activated ($reset = 0$), the st_sample is high (enabling the sampling), and, consequently, at the next rising edge of CLK_{ext} (begins the conversion), CLK_{state} is actived setting the st_13 to 1 (while st_sample goes to 0), repeating the process till st_reset and back to st_sample.

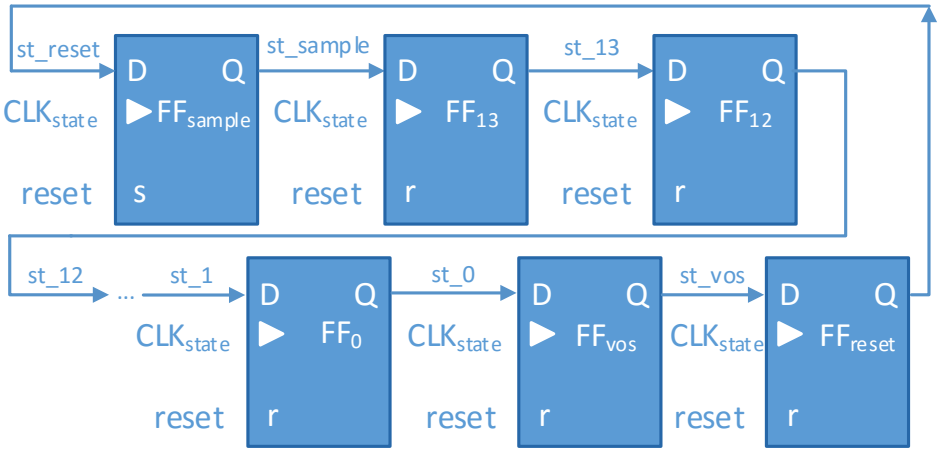

Figure 4-50 - Ring counter for ADC state machine.

Moreover, each one of the secondary set of registers, used for storing the (output) decision bit (that make the input word of the DAC), is designed as presented in Figure 4-51, which receives at the input the respective state (st_N) and resultant comparator output (q) that will produce the stored bit (b_N).

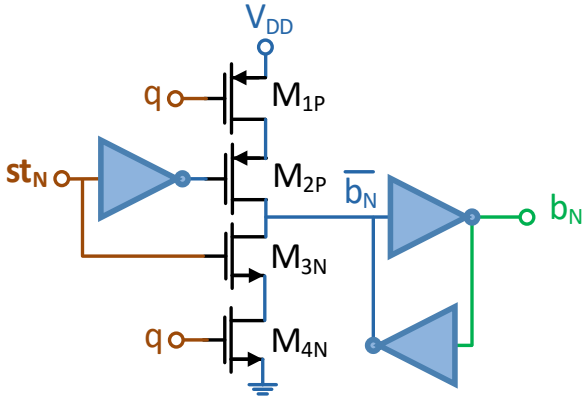

Figure 4-51 - Circuit of 1 bit register.

Remember that at reset state, both comparator outputs are at high, so when the st_N goes up, both M_{3N} and M_{4N} are conducting which pulls $\overline{b_N}$ down and, thus, b_N stays high. If the comparator decides a zero ($q = 0$), then (M_{4N} is cut-off) both M_{1P} and M_{2P} shall pull $\overline{b_N}$ up and, thus, put b_N to low. Again, if the comparator decides one, the signals would invert setting back b_N to high, as in the reset state, though note that the register are only sensitive to q as long as st_N is at high, this way none of the other registers are affected. In addition, the auxiliary inverter (at bottom of $\overline{b_N}$) is employed just to be safe that, even in presence of leakage current, the value of b_N is maintained, and, after each rising edge of CLK_{ext} every bit is delivered (as a digital word) to the ADC output.

4.6. ADC calibrations

In a SAR topology, we can state that non-linear errors only have origin in the sampling DAC block. Evidently, a poorly sampled signal will always have direct consequences on the final digital word, but the converters designer can control that situation. However, after the industrial manufacture, the basic circuit elements never have exactly the same size as their identical pair; causing mismatches in both capacitors and switches. This leads to variations of the capacitance value of the DAC capacitors (called random capacitor mismatches), which affects the linearity of the DAC (staircase) transfer function. On the other hand, it makes identical transistors to have different driving currents that placed in a differential input cause a differential offset voltage. An example of that happens when the comparator block inserts an offset error in its input, shifting the comparator referential zero of decision. which result in wrong bit decisions. The same might happen, when the DAC capacitor settle to a wrong reference voltage, what inserts a gain error in the DAC transfer function. Therefore, these effects have to be accounted.

As mentioned in section 2.1 and through [27], the static non-idealities of linear circuits are decomposed in offset, gain errors and non-linear errors, so ADCs are inherently non-linear, but they can be modeled as a linear system, by highlighting the sources of those errors in the circuit. Thus, the Figure 4-52 pinpoints the gain errors (G_{Esh}, G_{Edac}) in the ADC, which estimated through a digital calibration (of the sampling DAC) can fix the output digital word (i.e. the ADC transfer function, regardless of the DAC).

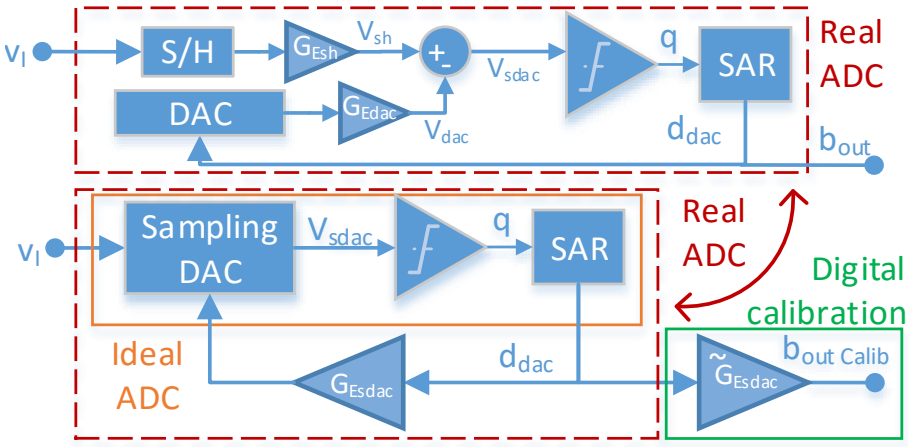

Figure 4-52 - SAR ADC with digital calibration of gain error and non-linearity of the sampling DAC.

Likewise, the Figure 4-53 pinpoints the offset error in the ADC, which can be referred just as one source at the ADC inputs, however, since the sampling DAC is treated with a digital calibration, the real impact of this error falls upon the comparator decision, hence the ADC only requires an offset voltage calibration for the comparator. Once the two situations were stated in those figures, in the following sections we will describe the suggested solutions.

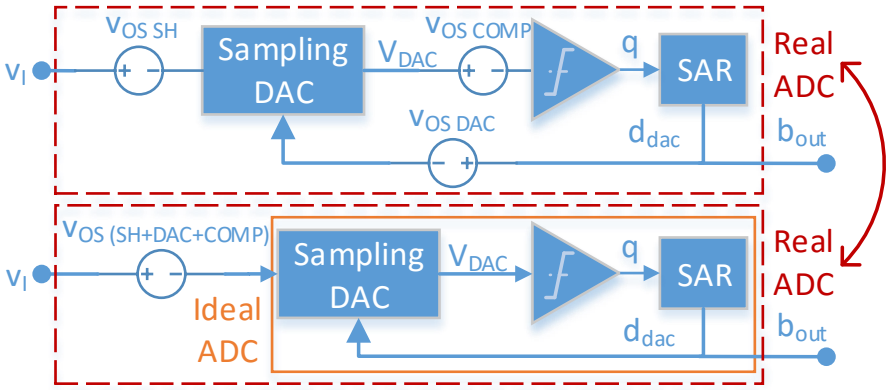

Figure 4-53 - SAR ADC with offset voltages effect.

4.6.1. DAC digital calibration

Typically, the DAC digital calibration is mainly employed to address random capacitor mismatches and the sensitivity of its topology to parasitics (in the capacitive divider nodes), but it also allows to fix the distortion in the ADC transfer function caused by redundancy. Although this proposed solution was not implemented, the main idea will be described. At startup, the relative capacitor weights are measured and, then, during conversion, the raw digital code (d_{DAC}) provided by the SAR block is calculated ($b_{out\ calib}$). This way, the capacitors can be sized based only on the noise constraint, without extra complexity, since the calibration is a post-processing step, which also maximizes the operating speed [27].

At first, we assume C_2 as C_{unit} (presented in **Error! Reference source not found.** as $2^0 C_{unit}$) and that all capacitors in the LSB group are well matched. Then, all the other capacitors (ISB and MSB group, leaving out the LSB) are measured regarding the C_{unit}, obtaining the relative capacitor weights as coefficients

$$k_n = d_n \times C_2\,, \tag{4.99}$$

that relate the contribution of every capacitor in the DAC array. Secondly, all those coefficient are normalized in relation to the MSB capacitor (C_{12}), since it has half the weight of C_{DAC} ($2^{11} C_{unit}$), in order to have a normalized coefficient of $\varphi_{12} = 2048$. Therefore, using the digital word correspondent to C_{12} (d_{12}), the normalized coefficients for every measured capacitors can be expressed as

$$\varphi_n = \frac{k_{12}}{d_{12}} d_n, \tag{4.100}$$

Now, let us justify analytically this calibration solution considering Figure 4-52, so assuming an input signal (v_I) that varies between $-V_{REF}$ and $+V_{REF}$, the digital output of an N-bit ADC, which ranges from -2^N to $+2^{N-1}$, is ideally given by

$$b_{out} = \frac{2^N}{2V_{REF}} v_I + \varepsilon_q = \frac{v_I}{\Delta} + \varepsilon_q, \tag{4.101}$$

where ε_q is the quantization error (which varies from 0 to 1). Then, simplifying the expression (4.64) of the sampling DAC output, assuming only the DAC non-linearity present ($G_{Esh} \approx 0$, $G_{Esdac} = G_{Edac}$), meaning that G_{Esdac} is only dependent of d_{dac}, without being affected by v_I, yields

$$\begin{cases} v_{sdac} = v_I - G_{Esdac}(\Delta \times d_{dac}) + \varepsilon_v \\ \varepsilon_v = G_{Esdac}(\Delta \times \varepsilon_q) \end{cases}, \tag{4.102}$$

where ε_v is the small voltage error originated from quantization. In turn, knowing that, in the end of the conversion, $v_{SDAC} = 0$, we can substitute (4.102) and express the DAC input as

$$d_{dac} = \frac{v_I}{G_{Esdac}\Delta} + \varepsilon_q. \tag{4.103}$$

Comparing the equations (4.101) and (4.103), it is like the ADC is converting another signal, thus, if the digital calibration estimates correctly the G_{Esdac} as $\tilde{G}_{Esdac}$, then the ADC output is fixed as

$$b_{out\ calib} = \tilde{G}_{Esdac} \times d_{dac} = \frac{v_I}{\Delta} + \tilde{G}_{Esdac} \times \varepsilon_q, \tag{4.104}$$

which becomes near the ideal output, even though it affects ε_q its contribution is so small that it is not problematic.

4.6.2. Comparator offset voltage calibration

As mentioned before, this sort of offset error in the comparator input can have origin in transistors mismatch but it also can be due to voltage discrepancies on the input routing of the ADC, meaning that the connections between the external input signal and the sampling DAC input might suffer from parasitic resistance. Unfortunately, the second origin would be signal dependent because the single-ended parasitic resistance would degrade differently the input routing as the signal changes, so this case need some special conditioning that was not approached in this work. On the other hand, the first origin causes a constant voltage error (in each corner case), which can be nullified through a complementary internal voltage.

An option to mitigate this error could be done by employing a pre-amplifying stage, however it involves a static consumption and does not reduce the contributions from the mismatch of charges injected by the switches commutations of the preceding block [27]. The transistors mismatch of the comparator input (differential pair) would reduce if we used larger dimensions, however it would be at the expense of more area and current consumption. Once none of those options are satisfactory, the reduction of the differential voltage of the comparator input (v_d) should be done through an iterative mechanism, which searches an estimation voltage that nullifies the error. So, the proposed solution

intends to replicate the differential pair by employing an auxiliary differential pair, whose purpose is to generate an input voltage (v_{Cal}) that approaches v_d, after n decisions of n samples (e.g. $n = 100$).

The idea of this solution is explained by [22] [27] through the model of Figure 4-54 that represents the comparator during the st_vos, in three blocks. Both differential pairs are represented by their transconductance, being gm_1 the main and gm_2 the auxiliary, and the result of their current output (respectively i_1 and i_2) is transformed (by R_0) in v_x. Then, the back to back inverters, being the third block, compares the result of $v_x - V_{OS3}$ with zero. Note that every block as its own offset voltage source (respectively V_{OS1}, V_{OS2} and V_{OS3}) at its input, but V_{OS3} represents the actual threshold voltage of the comparator decision (i.e. the offset that places the referential zero that we intend to nullify). Then, the output of the comparator goes to a control logic block that continuously selects if the calibration voltage (v_{cal} stored in C_L) should be increased or decreased, performing this way a discrete time feedback logic.

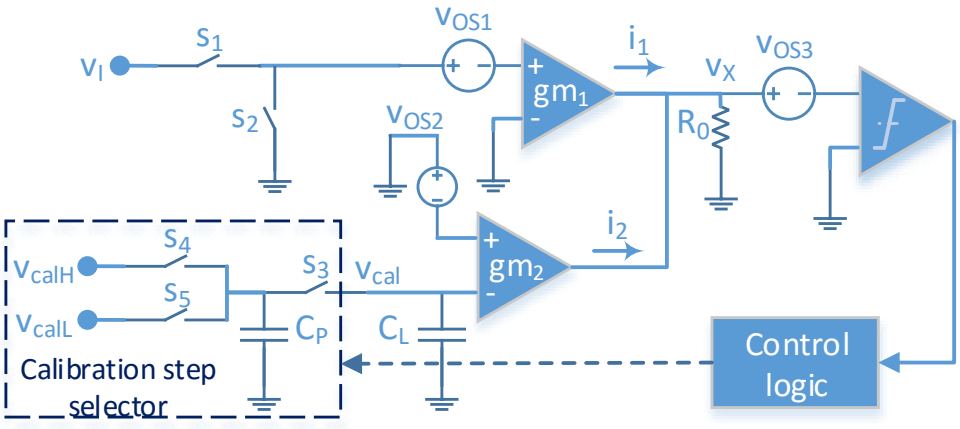

Figure 4-54 - Single ended model for the proposed method of offset voltage cancelation.

During a normal conversion operation, s_1 is closed (s_2 is opened) placing the single ended DAC output signal (v_I) at the input of the comparator, while the auxiliary amplifier is ignored ($i_2 = 0$). In the first conversion, during the st_vos, the s_1 is opened and s_2 is closed (i.e. the comparator input is short-circuited), it generates

$$v_x = -gm_1 R_0 V_{OS1}, \tag{4.105}$$

which, in turn, if $v_x - V_{OS3} > 0$ the comparator shall decide high or low otherwise. Next, accordingly to the decision bit, the control logic unit will increase or decrease v_{cal} by selecting (closing) s_4 or s_5 that pre-charges C_p (that is the node parasitic capacitor) respectively to V_{calH} or V_{calL}. After that pre-charge, s_4 and s_5 open and, in a following state, the s_3 will close and transfer the charge of C_p to C_L. Note that the $C_L \gg C_p$, thus the calibration step will be small.

So, for instance, when the comparator decides high, s_4 is selected (C_p is charged with V_{calH}) to increase v_{cal}, which consequently reduces v_x towards V_{OS3}. In order to estimate V_{OS3}, the process will repeat (after several n times), adjusting v_{cal} until is optimal point (v_{calopt}), which occurs when V_{OS2} compensates V_{OS1}. After this, the v_{cal} will continue to change around the v_{calopt}, since the comparator will be alternatively deciding high or low.

The estimated voltage (v_{cal}) is defined by the voltage at C_L that is adjusted through successive increments or decrements, whose single ended expression (by circuit analysis) is given by

$$\begin{cases} v_{calP}[n] \ = v_{calP}[n-1] + (V_{calH} - v_{calP}[n-1])\left(\dfrac{C_P}{C_P + C_L}\right) \\ v_{calN}[n] \ = v_{calN}[n-1] + (V_{calL} - v_{calN}[n-1])\left(\dfrac{C_P}{C_P + C_L}\right) \end{cases}. \tag{4.106}$$

The maximum range for v_{cal} is reached, when its single ended voltages reach their limit values,

$$max\left[v_{cal}[n]\right] = \begin{cases} max\left[v_{calP}[n]\right] \ = V_{calH} \\ max\left[v_{calN}[n]\right] \ = V_{calL} \end{cases}. \tag{4.107}$$

In turn, equalizing the single-ended equations through the initial condition we can obtain the initial calibration step, valid within its limits, as

$$\begin{aligned} \Delta V_{cal\ initial} &= (V_{calH} - v_{cal}[0])(C_P/C_P + C_L) \\ &= (V_{calL} - v_{cal}[0])(C_P/C_P + C_L). \end{aligned} \tag{4.108}$$

When the limits are reached, the calibration steps are not equal, as their expressions would be

$$\begin{cases} \Delta V_{calP} \ = (V_{calH} - V_{calH})(C_P/C_P + C_L) \\ \Delta V_{calN} \ = (V_{calL} - V_{calH})(C_P/C_P + C_L) \end{cases}. \tag{4.109}$$

hence, while ΔV_{calP} would be zero, ΔV_{calN} would be twice larger. In the worst case scenario the calibration voltage step is

$$\Delta V_{calP,N} = \frac{C_P}{C_P + C_L}(V_{calH} - V_{calL}). \tag{4.110}$$

However the presented model is a single-ended model, our circuit treats a differential voltage ($v_{cal\ diff} = v_{calP} - v_{calN}$), so the $\Delta V_{cal\ diff}$ is twice than $\Delta V_{calP,N}$. Nonetheless, the maximum offset voltage that can be mitigated by this method is given by the relation of transconductances of the differential pairs and the larger reference calibration voltage, seen as

$$V_{OSmax} = \pm\frac{g_{m2}}{g_{m1}}(V_{calH} - V_{calL}). \tag{4.111}$$

Although, increasing $V_{calH} - V_{calL}$ would increase the range, it would also increase the calibration step and, thus, it would be less precise. Therefore, a good approach would be to fixate $V_{calH} - V_{calL}$. On the other hand, the residual voltage originated by it (meaning the smallest offset voltage that it can achieve) is determined as

$$V_{OSres} = \pm 2\frac{g_{m2}}{g_{m1}}\frac{C_P}{C_P + C_L}(V_{calH} - V_{calL}). \tag{4.112}$$

In order to size this circuit and verify that the cancelation method is functional, we need a representative offset voltage, for that we do a Monte Carlo simulation with 100 runs (slow simulation) in the typical corner, where the comparator has at its input a staircase of voltage levels that varies from -10 mV to 10 mV. In each run, the comparator is triggered with a growing input voltage until its output decision changes (i.e. from 0 to 1), then the standard deviation of those threshold voltage, obtained as

$\sigma_{avg}(v_{OS}) = 3.2\ \text{mV}$, is used as a design estimative of the offset voltage. In turn, if we size the auxiliary differential pair five times smaller than the main, the calibration reference voltages centered in V_{CM} ($190\ \text{mV}$ for corner 14), in order to maintain the same common-mode used for the DAC, and a C_L far larger than the parasitic capacitive node, meaning if we stipulate

$$\begin{cases} g_{m2} = g_{m1}/5 \\ V_{calH} \approx V_{CM} + 100\ \text{mV} \\ V_{calL} \approx V_{CM} - 100\ \text{mV}' \\ C_L/C_P \approx 1000 \end{cases} \tag{4.113}$$

which for the slowest corner ($V_{CMcomp} = 190\ \text{mV}$) would origin

$$\begin{cases} V_{calH} \approx 290\ \text{mV} \\ V_{calL} \approx 90\ \text{mV} \\ \Delta V_{cal\ diff} = 190\ \mu\text{V} \\ V_{OSmax} = V_{CM}/5 = 38\ \text{mV} \\ V_{OSres} = \pm 76\ \mu\text{V} \end{cases} . \tag{4.114}$$

Theoretically, this way, this cancelation method would be able to mitigate the offset almost at a fourth of the quantization step, however the actual implementation, shown in Figure 4-55, has an impact of leakage current too great. As depicted in the figure (P-side), half of the auxiliary differential pair is composed by M_{8P} and M_{9P} (five times smaller copies of the main), which produces a calibration current controlled by v_{calP}. In a straightforward comparison between the calibration circuit model and the real one, the s_4 is done by M_{11P} for incremental step of the intermediate node ($v_{calstepP} = \Delta V_{cal\ diff}$), and likewise s_5 by M_{12P} for decremental steps. In turn, the charge of these steps is only transferred to C_{LP} (i.e. v_{calP}) when enabled M_{10P} (s_3) at given charge phase ($phchrg$). Nonetheless, the reset switches, also denoted, have the purpose to nullify the differential voltages impact during the comparator reset ($latch = 0$) and, as explained before, both the employed capacitors are made by PMOS with short-circuited terminals.

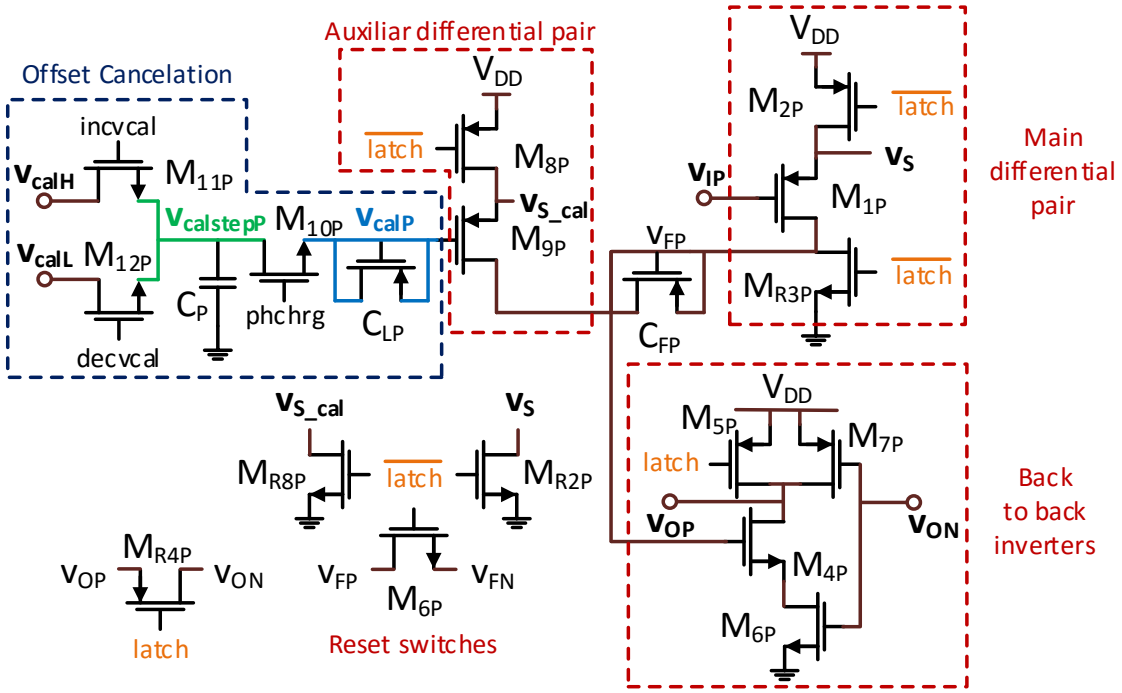

Figure 4-55 - Half of the comparator with offset cancelation circuit.

Now, looking just for the offset circuit we can observe similarities with the leakage current problem discussed about the sampling DAC switches. Once the switches are never (completely) turned off, due to leakage current, the capacitors are always being discharged, thereby limiting the circuit to a low frequency performance. This is demonstrated by relating the current of a simple circuit composed by a capacitor linked to a switch, namely using C_{LP} and M_{10P} from Figure 4-54, which results in

$$i_c = C_{LP}\frac{dv_{calP}}{dt} \Leftrightarrow \Delta V_{calP} = \frac{I_{leak}}{C_{LP}}\Delta t. \tag{4.115}$$

When V_{DD} decreases (e.g. $V_{DD} = 0.9\ \text{V} \longrightarrow 0.5\ \text{V}$), it results in slow switchings and increased difficulty to compensate the existing leakage current. As (4.115) shows, the I_{leak} in a longer time operation, causes a higher ΔV_{Cal} that discharges more quickly the C_{LP}. This way, the produced step ($\Delta V_{cal\ diff}$) reduces and the voltage estimation ($v_{cal\ diff}$) that the system encountered is lost.

Therefore, the followed approach was the same as for the sampling DAC switches, we first tried to manipulate the dimensions of the transistors, for a sufficient settle ON-resistance and high OFF-resistance. Although, M_{10P} is the greater responsible for leakage current in v_{calP}, both M_{11P} and M_{12P} are also responsible for it and required large sized to obtain a large OFF-resistance. Then, the settle or voltage leap (i.e. $\Delta V_{cal\ diff}$) is limited by a tradeoff between the ON-resistance switches and the capacitive relation (C_L/C_P), whilst it also depend of the phases that (dis)enable these three switches.

Since the offset comparison occurs in st_vos, we could, during the following st_reset, just enable M_{10P} to refresh v_{calP} and disable both M_{11P} and M_{12P}, this way giving a shorter time for v_{CalP} to settle than for $v_{calstepP}$ (that would have the remaining time of the period). Or, we could, during the following st_reset, just refresh $v_{calstepP}$, giving the remaining time of the period to refresh v_{CalP}. However, in both of these cases, even using oversizing switches combined with clock-boosts, plus manipulating the

capacitive ratio, was not enough to stop the reprocessing / loss of the search method, caused by the leakage. Hence, alternatively what could even be explored, for this mechanism to operate under these conditions, would be to create specific phases that only toggle these switches in a smaller state, instead of using the entire remaining time of the period.

5. Conclusion and future work

Whether for a need of health, safety or comfort there is a demand for better sensors in WSN, where the ADCs play an important role, as the module that translates the analog to the digital domain, ensuring the quality of the captured signal with the lowest power consumption as possible. After an overview between ADCs, showing their most important concepts and measures to characterize them, it is first made a distinction between the oversampling converters from the Nyquist converter. In turn, the most common converters are presented (the Flash ADC, the Integrating ADC and the Pipeline ADC). Then, a more detailed explanation about the SAR ADC is given, combined a summary of some state of the art works. Since there is no fine line that distinguishes the best topology for converters, some designers bet on hybrid versions. Nonetheless, the research works of the past decade show that the SAR topology is suitable for low power ADCs. Since it works in a recursive way and ensures the transistors operation in the sub-threshold region (where minimal consumption is achieved).

The challenge of this project was to create a functional SAR ADC with transistors supplied at $0.5\ \mathrm{V}$, though their nominal voltage were $0.9\ \mathrm{V}$. Briefly, it becomes difficult to obtain low ON-resistance switches and to deal with the (significant) leakage current. Thus, it results in slow switchings and increased difficulty to contain the charge in the nodes. This ADC was sized regarding as top guidelines, the time and the noise constraints. The time convention that we followed gave most of the period of time for conversion and the remaining for sampling. In turn, the noise restriction was used to limit the noise that each block was allowed to produced. Thus, limiting the value noise capacitor of the comparator and the unit capacitance of the DAC array.

The comparator is made of a differential integrator and cross coupled inverters, which, define respectively a phase of integration and regeneration. The integrator was sized to place the transistors of the differential pair in the sub-threshold region (namely in the weak inversion region), combined with a sufficient current supply that complies with the temporal goals. The converter is aimed to operate at a maximum sample rate of 500 kS/s, based on 16 corners plus the typical one. However, corner 2 had to be discard, since it implies a scenario that requires around 4 times larger sizes of the transistors than the second slowest corner (14). Even so, this case was only ensured by using a turbo mode that adds an extra capacitor to integration node of the comparator. This provides a higher voltage than the supply, accelerating the integration phase and, thus, the overall conversion time. Although, this method brings the advantage of internally producing a voltage higher than the supply (without requiring other external voltage), at the expense of more occupied area. It requires a greater complexity in its control circuit as well as in the adjustment of the counter-kickback effect.

The sampling DAC block was made of two capacitive arrays, which provides a pseudo-binary scale (due to use of redundancy), combined with a block of switches for each capacitor that ought to ensure a minimum error for sampling as for its switching references. For that to happen (where most of the design effort was spent) a custom topology was employed, to mitigate and differentially balance the leakage current, when those switches are OFF. In addition, clock-boosts are employed to drive the gates of the transistors used for sampling. First the capacitive array was scaled (accordingly to its bit weight)

and, only then, the respective switches were scaled similarly. However, the switches sizing have a mutual dependency to the ADC state machine.

Although the ADC has an asynchronous behavior, it is only resultant of the different time of each bit conversion, in fact after each bit decision the comparator is disabled for a fixed time (that allows the voltage of the capacitors to stabilize). The state machine assures this fixed time, thanks to a custom delay cell that mimics the behavior of the DAC switching references. The state machine is centralized in the delay block that, depending on the comparator outcome, creates the control (clock) signals of the comparator ($\overline{latch}$) and the ring counter (CLK_{state}), which produces the consecutive states of the ADC.

About the non-linearity issues we can state that their origin is mainly from the sampling DAC block, due to capacitors mismatches, however it can be mitigated by a digital calibration. On the other hand, the comparator might insert an offset voltage, which can cause wrong bit decisions. Although this is recovered by redundancy, the digital calibration that we intended to use requires a comparator with low offset voltage. Therefore, this converter requires a digital calibration and an offset voltage calibration. The last efforts in this work were fixed in an attempt to solve this problem with an analog calibration, unfortunately without success. Revising the state of art (section 3.3), the first work [12] suggests a re-sizing of the comparator with transistors with bigger dimensions, since the transistors become less susceptible to offsets at the cost of increasing their consumption. However, as seen in this project, enlarging the transistors sizes do not resolve sufficiently the impact of their current leakage. Hence it leads to believe that, to maintain the explored topology, we should use transistors with less leakage current (and better controlled gates), such as tri-gate transistors (FinFet) [29]. Or else apply another topology more complex, such as the [16] work reviewed uses a hybrid architecture.

Revising the primary goal of this project, it was not complied, since there have not been acquired top simulations that allow the ADC characterization, we cannot prove that this SAR ADC is operational. At the end of the project calendar, a proper solution for the comparator offset calibration was not found. Nonetheless, we can point out the difficulties faced, between corners, to size each block of the ADC, with the proposed topologies to deal with the significant leakage current. Leaving for future work to:

- Improve the comparator turbo mechanism.
- Simulate and re-size the blocks with non-ideal reference voltages;
- Optimize the delay chains, instead of using simple chains of inverters with higher length values and re-adjust the DAC delay cell;
- Optimize the circuit that generates the driving phases of the switches, namely the short-circuit pulse before the offset calibration state;
- Improve the comparator counter kickback voltage mechanism by creating a more complex logic that mimics better the integration voltage node, and also adjusting in two operating modes for using turbo ON and OFF;
- Explore a better (and functional) calibration topology for the comparator offset voltage.
- Design and simulate the respective layouts of every block.

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